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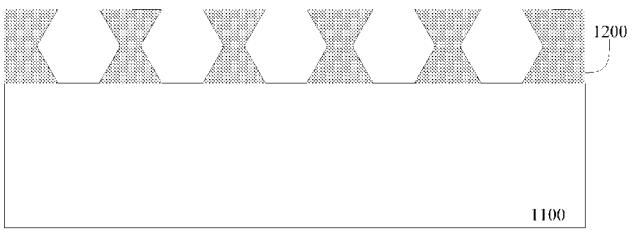


Fig. 2

(57) Abstract: A semiconductor structure and a method for forming the same are provided. The semiconductor structure comprises: a wafer (1100); a plurality of convex structures (1200) formed on the wafer (1100), in which every two adjacent convex structures (1200) are separated by a cavity in a predetermined pattern and arranged in an array, and the cavity between every two adjacent convex structures is less than 50nm in width; and a first semiconductor film (1300) formed on the plurality of convex structures (1200), in which a part of the first semiconductor film (1300) is spaced apart from the wafer (1100).

# SEMICONDUCTOR STRUCTURE AND METHOD FOR FORMING THE SAME

## FIELD

The present disclosure relates to a semiconductor manufacture and design, and more particularly to a semiconductor structure and a method for forming the same.

## BACKGROUND

For a long time, in order to achieve a higher chip density, a faster working speed and a lower power consumption, a feature size of a MOSFET (metal-oxide-semiconductor field effect transistor) is continuously scaled down according to Moore's law, and a working speed of the MOSFET is faster and faster. Currently, the feature size of the MOSFET has reached a nanometer level. However, a serious challenge is an emergence of a short-channel effect, such as a subthreshold voltage roll-off ($V_t$ roll-off), a DIBL (drain-induced barrier lowering) and a source-drain punch through, thus increasing an off-state leakage current. Therefore, a performance of the MOSFET may be deteriorated.

Therefore, for a conventional device, large leakage is a main constraint for scaling down.

## SUMMARY

The present disclosure is aimed to solve at least one of the above mentioned technical problems.

According to an aspect of the present disclosure, a semiconductor structure is provided. The semiconductor structure comprises: a wafer; a plurality of convex structures formed on the wafer, in which every two adjacent convex structures are separated by a cavity in a predetermined pattern and arranged in an array, and the cavity between every two adjacent convex structures is less than 50nm in width; and a first semiconductor film formed on the plurality of convex structures, in which a part of the first semiconductor film on the cavity is floated and spaced apart from the wafer.

In one embodiment, a width of each convex structure increases gradually from a middle part thereof to a top part thereof so that the cavity size between top parts of two

adjacent convex structures is less than that between middle parts of the two adjacent convex structures.

In one embodiment, a material forming each convex structure comprises Si, $Si_{1-x}C_x$, $Si_yGe_{1-y}$ or Ge.

In one embodiment, each convex structure comprises a bottom layer and a top layer, the bottom layer is a Si layer, and the top layer is a $Si_{1-x}C_x$ layer, a $Si_yGe_{1-y}$ layer, or a Ge layer.

In one embodiment, the first semiconductor film is formed by annealing the plurality of convex structures at a temperature of 300-1350 degrees Celsius in an ambient containing hydrogen.

In one embodiment, the ambient further comprises at least one gas selected from a group consisting of $SiH_4$, $GeH_4$, $SiH_2Cl_2$, and $SiHCl_3$.

In one embodiment, the first semiconductor film is a Si layer, a $Si_yGe_{1-y}$ layer, or a Ge layer.

In one embodiment, the semiconductor structure further comprises: a first high mobility material layer formed on the first semiconductor film.

According to another aspect of the present disclosure, a method for forming a semiconductor structure is provided. The method comprises steps of: providing a wafer; forming a plurality of convex structures on the wafer, in which every two adjacent convex structures are separated by a cavity in a predetermined pattern and arranged in an array, and the cavity between every two adjacent convex structures is less than 50nm in width; and forming a first semiconductor film on the plurality of convex structures, in which the first semiconductor film and the wafer are spaced apart by a predetermined height so that a part of the first semiconductor film on the cavity is floated and spaced apart from the wafer.

In one embodiment, a width of each convex structure increases gradually from a middle part thereof to a top part thereof so that the cavity size between top parts of two

adjacent convex structures is less than that between middle parts of the two adjacent convex structures.

In one embodiment, a material forming each convex structure comprises Si, $Si_{1-x}C_x$, $Si_yGe_{1-y}$ or Ge.

In one embodiment, each convex structure comprises a bottom layer and a top layer, the bottom layer is a Si layer, and the top layer is a $Si_{1-x}C_x$ layer, a $Si_yGe_{1-y}$ layer, or a Ge layer.

In one embodiment, the method according further comprises: partitioning the wafer into a plurality of first regions and a plurality of second regions according to an inputted layout file; removing the first semiconductor films and the convex structures in the plurality of second regions; and forming a MOS transistor structure in each first region, in which each convex structure in the each first region is a channel of the MOS transistor structure, and the first semiconductor films in the each first region are set as a source region and a drain region of the MOS transistor structure respectively.

In one embodiment, the method further comprises: partitioning the wafer into a plurality of first regions and a plurality of second regions according to an inputted layout file; removing the first semiconductor films and the convex structures in the plurality of second regions; and forming a MOS transistor structure in each first region, in which two adjacent convex structures in the plurality of first regions are set as a source region and a drain region of the MOS transistor structure respectively, and the first semiconductor film between the two adjacent convex structures is a channel of the MOS transistor structure respectively.

In one embodiment, the step of forming a first semiconductor film on the plurality of convex structures comprises: annealing the wafer and the plurality of convex structures at a temperature of 300-1350 degrees Celsius in an ambient containing hydrogen.

In one embodiment, the ambient further comprises at least one gas selected from a group consisting of $SiH_4$, $GeH_4$, $SiH_2Cl_2$, and $SiHCl_3$.

In one embodiment, the method further comprises: forming a first high mobility material layer on the first semiconductor film.

In one embodiment, the step of forming a first semiconductor film on the plurality of convex structures comprises: forming the first semiconductor film on the plurality of convex structures by epitaxy.

In one embodiment, the step of forming a plurality of convex structures on the wafer comprises: forming a second material layer on the wafer; implanting Si or Ge ions into the second material layer to form an ion-implanted layer in the second material layer; and selectively etching the second material layer to form the plurality of convex structures.

With a device formed by the semiconductor structure according to an embodiment of the present disclosure, because the first semiconductor film is spaced apart from the wafer, a leakage current is depressed, and consequently the semiconductor structure according to an embodiment of the present disclosure may inhibit a generation of the leakage current. Moreover, with the semiconductor structure according to an embodiment of the present disclosure, a high mobility channel layer, for example, a $Si_{1-x}C_x$ layer, a SiGe layer with high Ge content, a Ge layer, or an III-V group compound semiconductor layer, may be formed, thus improving a performance of a device.

In one embodiment, the floated part of the first semiconductor film is used as a source region and a drain region of a MOS transistor structure respectively, and a channel of the MOS transistor structure is set on the top of the convex structure. In this way, on one hand, dopants in the source and the drain of the MOS transistor structure may be prevented from diffusing into a substrate, so that it may be easy to fabricate an ultra-shallow junction. On the other hand, the source and the drain of the MOS transistor structure may not contact the substrate, thus inhibiting band-to-band tunneling (BTBT) leakage between the source and the drain of the MOS transistor structure and the

substrate. Furthermore, parasitic junction capacitance of the source and the drain of the MOS transistor structure may be reduced, thus improving the performance of the device.

In addition, in another embodiment, the floated part of the first semiconductor film is used as a channel of a MOS transistor structure, and a source region and a drain region of the MOS transistor structure is set on top of two adjacent convex structures respectively. In this way, dopants in the source and the drain of the MOS transistor structure may be prevented from diffusing into the channel of the MOS transistor structure, so that it may be easy to fabricate an ultra-shallow junction.

Additional aspects and advantages of the embodiments of the present disclosure will be given in part in the following descriptions, become apparent in part from the following descriptions, or be learned from the practice of the embodiments of the present disclosure.

## BRIEF DESCRIPTION OF THE DRAWINGS

These and other aspects and advantages of the disclosure will become apparent and more readily appreciated from the following descriptions taken in conjunction with the drawings in which:

Fig. 1 is a top view of a part of a semiconductor structure according to an embodiment of the present disclosure;

Fig. 2 is a cross-sectional view of a part of a semiconductor structure according to an embodiment of the present disclosure;

Fig. 3 is a cross-sectional view of a part of a semiconductor structure according to another embodiment of the present disclosure;

Fig. 4 is a cross-sectional view of a semiconductor structure according to an embodiment of the present disclosure;

Fig. 5 is a cross-sectional view of a semiconductor structure according to another embodiment of the present disclosure;

Fig. 6 is a cross-sectional view of a semiconductor structure according to still another embodiment of the present disclosure; and

Fig. 7 is a flow chart of a method for forming a semiconductor structure according to an embodiment of the present disclosure.

## DETAILED DESCRIPTION

Embodiments of the present disclosure will be described in detail in the following descriptions, examples of which are shown in the accompanying drawings, in which the same or similar elements and elements having same or similar functions are denoted by like reference numerals throughout the descriptions. The embodiments described herein with reference to the accompanying drawings are explanatory and illustrative, which are used to generally understand the present disclosure. The embodiments shall not be construed to limit the present disclosure.

Various embodiments and examples are provided in the following description to implement different structures of the present disclosure. In order to simplify the present disclosure, certain elements and settings will be described. However, these elements and settings are only examples and are not intended to limit the present disclosure. In addition, reference numerals may be repeated in different examples in the disclosure. This repeating is for the purpose of simplification and clarity and does not refer to relations between different embodiments and/or settings. Furthermore, examples of different processes and materials are provided in the present disclosure. However, it would be appreciated by those skilled in the art that other processes and/or materials may be also applied. Moreover, a structure in which a first feature is “on” a second feature may include an embodiment in which the first feature directly contacts the second feature and may include an embodiment in which an additional feature is prepared between the first feature and the second feature so that the first feature does not directly contact the second feature.

Fig. 1 is a top view of a part of a semiconductor structure according to an embodiment of the present disclosure. Fig. 2 is a cross-sectional view of a part of a semiconductor structure according to an embodiment of the present disclosure. Fig. 3 is a cross-sectional view of a part of a semiconductor structure according to another embodiment of the present disclosure. Fig. 4 is a cross-sectional view of a semiconductor

structure according to an embodiment of the present disclosure. Fig. 5 is a cross-sectional view of a semiconductor structure according to another embodiment of the present disclosure.

The semiconductor structure comprises a wafer 1100; a plurality of convex structures 1200 formed on the wafer 1100, in which every two adjacent convex structures 1200 are spaced apart by a cavity in a predetermined pattern and arranged in an array, as shown in Fig. 1. In some embodiments, the cavity between every two adjacent convex structures is less than 50nm in width, preferably, 30 nm. It should be noted that, in some embodiments, the width of the convex structures 1200 may be fixed in vertical dimension. However, in other embodiments, as shown in Figs. 2-3, a width of each convex structure 1200 increases gradually from a middle part thereof to a top part thereof so that the cavity size between top parts of two adjacent convex structures 1200 is less than that between middle parts of the two adjacent convex structures 1200. Therefore, a first semiconductor film 1300 may be formed by annealing the convex structures 1200 or by epitaxy. If the cavity size between top parts of two adjacent convex structures 1200 is less than that between middle parts of the two adjacent convex structures 1200, the above-mentioned “less than 50nm in width” refers to that the top width of the cavity is less than 50nm. The semiconductor structure according to an embodiment of the present disclosure may be applied to a device with small size, particularly used for alleviating a leakage of a small size device.

The semiconductor structure further comprises a first semiconductor film 1300 formed on the plurality of convex structures 1200, and the first semiconductor film 1300 and the wafer 1100 are spaced apart by a predetermined height. In other words, a part of the first semiconductor film 1300 on the cavity is floated and spaced apart from the wafer 1100. In some embodiments, the predetermined height may be determined according to the available largest etching depth, however, the predetermined height may be any height, provided that the first semiconductor film 1300 may not contact the wafer 1100. In some embodiments, the convex structures 1200 may have various shapes, for example,

a cylindrical shape or a cuboid shape, provided that the cavity between two adjacent convex structures 1200 is small enough to form the first semiconductor film 1300 by annealing the convex structures 1200 or by epitaxy. A lateral epitaxial growth rate of the first semiconductor film 1300 with a certain crystal orientation is not less than a longitudinal growth rate thereof, so that a gap between the top parts of two adjacent convex structures 1200 may be quickly sealed up by epitaxial materials. Therefore, the first semiconductor film 1300 may not contact the wafer 1100 directly. In some embodiments, the first semiconductor film 1300 is very thin, and is below about 10nm, and consequently may be used for fabricating an ultra-shallow junction.

In one embodiment, the wafer 1100 is a Si wafer or a SiGe wafer with low Ge content, and the first semiconductor film 1300 is a Si layer, a $Si_yGe_{1-y}$ layer, or a Ge layer. As used herein, the term "a SiGe layer with low Ge content" indicates that a content of Ge in the SiGe layer is lower than 50%, and the term "a SiGe layer with high Ge content" indicates that a content of Ge in the SiGe layer is higher than 50%. In another embodiment, if the first semiconductor film 1300 is formed by epitaxy, the first semiconductor film 1300 may also be a III-V Group compound semiconductor layer.

In one embodiment, a material forming each convex structure 1200 comprises Si, $Si_{1-x}C_x$, $Si_yGe_{1-y}$ or Ge. In some embodiments, the first semiconductor film 1300 may be formed by annealing the wafer 1100 and the plurality of convex structures 1200 or by epitaxy. In some embodiments, the annealing is performed at a temperature of 300-1350 degrees Celsius in an ambient containing hydrogen to migrate atoms on surfaces of the plurality of convex structures 1200. Since the ambient contains hydrogen, a surface of the first semiconductor film 1300 may be activated. Preferably, the ambient further comprises at least one gas selected from a group consisting of $SiH_4$, $GeH_4$, $SiH_2Cl_2$, and $SiHCl_3$. A small amount of Si and/or Ge atoms are deposited on the surface of the first semiconductor film 1300 by decomposing the at least one gas, so that the surface of the first semiconductor film 1300 may be flattened, and a required flatness is achieved. After the annealing, the top parts of two

adjacent convex structures 1200 may be connected with each other to form the first semiconductor film 1300. In this embodiment, the higher the content of Ge in the first semiconductor film 1300, the lower the annealing temperature is. For example, if the first semiconductor film 1300 is a Ge layer, the annealing temperature may be 300 degrees Celsius.

In one embodiment, each convex structure 1200 comprises a bottom layer and a top layer. Fig. 6 is a cross-sectional view of a semiconductor structure according to still another embodiment of the present disclosure. In some embodiments, the bottom layer is a Si layer, and the top layer is a $Si_{1-x}C_x$ layer, a $Si_yGe_{1-y}$ layer, or a Ge layer. As shown in Fig. 6, each convex structure 1200 comprises a SiGe layer with low Ge content 1210 and a Ge layer 1220. In this way, the SiGe layer with low Ge content 1210 may be used as a buffer layer between the wafer 1100 and the Ge layer 1220.

In one embodiment, the semiconductor structure further comprises a first high mobility material layer formed on the first semiconductor film 1300.

Fig. 7 is a flow chart of a method for forming a semiconductor structure according to an embodiment of the present disclosure. The method comprises the following steps.

Step S701, a wafer is provided. The wafer is a Si wafer, a SOI (silicon on insulator) wafer, or a SiGe wafer with low Ge content.

Step S702, a plurality of convex structures are formed on the wafer, in which every two adjacent convex structures are separated apart by a cavity in a predetermined pattern and arranged in an array. In some embodiments, a cavity between every two adjacent convex structures is less than 50nm in width, and preferably, 30nm. As shown in Figs. 2-3, a width of each convex structure increases gradually from a middle part thereof to a top part thereof so that the cavity size between top parts of two adjacent convex structures is less than that between middle parts of the two adjacent convex structures. Therefore, a first semiconductor film may be formed by annealing the convex structures or by epitaxy. In some embodiments, a material forming each convex structure comprises Si, $Si_{1-x}C_x$, $Si_yGe_{1-y}$ or Ge. In one embodiment, each convex structure comprises a

bottom layer and a top layer, the bottom layer is a Si layer, and the top layer is a $Si_{1-x}C_x$ layer, a $Si_yGe_{1-y}$ layer, or a Ge layer.

In some embodiments, the plurality of convex structures may be formed by etching. For example, at least one second material layer is formed on the wafer, and then the at least one second material layer is etched to form the plurality of convex structures, in which the at least one second material layer is a Si layer, a SiGe layer or a Ge layer. Certainly, in other embodiments, a surface layer of the wafer is used as the second material layer, that is, a surface of the wafer is directly etched to form the plurality of convex structures.

Preferably, in order to form the plurality of convex structures shown in Fig. 2, the second material layer may be etched by an anisotropic wet etching.

Alternatively, in another preferred embodiment, Si or Ge ions are implanted into the second material layer to form an ion-implanted layer in the second material layer, and then the second material layer is selectively etched by a dry etching to form the plurality of convex structures. Because crystal structures in the ion-implanted layer are damaged seriously, an etching rate in the ion-implanted layer is greater than that in other parts of the second material layer, thus forming the plurality of convex structures shown in Fig. 3.

Step S703, a first semiconductor film is formed on the plurality of convex structures by annealing or epitaxy, and the first semiconductor film and the wafer are spaced apart by a predetermined height. In other words, a part of the first semiconductor film on the cavity is floated and spaced apart from the wafer. In some embodiments, if a first semiconductor film is formed by annealing, the first semiconductor film is a Si layer, a $Si_yGe_{1-y}$ layer, or a Ge layer. In some embodiments, the first semiconductor film may be formed by annealing the wafer and the plurality of convex structures. In some embodiments, the annealing is performed at a temperature of 300-1350 degrees Celsius in an ambient containing hydrogen to migrate atoms on surfaces of the plurality of convex structures. Preferably, the ambient further comprises at least one

gas selected from a group consisting of $SiH_4$, $GeH_4$, $SiH_2Cl_2$, and $SiHCl_3$, so that a surface of the first semiconductor film may be flattened.

In another embodiment, the first semiconductor film may also be formed by epitaxy. In some embodiments, the wafer may be a Si wafer, a $Si_{1-x}C_x$ wafer, a SiGe wafer or a Ge wafer with a surface of a crystal orientation (100), in which x is within a range from 0 to 0.1. Because a lateral epitaxial growth rate of the first semiconductor film with a certain crystal orientation is not less than a longitudinal growth rate thereof, a gap between top parts of two adjacent convex structures may be quickly sealed up by epitaxial materials. Therefore, the first semiconductor film may not contact with the wafer directly, so that a part of the first semiconductor film may be spaced apart from the wafer. In some embodiments, the first semiconductor film is very thin, and is below about 10nm, and consequently may be used for fabricating an ultra-shallow junction. In another embodiment, if the first semiconductor film is formed by epitaxy, the first semiconductor film may also be an III-V group compound semiconductor layer.

In one preferred embodiment, after the annealing or the epitaxy, if the first semiconductor film is thick, the first semiconductor film may be subjected to an etching or a thinning process.

Step S704, the wafer is partitioned into a plurality of first regions and a plurality of second regions according to an inputted layout file, in which a MOS transistor structure will be formed in each first region. In some embodiments, a MOS transistor structure will be formed in each first region, and an interface circuit, an isolation structure, a pad and so on will be formed in each second region.

Step S705, the first semiconductor films and the convex structures in the plurality of second regions are removed.

Step S706, a MOS transistor structure is formed in each first region. In one embodiment, a channel of the MOS transistor structure is set on top of the convex structure in each first region, and the adjacent floated parts of the first semiconductor film in the each first region are set as a source region and a drain

region of the MOS transistor structure respectively. In another embodiment, two adjacent convex structures in each first region are set as a source region and a drain region of the MOS transistor structure respectively, and the floated part of the first semiconductor film between the two adjacent convex structures is a channel of the MOS transistor structure. In other embodiments, other similar devices may also be formed.

In one embodiment, the method for forming the semiconductor structure further comprises forming a first high mobility material layer on the first semiconductor film.

It should be noted that, in the above embodiments, the MOS transistor structure is described as an example, however, the semiconductor structure according to an embodiment of the present disclosure may also be applied to other devices.

With a device formed by the semiconductor structure according to an embodiment of the present disclosure, because the first semiconductor film is spaced apart from the wafer, a leakage current is depressed, and consequently the semiconductor structure according to an embodiment of the present disclosure may inhibit a generation of the leakage current. Moreover, with the semiconductor structure according to an embodiment of the present disclosure, a high mobility channel layer, for example, a $Si_{1-x}C_x$ layer, a SiGe layer with high Ge content, a Ge layer, or a III-V group compound semiconductor layer, may be formed, thus improving a performance of a device.

In one embodiment, the adjacent floated part of the first semiconductor film is used as a source region and a drain region of a MOS transistor structure respectively, and a channel of the MOS transistor structure is set on the top of the convex structure. In this way, on one hand, dopants in the source and the drain of the MOS transistor structure may be prevented from diffusing into a substrate, so that an ultra-shallow junction may be easy to fabricate. On the other hand, the source and the drain of the MOS transistor structure may not contact with the substrate, thus inhibiting BTBT leakage between the source and the drain of the MOS transistor structure and the substrate. Furthermore,

parasitic junction capacitance of the source and the drain of the MOS transistor structure may be reduced, thus improving the performance of the device.

In addition, in another embodiment, the floated part of the first semiconductor film is used as a channel of a MOS transistor structure, and the convex structures are used as a source region and a drain region of the MOS transistor structure respectively. In this way, dopants in the source and the drain of the MOS transistor structure may be prevented from diffusing into the channel of the MOS transistor structure, so that an ultra-shallow junction may be easy to fabricate.

Although explanatory embodiments have been shown and described, it would be appreciated by those skilled in the art that changes, alternatives, and modifications all falling into the scope of the claims and their equivalents may be made in the embodiments without departing from spirit and principles of the disclosure.

WHAT IS CLAIMED IS:

1. A semiconductor structure, comprising:

a wafer;

a plurality of convex structures formed on the wafer, wherein every two adjacent convex structures are separated by a cavity in a predetermined pattern and arranged in an array, and the cavity between every two adjacent convex structures is less than 50nm in width; and

a first semiconductor film formed on the plurality of convex structures, wherein a part of the first semiconductor film on the cavity is floated and spaced apart from the wafer.

2. The semiconductor structure according to claim 1, wherein a width of each convex structure increases gradually from a middle part thereof to a top part thereof so that the cavity size between top parts of two adjacent convex structures is less than that between middle parts of the two adjacent convex structures.

3. The semiconductor structure according to claim 1, wherein a material forming each convex structure comprises Si, $Si_{1-x}C_x$, $Si_yGe_{1-y}$ or Ge.

4. The semiconductor structure according to claim 1, wherein each convex structure comprises a bottom layer and a top layer, the bottom layer is a Si layer, and the top layer is a $Si_{1-x}C_x$ layer, a $Si_yGe_{1-y}$ layer, or a Ge layer.

5. The semiconductor structure according to claim 1, wherein the first semiconductor film is formed by annealing the plurality of convex structures at a temperature of 300-1350 degrees Celsius in an ambient containing hydrogen.

6. The semiconductor structure according to claim 5, wherein the ambient further comprises at least one gas selected from a group consisting of $SiH_4$, $GeH_4$, $SiH_2Cl_2$, and $SiHCl_3$.

7. The semiconductor structure according to claim 1, wherein the first semiconductor film is a Si layer, a $Si_yGe_{1-y}$ layer, or a Ge layer.

8. The semiconductor structure according to claim 1, further comprising:

a first high mobility material layer formed on the first semiconductor film.

9. A method for forming a semiconductor structure, comprising steps of:

providing a wafer;

forming a plurality of convex structures on the wafer, wherein every two adjacent convex structures are separated by a cavity in a predetermined pattern and arranged in an array, and the cavity between every two adjacent convex structures is less than 50nm in width; and

forming a first semiconductor film on the plurality of convex structures, wherein a part of the first semiconductor film on the cavity is floated and spaced apart from the wafer.

10. The method according to claim 9, wherein a width of each convex structure increases gradually from a middle part thereof to a top part thereof so that the cavity size between top parts of two adjacent convex structures is less than that between middle parts of the two adjacent convex structures.

11. The method according to claim 9, wherein a material forming each convex structure comprises Si, $Si_{1-x}C_x$, $Si_yGe_{1-y}$ or Ge.

12. The method according to claim 9, wherein each convex structure comprises a bottom layer and a top layer, the bottom layer is a Si layer, and the top layer is a $Si_{1-x}C_x$ layer, a $Si_yGe_{1-y}$ layer, or a Ge layer.

13. The method according to claim 9, further comprising:

partitioning the wafer into a plurality of first regions and a plurality of second regions according to an inputted layout file;

removing the first semiconductor films and the convex structures in the plurality of second regions; and

forming a MOS transistor structure in each first region, wherein a channel of the MOS transistor structure is set on a top of the convex structure, and a source region and a drain region of the MOS transistor structure are set in the floated part of the first semiconductor film respectively.

14. The method according to claim 9, further comprising:

partitioning the wafer into a plurality of first regions and a plurality of second regions according to an inputted layout file;

removing the first semiconductor films and the convex structures in the plurality of second regions; and

forming a MOS transistor structure in each first region, wherein a source region and a drain region of the MOS transistor structure are set on the top of two adjacent convex structures in the plurality of first regions respectively, and a channel of the MOS transistor structure is set in the floated part of the first semiconductor film between the two adjacent convex structures respectively.

15. The method according to claim 9, wherein the step of forming a first semiconductor film on the plurality of convex structures comprises:

annealing the wafer and the plurality of convex structures at a temperature of 300-1350 degrees Celsius in an ambient containing hydrogen.

16. The method according to claim 15, wherein the ambient further comprises at least one gas selected from a group consisting of $SiH_4$, $GeH_4$, $SiH_2Cl_2$, and $SiHCl_3$.

17. The method according to claim 9, further comprising:

forming a first high mobility material layer on the first semiconductor film.

18. The method according to claim 9, wherein the step of forming a first semiconductor film on the plurality of convex structures comprises:

forming the first semiconductor film on the plurality of convex structures by epitaxy.

19. The method according to claim 10, wherein the step of forming a plurality of convex structures on the wafer comprises:

forming a second material layer on the wafer;

implanting Si or Ge ions into the second material layer to form an ion-implanted layer in the second material layer; and

selectively etching the second material layer to form the plurality of convex structures.

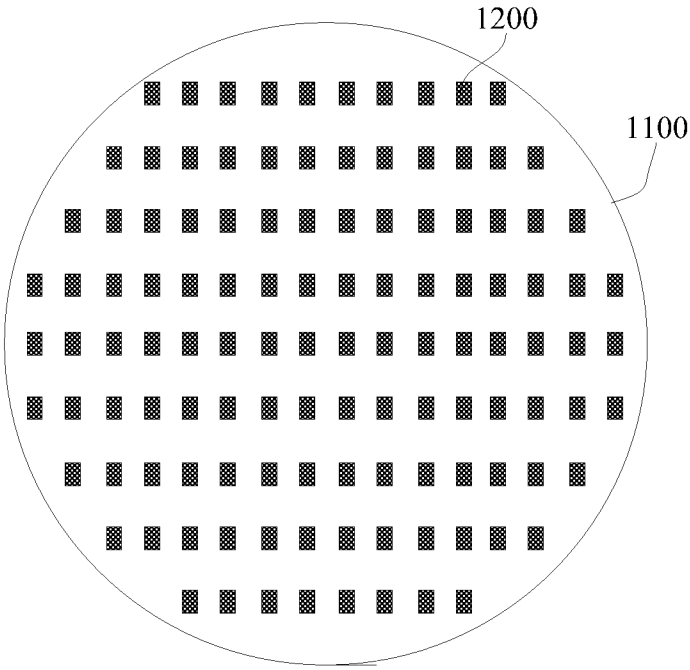


Fig. 1

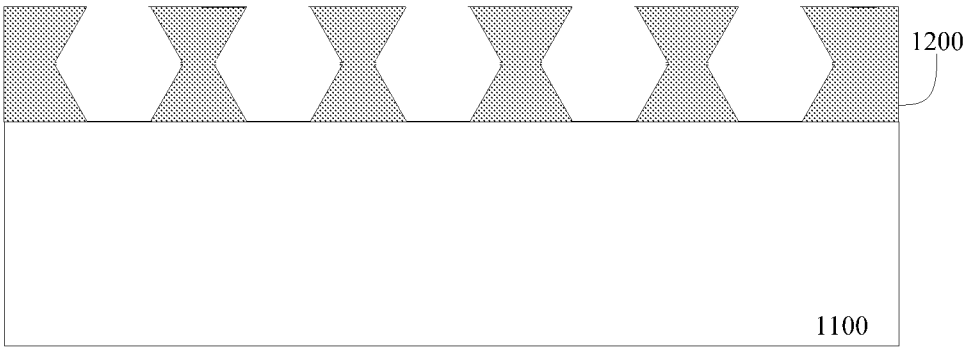


Fig. 2

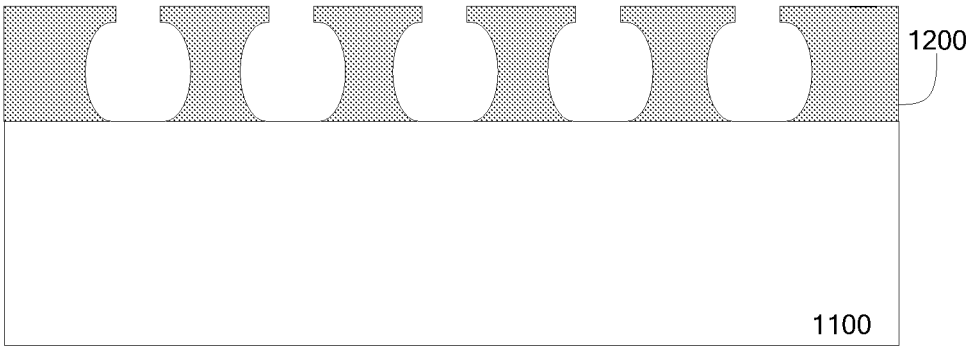


Fig. 3

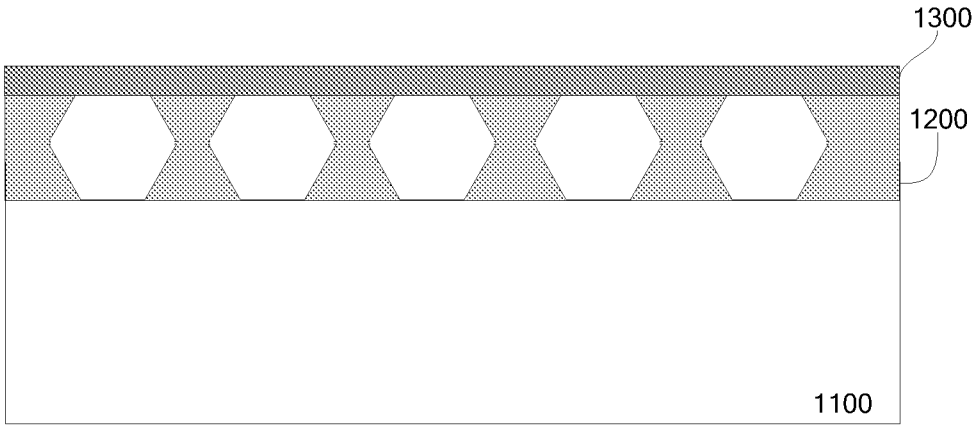


Fig. 4

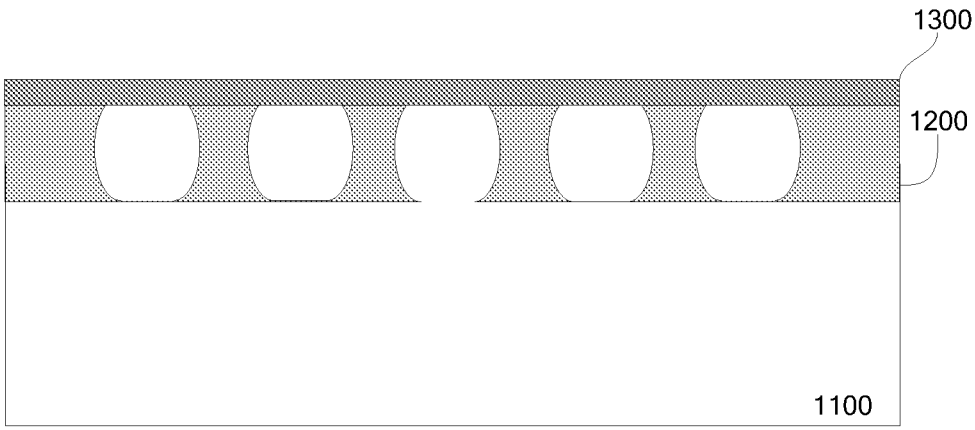


Fig. 5

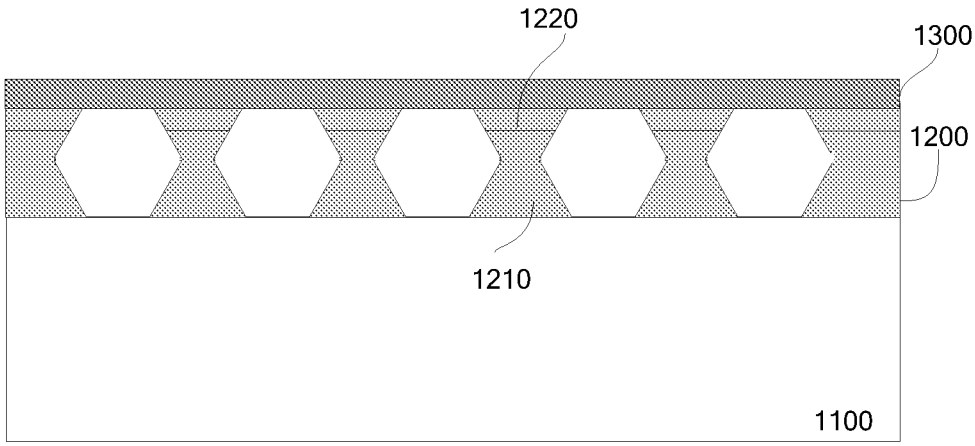


Fig. 6

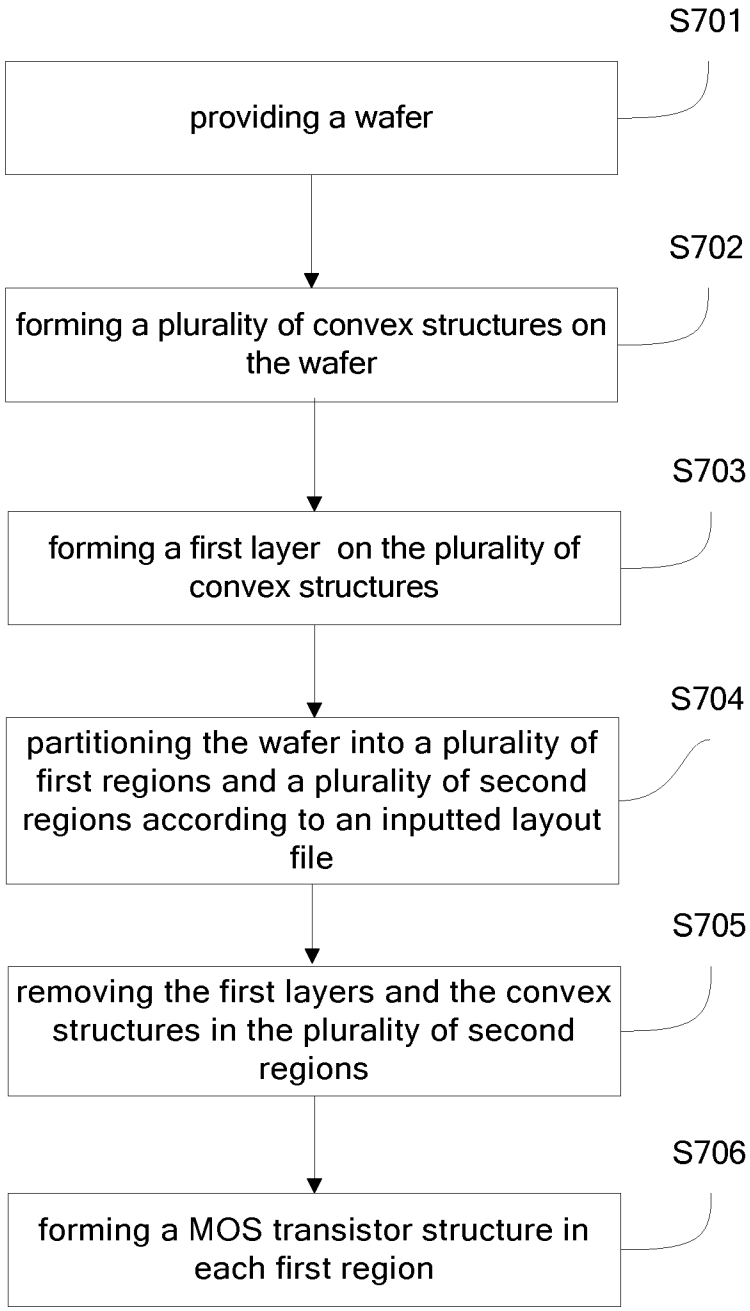
S701
providing a wafer
S702
forming a plurality of convex structures on the wafer
S703
forming a first layer on the plurality of convex structures
S704
partitioning the wafer into a plurality of first regions and a plurality of second regions according to an inputted layout file
S705
removing the first layers and the convex structures in the plurality of second regions
S706
forming a MOS transistor structure in each first region

Fig. 7

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2011/082109

**A. CLASSIFICATION OF SUBJECT MATTER**

See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC:H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS,CNKI,WPI,EPODOC
Substrate, wafer, convex, concave, projection, recess, protrusion, epitaxial, etch, annealing, nano

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | CN101997071A (SAMSUNG ELECTRONICS CO LTD) 30 Mar. 2011(30.03.2011) Paragraphs [0035]-[0056] of description, Figures 1-6 | 1-19 |
| X | CN1828837A (SHANGHAI INST MICROSYS & INF) 06 Sep. 2006(06.09.2006) Page 2 line 15- page 4 line 29, Figure 1 | 1-19 |
| PX | CN102208440A (TSINGHUA UNIVERSITY) 05 Oct. 2011(05.10.2011) the whole document | 1-19 |
| PX | CN102214681A (TSINGHUA UNIVERSITY) 12 Oct. 2011(12.10.2011) the whole document | 1-19 |
| PX | CN102214682A (TSINGHUA UNIVERSITY) 12 Oct. 2011(12.10.2011) the whole document | 1-19 |
| PX | CN102214683A (TSINGHUA UNIVERSITY) 12 Oct. 2011(12.10.2011) the whole document | 1-19 |
| PX | CN102214685A (TSINGHUA UNIVERSITY) 12 Oct. 2011(12.10.2011) the whole document | 1-19 |
| A | CN101378017A (SUZHOU NANOWIN SCIENCE AND TECHNOLOGY CO LTD) 04 Mar. 2009(04.03.2009) the whole document | 1-19 |

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 03 Feb. 2012(03.02.2012) | **22 Mar. 2012 (22.03.2012)** |
| Name and mailing address of the ISA/CN<br>The State Intellectual Property Office, the P.R.China<br>6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088<br>Facsimile No. 86-10-62019451 | Authorized officer<br>DAI,Yongchao<br>Telephone No. (86-10)62411564 |

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Information on patent family members

International application No.
PCT/CN2011/082109

| Patent Documents referred in the Report | Publication Date | Patent Family | Publication Date |
|---|---|---|---|
| CN101997071A | 30.03.2011 | JP2011040760A | 24.02.2011 |
| | | US2011037098A1 | 17.02.2011 |
| | | EP2287924A2 | 23.02.2011 |
| | | KR20110018105A | 23.02.2011 |
| CN1828837A | 06.09.2006 | CN1828837B | 20.04.2011 |
| CN102208440A | 05.10.2011 | NONE | |
| CN102214681A | 12.10.2011 | NONE | |
| CN102214682A | 12.10.2011 | NONE | |
| CN102214683A | 12.10.2011 | NONE | |
| CN102214685A | 12.10.2011 | NONE | |
| CN101378017A | 04.03.2009 | CN101378017B | 01.12.2010 |

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2011/082109

**In continuous of A. CLASSIFICATION OF SUBJECT MATTER of second sheet**

H01L 29/06 (2006.01) i

H01L 21/02 (2006.01) i

H01L 21/336 (2006.01) i