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Bruckheim

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[45] **Sept. 24, 1974**

[54] HEART SURVEILLANCE DEVICE

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[51] **Int. Cl.** **A61b 5/04**

[58] **Field of Search** ..... 128/2.06 F, 2.06 A, 2.05 T, 128/2.06 R, 2.06 G

[56] **References Cited**

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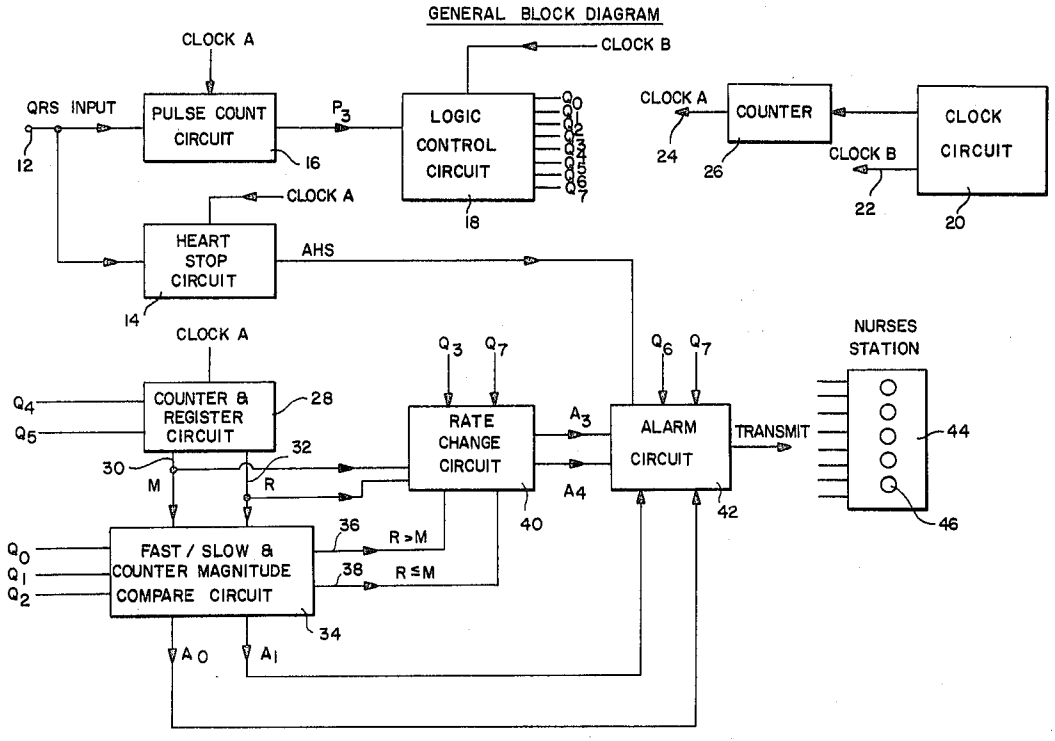
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Attorney, Agent, or Firm—Fidelman, Wolffe, Leitner and Hiney

[57] **ABSTRACT**

A device which monitors the interval between every other heartbeat to determine if the heart rate is too fast or too slow. The previously monitored interval is compared to the present interval to determine whether there has been an abrupt change of heart rate and if there has been a change of heart rhythm. Time intervals are measured digitally using a first pulse train and the determinations are made digitally between two pulses of said first pulse train under the control of a second pulse train. The occurrence of every heart beat is monitored to determine if the heart has stopped beating.

14 Claims, 7 Drawing Figures



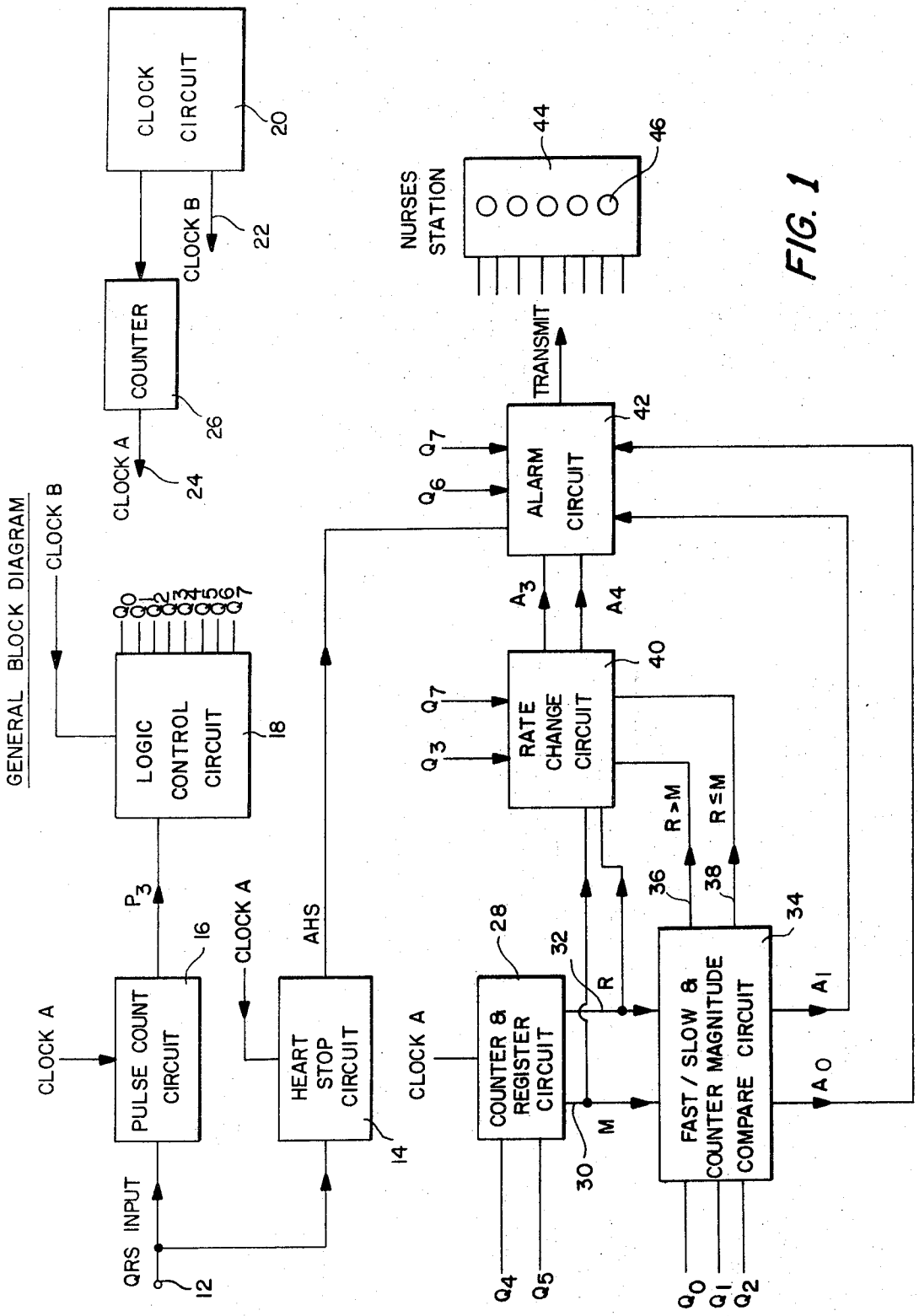

GENERAL BLOCK DIAGRAM
CLOCK CIRCUIT
20
CLOCK B
22
COUNTER
26
CLOCK A
24
NURSES STATION
44
46
TRANSMIT
ALARM CIRCUIT
42
LOGIC CONTROL CIRCUIT
18
RATE CHANGE CIRCUIT
40
PULSE COUNT CIRCUIT
16
HEART STOP CIRCUIT
14
COUNTER & REGISTER CIRCUIT
28
FAST / SLOW & COUNTER MAGNITUDE COMPARE CIRCUIT
34
QRS INPUT
12
CLOCK A
CLOCK B
AHS
R
M
R>M
R≤M
A3
A4
A1
A0
P3
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
30
32
36
38

FIG. 1

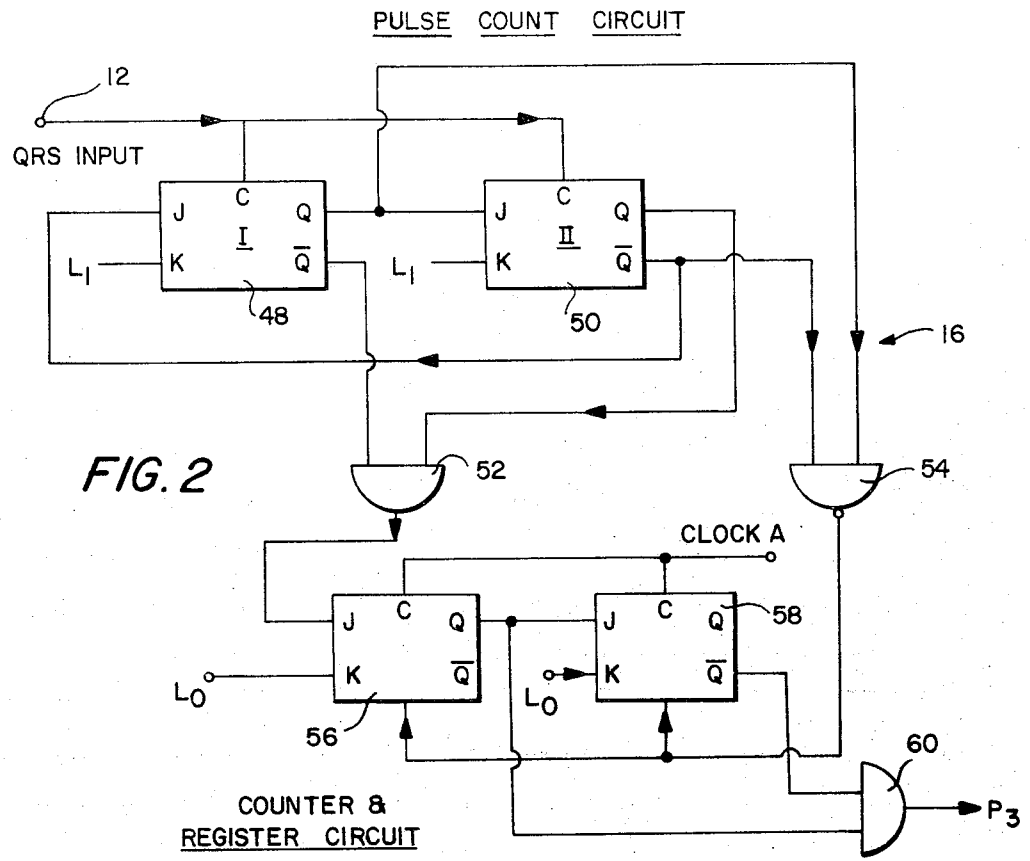


FIG. 2

FIG. 3

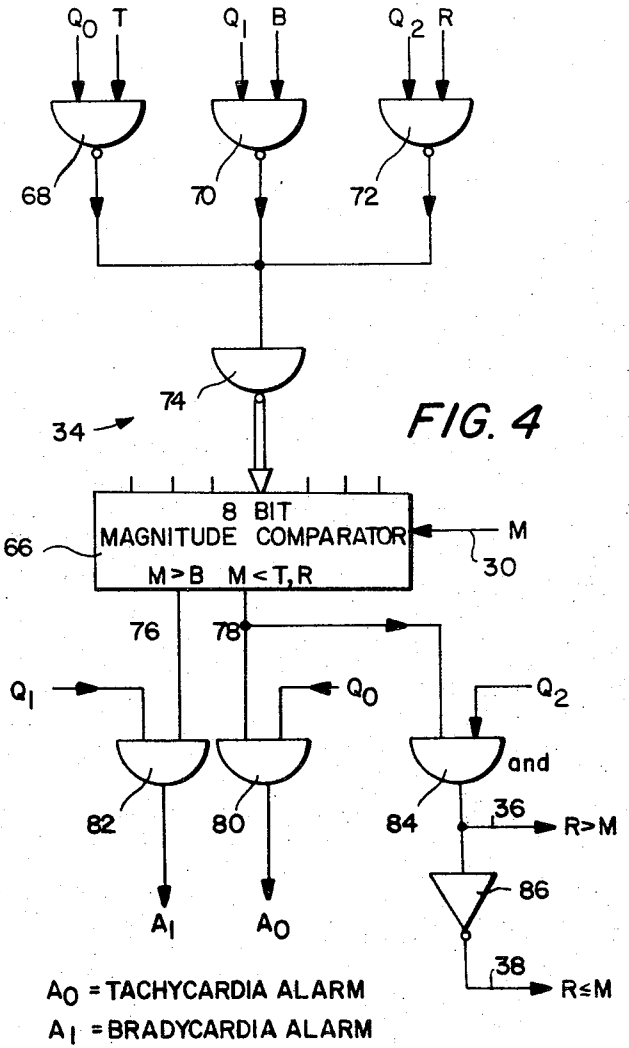


FIG. 4

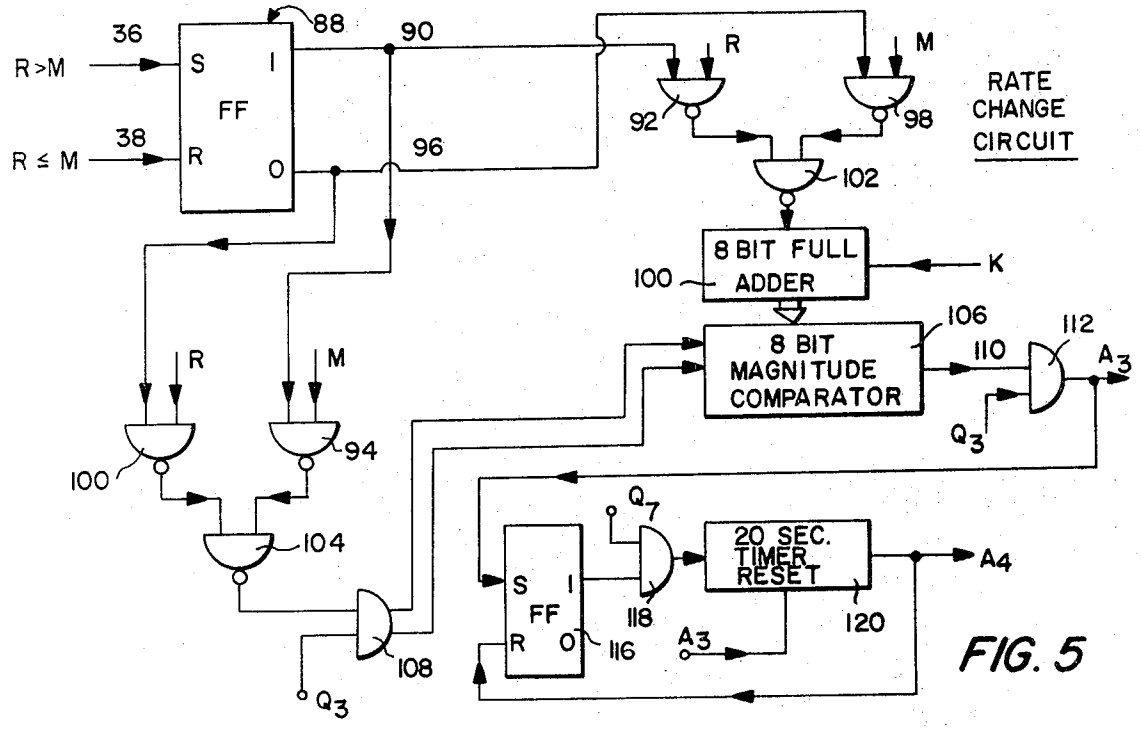


FIG. 5

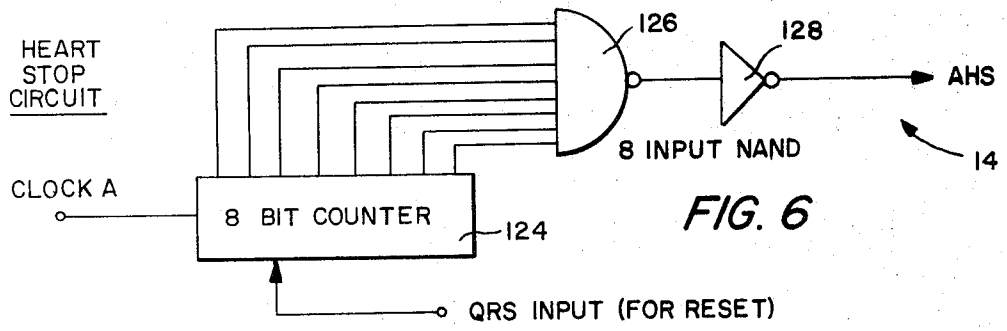


FIG. 6

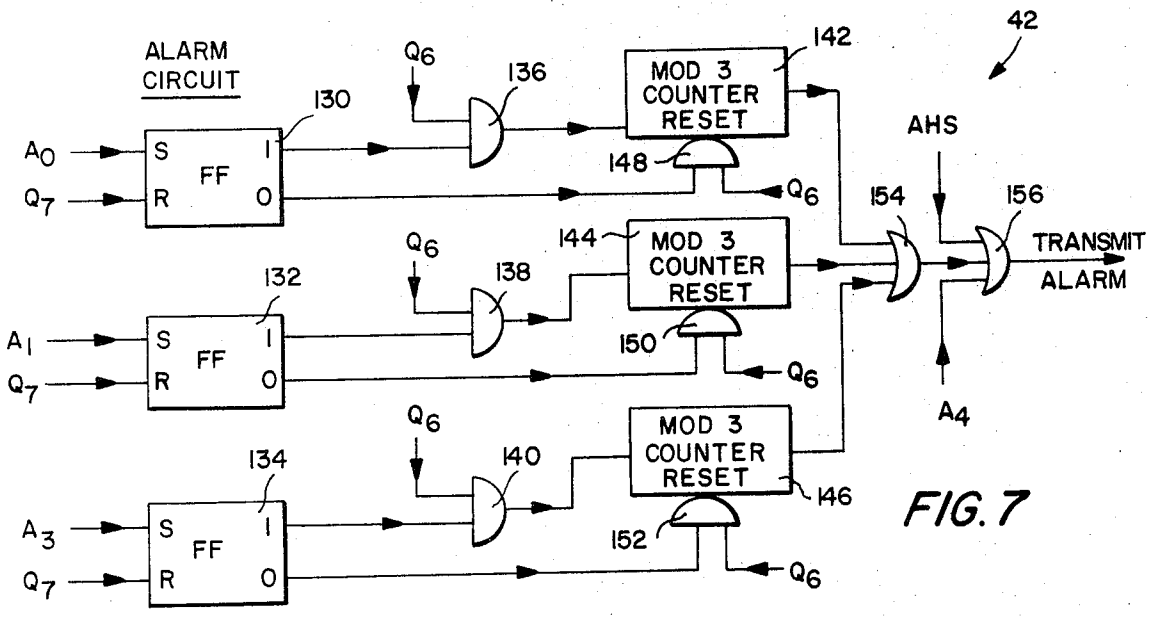


FIG. 7

HEART SURVEILLANCE DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to heart monitoring devices and more specifically to a heart rate surveillance device which provides an indication of a dangerous heart condition with the minimization of false alarms.

2. Description of the Prior Art

Generally, patients with acute myocardial infarctions are kept under observation for 72 hours in a Coronary Care Unit. During this time, the instance of potential fatal arrhythmiae is the greatest. The patients are then transferred to a regular medical ward for up to 21 days where they are given normal care and kept under partial observation. In the general medical ward, the heart patient is not given sufficient care nor monitoring and an alarming number of patients die suddenly and unexpectedly out of the intensive care units.

A majority of the heart monitoring devices are fairly complex and expensive. They are used specifically in operating rooms and intensive care units for monitoring the ECG-QRS wave form. The expense of the prior art units have made their use in the general ward prohibitive. Other units have been provided which give alarms or indication of fast or slow heart rates, but they do not give indications of any other abnormal heart conditions which lead to heart failure or to an early indication of serious heart anomaly.

The prior art heart rate monitoring devices have been so sophisticated and transmit so much information that the staff which must monitor them in the general wards tend to ignore their frequent indications or turn them off. Consequently, there exists a need for an inexpensive heart monitor which will minimize the number of false alarms and produce an indication which the monitoring personnel find credible.

SUMMARY OF THE INVENTION

The present heart surveillance device provides an alert mechanism to a distant nursing station from any room, semi-private or private, within a hospital complex. The severe conditions which the present device would monitor provides an indication of: a complete heart blockage or stoppage; an abnormally high heart rate or tachycardia; an abnormally low heart rate such as in the case of partial or complete heart block, in effect producing a bradycardia; and a sudden change of heart rate or a change in a previously established rate pattern, such as sudden and spontaneous auricular fibrillation or frequent runs of premature ventricular contractions as well as bigeminy and other manifestations of toxicity. An immediate indication is given of the complete heart block and a change of heart rhythm persisting for twenty seconds while the occurrence of tachycardia or bradycardia or sudden changes in the heart rate is indicated if they occur in three consecutive analysis periods. The use of three consecutive alarms and the twenty second verification period lowers the false alarm rate and prevents an alert from being transmitted due to an abnormal artifact such as muscle spasm or movement of the EKG probe. Digital logic with a free running clock is used to measure time periods and a second clock for command signals is used for the determination of the conditions listed above. The present device measures the time between every other heart beat rather than each ventricular complex because of the frequent presence of occasional but not crucial premature ventricular contractions which can occur in normal individuals without danger to their welfare and which are never considered to be pathological when few in number. Since a premature ventricular contraction and a normal heartbeat will equal two normal heartbeats, the measuring of the period between every other heartbeat minimizes the effect of nonreoccurrence of premature ventricular contractions. Thus, unnecessary false alarms will be minimized.

OBJECTS OF THE INVENTION

Accordingly, it is an object of the present invention to provide a heart surveillance device which is relatively inexpensive and minimizes the number of false alarms so as to increase credibility of indications.

Another object is to provide an indication to hospital personnel who do not have the time for intensive monitoring and indication of the onset or occurrence of a dangerous heart condition by preprocessing the EKG waveform at bedside and transmitting an alert rather than transmitting the EKG to a central processing station.

A further object of the invention is the provision of immediate indication of heart stoppage or a change in heart rhythm and an indication of the continuance over a selected number of periods of slow heart rate, fast heart rate, or sudden changes of heart rates.

Still another object of the invention is to provide a simple and inexpensive digital logic to provide indications previously enumerated.

Other objects, advantages and novel features of the present inveniton will become apparent from the following detailed description of the invention when considered in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating the components of the heart surveillance device according to the present invention;

FIG. 2 is a schematic of the logic of the pulse count circuit;

FIG. 3 is a schematic of the logic of the counter and register circuit;

FIG. 4 is a schematic of the logic of the fast-slow counter magnitude and compare circuit;

FIG. 5 is a schematic of the logic of the rate change circuit;

FIG. 6 is a schematic of the logic of the heart stop circuit; and

FIG. 7 is a schematic of the logic of the alarm circuit.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 illustrates a preferred embodiment of the heart surveillance device having a pulse representing presence of a QRS heart signal at input **12.** The QRS pulse is produced by amplification, filtering, double differentiation and a pulse generation circuit, all of which are not shown since they are well known in the art and are not a part of the present invention. The QRS pulse is applied to heart stop circuit **14** which produces a heart stop alarm signal if a heartbeat does not occur

within a predetermined time following the previous heartbeat. As is true with all of the circuits of the present invention, time intervals and periods are measured and logic functions are performed digitally. Thus, heart stop circuit **14** is driven by a pulse train from clock A to determine the predetermined time. The QRS input pulse at **12** is also applied to the pulse count circuit **16** which is also driven by clock A, which produces an output pulse P3 upon the occurrence of every other QRS input. The pulse P3 is applied to logic control circuit **18** which is a shift register driven by clock B and has successive outputs Q0–Q7.

Clock circuit **20** is a free running multi-vibrator producing a first pulse train at **22** designated as clock B of a frequency of 960 Hz and a second pulse train designated as clock A at output **24** of a frequency of 60 Hz. The 960 Hz pulse train is converted to the 60 Hz pulse train by a divide-by-16 counter **26.** Any clock circuit or plurality of clock circuits may be substituted for the multi-vibrator **20,** as well as the 960 Hz and 60 Hz pulse trains. The important factor is that the relationship between pulse trains of clock A and clock B must be such that the logic control signals Q0–Q7 occur between pulse P3 and the succeeding pulse of clock A.

The heart rate between alternate QRS inputs is measured by counter and register circuit **28** whereby clock A drives a counter until set by logic control pulse Q4 which causes the count to be moved from the counter to the register and be stored therein. Upon the application of logic control pulse Q5 to counter and register circuit **28,** the counter is cleared and starts a new measuring interval. Counter and register circuit **28** has an output M at **30** which represents the present count and an output R at **32** which represents the stored count of the previous interval. The values of M and R from outputs **30** and **32** are connected to the fast slow and counter magnitude compare circuit **34.** Upon the application of logic control pulse Q0, the present value of the heart count M is first compared with a user selected count representing, for example, **100** beats per minute to determine whether the heartbeat is in tachycardia. Upon the application of logic control pulse Q1, the value M is then compared with a second user selected count representing, for example, 60 beats per minute, to determine whether the heart rate is in bradycardia. It is important to realize that higher counts represent slower heart rates and vice versa. Upon the application of logic control pusle Q2, the value M for the present analysis interval is compared with the value R of the previous interval to determine which is larger. If the present count M is smaller than the first reference count, the heart rate is too fast, and the fast/slow and counter magnitude compare circuit **34** produces an output signal A0; and if the count M is larger than the second reference count, the heart rate is too slow and the compare circuit produces an output A1. The fast/slow and counter magnitude compare circuit **34** also provides an output on line **36** indicating that the stored value R of the previous interval is greater than the present count M and provides an output on line **38** if the previous stored count R is equal to or less than the present count M.

The present count M on line **30** and the previous count R on line **32,** as well as the signal representing whether R is larger than, equal to or smaller than M from lines **36** and **38** are all connected to the rate of change circuit **40.** A rate of change is calculated in response to logic control pulse Q3 to determine whether the difference between the present count M and the previously stored count R is greater than a user specified count K. The particular circuit, to be explained later, adds K to the smaller of R or M and compares it with the larger of R or M and produces an alarm output signal A3 if the heart rate has changed from one cycle to the next by a count of more than K. Rate change circuit **40** also uses the input information to determine whether the heart rate has changed by more than K only once in twenty seconds and thus assumed a new rhythm. Alarm signal A4 is an indication that there has been a one-time transient rhythm change. Logic control pulse Q7 is also fed into rate change circuit **40** to reset the rhythm change alarm logic.

The alarm heart signal (AHS) from heart stop circuit **14,** the too-fast alarm signal A0, and the too-slow alarm signal A1 from fast-slow and counter magnitude compare circuit **34,** the change of rate alarm signal A3 and the change of rhythm alarm signal A4 from rate change circuit **40** are all fed into an alarm circuit **42.** Alarm circuit **42** also has inputs for logic control pulses Q6 and Q7. An alarm signal is transmitted from alarm circuit **42** either through a nurse's call button or by FM transmission to a nurses' station **44.** The nurses' station **44** is shown having a plurality of lights and/or aural alarms **46** which would indicate an alarm condition in a specific heart surveillance unit.

It has been found that in order to reduce the number of false alarms transmitted, the occurrence of a fast heart rate (A0) or the occurrence of a slow heart rate (A1), or the occurrence of a drastic rate change (A3), should be monitored to determine if the individual alarm signals occur for three consecutive analysis intervals. Thus, the alarm circuit **42** uses a logic control signal Q6 to increment the logic to measure the occurrence of a given alarm condition for three consecutive intervals and logic control pulse Q7 is used to reset the flip-flops as will be explained later.

The use of three consecutive signals prevents the transmission of alarm for premature ventricular contractions and various noise and artifact conditions. For example, if the premature ventricular contraction occurs on the third QRS beat, the interval between beats 1 and 3 would be short and the intervals between beats 3 and 5 would be long. Thus, the rate change circuit could produce an alarm signal A3 during two intervals for a premature ventricular contraction occurring on the third beat, and yet alarm circuit **42** will not transmit an alarm because of the normality of the interval between heartbeats 5 and 7. It is highly improbable that premature ventricular contractions, except for an abnormal condition, will occur frequently enough to produce the false alarm prevented by the present system. The alarm signals AHS and A4, representing a heart stop alarm and change of rhythm alarm respectively, are immediately transmitted by alarm circuit **42** to the nurses' station **44** without delay or storage for consecutive intervals.

The specific digital logic for the circuits shown in FIG. 1 are illustrated in FIGS. 2–7. The pulse counter circuit **16,** as shown in FIG. 2, has the QRS input at **12** fed into two JK flip-flops **48** and **50** which, in combination with and gate **52,** comprises a mod 3 counter. Upon the occurrence of the third QRS input, or every other input thereafter, the two JK flip-flops **56** and **58** receive an input signal from andgate **52** and upon the

receipt of a pulse from clock A, transmit a pulse P3 through andgate **60.** The two JK flip-flops **56** and **58** are reset from a signal from andgate **54** and the JK flip-flops **48** and **50.** As noted in FIG. **1,** the output pulse P3, which represents every other QRS input, is transmitted to logic control circuit **18.**

The counter and register circuit **28** is shown in FIG. **3** as having an 8 bit counter **62** and an 8 bit register **64.** Counter **62** is driven by the pulses from clock A and is reset by control logic pulse Q5. The 8 bit register **64** loads the count M from counter **62** upon receipt of logic control pusle Q4. The electrical interfaces in FIG. **3** representing the present count M of 8 bit counter **62** and the previous count R in 8 bit register **64** are represented by double lines but are to be taken as 8 electrical connections transferring bit for bit the count in **62** to the register of **64.** The output **30** of the count M and **32** of the count R are also shown in FIG. **3.**

The fast/slow and counter magnitude comparing circuit **34,** as shown in FIG. **4,** has an 8 bit magnitude comparer **66** which receives the count stored in counter 62 bit by bit by a connection **30.** The 8 bit magnitude comparer **66** must compare the present count M with a user specified reference for fast count which will be T, with a user specified reference for a slow count which will be B, and with the previous count R in register **64.** The count or value per bit for the references T and B and the previously stored count R are transmitted through nandgates **68, 70** and **72** in response to logic control pulses Q0, Q1 and Q2, respectively. The outputs of the nandgates are fed through a nandgate **74** to one bit in the magnitude comparator **66.** The nandgates **68, 70, 72** and **74** comprise the logic for only one bit and it is to be understood that each bit has identical logic.

The magnitude comparator **66** has an output **76** which indicates that the number count M is larger than the other input via nandgate **74** and an output **78** which indicates that the count M is less than the input through nandgate **74.** At Q0, the value T is loaded into the magnitude comparator **66** with the value M. If the heart rate is too fast, which indicates tachycardia, an output will appear on line **78** which is gated with the logic control pulse Q0 to andgate **80** to produce alarm signal A0. Upon the application of logic control pulse Q1, the value B is loaded into magnitude comparator **66** to be compared with the value M and provides an output on **76** indicating bradycardia, if the value M is greater than B. The output on **76** is gated with logic control pulse Q1 to andgate **82** to provide an alarm output A1 indicating slow heartbeat.

Upon the application of control logic pulse Q2, the value of the previously stored count R is loaded into magnitude comparator **66** from nandgate **72** to be compared with the present count M. If the value R is greater than the value M, an output appearing at **78** is transmitted through andgate **8** by the control signal Q2. If this output is present, an output on line **36** indicates that R is greater than M. If the signal is not transmitted through andgate **84,** the inverter **86** provides an output at **38** indicating that M is greater than or equal to R. This is to be used in the rate change circuit as will be explained hereafter. Thus, the fast-slow and counter magnitude compare circuit compares the first reference value T for determining tachycardia on the application of logic control signal Q0; compares a second reference value B for determining bradycardia on the application of logic control signal Q1; and compares the previously stored count R with the present count M to determine which is the larger in response to logic control signal Q2.

The rate change circuit **40,** as illustrated in FIG. **5,** has the inputs **36** indicating that R is greater than M and the input **38** indicating that M is greater than or equal to R connected to the set and reset terminals of flip-flop **88,** respectively. The one output logic from flip flop **88** indicating that R is greater than M at **90** is connected to nandgate **92** and **94,** whose other input is the value R and the value M, respectively. Similarly, for the zero output at **96,** it is connected to nandgates **98** and **100,** whose other inputs are the value M and R, respectively. Thus, if R is greater than M, flip-flop **88** has an output on the logic **1** at **90,** nandgates **92** and **94** would basically be inhibited and a single bit of value R would be transmitted through nandgate **104** and a single bit of value M would be transmitted through nandgate **102.** Obviously, if the reverse were true and M was greater than or equal to R, flip-flop **88** would have an output on the zero logic **96** and a single bit value of M would be transmitted through nandgate **94** and the value of R would be transmitted through nandgate **102.**

The smaller of the two values R and M, which is transmitted through nangate **92** or **98,** is loaded into an **8** bit full adder **100** through nandgate **102.** Herein the user selected value K is added to the smaller of the values of R or M. As noted previously, the logic elements **92, 98** and **102** are shown for one bit only and thus there will be eight of these so that the 8 bit adder can be fully loaded. The sum of the smaller of R or M and the value K is loaded into an 8 bit magnitude comparator **106.** Here the value of the sum is compared with the value of the larger of R or M as transmitted through nandgates **100** or **94** and nandgates **104** and andgate **108** which is activated by logic control pulse Q3. As indicated above, logic elements **100, 94, 104** and **108** are shown only for a single bit. The output at **110** of magnitude comparator **106** indicates that the value of the smaller of R or M added to K is greater than the larger of R or M. This signal is gated by logic control signal Q3 in andgate **112** to produce rate change alarm A3. Thus, upon the occurrence of logic control pulse Q3, the value of the present count M and the value of the previous count R and the constant K are compared to determine whether the change of heartbeat rate between R and M has exceeded the constant K and thus provides a rate change alarm signal A3.

Rate change circuit **40** also includes circuitry to determine whether there has been a single change of rhythm. The A3 rate change alarm signal is transmitted to the set terminal of flip-flop **116.** The one output of flip-flop **116** is connected to andgate **118** whose other input is logic control pulse Q7. The output of andgate **118** is connected to a 20-second timer **120** which could be a counter driven by the pulses of clock A. The 20-second timer **120** is reset by the rate change alarm signal A3. The reset terminal of flip-flop **116** is connected to A4. The occurrence of the first rate change alarm signal A3 starts the timer **120.** If another rate change alarm signal A3 does not occur within **20** seconds, timer **120** will produce a change of rhythm alarm signal A4. This is accomplished by the use of the logic control pulse Q7 which allows the timer to be reset by A3 before being triggered by the following Q7 pulse. Suc-

ceeding Q7 pulses will not affect the timer mechanism. If, before the timer reaches 20 seconds, another A3 pulse is generated, the timer will be reset and be retriggered by the next Q7 pulse. Thus, a change of rhythm alarm A4 is generated if after having generated a single A3 alarm, no additional A3 alarm is generated for at least 20 seconds following the first alarm signal A3. That is, the heart has changed from one stable rhythm to another stable rhythm exceeding the rate of change factor K.

Heart stop circuit 14, as illustrated in FIG. 6, has an 8 bit counter 124 that is driven by clock A and reset by the QRS input pulses representing the beat. If counter 124 should reach the count 256, nandgate 126 will be in its low logic state and inverter 128 will produce a heart stoppage alarm signal AHS. Thus, an alarm is set if the heartbeat is not received within 4.25 seconds (for clock A at 60 Hz) from the last received heartbeat. The count 256 and the timer are but examples of limits to which the system can be set.

The heart stop alarm signal AHS from circuit 14, the fast heart rate signal A0 and the slow heart rate signal A1 from fast-slow encounter magnitude comparer circuit 34, and the rate change alarm signal A3 and the rhythm change alarm signal A 4 from rate change circuit 40 are all transmitted to alarm circuit 42 illustrated in detail in FIG. 7. The alarm signals A0, A1 and A3, are connected to the set input of flip-flops 130,132 and 134, respectively. The one logic output of flip-flops 132,130 and 134 are connected to andgates 136, 138, and 140, whose other input is logic control pulse Q6. The output of the andgates 136,138 and 140 are connected to mod 3 counters 142, 144 and 146, which are reset by andgates 148, 150 and 152, respectively. The outputs of the mod 3 counters 142, 144, 146 are fed into an OR gate 154 which has its output connected to OR gate 156. Also connected to the input of OR gate 156 are the heart stop alarm signal AHS and the rhythm change alarm signal A4. The output of 156 is transmitted as an alarm signal to the nurses' station 44 shown in FIG. 1.

The alarm circuit 42 takes the alarm signals A0, A1 and A3 and sets the respective flip-flops if any one of the signals occur. When logic control pulses Q6 occur, the mod 3 counters 142, 144 and 146 are incremented by one if the alarm signal is present. Q7 then resets all the flip-flops 130, 132, 134. Upon the next interval between every other pulse, if alarm signal A0, A1 or A3 is not present, the flip-flops 130, 132, 134 remain in their reset state and upon the occurrence of control logic pulse Q6 andgates 148, 150 and 152 reset the mod 3 counters 140, 144 and 150. But if one of the alarm signals A0, A1, A3 occur during three consecutive intervals, the flip-flops 130, 132, 134 will always be in the one state and transmit on the occurrence of logic control pulse Q6 through andgates 136, 138, 140 to increment the mod 3 counters 142, 144 and 146 to a count of 3 and produce an output signal. Thus, if either alarm signal A0 or alarm signal A1 or alarm signal A3 individually occurs for three consecutive analysis intervals, an output is transmitted through OR gate 154 and 156 to be transmitted to the nurses' station. The severity of heart stoppage or change of rhythm is built into the present system by the transmission of the heart stop alarm signal AHS and the rhythm change alarm signal A4 directly through OR gate 156 to the nurses' station.

The logic control circuit, as shown in FIG. 1, is used to transfer information, reset counters and flip-flops and perform certain comparisons and calculations in a given sequence at a given time. The circuit may be comprised of two 5 bit shift registers in tandem, which upon receipt of the P3 pulse representing every other QRS input pulse from the pulse counter circuit 16, can generate 8 consecutive pulses at the frequency of clock B. Since the clock B is at a much higher frequency than clock A, the logic control pusles Q0-Q7 occur well before the arrival of the next pulse from clock A and are used as follows:

Q0 = compare count for high heart rate or tachycardia;

Q1 = compare count for low heart rate or bradycardia;

Q2 = compare current count M with previous count R;

Q3 = sum K with the smaller of the current count M or the previous count R and compare with larger of the current count M or the previous count R

Q4 = load current count M into storage register

Q5 = clear counter

Q6 = incrementing mod 3 alarm counters or resetting said counters;

Q7 = reset alarm flip-flops and initiate change of rhythm timer;

The heart surveillance device of the present invention is a digital system providing an alarm upon the occurrence of a fast heart rate or a slow heart rate or a drastic change of rate individually during three consecutive intervals or an alarm instantaneously for a heart stoppage or a change of heart rhythm. The system measures the heart rate between every other heartbeat and consequently reduces the number of false alarms transmitted. A sequence of logic control pulses Q0–Q7 perform the following in sequence:

The present heart rate is compared with a first user selected standard to determine tachycardia;

the present heart rate is compared with a second user selected standard to determine bradycardia;

the present heart rate is compared with the heart rate from the previous period;

a user selected constant, the present heart rate, and the previous interval heart rate are compared to determine whether there has been a drastic change rate of heart rate;

the present heart rate is transferred to storage, thus representing the previous interval heart rate;

the present heart rate counter is cleared;

and the alarm logic is incremented and/or cleared.

Although the invention has been described and illustrated in detail, it is to be clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation. The frequency of the clocks A and B and the reference values selected for tachycardia, bradycardia, K, as well as the 20-second timer for rhythm change are but examples, the spirit and scope of the invention being limited only by the terms of the appended claims.

What is claimed:

1. A device for monitoring heart rate comprising:

means responsive to every other heart beat for producing a signal proportional to time therebetween;

means for storing said time signal;

means for establishing a first, second and third reference signals;

means for comparing said time signal with said first reference signal and with said second reference signal and producing a first output signal when said times signal is greater than said first reference signal or less than said second reference signal;

means for comparing said time signal, a previously stored time signal, and said third reference signal and producing a second output signal when difference between said time signal and said previously stored signal exceeds said third reference signal; and

means for indicating presence of said first or second output signals.

2. A device as in claim **1** including means for measuring time between every heartbeat, and for producing a third output signal when said measured time exceeds a first reference value.

3. A device as in claim **2** including means responsive to said second output signal for producing a fourth output signal if said second output signal does not reoccur in a predetermined period of time.

4. A device as in claim **3** wherein said indicating means instantaneously indicates presence of said third or fourth output signals.

5. A device as in claim **4** wherein said indicating means provides an indication of the presence of said first or said second output signals for at least three consecutive time signals.

6. A device as in claim **1** wherein said first output signal comprises a fifth output signal for a time signal greater than said first reference signal and a sixth output signal for a time signal less than said second reference signal, and said indicating means providing an indication for presence of said second output signal for at least three consecutive time signals, of said fifth output signal for at least three consecutive time signals, and of said sixth output signal for at least three consecutive time signals.

7. A device as in claim **1** wherein said means for comparing said time signal, said stored time signal and said third reference signal comprises means for determining which is larger, said time signal or said stored time signal, means for adding said third reference signal to the non-larger time signal, and means for producing said second output signal when the sum of said third reference signal plus said non-larger time signal exceeds said larger time signal.

8. A device for monitoring heart rate comprising:

a first clock means for producing a first series of pulses at a first rate;

a second clock means for producing a second series of pulses at a rate slower than said first rate;

a first pulse accumulator means for accumulating said second series of pulses;

a storage means for storing a previous accumulated count;

first comparison means for comparing said accumulated count with a first and a second reference count and producing a first output if said accumulated count exceeds said first reference and a second output if said second reference exceeds said accumulated count;

second comparison means for comparing said accumulated count and said stored accumulated count and producing a third output if said accumulated counts differ by a predetermined value; and

control means responsive to every other heartbeat to produce a series of control pulses at said first pulse rate for stopping said first pulse accumulation, transferring said accumulated pulses to said storage means, and activating said first and second comparison means between a last pulse of accumulated count and a next pulse of said second series of pulses.

9. A device as in claim **8** including a second pulse accumulator means for accumulating said second series of pulses and for producing a fourth output at a predetermined accumulated count; said second pulse accumulator being reset at every heartbeat.

10. A device as in claim **8** including a timing means initiated by a first third output and reset by a subsequent third output for producing a fifth output if not reset before a preset time period.

11. A device as in claim **8** including an indicator means for indicating the existance of said first or second or third output for at least three accumulated counts.

12. A device as in claim **8** wherein said control means initiates on a first control pulse said first comparison means for said first output, initiates on a second control pulse said first comparison means for said second output, initiates on a third control pulse said second comparison means for said third output, transfers on a fifth control pulse said accumulated count to said storage means, and clearing on a sixth control pulse said first accumulator means.

13. A device for monitoring heart rate comprising:

means for measuring heart rate over a period defined by alternate heart beats;

means for storing a previous measured heart rate;

means responsive to said measured heart rate for producing a first output when said measured heart rate is below a first predetermined value;

means responsive to said measured heart rate for producing a second output when said measured heart rate is above a second predetermined value;

means responsive to said measured heart rate and said stored heart rate for producing a third output for a rate change above a third predetermined value; and

means for indicating the existence for at least three consecutive periods of any one of said outputs.

14. A device as in claim **13** including:

means for producing a fourth output when a heartbeat does not occur within a first predetermined time;

means responsive to said third output for producing a fifth output for a change of rhythm; and

said indicator means indicating the existence of said fourth or fifth output immediately.

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