

[54] **FAIL-SAFE CODE KEYING TRANSMITTER**

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[51] Int. Cl. **H04b 1/04**

[58] Field of Search ... 325/105, 123, 161, 170, 164;
307/260, 261; 328/21, 165, 167; 332/37 R,
37 D; 178/66 A, 68

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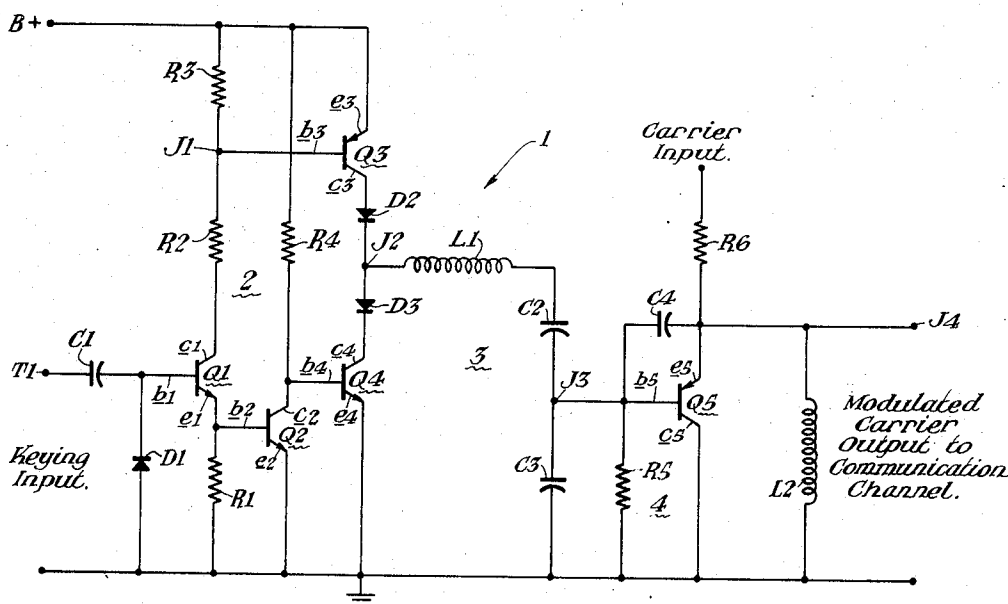
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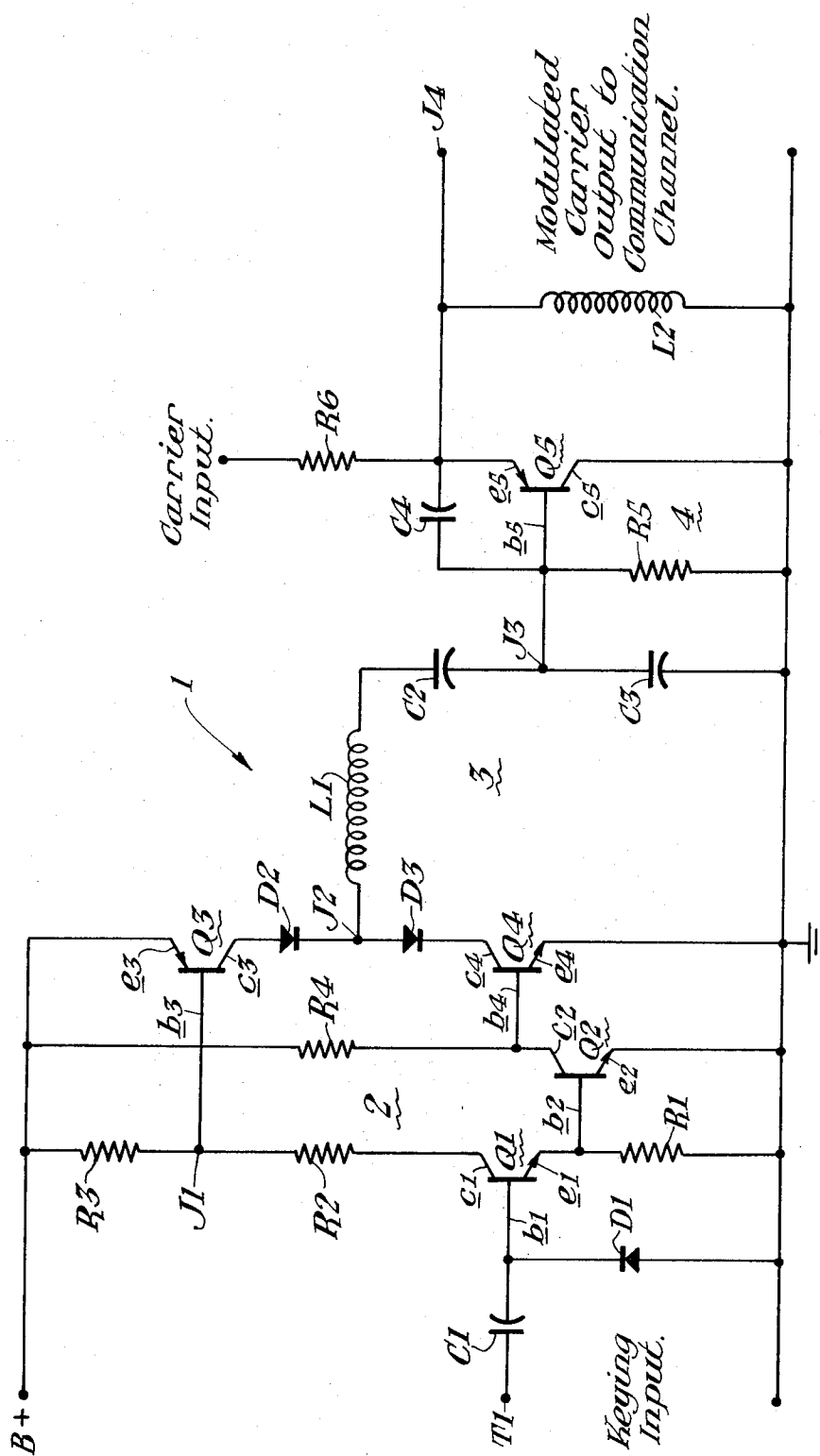
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ABSTRACT

This disclosure relates to a fail-safe code keying transmitter wherein a modulating signal is reshaped to remove the harmonic producing portions therefrom prior to the modulation of a carrier wave. The code keying transmitter includes an electronic switching circuit and a series resonant L-C circuit for transforming the leading edge of the square-wave input signal into one half cycle of a cosine wave and for transforming the trailing edge of the square wave input signal into another half cycle of a cosine wave and employs a modulating circuit for varying the carrier wave in accordance with the transformed cosine wave.

6 Claims, 2 Drawing Figures





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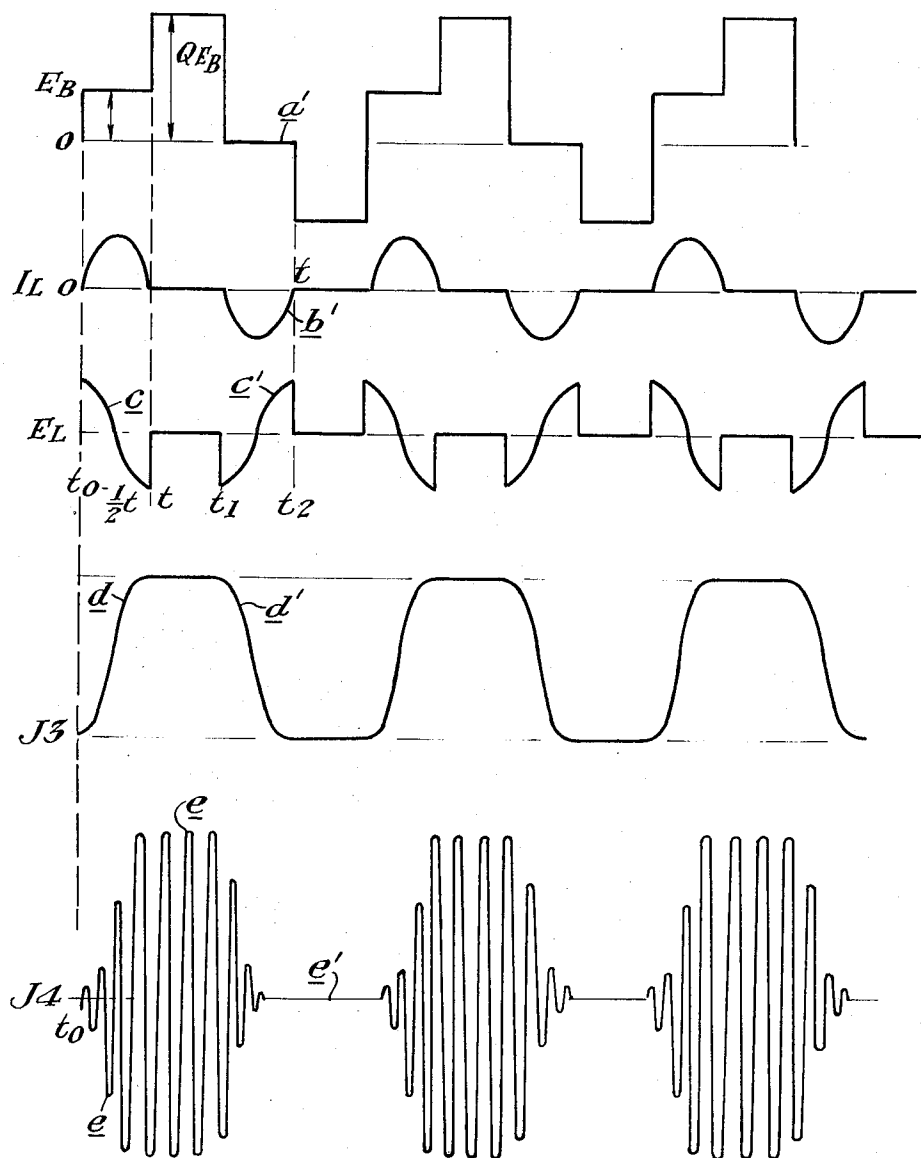


Fig. 2.

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FAIL-SAFE CODE KEYING TRANSMITTER

My invention relates to a coded type of fail-safe keying transmitter and more particularly to an electronic transmission circuit arrangement for removing sharp harmonic producing portions from a square wave signal by transforming the leading and trailing edges of the square wave signal into appropriate sections of a raised cosine wave and for modulating a carrier frequency signal in accordance with the raised cosine wave.

In certain types of signal and communication systems, such as railroad and mass and/or rapid transit operations, information and commands are transmitted from one location to another in coded form. Usually the coded format takes the form of a series of marks and spaces, such as a train of rectangular or square wave pulses. It will be appreciated that rectangular or square waves have sharp demarcation portions which are troublesome to various circuits, particularly to carrier transmission systems which employ tuned receiver circuits. The problem arises from the fact that a rectangular wave form contains an infinite number of harmonics of the fundamental frequency. It has been found that these harmonics are capable of interfering with the normal operation of other receiver circuits in the system. For example, a harmonic of sufficient amplitude will pass through an unrelated receiver circuit tuned to the frequency of the harmonic and will cause the receiver to perform its function, such as, picking up or energizing a relay or the like. In a vital transmission system, this is wholly unacceptable in that a falsely operated circuit could establish a condition which could cause damage to the equipment or could result in injury or death to attending personnel. Thus, the harmonics should be removed from the coded signals prior to usage in a vital type of transmission system. In an ordinary or nonvital system, it is desirable to eliminate the harmonics simply in order to prevent cross-talk and noise signals from interfering with other circuits. Another requirement of a vital operation is that each portion or circuit of the transmission system itself must be capable of functioning in fail-safe fashion. Thus, under no circumstance should a critical circuit or component failure be permitted to allow a transmitter to produce a modulating signal having a square wave envelope, except at greatly reduced levels.

Accordingly, it is an object of my invention to provide a circuit arrangement for shaping the wave form of a modulating signal in order to remove the presence of harmonics prior to the modulation of a carrier wave.

Another object of my invention is to provide a fail-safe code keying transmitter circuit for removing sharp harmonic producing portions from a modulated carrier wave form.

A further object of my invention is to provide a fail-safe circuit arrangement for transforming the leading and trailing edges of a square wave signal into the respective half cycles of a raised cosine wave and thereafter modulating a carrier signal for transmission over a communication channel.

Yet another object of my invention is to provide a transmitter circuit which eliminates harmonics in a modulated carrier signal and which operates in a fail-safe manner.

Yet a further object of my invention is to provide a code keying carrier transmitter for producing a modulated carrier signal having an envelope in the form of

a raised cosine wave so that harmonics are not present.

Still another object of my invention is to provide a new and improved transmitter for transforming harmonic frequency signals from a substantially square wave form by transforming the leading edge of the wave form into one half cycle of a raised cosine wave and by transforming the trailing edge of the wave form into the other half cycle of a raised cosine wave and thereafter modulating a carrier signal with the transformed wave.

Still a further object of my invention is to provide a wave shaping circuit which eliminates sharp harmonic producing portions of a modulated carrier signal and which does it in a fail-safe fashion.

Still yet another object of my invention is to provide a fail-safe electronic circuit arrangement including a switching circuit and a series L-C network which removes harmonic producing portions of an input signal by transforming each harmonic producing portion into a cosine function and a modulating circuit having a carrier input which is modulated by the transformed signal.

Still yet a further object of my invention is to provide a code keying transmitting circuit including an electronic switching circuit, an inductance-capacitance circuit and a clipping modulating circuit which are economical in cost, simple in construction, reliable, and efficient in operation.

Briefly, the present invention relates to a fail-safe code keying transmitter including an electronic switching circuit, a series resonant L-C circuit, and a clipping modulating circuit. The electronic switching circuit employs a pair of driving transistors and a pair of series-connected driven transistors. The driving transistors are connected in cascade so that both transistors are simultaneously rendered conductive and nonconductive by the square wave input signals. The conduction of the driving transistors causes one of the driven transistors to be conductive and causes the other driven transistor to be cut off. The conduction of the one driven transistor establishes a charging circuit path for the series resonant L-C circuit so that the leading edges of the square wave input signals are transformed into one half cycle of a raised cosine wave. Conversely, the nonconduction of the driving transistors causes the one driven transistor to cut off and causes the other driven transistor to conduct. The conduction of the other driven transistor establishes a discharge circuit path for the series resonant L-C circuit so that the trailing edges of the square wave input signals are transformed into another half cycle of a raised cosine wave. The transformed waves are applied to the input of the clipping modulating circuit upon which is impressed a carrier signal. A modulated carrier signal is derived from the output of the modulating circuit and the modulations will have an envelope in the form of a raised cosine wave so that no accompanying harmonics are transmitted over the communication channel.

The foregoing objects and other additional features and advantages of my invention will become more fully evident from the following detailed description when considered in connection with the accompanying drawings wherein:

FIG. 1 is a schematic circuit diagram illustrating a preferred embodiment of the present invention.

FIG. 2 is a diagrammatic illustration of a series of wave forms which will be helpful in understanding the

theory and operation of the present invention shown in FIG. 1.

Referring now to the drawings and in particular to FIG. 1, there is shown a fail-safe code keying transmitter circuit which is generally represented by the numeral 1. The code keying transmitter circuit 1 includes a switching circuit generally characterized by the numeral 2, and a series-resonant circuit generally characterized by the numeral 3.

The switching circuit includes a driving network having a pair of cascaded transistors and a driven network having a pair of series connected transistors. The first stage of the driving network includes an NPN transistor Q1 having an emitter electrode *e1*, a collector electrode *c1*, and a base electrode *b1*. The base electrode *b1* of transistor Q1 is connected to input keying terminal T1 through coupling capacitor C1. The emitter electrode *e1* of transistor Q1 is connected to a reference potential, such as ground, by resistor R1. A diode D1 has its cathode connected to the base electrode *b1* of transistor Q1. The anode of diode D1 is directly connected to ground. The diode D1 limits the amount of reverse voltage that can be applied to transistor Q1 to prevent damage to the emitter-to-base diode or the transistor Q1 and also results in symmetrical clipping of the input signal. The collector electrode *c1* is connected to positive terminal B+ of a suitable source of d.c. supply potential (not shown) by a pair of series connected resistors R2 and R3.

The second stage of the driving network includes an NPN transistor Q2 having an emitter-electrode *e2*, a collector electrode *c2*, and a base electrode *b2*. The base electrode *b2* of transistor Q2 is directly connected to the emitter electrode *e1* of transistor Q1. The emitter electrode *e2* of transistor Q2 is directly connected to ground while the collector electrode *c2* of transistor Q2 is connected to the positive terminal B+ by resistor R4.

The driven network of the switching circuit includes a first PNP transistor Q3 having an emitter electrode *e3*, a collector electrode *c3*, and a base electrode *b3*. The base electrode *b3* of transistor Q3 is directly connected to a junction point J1 formed between resistors R2 and R3. The emitter electrode *e3* of transistor Q3 is directly connected to the positive terminal B+ of the d.c. supply source. The collector electrode *c3* of transistor Q3 is connected to the anode of an isolation diode D2. The cathode of the diode D2 is connected to a junction point J2.

The driven network also includes a second NPN transistor Q4 having an emitter electrode *e4*, a collector electrode *c4*, and a base electrode *b4*. The base electrode *b4* of transistor Q4 is directly connected to the collector electrode *c2* of transistor Q2 while the emitter electrode *e4* of transistor Q4 is directly connected to ground. The collector electrode *c4* of transistor Q4 is connected to the cathode of an isolation diode D3 while the anode of the diode D3 is connected to the junction point J2. Thus, it will be seen that the conductive condition of transistor Q3 is controlled by the transistor Q1 while the conductive condition of transistor Q4 is controlled by transistor Q2.

The series resonant circuit which is tuned to the fundamental frequency of the square wave signals applied to terminal T1 includes an inductor L1 and a pair of capacitors C2 and C3. One end of the inductor L1 is connected to the junction point J2 while the other end of

the inductor L1 is connected to the upper plate of the capacitor C2. The lower plate of the capacitor C2 is coupled to the upper plate of a capacitor C3 while the lower plate of capacitor C3 is directly connected to ground. The capacitors C2 and C3 form a capacitance divider wherein a preselected amount of output voltage is derived from across capacitor C3, namely, between junction point J3 and ground. For example, the capacitance divider permits the output voltage to be reduced to a given level and allows the d.c. zero line to be moved to an optimum position.

The clipping modulating circuit includes an active element in the form of a PNP transistor Q5 arranged in an emitter-follower configuration. The transistor Q5 includes an electrode amplifying emitter *e5*, a collector electrode *c5* and a base electrode *b5*. The base electrode *b5* of transistor Q5 is directly connected to junction point J3 and is connected to ground by biasing resistor R5 with resulting base injection. The collector electrode *c5* of transistor Q5 is directly connected to ground while its emitter electrode *e5* is connected to a suitable source of carrier wave signals by resistor R6. The collector electrode *c5* is also coupled to the base electrode *b5* by means of tuning capacitor C4. An inductor L2 is connected between the emitter electrode *e5* and collector electrode *c5*, and the modulated output signals are effectively derived across junction point J4 and ground, as will be described in detail hereinafter. It will be appreciated that the capacitor C4 and the inductor L2 form a resonant circuit which is tuned to the frequency of the carrier signal. It will be understood that since the capacitive value of capacitor C3 is several orders of magnitude greater than that of capacitor C4, the left-hand plate of capacitor C4 is effectively connected to ground so that an a.c. path is available for the carrier frequency signals.

In describing the operation, let us initially assume that the circuit is intact and is operating properly and that a series of coded square or rectangular waves are applied across input terminals T1 and T2. After a few cycles of operation, the output appearing across junction J4 and ground will be an amplitude modulated carrier signal having an envelope or outline of raised cosine waves. Thus, when a positive voltage appears on input terminal T1, the transistor Q1 is rendered conductive. The conduction of transistor Q1 causes forward biasing of the base emitter of the transistor Q2 so that transistor Q2 is also rendered conductive. The conduction of transistor Q2 zero biases transistor Q4 so that transistor Q4 is cut off. However, the conduction of transistor Q1 causes forward biasing of transistor Q3 so that transistor Q3 is rendered conductive. The conduction of transistor Q3 establishes a circuit path from the positive terminal B+ through emitter electrode *e3*, collector electrode *c3*, diode D2, through the series resonant circuit including inductor L1 and capacitors C2 and C3 to ground. Thus, the voltage at junction point J2 will suddenly rise to the B+ level, as shown in curve *a* of FIG. 2. The voltage swing is unimpeded since transistor Q4 is cut off. The increase in voltage causes current to begin flowing through the L-C circuit, and the amount of current flowing through the inductor L1 is represented by the wave form as shown by the curve *b* representing *I_L*. The current rises from a zero value to a maximum positive peak value and then returns to a zero level within a period of time dependent upon the L-C characteristic of the circuit. The reversal current

in inductor L1, which would normally occur in a resonant circuit, is prevented by the isolation diode D2. When the current through and voltage across inductor L1 return to zero, the junction J2 will be at the same potential as the voltage across capacitors C2 and C3, which will be supply voltage multiplied by the transistor Q5 resonant circuit formed by inductor L1 and capacitors C2 and C3. Conversely, the initial voltage across the inductor is at a maximum level but is 90° out of phase with the current as shown by the curve *c* of E_L . At $\frac{1}{2} t$, the voltage E_L passes through the zero point, and then reaches a maximum negative level at time t , at which time it quickly returns to the zero level. Initially, the voltage across capacitors C2 and C3 is at some negative value since E_C is a function of E_B and E_L , namely, $E_C = E_B - E_L$. The charging current builds up the voltage across the capacitors C2 and C3. Thus, the output voltage developed across capacitor C3 and appearing at junction J3 follows the wave form as shown by curve *d*, namely, a raised cosine wave. It will be appreciated that the rise time of the output wave form *d* is equal to one-half of a cycle of the resonant frequency of the L-C network. Thus the output voltage across capacitor C3 will continue to rise until a maximum level is reached at time t , as shown by curve *d* in FIG. 2. Thus, the leading edge of the pulse *a* is transformed into a gradual rising cosine wave so that the sharp harmonic producing portions are removed from the rectangular input signal. At time t , the voltage at junction point J2 is raised to Q times E_B where Q is the gain of the resonant circuit. The output voltage across capacitor C3 will remain at its maximum positive level throughout the remainder of the marking pulse. That is, since the current is at zero and the voltage across the inductor has returned to zero, the voltage will stop changing as shown by curve *d*. It will be noted that no power is lost during the period from t to t_1 , during the zero current period or dead space time since diode D2 blocks reverse current flow to the B+ supply terminal and the diode D3 and nonconducting transistor Q4 block current flow to ground and the resistive value of resistor R5 is relatively high so that little change occurs during this period.

Now when the trailing edge of the marking pulse appears at the input terminal T1, the transistor Q1 will revert to a nonconducting condition since the input voltage is zero during the ensuing spacing period. The nonconduction of transistor Q1 removes the forward biasing from base-emitter electrodes of transistor Q3 so that transistor Q3 is rendered nonconductive. In addition, the nonconduction of transistor Q1 removes the forward biasing from transistor Q2 so that it is rendered nonconductive. The nonconduction of transistor Q2 causes a positive biasing voltage to appear on the base electrode *b4* so that transistor Q4 is rendered conductive. The conduction of transistor Q4 establishes a discharge circuit path for the series resonant frequency circuit through diode D3 and the base-emitter electrodes of transistor Q4. The conduction of the transistor Q4 pulls the junction point J2 down to a zero potential or ground level, as shown by the curve *a'*. Thus, at time t_2 the current I_L begins flowing through inductor L1 in the reverse direction and goes through a negative cycle between times t_2 and t_3 as shown by the curve *b'*. Also at time t_2 the voltage across inductor E_L instantly goes to a maximum negative level and gradually moves in a positive direction until time t_3 , at which time it sud-

denly drops to a zero value as shown by the curve *c'*. Isolation diode D3 prevents the resonant circuit from causing current to flow in the reverse direction. During this period the voltage across capacitor C3 gradually decreases as shown by the curve *d'* which in fact is the other half cycle of the cosine wave form. Thus, during the trailing edge, the output signal also follows a cosine wave having a decay time which is proportional to one-half cycle of the resonant frequency of the L-C circuit. Again, the sharp harmonic producing portions of the input signal are removed so that unwanted harmonic frequencies are removed from the output. The output wave will assume a maximum negative level and will remain at this level until a subsequent marking pulse appears on the input terminal T1. That is, since the current is at zero and the voltage across the inductor has returned to zero, the voltage across capacitors C2 and C3 will stop changing. It will be appreciated that the peak-to-peak amplitude of the output voltage developed across capacitor C3 is $C3/(C2+C3)$ times the total voltage developed across capacitors C2 and C3, wherein the total voltage is Q times the voltage B+. It will be appreciated that each and every subsequent marking pulse of the train will cause a similar shaping effect so that no harmonics will exist in the output voltage developed across capacitor C3. Thus, the square or rectangular input signals are transposed into sections of raised cosine waves so that all harmonic frequencies are removed from the output voltage on junction J3.

If it is assumed that the carrier is undergoing full or 100 percent modulation, then the amplitude of the carrier is at times twice its unmodulated value, as shown at *e* in FIG. 2, and at other times zero as shown at *e'* in FIG. 2. As the instantaneous value of the modulating signal changes, it will be seen that a variation occurs in the biasing voltage on base electrode *b5*. At time t_0 , no output is available at the junction point J4 since the carrier signal is shunted to ground by the conduction of transistor Q5. That is, the junction point J4 is effectively tied to ground through the emitter-collector electrodes of transistor Q5. Now as the modulating signal begins to rise a reverse biasing voltage will appear on the base electrode *e5* of transistor Q5. It will be seen that the amount of voltage is equal to the instantaneous value as shown by curve *d*. Thus, the modulating signal will drive transistor Q5 to cutoff. The carrier signal is now fed to the resonant circuit formed by capacitor C4 and inductor L2. Now when the instantaneous positive value of the carrier signal exceeds the instantaneous value of the modulating signal, the transistor Q5 will begin conducting and will clip the remaining portion of the carrier signal. However, since the resonant circuit has sufficient Q , the inductance and capacitance will resonate at the frequency of the carrier and will cause the modulated output signal to have a negative portion as shown by $-e$. The modulating circuit will continue to clip the carrier signal in accordance with the instantaneous value of the modulating signal so that the leading edge of the modulated signal will resemble the wave form of curve *d*. If we assume that the peak value of the carrier signal is equal to the maximum value of the modulating signal, then the modulated signal will have a peak-to-peak value of twice the carrier signal during time t to t_1 . At time t_1 , the trailing edge *d* of the modulating signal will begin so that the amplitude of the modulated signal will commence to decrease until at time t_2 no modulations will be produced on junction

point J4. The same type of operation and modulation will occur upon the appearance of each subsequent modulating pulse so that the envelope or outline of the modulated signal will resemble the wave form of the modulating signal as shown in FIG. 2.

Further, as previously mentioned, the code keying transmitting circuit 1 operates in a fail-safe manner in that the failure of any active or passive element results in its inability to perform the necessary switching or modulating function. One of the most critical failures is the possibility of turns shorting in the inductor L1. However, while the shorting of turns causes a squaring of the output voltage, it will be appreciated that the amplitude of the output voltage will be only 1/Q times as great. Thus, it can be seen that any other failure which tends to distort the desired wave shape also greatly reduces the amplitude of the output. Therefore, most circuits will be insensitive and will not be adversely affected by such any spurious frequency signal generation at such greatly reduced levels. An unsafe failure could normally occur if the capacitor C3 would become open-circuited since the modulating signal would become distorted. However, it has been found that by employing the capacitor C3 as the return to ground path for the capacitor C4, the opening of the capacitor C3 interrupts the carrier frequency resonant circuit of the modulating circuit. Thus, even though the modulating signal is distorted, the modulating signal is no longer tuned to the carrier frequency so that little, if any, output is available at junction point J4. Thus, the code keying transmitter 1 operates in a fail-safe fashion to prevent harmonic frequencies from interfering with other frequency sensitive circuits in the system.

The modulated signals may be conveyed by a suitable communication channel, such as, line wires or track rails, to a remote location for controlling various functions in the field. Thus, the modulated signals present no interference problems to other tuned circuits in the area since the only sidebands would be those equal to the carrier frequency plus and minus the modulation frequency.

It is understood that while my invention has been described in relation to railroad and/or mass transit operations, it is quite obvious that its use is not merely limited thereto but may be employed in other surroundings and environments which have similar operating conditions and require the removal of harmonic frequency signals. It will also be apparent that some modifications and changes can be made in the presently described invention and, therefore, it is understood that

all changes, equivalents, and modifications within the spirit and scope of the present invention are herein meant to be included in the appended claims.

I claim:

1. A fail-safe circuit arrangement for removing sharp harmonic producing portions from square wave signals prior to modulation of a carrier wave signal comprising, a source of square wave signals, an electronic switching circuit connected to said source of square wave signals, said switching circuit including a first and a second driving transistor and a first and a second driven transistor, said first driving transistor controlling the conductive condition of said first driven transistor and said second driving transistor controlling the conductive condition of said second driven transistor so that said first and said second driven transistors are alternately rendered conductive, a series L-C circuit tuned to the fundamental frequency of said square wave signals connected to said first and said second driven transistors wherein the conduction of said first driven transistor causes the leading edge of said input signals to be transformed into one-half cycle of a raised cosine wave form and the conduction of said second driven transistor causes the trailing edge of said input signals to be transformed into another half cycle of a raised cosine wave form, and a clipping modulator circuit for varying the amplitude of a carrier signal in accordance with the transformed raised cosine wave form.

2. A fail-safe circuit arrangement as defined in claim 1, wherein said clipping modulator circuit includes a transistor amplifier connected in a common-emitter configuration.

3. A fail-safe circuit arrangement as defined in claim 1, wherein said slipping modulator circuit includes an L-C resonant circuit tuned to the frequency of said carrier signal.

4. A fail-safe circuit arrangement as defined in claim 3, wherein said L-C circuit includes a pair of capacitors forming a capacitance voltage divider.

5. A fail-safe circuit arrangement as defined in claim 4, wherein an a.c. circuit path for said L-C carrier resonant circuit is completed through one of said pair of capacitors forming the capacitance voltage divider.

6. A fail-safe circuit arrangement as defined in claim 1, wherein a first isolating diode is connected between the input of said L-C circuit and the output of said first driven transistor and a second isolating diode is connected between the input of said L-C circuit and the output of said second driven transistor.

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,794,920 Dated February 26, 1974

Inventor(s) John O. G. Darrow

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 8, line 34, "slipping" should be ---clipping---

Signed and sealed this 10th day of September 1974.

(SEAL)
Attest:

McCOY M. GIBSON, JR.
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents