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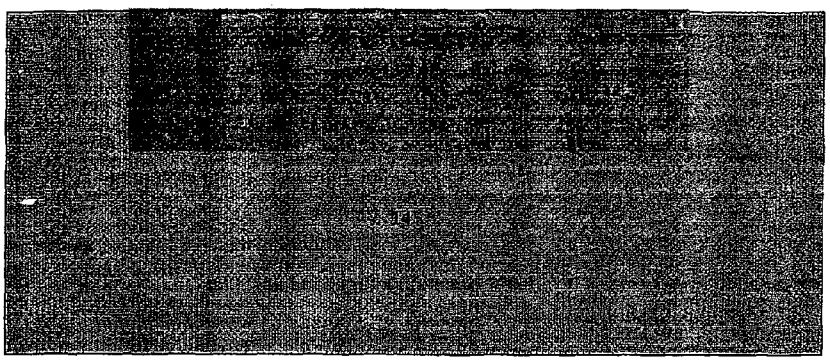

Figure 1.

(57) Abstract: The present invention provides a method to manufacture a silicon diaphragm, wherein an oxide layer (12) is embedded in the silicon substrate. (14) that acts as a support during the grinding and polishing processes. Further to that, the formation of the embedded oxide (12) is fully compatible with standard integrated circuit processing.

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SILICON DIAPHRAGM FORMATION WITH EMBEDDED OXIDE SUPPORT

Field of invention

The present invention relates to a silicon diaphragm with embedded oxide as support and specifically, a method to manufacture such diaphragm.

Background of the invention

Flexural silicon diaphragms or membranes are widely used in various types of bio- and RF-based micro-electromechanical devices and systems (MEMS). The said MEMS devices are actuators, capacitive sensors, pressure sensors, microphones etc, and micro-fluidic devices such as micro-pumps, micro-valves, and micro-dispensers.

The common methods to form silicon diaphragms are chemical etching, followed by etch-stop techniques and precision grinding and polishing. The main advantages in the silicon grinding process are its purely physical nature and its time efficiency, wherein the desired thickness of the silicon diaphragm can be obtained within a few minutes, as compared to etching process that may take hours to achieve. Also, it does not produce imperfections on the silicon diaphragm commonly found in chemical etching process, such as shallow pits or hillocks and micro-grass (black silicon).

Nonetheless, the grinding and polishing processes have its own weaknesses i.e. they can cause bending, cracking,

and deformation of the silicon diaphragm, especially when the diaphragm is grinded to less than 200 μm thick. As stated in Tables 1 and 2 in "Investigation of precision grinding process for production of silicon diaphragms", Prochaska et al., Journal of Micro/Nanolithography, MEMS and MOEMS, Vol. 1, 2002, the magnitude of the deformation relies on the thickness and diameter of the diaphragm. It is mainly because the diaphragm is unsupported by any means and the vacuum pressure acting on the diaphragm during the grinding process (Figure 4).

US patent no. 6551851 discloses a method to manufacture a silicon diaphragm that utilizes a precision grinding technique after etching a cavity in a wafer. The method comprising forming a diaphragm by reducing the thickness of a first wafer by grinding, wherein said diaphragm is supported by porous silicon during the grinding process. The porous silicon serves as a sacrificial material, which is then removed by means of chemical etching to form a cavity under the diaphragm. To produce the porous silicon, the silicon substrate is immersed in an acid mixture (hydrofluoric acid, ethanol and water), and the substrate is illuminated from the back using a tungsten halogen lamp (Figure 5). The depth of the porous silicon is in a range of 7 to 15 μm.

However, there are several issues associated with the use of porous silicon. For example, the porous silicon formation is a non-integrated circuit (IC) or complementary metal-oxide-semiconductor (CMOS) process. Due to the porosity nature of the silicon, deformation may take place during the grinding process. Also, the depth of the porous

silicon is only limited to less than 15 μm. Furthermore, the removal of the porous silicon after the grinding process involves the use of aqueous potassium hydroxide (KOH) solution, which is a silicon etch that may cause potential damage to the silicon diaphragm or other attached silicon-based structures due to its corrosive nature. Therefore, the etch rate must be slow enough to ensure that the reaction does not become violent, causing delicate microstructures to be destroyed by bubbles.

Luoto et al. (MEMS on cavity-SOI wafers, Solid-State Electronics, Vol. 51, 2007) describes a method to form silicon-on-insulator (SOI) wafers with pre-etched cavities (Figure 6), wherein the said method comprises the following steps: a cavity and pillars are etched into a handle substrate by using wet or dry etching methods, followed by thermal oxidation; direct bonding of the handle wafer to a diaphragm wafer; thinning of the diaphragm wafer by grinding and polishing; and removal of the thermal oxide on the silicon pillars.

As described above, the formed silicon pillars are not removed from the silicon diaphragm. The presence of the silicon pillars is not desirable, especially when there are other structures beneath the diaphragm or a large diaphragm deflection is required that is limited to a maximum of 2 μm. Also, to fabricate a diaphragm with a large diameter, more silicon pillars are needed, which in turn will impact the bond quality and yield significantly. Furthermore, to release the diaphragm, the oxide layer on the top of the silicon pillars are removed through the etch holes in the

diaphragm, which is not desirable as micro-fluidic applications need to be leak-tight.

Summary of the present invention

Accordingly, it is an object of the present invention to provide a method to manufacture a silicon diaphragm, wherein an oxide layer is embedded in the silicon substrate that acts as a support during the grinding and polishing processes. Furthermore, the formation of the embedded oxide is fully compatible with standard integrated circuit processing.

Brief description of the drawings

Figure 1 is a schematic view of the silicon substrate with the embedded oxide support.

Figure 2 is a diagram that illustrates the integration of the silicon substrate with embedded oxide support with other MEMS structures.

Figure 3 shows a flow chart of the formation of the silicon substrate with the embedded oxide support according to the present invention.

Figure 4 is a diagram depicting the diaphragm deformation during the grinding process.

Figure 5 shows a process for producing porous silicon and a schematic view of a cavity containing porous silicon formed in a silicon wafer according to prior art 1.

Figure 6 is a schematic diagram of a silicon diaphragm according to prior art 2.

Figures 7a to 7f show the process steps of embedding the oxide in the silicon substrate.

Figures 8a to 8d show the process steps of thinning the silicon substrate with the embedded oxide.

Detailed description of the present invention

Figure 1 shows a silicon substrate (14) with the embedded oxide (12) support.

Figure 2 illustrates the integration of the silicon substrate (14) with embedded oxide (12) support with other MEMS structures to form micro-/nano-dispensers, micro-pump and tunable capacitor.

Figure 3 shows a general flow chart of the formation of the silicon substrate (12) with the embedded oxide (14) support according to the present invention.

Figure 4 shows the diaphragm deformation during the grinding process.

Figure 5 shows a process for producing porous silicon and a schematic view of a cavity containing porous silicon formed in a silicon wafer according to prior art 1 (US 6,551,851 B2).

Figure 6 shows the schematic diagram of a silicon diaphragm according to prior art 2 (Luoto et al).

Figures 7a to 7f show the process steps to embed the oxide in the silicon substrate.

The process starts as shown in Figure 7a, wherein a layer of silicon dioxide (12) is deposited onto the silicon substrate (14), by means of thermal oxidation or chemical vapour deposition (CVD) method. The said silicon dioxide layer (12) acts as the masking agent during the etching process of the silicon.

As shown in Figure 7b, the silicon dioxide layer (12) is then etched to expose the regions of the silicon substrate. Tetrafluoromethane (CF_4) and trifluoromethane (CHF_3) plasma or in hydrofluoric based acid (HF) are used for the etching process.

The next step involves the use of inductively coupled plasma deep reactive ion etching (ICP-DRIE), combined with sulfur hexafluoride (SF_6) and octafluorocyclobutane (C_4F_8). They are used to etch the exposed regions of the silicon substrate to form micro- or nano- pillars and deep trenches with vertical sidewalls, as shown in Figure 7c. SF_6 acts as the etching agent whilst C_4F_8 promotes passivation process to form the vertical sidewalls.

After that, as shown in Figure 7d, the silicon dioxide layer (12) is removed using hydrofluoric based acid (HF).

The embedded oxide (12) is formed by thermally oxidizing the silicon pillars found in the silicon substrate (14), as shown in Figure 7e. The silicon pillars are consumed entirely and all the trenches are closed to form a uniform oxide layer.

Lastly, as shown in Figure 7f, for the oxide layer (12) to be in-plane with the silicon substrate, the oxide layer (12) is planarised by means of an etching process. A combination of tetrafluoromethane (CF_4) and trifluoromethane (CHF_3) plasma or chemical-mechanical polishing (CMP) is used for the etching process.

Figures 8a to 8d show the process steps of thinning the silicon substrate with the embedded oxide.

As seen in Figure 8b, the silicon substrate with the embedded oxide is bonded to a second substrate, i.e. a device wafer (16) (capacitive sensors, pressure sensors, microphones, micro-fluidic devices such as micro-pumps, micro-valves, micro-dispensers). The method to bond both of the substrates is not limited to fusion, anodic bonding, eutectic and adhesive type bonding.

Next, grinding and chemical mechanical polishing (CMP) processes are performed on the silicon substrate (14) with the embedded oxide (12) to form the silicon diaphragm, as seen in Figure 8c. The embedded oxide (12) acts as a support to ensure that no bending or deformation takes place.

Lastly, as seen in Figure 8d, the embedded oxide (12) is removed by etching process, using hydrofluoric based acid (HF) through the open channels in the second substrate (16).

Claims

1. A method to embed oxide (12) in the silicon substrate (14) comprising the steps of

depositing a layer of silicon dioxide (12) onto a silicon substrate (14);

etching of silicon dioxide (12) to expose silicon regions;

etching the exposed silicon substrate (14) to form silicon pillars and trenches with vertical sidewalls;

removing the silicon dioxide layer (12);

forming the embedded oxide (12) by thermal oxidation; and

planarising the oxide layer (12) to be in-plane with the silicon substrate (14).

2. The method according to claim 1 wherein thermal oxidation or chemical vapour deposition method is used to deposit a layer of silicon dioxide (12) onto a silicon substrate (14).

3. The method according to claim 1 wherein the silicon dioxide layer (12) is etched by tetrafluoromethane (CF_4) and trifluoromethane (CHF_3) plasma or in hydrofluoric based acid (HF) to expose silicon regions in the silicon substrate (14).

4. The method according to claim 1 wherein the exposed regions in the silicon substrate (14) are etched by inductively coupled plasma deep reactive ion etching (ICP-DRIE), combined with sulfur hexafluoride (SF_6) and

octafluorocyclobutane (C_4F_8) to form silicon pillars and trenches with vertical sidewalls.

5. The method according to claims 1 and 4 wherein the silicon pillars are in micro- and nano- dimensions.

6. The method according to claim 1 wherein the silicon dioxide layer (12) is removed by hydrofluoric based acid (HF).

7. The method according to claim 1 wherein the silicon pillars are consumed entirely and all trenches are closed when the silicon pillars are thermally oxidized to form the embedded oxide (14).

8. The method according to claims 1 and 7 wherein the oxide layer (12) is planarised by a combination of tetrafluoromethane (CF_4) and trifluoromethane (CHF_3) plasma or by chemical-mechanical polishing (CMP).

9. A method for manufacturing silicon diaphragm in micro- and nano- dimensions with embedded oxide (12) as support comprising the steps of

depositing a layer of silicon dioxide (12) onto a silicon substrate (14);

etching of silicon dioxide to expose silicon regions;

etching the exposed silicon substrate (14) to form silicon pillars and trenches with vertical sidewalls;

removing the silicon dioxide layer (12);

forming the embedded oxide (12) by thermal oxidation;

planarising the oxide layer (12) to be in-plane with the silicon substrate (14);

bonding the silicon substrate (14) containing the embedded oxide (12) to a second substrate (16);

thinning of the silicon substrate (14) containing the embedded oxide (12) by grinding and chemical-mechanical polishing (CMP) to form the silicon diaphragm; and

removing the embedded oxide (12).

10. The method according to claim 9 wherein the second substrate (16) bonded to the silicon substrate (14) is a device wafer, not limited to capacitive sensors, pressure sensors, microphones, and micro-fluidic devices such as micro-pumps, micro-valves, and micro-dispensers.

11. The method according to claim 9 wherein bonding of the two substrates is performed with a method not limited to fusion, anodic bonding, eutectic and adhesive type binding.

12. The method according to claim 9 wherein the embedded oxide (12) is removed by a wet chemical etchant not limited to hydrofluoric based acid (HF).

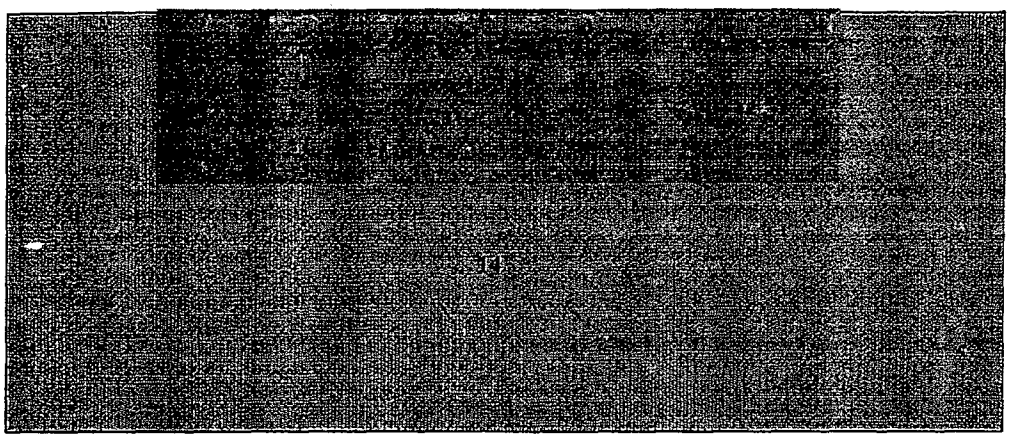

Figure 1.

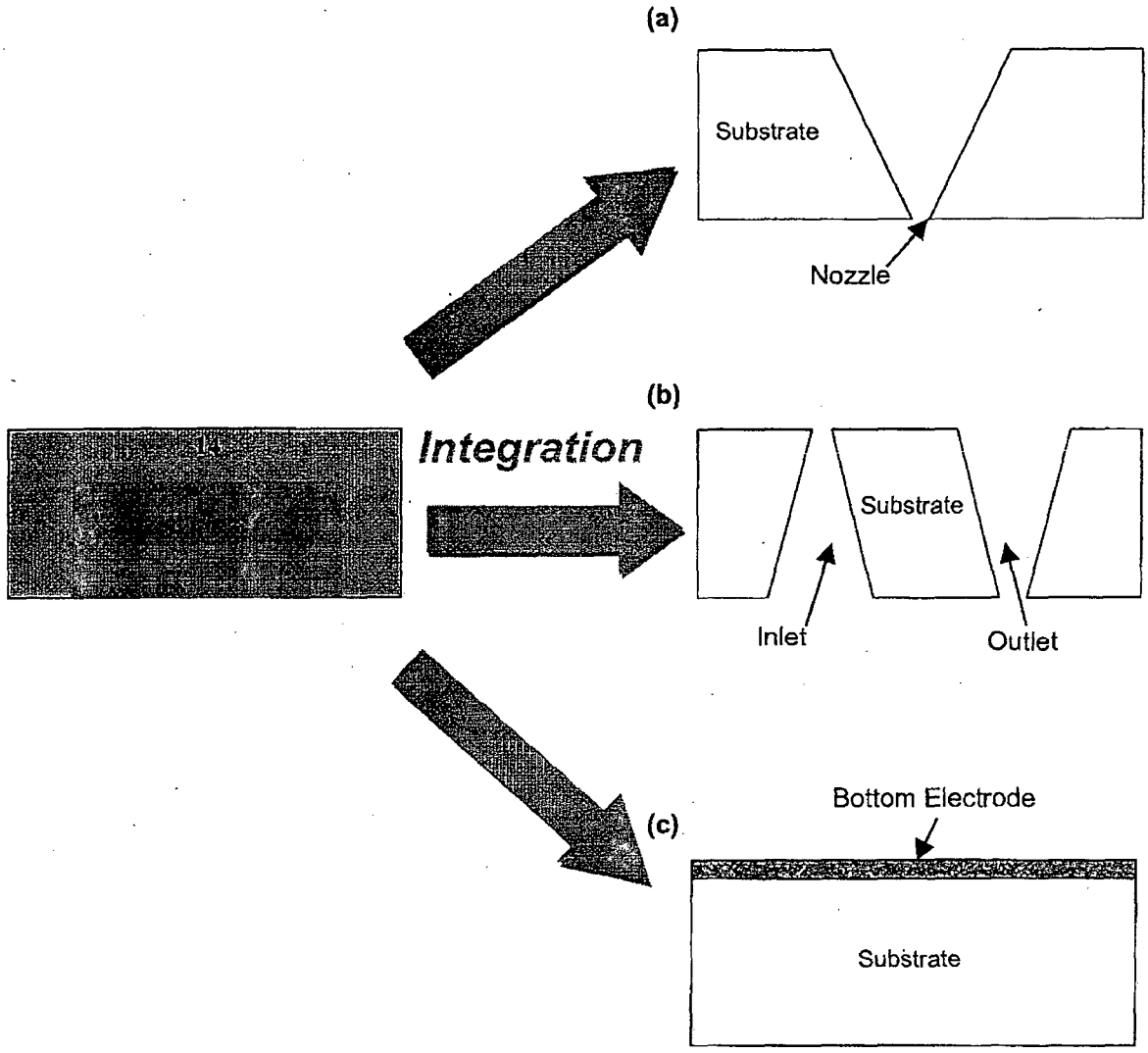
(a)
Substrate
Nozzle
(b)
Integration
Substrate
Inlet
Outlet
(c)
Bottom Electrode
Substrate

Figure 2.

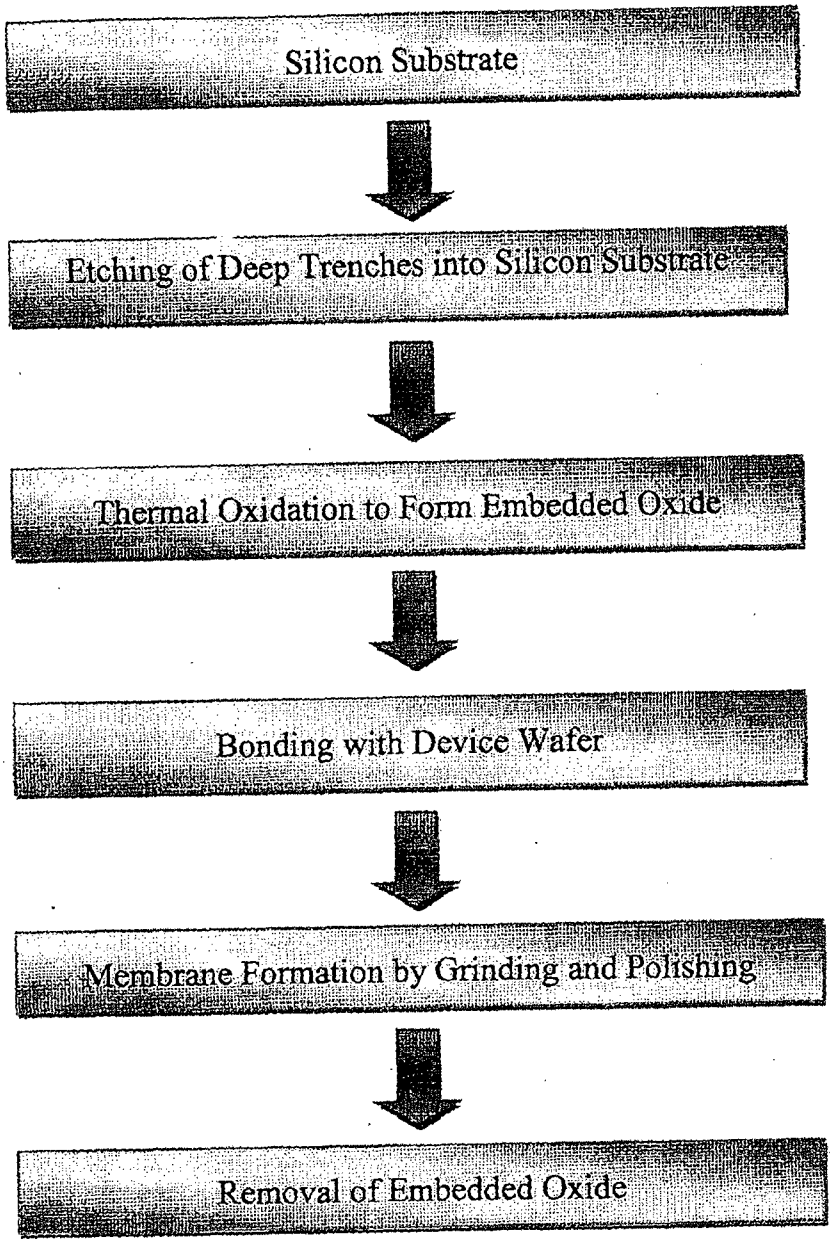
Silicon Substrate
Etching of Deep Trenches into Silicon Substrate
Thermal Oxidation to Form Embedded Oxide
Bonding with Device Wafer
Membrane Formation by Grinding and Polishing
Removal of Embedded Oxide

Figure 3

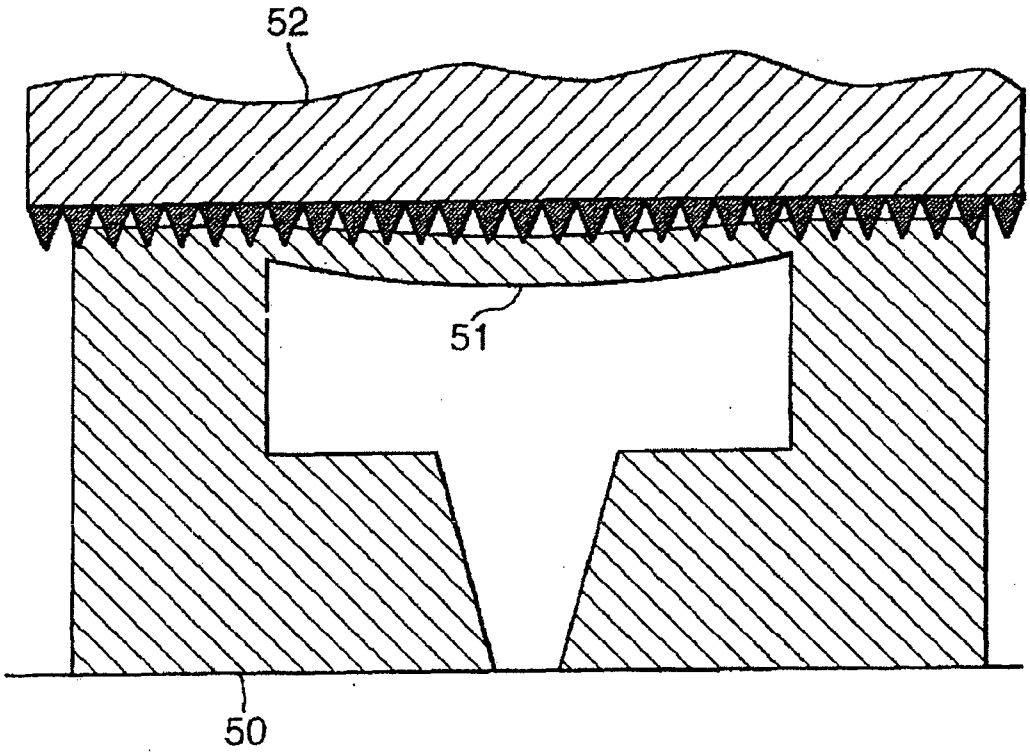

Figure 4

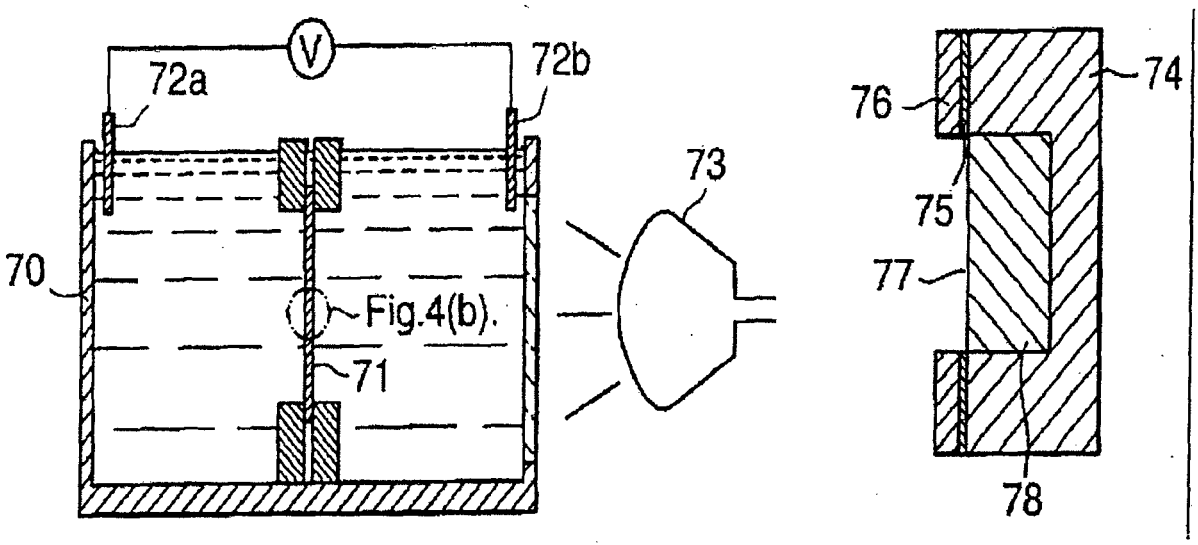

Figure 5

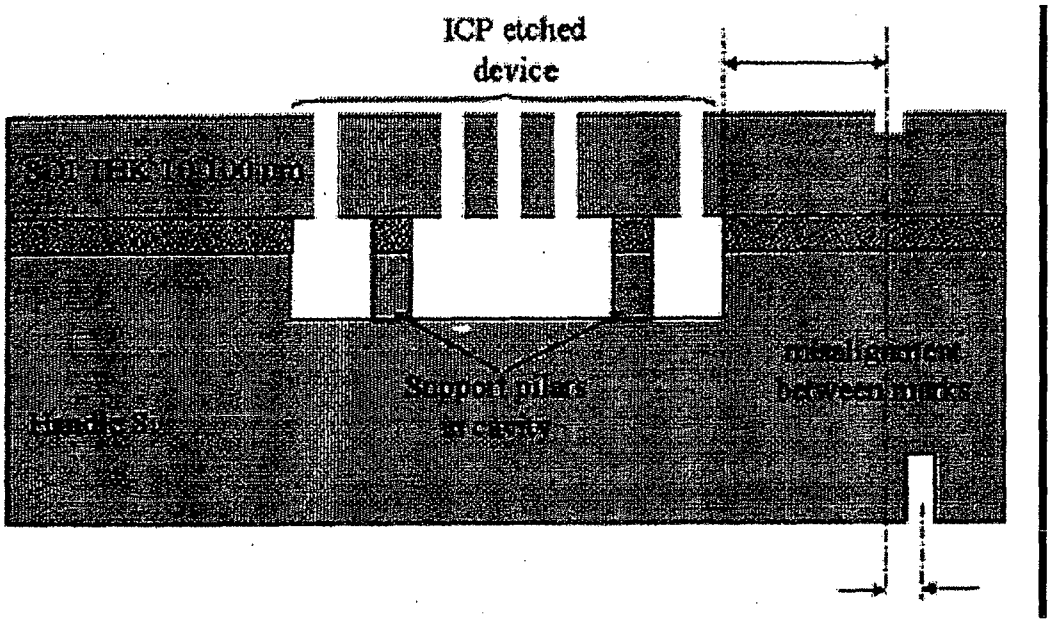

Figure 6

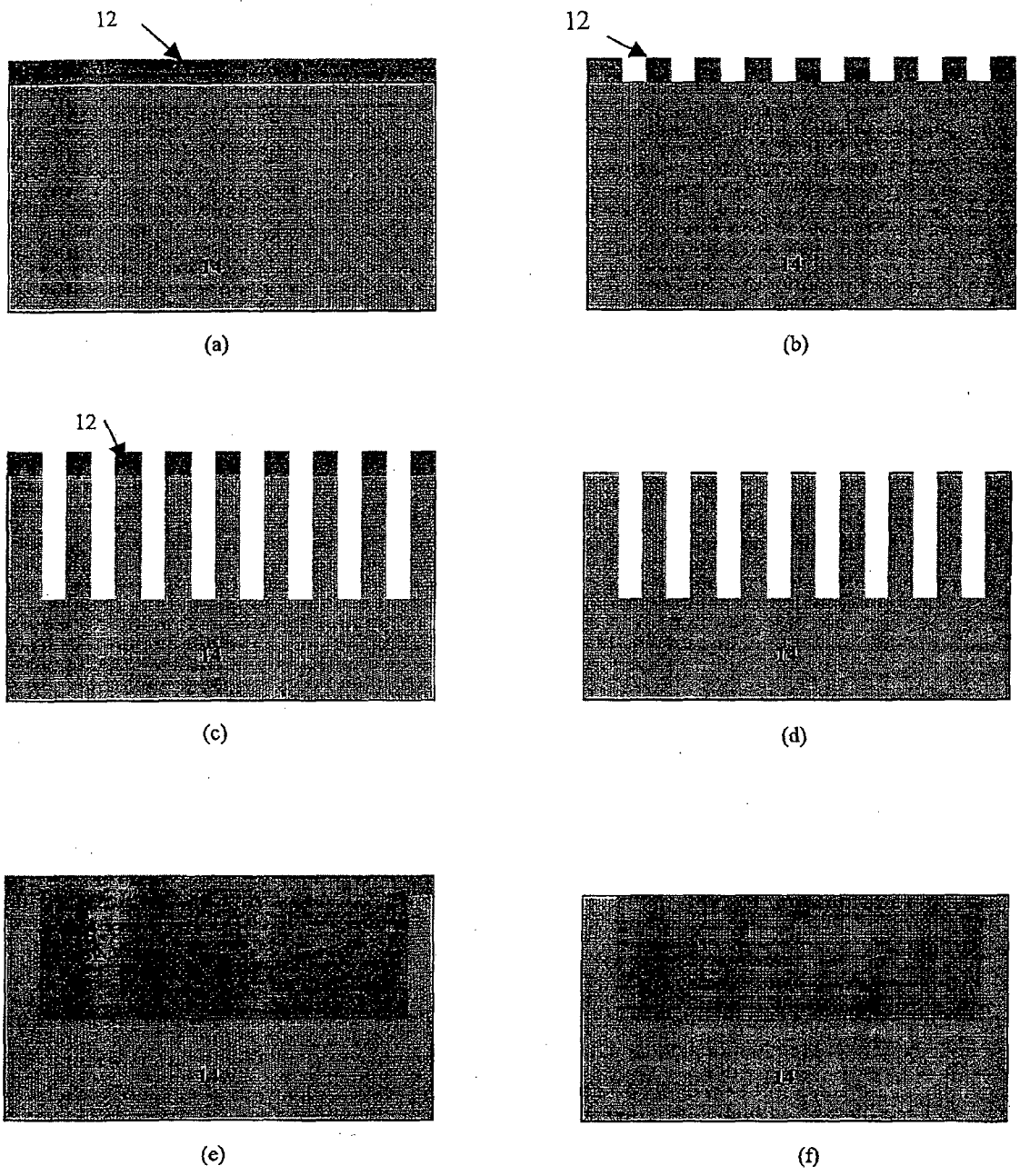

Figure 7

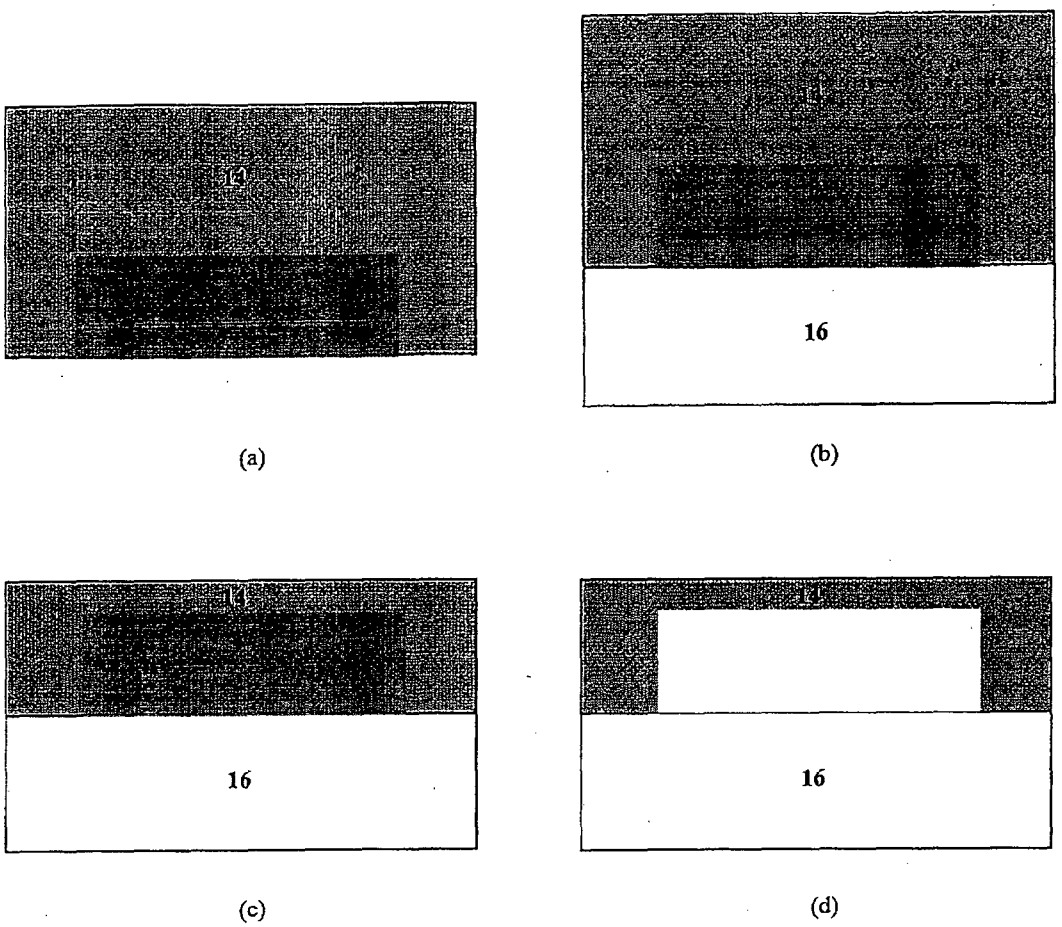

Figure 8