

[54] **DIGITAL FREQUENCY SYNTHESIZER**

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[22] Filed: **April 15, 1971**

[21] Appl. No.: **134,296**

[52] U.S. Cl. **328/17, 307/225, 307/271, 328/14, 328/39, 328/60, 328/62**

[51] Int. Cl. **H03b 19/00**

[58] Field of Search..... **328/14, 17, 27, 29, 30, 39, 328/60, 62, 161; 307/225, 271**

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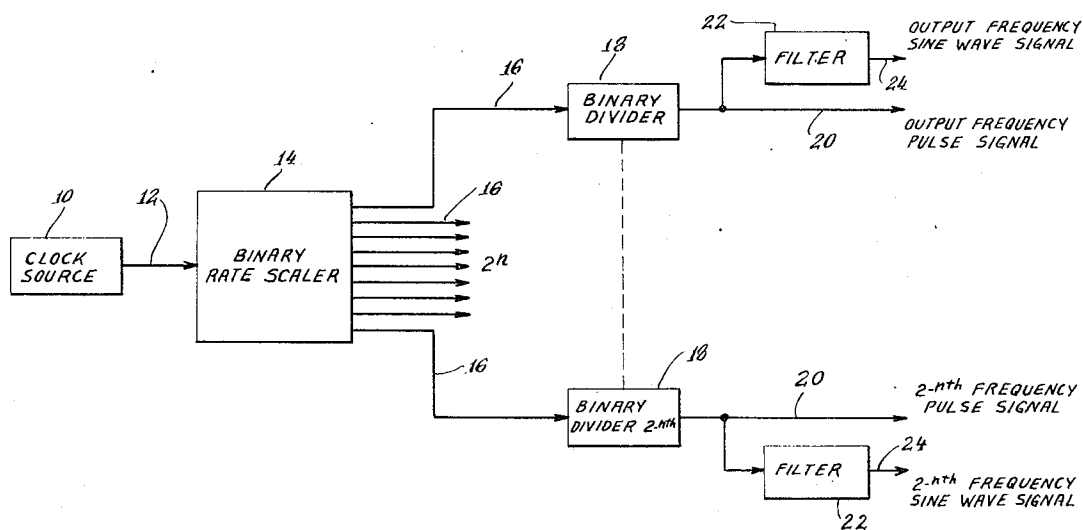
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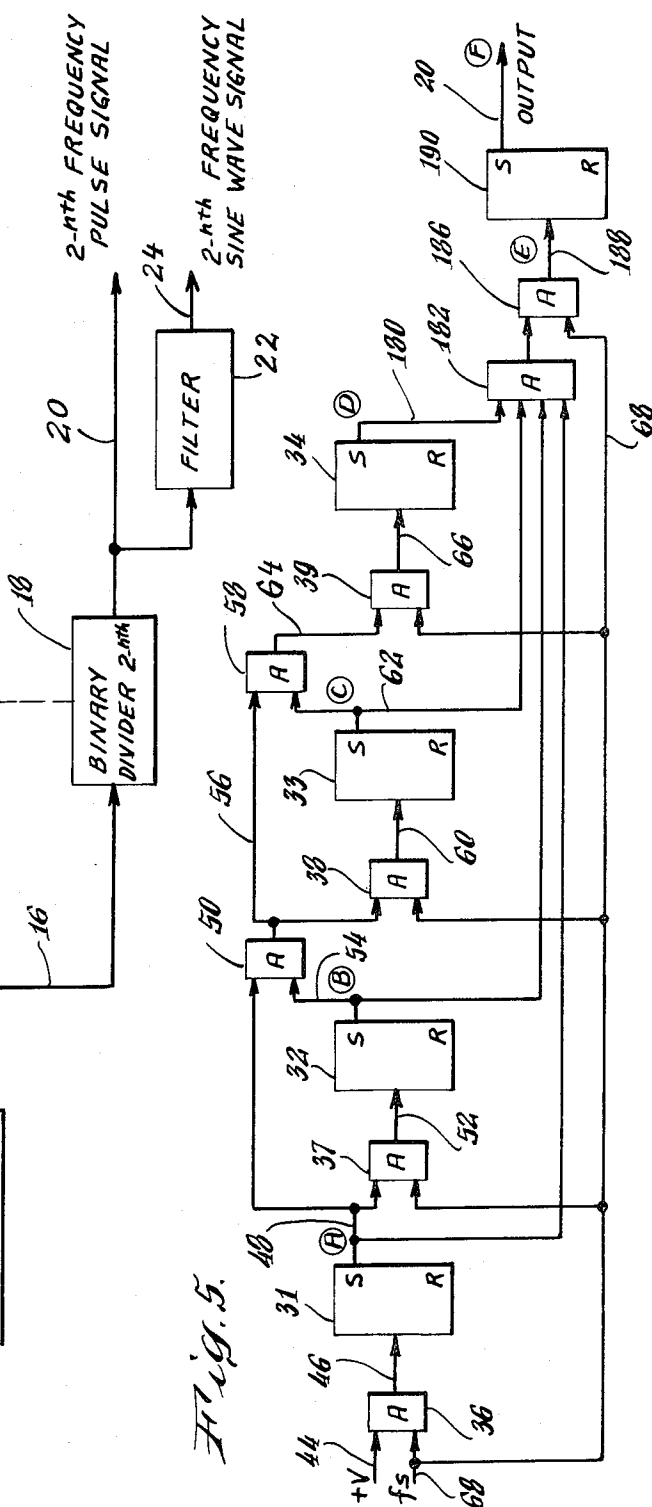
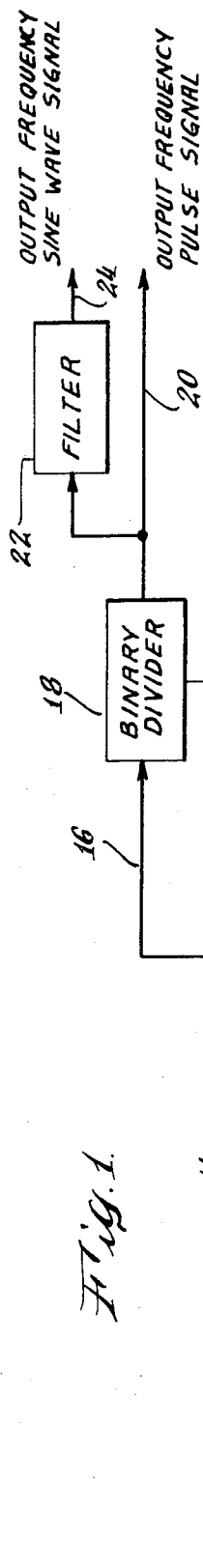
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[57] **ABSTRACT**

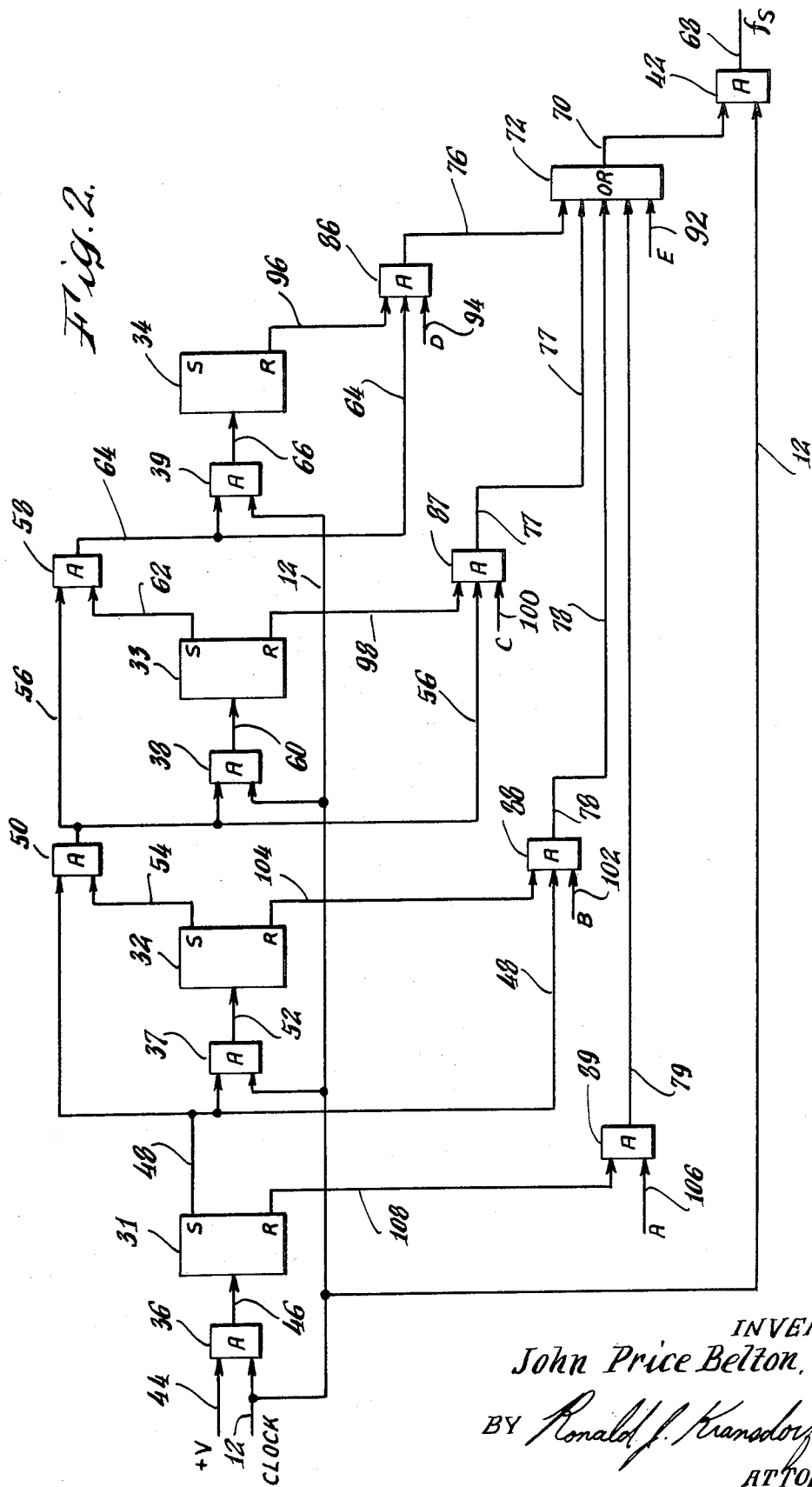
A circuit for simultaneously generating a plurality of signals at related frequencies. A clock source, the frequency of which is greater than the frequency of any of the signals to be generated, is applied to the input to a scaler circuit. The scaler circuit generates a plurality of output signals, there being an output signal from the scaler circuit corresponding to each of the related frequency signals to be generated. At least some of the signals from the scaler have non-uniform pulse-to-pulse spacing. The outputs from the scaler circuit are then converted into signals at the desired frequencies with substantially uniform pulse-to-pulse spacing. For the preferred embodiment of the invention, this is accomplished by scaling the signals from the scaler circuit at frequencies which are multiples of the corresponding signals of related frequencies and then dividing down each signal from the scaler to obtain the desired signals.

7 Claims, 6 Drawing Figures

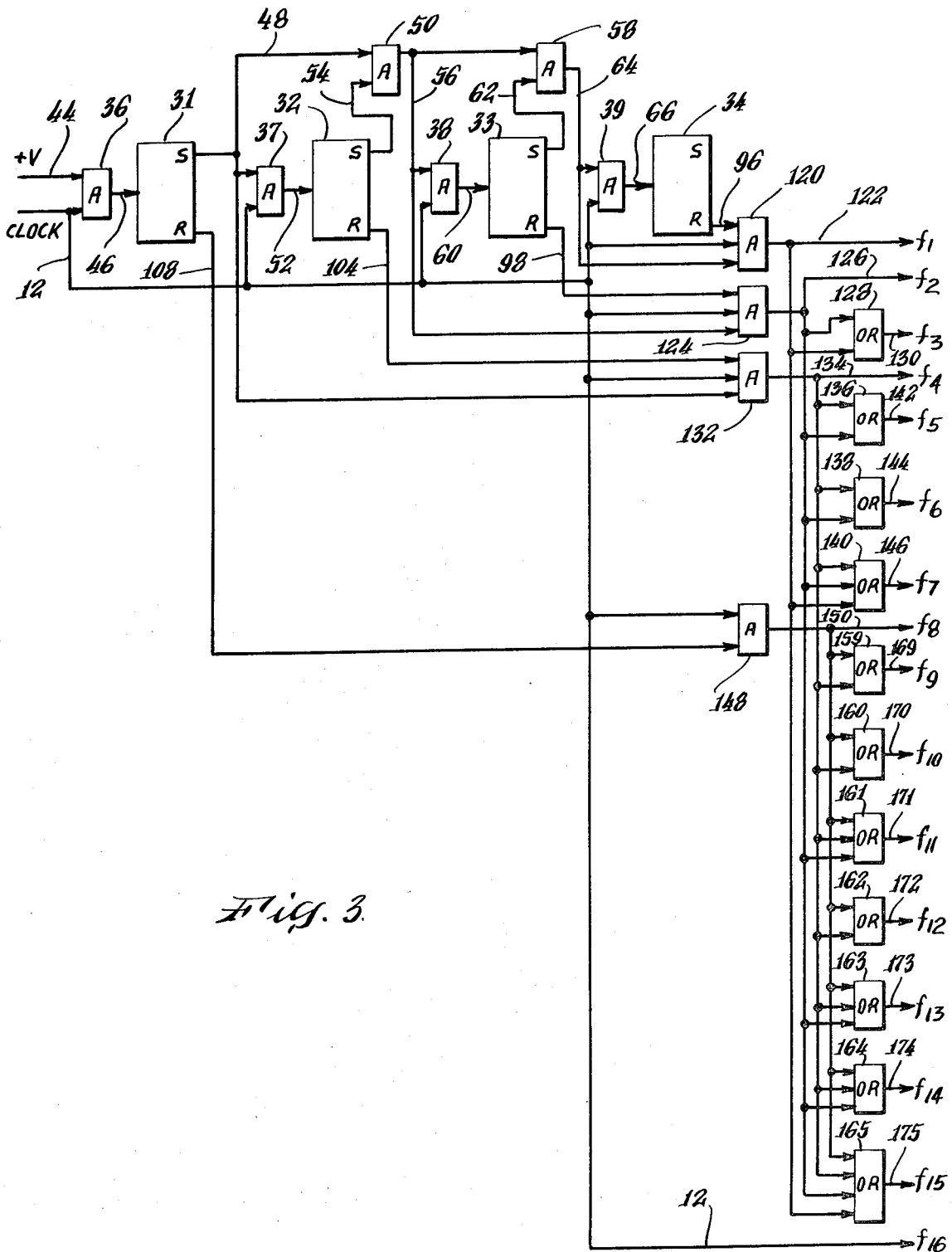




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A	B	C	D	E
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
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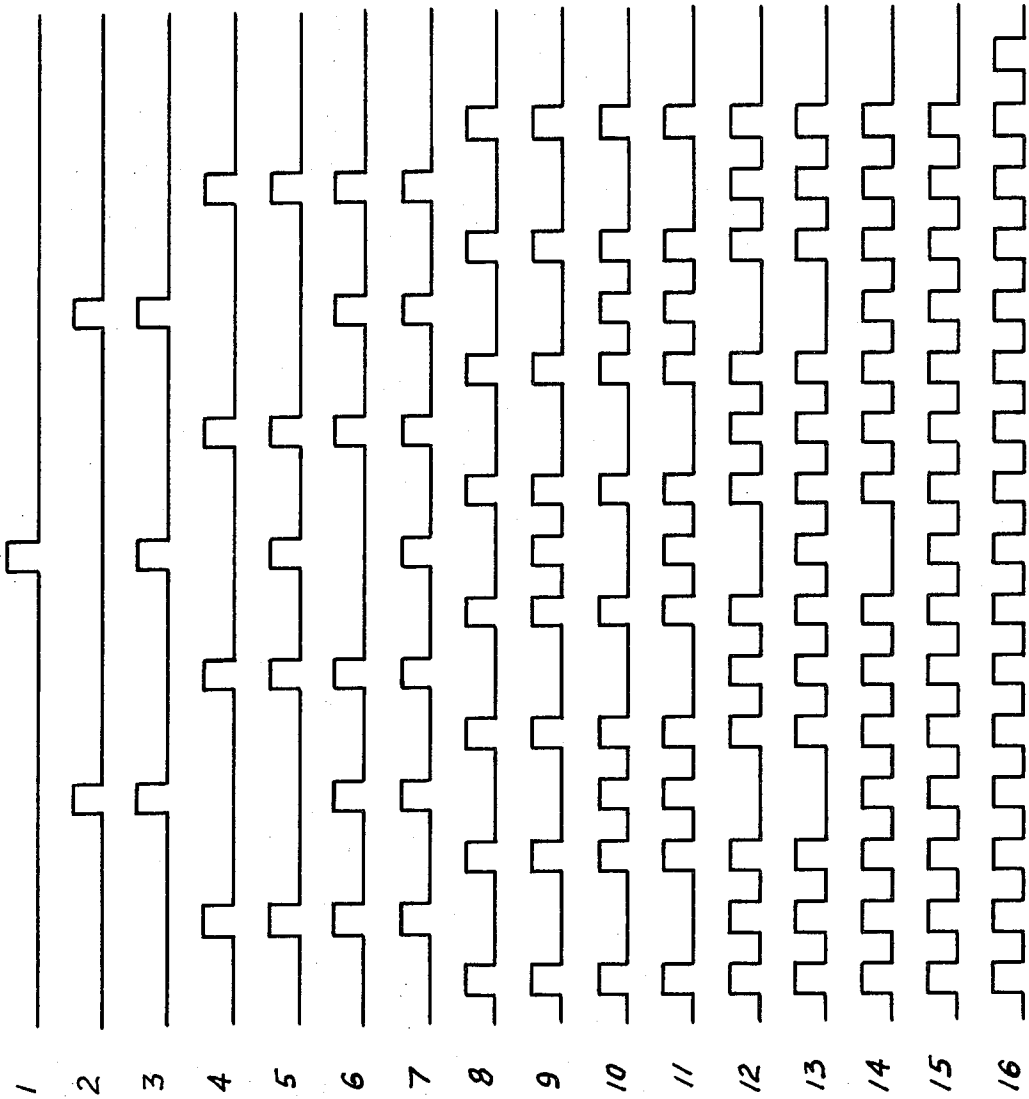


Fig. 4.

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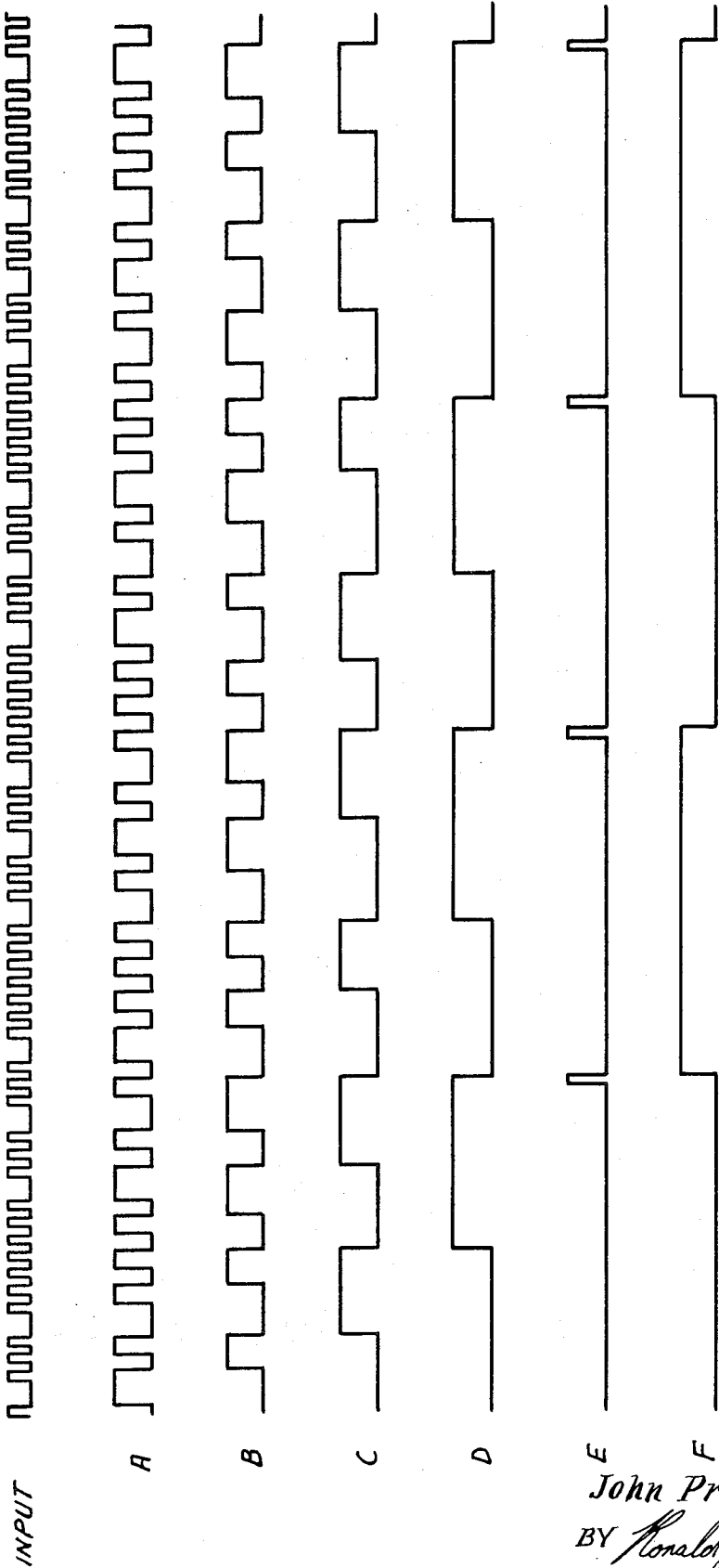


Fig. 6.

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DIGITAL FREQUENCY SYNTHESIZER

This invention relates to a circuit for simultaneously generating a plurality of signals at different frequencies, and more particularly to a circuit for generating a plurality of harmonically related pulse signals.

BACKGROUND OF THE INVENTION

There are numerous applications in electrical and electronic systems in which a requirement exists for the simultaneous generation of a plurality of pulse or sine-wave signals at related frequencies. An example of one such application is a spectrum analyzer disclosed in copending application Ser. No. 799,067, filed Feb. 13, 1969 on behalf of George S. Kang, entitled "Spectrum Analyzer" and assigned to the assignee of the instant application.

For such applications, the standard approach has been to start with a clock frequency which is a common denominator of the N number of desired frequencies and to divide down the clock frequency in separate binary dividers. If it is assumed, for example, that 12 harmonically related signals, in 1 kHz steps from 1 to 12 kHz, with 50 percent duty cycles are required, the common denominator clock frequency would be 55.44 MHz. Since the state of the art toggle rate for transistor-transistor logic (TTL) is 75 MHz, and for emitter-couple logic is 300 MHz the clock required to generate the above group of signals using the conventional frequency synthesizer approach is well within the state of the art. However, if 13 rather than 12 signals are required, the common denominator clock frequency becomes 720.72 MHz while for 20 harmonically related signals the common denominator frequency becomes 3,491,888.40 MHz. Such frequencies are clearly beyond the toggle rate capabilities of existing hardware. It is thus seen that the conventional approach for generating a plurality of related frequency signals imposes severe limitations both as to the number of harmonically related signals which may be generated and as to the frequency range for these signals.

Another digital technique which is available for generating 20 harmonically related frequency signals is known as sequential function generation by indirect logic. This technique involves drawing the desired output waveforms for a specific period. The period is then divided into N discrete intervals. The number of intervals depends on the accuracy to which the system is designed. For a reasonable level of accuracy, the period would be divided into 2,500 discrete intervals, an operation requiring the use of a 15-stage counter with a toggle rate of 2 MHz. The problem with this technique is that of working with 15 variables to generate a usable Boolean equation. While various techniques are available for generating the required Boolean equations, such as for example the Quine-McClusky method, the significant amount of engineering time required to design a single system of this type makes the use of this technique undesirable.

From the above it is apparent that a need exists for a relatively simple and straight-forward technique for simultaneously generating a large number of related frequency signals. This technique should permit the frequency range for the signals to be fairly wide and should not require the use of a clock frequency higher than the toggle rate for state of the art devices.

It is therefore a primary object of this invention to provide an improved frequency synthesizer.

A more specific object of this invention is to provide a device capable of simultaneously generating a relatively large number of related frequency signals which device is relatively simple and straight-forward to design and implement.

Another object of this invention is to provide a device of the type indicated above which is capable of generating outputs over a fairly wide range of frequencies.

Still another object of this invention is to provide a device of the type indicated above which is capable of operating with clock signals the frequency of which is no greater than the toggle rate for state of the art technology.

BRIEF DESCRIPTION OF INVENTION

In accordance with these objects this invention provides a circuit for simultaneously generating a plurality of pulse signals at different frequencies. For preferred embodiments of the invention the pulse signals are harmonically related. The circuit includes a clock signal source, the frequency of which is M times the highest frequency of the signals to be generated where M is an integer. A scaler means is also provided for converting the clock signal into a plurality of signals each of which is at a frequency which is a multiple of one of the different frequencies to be generated. At least some of the signals from the scaler have non-uniform pulse-to-pulse spacing. The final element in the circuit is a means for dividing down the signals from the scaler to generate signals at the desired different frequencies with each signal having substantially uniform pulse-to-pulse spacing. Filters may be provided at the output from the dividing means to convert the pulse signals into sine-wave signals.

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of preferred embodiments of the invention as illustrated in the accompanying drawings:

DESCRIPTION OF DRAWINGS

FIG. 1 is a general block diagram of a preferred embodiment of the invention.

FIG. 2 is a detailed diagram of a generalized scaler circuit suitable for use as a binary rate scaler in FIG. 1.

FIG. 3 is a detailed block diagram of an alternative configuration for the binary rate scaler of FIG. 1.

FIG. 4 is a diagram illustrating the various outputs obtained from the binary rate scaler.

FIG. 5 is a detailed block diagram of one of the binary dividers shown in FIG. 1.

FIG. 6 is a diagram illustrating the waveforms appearing at various points in the circuit shown in FIG. 5.

DETAILED DESCRIPTION OF INVENTION

Referring now to FIG. 1, it is seen that the pulses from a clock source 10 are applied through a line 12 to a binary rate scaler circuit 14. The only requirements on source 10 are that it be a stable source and that it be at a selected frequency. The manner in which the frequency for source 10 is determined will be described

shortly. In applications where the output pulse trains desired from the circuit will from time to time be changed, source 10 may be made variable.

Scaler 14 is operative to simultaneously divide the clock frequency into 2^N harmonically related frequencies where N is the number of flip flops in a binary counter contained within the scaler. A gating network is provided which monitors the output from each flip flop and gates out selected clock pulses on each of the 2^N lines 16. For a preferred embodiment of the invention, a clock pulse is required to switch each of the flip flops from its reset to its set state. The gating circuit selectively passes the clock pulses which cause one or more of these transitions to each of the lines 16.

From the mode of operation described above, it is apparent that uniform output pulse spacing is not obtained on all of the lines 16. FIG. 4, which shows the output pulses from an illustrative binary rate scaler, illustrates this non-uniformity in pulse spacing. Since, in most applications, it is necessary to provide the output with a pulse-to-pulse non-uniformity which is generally less than 1%, additional processing is required to minimize this non-uniformity or jitter. In FIG. 1, this is accomplished by scaling at a rate higher than desired and then reducing the rate for the signal on each line 16 by use of a synchronous binary divider 18. The desired output frequency is obtained with a reduction of jitter equal to the ratio of the scaling frequency to the divider output frequency.

The 2^N harmonically related frequencies, which are generated simultaneously on the lines 16 are clocked through the synchronous binary dividers 18 to minimize propagation delays between the output signals on lines 20 which might otherwise appear. As an example of the way in which the binary dividers 18 operate, for a 1 kHz output frequency using a 2.56 MHz clock, the binary rate scaler output has a 128 kHz repetition rate with a 2.5 percent duty cycle. The synchronous binary divider includes six stages which divide by 64 to generate a signal having a 2 kHz repetition rate and a .04 percent duty cycle. A final divide-by-two stage then develops the desired 1 kHz pulse with a 50 percent duty cycle.

The signals appearing on each of the lines 20 are pulse signals. If it is desired to obtain sine-wave rather than pulse signals, the signals on lines 20 may be passed through filters 22 to lines 24. While for purposes of illustration, both a pulse output line 20 and a sine-wave output line 24 have been shown in FIG. 1, in most applications only one or the other of these outputs would be utilized.

To determine the frequency of clock source 10, the following equation may be utilized:

$$F_{clk} = (\text{highest synthesized frequency}) (2^S)$$

where S is the number of division stages in binary dividers 18. Thus, to generate 20 harmonically related frequencies with a frequency range of 1 to 20 kHz, in 1 kHz increments, with jitter of no more than .8 percent, a seven stage binary divider (six stages of binary division plus a divide by two stage) is required in each binary divider 18. The clock frequency is thus:

$$F_{clk} = (20 \text{ kHz}) (2^7) \\ = 2.56 \text{ MHz}$$

It is thus seen that, using the technique of this invention, a frequency synthesizer for 20 harmonically related frequencies may be easily obtained utilizing state of the art technology. It is apparent that this technique could easily be utilized to generate a much larger number of harmonically related signals or to generate the same number of harmonically related signals operating in a higher frequency range or with larger increments between signals.

DETAILED DESCRIPTION OF BINARY RATE SCALER

FIG. 2 is a schematic block diagram of a generalized binary rate scaler stage which is capable of generating any one of the 16 harmonically related frequency signals shown in FIG. 4. The circuit consists of a four-stage synchronous counter, flip flops 31-34, and a gating circuit at the output from the counter.

In operation, the clock signal on line 12 is applied as one input to each of four AND gates 36-39 and as one input to AND gate 42. The other input to AND gate 36 is a positive voltage level on line 44. Thus, for each clock pulse on line 12, AND gate 36 is fully conditioned to generate an output on line 46 which transfers flip flop 31 from whatever state it is in to its opposite state. Output line 48 from the set side of flip flop 31 is applied as the other input to AND gate 37 and as one input to AND gate 50. AND gate 37 is thus fully conditioned for each clock pulse which is received when flip flop 31 is in its set state, or in other words, for every other clock pulse. Output line 52 from AND gate 37 is connected as the transfer input to flip flop 32. Output line 54 from the set side of flip flop 32 is connected as the other input to AND gate 50. AND gate 50 is thus fully conditioned when both flip flops 31 and 32 are in their set state, or in other words, for every fourth clock pulse. Output line 56 from AND gate 50 is connected as the other input to AND gate 38 and as one input to AND gate 58. AND gate 38 is thus fully conditioned on every fourth clock pulse to generate an output on line 60 which is applied to transfer flip flop 33. Output line 62 from the set side of flip flop 33 is connected as the other input to AND gate 58. AND gate 58 is thus fully conditioned when flip flops 31, 32 and 33 are all in their set state, or in other words, for every eighth clock pulse. Output line 64 from AND gate 58 is connected as the other input to AND gate 39. AND gate 39 is thus fully conditioned for every eighth clock pulse to generate an output on line 66 which is applied to transfer the state of flip flop 34. It is thus seen that flip flops 31-34 and their related gating circuits function as a four-state synchronous binary counter.

As was indicated previously, the clock line 12 is one input to AND gate 42. The control input to this AND gate, the input which determines which of the clock pulses on line 12 will be gated through to scaler output line 68, is output line 70 from OR gate 72. The inputs to OR gate 72 are output lines 76-79 from AND gates 86-89 respectively and a control line 92 which is designated the E line. Referring to line 16 of FIG. 4, it is seen that when the E line is true, when a positive

potential is applied to the E line, all clock pulses received on line 12 are gated through to circuit output line 68. This results from the continuous presence of a conditioning level on line 70.

Referring now to line 1 of FIG. 4, it is seen that when only the D control line 94 is energized, the circuit passes only a single clock pulse for each cycle of the scaler synchronous counter, this pulse being passed at the mid point of the cycle. The pulse is, in fact, passed when flip flop 34 is switched from its reset to its set state. This is accomplished by applying reset-side output line 96 from flip flop 34, output line 64 from AND gate 58, and D line 94 as inputs to AND gate 86. Since the first clock pulse which occurs after a signal appears on line 64 causes flip flop 34 to transfer, AND gate 86 is fully conditioned only for the clock pulse which switches flip flop 34 from its reset to its set state, a clock pulse which occurs only once in sixteen clock pulses. The desired output is thus provided.

Referring now to line 2 of FIG. 4, it is seen that when a C control signal is present, the circuit passes two clock pulses for each counter cycle. This is accomplished by passing the clock pulse which causes flip flop 33 to transfer from its reset to its set state. Thus, reset-side output line 98 from flip flop 33, output line 56 from AND gate 50, and the C control line 100 are connected as the inputs to AND gate 87. AND gate 87 is thus fully conditioned to generate a conditioning signal on line 77 at the two times during the counter cycle when flip flop 33 transfers from its reset to its set state. The desired output from the scaler is thus achieved.

Referring to line 3 of FIG. 4, it is seen that the third harmonic signal is obtained by applying control signals to both the D control line 94 and the C control line 100. The output on line 68 under these conditions is seen to be the sum of the outputs on lines 1 and 2.

From line 4 of FIG. 4, it is seen that the fourth harmonic signal is obtained by energizing the B control line 102. B control line 102 is connected as one input to AND gate 88, the other inputs to this AND gate being the reset-side output line 104 from flip flop 32 and the set-side output line 48 from flip flop 31. From previous discussion, it is apparent that AND gate 88 is thus fully conditioned when a control signal appears on line 102 and flip flop 32 is about to be transferred from its reset to its set state. This will occur four times for each cycle of the scaler counter. Conditioning signals thus appear on line 78 four times for each cycle of the counter gating through the desired fourth harmonic clock signals.

Lines 5, 6 and 7 of FIG. 4 show that the fifth, sixth and seventh harmonic signals are obtained by combining a signal on B control line 102 with a signal on C control line 100 and/or D control line 94. This results in a summing of clock pulses in much the same way as was done for the third harmonic signal.

From the eighth line of FIG. 4, it is seen that the eighth harmonic signal is obtained by applying a signal to A control line 106. A control line 106 is one of the inputs to AND gate 89, the other input to this AND gate being reset-side output line 108 from flip flop 31. AND gate 89 is thus fully conditioned for every other clock pulse when a signal appears on the A control line resulting in eight control pulses per counter cycle on line 79. These control signals gate out the desired eighth harmonic signal on line 68.

Lines 9-15 of FIG. 4 illustrate the combinations of control signals B, C and D with control signal A which are required in order to generate the ninth-fifteenth harmonic signals respectively on line 68. The non-uniformity of pulse spacing which is to be corrected by binary dividers 18 may be easily seen for many of these signals.

The circuit shown in FIG. 2 is limited in that it is capable of generating only one of the signals shown in FIG. 4 at a given time depending on the inputs to the control lines. FIG. 3 shows a binary rate scaler circuit which utilizes a minimum of hardware to generate all 16 of the signals shown in FIG. 4. The synchronous counter in FIG. 3 is identical to that shown in FIG. 2 and like reference numerals have been used for the counter elements in both figures. AND gate 120 in FIG. 3 has the same inputs as AND gate 86 in FIG. 2 except that clock line 12 has been substituted for the D control line 94. AND gate 120 thus passes the single clock pulse shown on line 1 of FIG. 4 on to f1 line 122. Similarly, the inputs to AND gate 124 in FIG. 3 are the same as the inputs to AND gate 87 in FIG. 2 except that clock line 12 is substituted for the Control line 100. The second harmonic signal on line 2 of FIG. 4 thus appears on f2 line 126. Lines 122 and 126 are the inputs to OR gate 128. The third harmonic signal on line 3 of FIG. 4 thus appears on f3 line 130.

The inputs to AND gate 132 in FIG. 3 are the same as the inputs to AND gate 88 in FIG. 2 except for the substitution of clock line 12 for the B control line 102. The fourth harmonic signal on line 4 of FIG. 4 thus appears on f4 line 134. Lines 122, 126 and 134 are selectively connected as the inputs to OR gates 136, 138 and 140 resulting in a fifth harmonic signal on f5 line 142, a sixth harmonic signal on f6 line 144 and a seventh harmonic signal on f7 line 146.

Since the inputs to AND gate 148 in FIG. 4 are the same as the inputs to AND gate 89 in FIG. 2 except for the substitution of clock line 12 for the A control line 106, an eighth harmonic signal appears on f8 line 150. F8 line 150 in conjunction with one or more of the lines 122, 126 and 134 are selectively connected as inputs to OR gates 159-165 to generate the required ninth through fifteenth harmonic signals on f9 line 169 through f15 line 175 respectively. Clock line 12 is connected directly as the f16 output.

BINARY DIVIDER DETAILED DESCRIPTION

Referring now to FIG. 5, a single binary divider 18 is shown. For purposes of illustration, a four-stage binary divider followed by a divide by two binary divider stage is shown. However, it should be understood that for applications where higher accuracies (a lower percentage of pulse-to-pulse non-uniformity) is required, a greater number of divider stages may be utilized. For example, in the illustrative situation mentioned above, six stages of binary dividers are utilized to achieve the required accuracy.

In FIG. 5 the first four stages of the binary divider are connected as a synchronous counter and operate in an identical manner to the four-stage counter shown in FIG. 2. The only difference is that synthesizer frequency output line 68 is connected as a circuit input rather than clock line 12. Like elements in FIGS. 2 and 5 have been given the same reference numerals. FIG. 6 illus-

trates the binary pulse trains which appear at various points in the circuit of FIG. 5. The input to the divider on fS line 68 is shown on the first line of FIG. 6. The resulting pulse trains which appear on the set-side output lines 48, 54, 62, and 180 from flip flops 31-34 respectively, are shown on lines A-D of FIG. 6. It is seen that while a small amount of jitter remains on line 62 (line C of FIG. 6) this jitter has been substantially eliminated in the output on line 180 from the last of the four divider stages (point D in the circuit).

The signals on lines 48, 54, 62, and 180 are connected as the inputs to AND gate 182. Thus, at times when all four flip flops of the counter are in their set state, AND gate 182 is fully conditioned to generate an output signal on line 184 which is applied as one input to AND gate 186. The other input to AND gate 186 is the fS line 68. The next pulse appearing on fS line 68 thus fully conditions AND gate 186 to generate a pulse on line 188 which is applied as the transfer input to binary flip flop 190. The pulses which appear on line 188 are shown on line E of FIG. 6. The output line 20 for the binary divider 18 is the set side output line of flip flop 190. The resulting jitter-free 50 percent duty cycle signal appearing on line 20 is shown on line F of FIG. 6.

While for the preferred embodiment of the invention described above, the output signals have been harmonically related, the circuit of this invention may be utilized to generate pulses having a wide range of variations in intrapulse spacing by suitably selecting the gating circuitry of the binary rate scaler 14 and by suitably adjusting the divide ratios of the binary dividers 18. It should be noted that if a division stage is missing from one of the dividers, a delay may have to be introduced in this divider to maintain the pulse trains in synchronism. Delays or gating circuitry might also be required to compensate for propagation or other delays introduced by the components utilized in the various circuits described above.

It should also be noted that while particular counter and gating circuitry has been shown for purposes of illustration for the binary rate scaler, any circuitry capable of performing the required functions might be utilized. Similarly, while a particular binary divider configuration has been disclosed, other divider configurations might be utilized and the number of stages required might be reduced where non-binary logic is employed. All that is required is that a means be provided for dividing down the scaler output signals by the required ratio in order to reduce non-uniformity in pulse-to-pulse spacing. Other equivalent means for reducing or eliminating this non-uniformity might also be employed. In some applications it might also be possible to perform the functions of some or all of the elements of the circuit by use of software techniques.

Thus, while the invention has been particularly shown and described with reference to preferred em-

bodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. A circuit for simultaneously generating a plurality of pulse signals at different frequencies comprising:
 - a clock signal source, the frequency of said clock signal source being greater than the frequency of any of said different frequencies;
 - scaler means for converting said clock signal into a plurality of pulse trains each of which is at a frequency which is a multiple of one of said different frequencies and at least some of the signals from said scaler means having non-uniform pulse-to-pulse spacing;
 - said scaler means including a multistage synchronous counter, and gating means responsive to output pulses from selected one or more stages of said counter for generating at least one of the pulse trains from said scaler; and
 - dividing means for dividing down the signals from said scaler means to generate signals at said different frequencies;
- the frequency of said clock signal source being chosen sufficiently high so that the pulse trains provided by said scaler means have frequencies which permit the pulse trains to be divided down by said dividing means by an amount sufficient to cause the resulting output signals at said different frequencies generated by said dividing means to have substantially uniform pulse-to-pulse spacing.
2. A circuit of the type described in claim 1 wherein said different frequencies are harmonically related.
3. A circuit of the type described in claim 1 wherein said dividing means includes a multistage synchronous counter for each signal from said scaler which is to be divided down, the output from the last stage of said counter being one of said signals of different frequency.
4. A circuit of the type described in claim 3 wherein the number of stages of the counter of said dividing means is equal to N where 2^N is the quantity by which the signal from said scaler is to be divided down.
5. A circuit of the type described in claim 1 wherein said scaler has a single synchronous counter and wherein said gating means includes a separate gating means for each of said plurality of signals from said scaler.
6. A circuit of the type described in claim 1 including means for converting the plurality of pulse signals into a plurality of sine-wave signals.
7. A circuit of the type described in claim 1 wherein the frequency of said clock signal is M times the frequency of the highest frequency signal to be generated, where M is the divide ratio of said dividing means.

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