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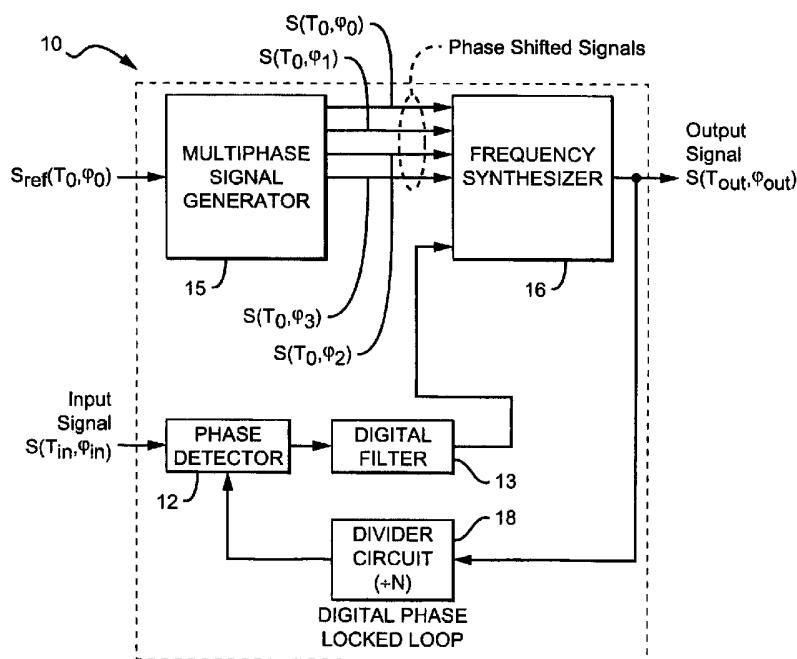
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- (71) Applicant (for all designated States except US): **ANA-LOG DEVICES, INC.** [US/US]; One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106 (US).
- (72) Inventor: **LANIER, Tyre, Paul**; 427-G Guilford College Road, Greensboro, NC 27409 (US).
- (74) Agents: **KOPPEL, Richard, S.** et al.; 555 St. Charles Drive, Suite 107, Thousand Oaks, CA 91360 (US).
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(54) Title: FREQUENCY SYNTHESIZER AND METHOD



(57) Abstract: A fractional frequency synthesizer includes a circuit which alternately outputs multiple output signals having different respective periods to drive the average period of the output signal to within a predetermined number of phase steps of a desired period. The phase steps are provided by a plurality of phase-shifted reference clock signals, having the same frequency. The average period of the output signal is a fractional multiple of the period of the reference clock signals.

FREQUENCY SYNTHESIZER AND METHOD

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] This invention relates generally to electronic circuits and, more particularly, to electronic circuits which generate a sequence of pulses with a desired period.

Description of the Related Art

[0002] Electronic circuits can generate a sequence of pulses which can be used in many applications, such as clocks and pulse generators. In various applications it may be desired to generate a sequence of pulses with a period which is either an integer multiple or a non-integer multiple of a reference clock period. A non-integer multiple can be represented as $M/N=P.Q$, where M and N are natural numbers and P and Q are integer and decimal numbers, respectively. Hence, M/N is a rational number expressed as a fraction and $P.Q$ is its equivalent expressed as a decimal. In an example, if the reference clock period is 10 ns (i.e. 100 MHz), then to produce a signal with a period of 48.8 ns (i.e. 20.5 MHz), the reference clock period can be multiplied by 4.88 (i.e. $M=488$, $N=100$, $P=4$, and $Q=0.88$). This is equivalent to dividing the reference clock frequency by 4.88 (i.e. $100 \text{ MHz}/4.88=20.5 \text{ MHz}$).

[0003] Several approaches have been proposed to generate output signals with a period which is a non-integer multiple of a reference period. However, these approaches have jitter which limits their usefulness.

Jitter refers to variations in the pulse positions caused by switching between two signals with different phases and appears in the output signal as noise and/or an unintended frequency modulation. Noise typically decreases the signal-to-noise ratio of the system.

[0004] Jitter can cause errors in the phase determination of the output signal and, consequently, can reduce the phase margin. The phase of the output signal can be used in many applications, such as analog-to-digital and digital-to-analog converters to define time-points at which the data is sampled. If the phase of the output signal jitters, then there can be errors in the time-points which will affect the overall signal quality.

[0005] One way to generate signals with non-integer multiple periods is the rational-rate approach. This approach, as disclosed in U.S. Patent Number 5,088,057, divides the reference clock frequency by two different integer values to generate two sub-frequencies. The system then switches between the two sub-frequencies to produce an average clock frequency. However, one problem with the rational-rate approach is that the average clock frequency appears to jitter between the phases of the two sub-frequencies. Because the sub-frequencies are generated by dividing by integer numbers, the jitter is on the order of a clock cycle.

[0006] Another approach is referred as fractional-frequency divider. As disclosed in U.S. Patent Number 6,157,694, the system provides several phase-shifted reference signals which have pulse edges shifted over the reference signal period. One pulse edge is outputted at a particular time in response to a trigger signal to provide a high-to-low or a low-to-high pulse edge for the output signal. Hence, the timing of the triggering events determines the frequency of the output signal.

However, the fractional-frequency approach also generates jitter in the output signal because the switching is between two phase-shifted signals whose pulse edges, in general, do not always occur at the correct time.

[0007] In the rational-rate and fractional frequency approaches, jitter can be reduced by increasing the frequency of the reference signal. Jitter can also be reduced in the fractional frequency approach by increasing the number of phase-shifted signals. However, increasing the reference frequency and the number of phase-shifted signals increases the complexity and cost of the circuitry. Consequently, there is a need for a frequency synthesizer which provides an output signal with an arbitrary period and less jitter, using a lower frequency reference signal and fewer phase shifted signals.

SUMMARY OF THE INVENTION

[0008] The present invention provides a frequency synthesizer with a circuit which alternately outputs multiple output signals having different periods so that an average period of an output signal is driven to within a predetermined number of phase steps of a desired period. The multiple output signals can be outputted by techniques such as dithering or in response to an error signal which is proportional to the difference between the average and desired periods. The phase steps are provided by a plurality of phase-shifted reference clock signals so that the output signal can be driven to within one phase step of the desired period.

[0009] In another aspect of the present invention, a signal processing system with a frequency synthesizer includes a signal selection circuit which outputs a

selected phase-shifted reference signal in a plurality of phase-shifted reference signals in response to a control signal. A toggle circuit is coupled to an output of the signal selection circuit and alternately outputs multiple output signals in response to a select signal. A control circuit is coupled to an output of the signal selection circuit and provides the control and select signals to the signal selection and toggle circuits, respectively. In this way, the multiple output signals provide the output signal with an average period driven to within a predetermined number of phase steps of a desired period.

[0010] These and other features, aspects, and advantages of the present invention will become better understood with reference to the following drawings, description, and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] FIG. 1 is a simplified block diagram of a communication system in accordance with the present invention;

[0012] FIG. 2 is a simplified block diagram of a phase locked loop included in FIG. 1;

[0013] FIG. 3 is a simplified block diagram of a frequency synthesizer shown in FIG. 2;

[0014] FIG. 4 is a timing diagram of the phase-shifted reference signals shown in FIG. 2;

[0015] FIG. 5 is a more detailed block diagram of the frequency synthesizer shown in FIG. 3;

[0016] FIG. 6 is a more detailed block diagram of the pre-calculation logic circuit shown in FIG. 5;

[0017] FIG. 7 is a simplified block diagram of the clock synthesis logic circuit shown in FIG. 5;

[0018] FIG. 8 is a more detailed block diagram of the clock synthesis logic shown in FIG. 7;

[0019] FIG. 9 is a block diagram illustrating another embodiment of the pre-calculation logic circuit shown in FIG. 5;

[0020] FIG. 10 is a block diagram illustrating another embodiment of the signal selection circuit shown in FIG. 7;

[0021] FIG. 11 is a simplified flow diagram of a method of providing an output signal in accordance with the present invention; and

[0022] FIG. 12 is a simplified flow diagram of another method of providing the output signal in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0023] FIG. 1 is a simplified block diagram of a communication system 30 which implements one embodiment of the invention. System 30 includes a signal processing system 31 coupled to a digital phase locked loop (PLL) 10 through an analog PLL 11. System 31 includes an analog-to-digital converter (ADC) 32 which receives inputs from a digital-to-analog converter (DAC) 36 through a data transmission system 34. PLLs 10 and 11 can be included in communication systems other than the one illustrated in FIG. 1 to provide a sequence of pulses with a desired period, where the period can be an integer or a non-integer multiple of a reference clock period. However, PLLs 10 and 11 are shown in communication system 30 to illustrate one particular embodiment of the invention.

[0024] PLL 10 provides a clock signal $S(T_{out}, \phi_{out})$ in response to both an input signal $S(T_{in}, \phi_{in})$ and a reference

signal $S_{\text{ref}}(T_0, \phi_0)$, in which T_{out} can be an integer (i.e. 5) or a non-integer multiple (i.e. 4.33) of T_{in} . PLL 11 provides a clock signal $S(T'_{\text{out}}, \phi_{\text{out}})$, in response to $S(T_{\text{out}}, \phi_{\text{out}})$, to ADC 32, DAC 36, and system 34. T refers to a signal period, f refers to a signal frequency ($f=1/T$), and ϕ refers to a signal phase.

[0025] PLL 11 is an optional component in system 30, and is included to multiply T_{out} by a small value to provide T'_{out} . Analog PLLs can typically multiply signal periods by smaller numbers faster and more accurately than digital PLLs. Analog PLLs can also filter out high frequency noise better than digital PLLs. Hence, digital PLL 10 can provide T_{out} by multiplying T_{in} by a larger integer or non-integer number. Analog PLL 11 can then multiply T_{out} by a smaller integer number to provide T'_{out} , and filter high frequency noise that may be in signal $S(T_{\text{out}}, \phi_{\text{out}})$.

[0026] In operation, ADC 32 samples signal S_{Analog} at a frequency f_{out} to provide a corresponding digital signal S_{Digital} . S_{Digital} is processed by and transmitted through system 34, where system 34 outputs a digital signal S'_{Digital} . S'_{Digital} is provided to converter 36, where it is converted back into an analog signal S'_{Analog} . Hence, ADC 32 and DAC 36 sample the corresponding data at a rate determined by T'_{out} , where T'_{out} can be within one phase step of the desired period. This reduces the jitter and also increases the signal-to-noise ratio of the converted signals when T'_{out} is an integer or non-integer multiple of T_{in} .

[0027] DAC 36 is illustrated for simplicity and ease of discussion and can be replaced with another digital system, such as a display device or a data processing system. A display device can be used when it is desired to provide information included in S'_{Digital} in a visual format, such as in a video system. A data processing system can be used when it is desired to perform calculations or otherwise manipulate data in response to S'_{Digital} .

[0028] FIG. 2 illustrates a more detailed view of digital PLL 10. PLL 10 includes a phase detector 12 coupled to a frequency synthesizer 16 through a digital filter 13. A multiphase signal generator 15 is also connected to frequency synthesizer 16. Detector 12 receives S_{Analog} , generator 15 receives $S_{\text{ref}}(T_0, \phi_0)$, and synthesizer 16 provides $S(T_{\text{out}}, \phi_{\text{out}})$.

[0029] Filter 13 can include a finite impulse response filter, an infinite impulse response filter, or another digital filter. If filter 13 includes an analog filter, then PLL 10 corresponds to an analog PLL. In this case, the analog filter can include a low pass filter or another analog filter which can filter a desired range of frequencies and/or provide signal amplification. For the analog PLL case, an external reference signal may not be needed because $S_{\text{ref}}(T_0, \phi_0)$ can be generated internally by the analog filter and provided to generator 15. PLL 11 can be an analog version of PLL 10, which can multiply T_{out} by an integer or a non-integer number, with filter 13 replaced with an analog filter.

[0030] Generator 15 provides phase-shifted signals of $S_{\text{ref}}(T_0, \phi_0)$, denoted as $S(T_0, \phi_0)$, $S(T_0, \phi_1)$, $S(T_0, \phi_2)$, and $S(T_0, \phi_3)$ (i.e. "the phase-shifted signals"). Generator 15

can include a multi-phase ring oscillator, a digital delay line, or a delayed locked loop to generate the phase-shifted signals.

[0031] A divider circuit 18 is coupled between synthesizer 16 and phase detector 12. If the divisor of divider circuit 18 is N , then the period of a signal fed back to phase detector 12 is equal to $N \cdot T_{out}$ and is denoted as $S(N \cdot T_{out}, \phi_{out})$. Hence, synthesizer 16 can provide a signal with a period that is a multiple of T_{in} , where ϕ_{in} equals ϕ_{out} when $S(T_{in}, \phi_{in})$ and $S(T_{out}, \phi_{out})$ are locked.

[0032] Period T_0 is typically much smaller than both T_{in} and T_{out} so that frequency f_0 is greater than f_{in} and f_{out} . In this way, $S_{ref}(T_0, \phi_0)$ will have pulse edges positioned (i.e. phase-shifted) at closely spaced time intervals compared to both $S(T_{in}, \phi_{in})$ and $S(T_{out}, \phi_{out})$. These pulse edges can be selected at particular times by synthesizer 16 to provide signals which approximate $S(T_{out}, \phi_{out})$, as will be discussed in more detail below.

[0033] In operation, input signal $S(T_{in}, \phi_{in})$ is provided to phase detector 12 which detects ϕ_{in} . PLL 10 adjusts the period and phase of $S(T_{out}, \phi_{out})$ in response to $S_{ref}(T_0, \phi_0)$ and $S(T_{in}, \phi_{in})$. Detector 12 compares phase ϕ_{in} with phase ϕ_{out} and provides to filter 13 a signal denoted as $S(\phi_{in} - \phi_{out})$ which is proportional to the difference between the two phases (i.e. $\phi_{in} - \phi_{out}$). The frequency response of filter 13 is chosen to minimize high frequency fluctuations in the phases between signals $S(T_{in}, \phi_{in})$ and $S(T_{out}, \phi_{out})$ so that $S(\phi_{in} - \phi_{out})$ is approximately a constant signal. Frequency synthesizer 16 determines which phase-shifted signal should be outputted at a particular time so that

$T_{out} = (M/N) \cdot T_{in} = P \cdot Q \cdot T_{in}$. This equation can be rewritten as $T_{out} = (M \cdot m/N) \cdot T_{in} = (P \cdot Q) \cdot m \cdot T_{in}$, where m is the number of phase steps per clock cycle. One phase step is the time spacing between the phase-shifted reference signals.

[0034] FIG. 3 illustrates one embodiment of synthesizer 16. Synthesizer 16 includes a signal selection circuit 21 which outputs a clock signal S_{clock} to a toggle circuit 23 and a control circuit 26. Control circuit 26 provides a phase control signal $S_{control}$ to circuit 21 and an enable signal S_{enable} to toggle circuit 23. Circuit 21 outputs a desired phase-shifted signal to circuits 23 and 26 in response to $S_{control}$. Hence, S_{clock} is a composite signal determined by $S_{control}$ and formed from the phase-shifted signals. Trigger circuit 23 outputs high-to-low or low-to-high pulse edges at predetermined times in response to S_{clock} to form an output signal.

[0035] Generally, two or more output signals are selectively outputted so that the average is $S(T_{out}, \phi_{out})$. For simplicity and ease of discussion, it is assumed that two signals, denoted as $S(T_{out1}, \phi_{out1})$ and $S(T_{out2}, \phi_{out2})$, are outputted by circuit 23. The predetermined times can be chosen so that the periods of the two output signals average to T_{out} ($T_{out} = (T_{out1} + T_{out2})/2$). Control circuit 26 can choose T_{out1} and T_{out2} similar to the rational rate approach so that the jitter is driven to a predetermined number of phase steps. The predetermined number of phase steps is generally less than m phase steps and, preferably, one phase step.

[0036] FIG. 4 illustrates a timing diagram 40 showing the phase-shifted reference signals and signals $S(T_{out1}, \phi_{out1})$, $S(T_{out2}, \phi_{out2})$, and $S(T_{out}, \phi_{out})$. A blown-up portion 50 of timing diagram 40 is also illustrated. As shown in blown-up portion 50, the phase-shifted signals

are same as signal $S_{ref}(T_0, \phi_0)$ except for having shifted phases (i.e. $\phi_0=0^\circ$, $\phi_1=90^\circ$, $\phi_2=180^\circ$, and $\phi_3=270^\circ$, for example) so that the phase-shifted signals are spaced apart over T_0 . The phases can be shifted in a manner similar to the fractional frequency divider approach. The accuracy of the output signal generally increases and the jitter decreases with more phase-shifted signals because there is better time resolution (i.e. the spacing between the phase shifted signals decreases).

[0037] In an example, assume it is desired to make T_{out} equal to $4.85 \cdot T_0$. Control circuit 26 determines that $4.85 \cdot T_0$ is between $T_{out1}=4.75 \cdot T_0$ and $T_{out2}=5.0 \cdot T_0$, where $4.75 \cdot T_0$ is four reference signal periods and four phase steps and $5.0 \cdot T_0$ is five reference signal periods and zero phase steps. If circuit 23 alternately outputs $S(T_{out1}, \phi_{out1})$ and $S(T_{out2}, \phi_{out2})$ an equal number of times over M clock cycles, then T_{out} will be $4.875 \cdot T_0$ ($(4.75 \cdot T_0 + 5.0 \cdot T_0) / 2 = 4.875 \cdot T_0$) which is within one phase step of $4.85 \cdot T_0$.

[0038] However, if circuit 23 outputs $S(T_{out1}, \phi_{out1})$ slightly more, then T_{out} can be driven closer to $4.85 \cdot T_0$. This is because the average will be reduced since T_{out1} is less than T_{out2} . T_{out1} can equal T_{out2} if T_{out} is an integer multiple of T_0 . In this case, T_{out1} and T_{out2} will also be integer multiples of T_0 and the jitter will be minimal if toggle circuit 23 outputs only T_{out1} or T_{out2} without alternating between them.

[0039] Hence, synthesizer 16 provides $S(T_{out}, \phi_{out})$ with a period T_0 that is an average of T_{out1} and T_{out2} . The average can be adjusted by changing $S_{Control}$ and S_{Enable} so that T_{out1} and T_{out2} are outputted a certain number of times over N clock cycles. If $S(T_{out1}, \phi_{out1})$ is outputted more, then T_{out} will decrease and if $S(T_{out2}, \phi_{out2})$ outputted more,

then T_{out} will increase. In this way, the jitter of $S(T_{out}, \phi_{out})$ can be driven to be on the order of one phase step if T_{out1} and T_{out2} are chosen to be within one phase step of T_0 .

[0040] FIG. 5 illustrates a more detailed block diagram of synthesizer 16 illustrated in FIG. 3. In FIG. 5, signal selection circuit 21 includes a multiplexer and toggle circuit 23 includes a D-Flip Flop. Control circuit 26 includes a pre-calculation logic circuit 27 coupled to a clock synthesis logic circuit 28. Clock synthesis circuit 28 determines the reference clock cycles and the phase steps to provide $S(T_{out1}, \phi_{out1})$ and $S(T_{out2}, \phi_{out2})$. Circuit 21 can include other electronic circuitry which can receive multiple input signals and output one of the signals in response to a control signal, but a multiplexer is illustrated here for simplicity. Toggle circuit 23 can include other toggling circuitry, such as a J-K Flip Flop or a latch which can change the state of its output in response to an input signal.

[0041] Precalculation logic circuit 27 receives M , m , and N and, in response, outputs to logic circuit 28 P' , $P'+1$, $-N \cdot Q'$, and $(1-Q') \cdot N$ according to the equality given by $M \cdot m / N = (P \cdot Q) \cdot m = P' \cdot Q'$. M and N are natural numbers and P and Q are integer and decimal numbers, respectively. Hence, M/N is a rational number expressed as a fraction and $P \cdot Q$ is its equivalent expressed as a decimal. P' is an integer number and Q' is a decimal number, respectively, of $(P \cdot Q) \cdot m$, which is the number of phase steps per clock cycle.

[0042] Hence, P' can be the number of phase steps in T_{out1} and $P'+1$ can be the number of phase steps in T_{out2} . Values $-N \cdot Q'$ and $(1-Q') \cdot N$ are the error in the number of

phase steps over N clock cycles if only $S(T_{\text{Out1}}, \phi_{\text{Out1}})$ or $S(T_{\text{Out2}}, \phi_{\text{Out2}})$, respectively, are outputted. Logic circuit 28 can provide S_{Enable} and S_{Control} to toggle circuit 23 and selection circuit 21, respectively, so that circuit 23 selectively outputs $S(T_{\text{Out1}}, \phi_{\text{Out1}})$ and $S(T_{\text{Out2}}, \phi_{\text{Out2}})$, as discussed above, in response to signals P' , $P'+1$, $-N \cdot Q'$, and $(1-Q') \cdot N$. In this way, $S(T_{\text{Out}}, \phi_{\text{Out}})$ is driven to be the average of $S(T_{\text{Out1}}, \phi_{\text{Out1}})$ and $S(T_{\text{Out2}}, \phi_{\text{Out2}})$.

[0043] In an example, assume it is desired to make T_{Out} equal to $4.58 \cdot T_0$. This can be rewritten as $(458/100) \cdot T_0$, so that $M=458$ and $N=100$. If there are $m=32$ phase steps per clock cycle, then $M \cdot m/N = (P \cdot Q) \cdot m = 146.56$ phase steps per reference signal period and $P'=146$ and $Q'=0.56$. In other words, 14,656 phase steps should be provided for every 100 reference clock cycles (i.e. $N=100$). In this case, precalculation circuit 27 will make $T_{\text{Out1}}=P'=146$ phase steps, $T_{\text{Out2}}=P'+1=147$ phase steps, $-Q' \cdot N=-56$ phase steps, and $(1-Q') \cdot N=44$ phase steps.

[0044] If T_{Out1} is outputted for $N=100$ clock cycles, then T_{Out} will be 14,600 phase steps which is underestimated by $-Q' \cdot N=-56$ phase steps. If T_{Out2} is outputted for $N=100$ clock cycles, then T_{Out} will be 14,700 phase steps which is overestimated by $(1-Q') \cdot N=44$ phase steps. Hence, values $-Q' \cdot N$ and $(1-Q') \cdot N$ are the errors in estimating T_{Out} by T_{Out1} and T_{Out2} , respectively, over $m \cdot M$ phase steps. Logic circuit 28 controls circuits 21 and 23 so that they alternately output one of $T_{\text{Out1}}=146$ phase steps and $T_{\text{Out2}}=147$ phase steps in response to logic circuit 28 so that an average of 14,566 phase steps are outputted after $N=100$ clock cycles. This will provide an average period of 146.56 phase steps per clock cycle, as desired.

[0045] FIG. 6 illustrates a simplified block diagram of circuit 27. Circuit 27 includes an A/B divider 81 where an input A is coupled to signals M and m through a multiplier 80. Multiplier 80 multiplies signal M by m and signal N is provided to input B. Signals N, m, and M can be provided from a memory element included in synthesizer 16 or they can be provided externally. Divider 81 forms the ratio $m \cdot M / N$ and outputs P' and Q' at respective outputs. An adder 84 adds one to P' to provide $P' + 1$. A multiplier 83 provides signal $-Q' \cdot N$ and a logic circuit 82 is coupled to divider 81 to provide signal $(1 - Q') \cdot N$.

[0046] FIG. 7 illustrates a simplified block diagram of clock synthesis logic circuit 28. Circuit 28 includes a signal selection circuit 70 coupled to a delay circuit 72 through a phase circuit 71. Circuit 70 receives signals P' , $P' + 1$, $-Q' \cdot N$, and $(1 - Q') \cdot N$ from circuit 27 and delay circuit 72 outputs S_{Enable} to both circuits 70 and 71. Circuit 70 provides $S(T_{\text{out1}}, \phi_{\text{out1}})$ and $S(T_{\text{out2}}, \phi_{\text{out2}})$ at different times to circuit 71 and circuit 71 provides a signal S_{Delay} to circuit 72 where S_{Delay} is equal to P. Circuit 71 also outputs signals S_{Control} and S_{Enable} to signal selection circuit 21 and toggle circuit 23, respectively (See FIG. 5).

[0047] In operation, circuit 70 determines which signal period, $T_{\text{out1}} = P'$ or $T_{\text{out2}} = P' + 1$, is outputted to circuit 71. This can be done by forming an error signal, denoted as S_{Error} , which is equal to the error in the number of phase steps in providing $m \cdot M$ phase steps. For example, if the average output period is less than the desired output period (i.e. T_{out}), then circuit 28 is underestimating the desired period. In this case, circuit 70 will output T_{out2} more to overestimate the

period for a certain number of clock cycles so that the average period is increased to the desired period. If the average period is greater than the desired period, then circuit 70 will output T_{out1} more to underestimate the desired period for a certain number of clock cycles so that the average period is decreased to the desired period.

[0048] Circuit 72 determines the number of full clock cycles, as indicated by P , that are in T_{out1} and T_{out2} . Circuit 72 can determine the number of clock cycles by counting up, down, or by delaying for a predetermined amount of time before triggering S_{Enable} . S_{Enable} is also provided to toggle circuit 23 so that it will be triggered at the correct time points to provide $S(T_{out1}, \phi_{out1})$ and $S(T_{out2}, \phi_{out2})$ with the correct high-to-low and low-to-high pulse edges as provided by signal selection circuit 21.

[0049] In response to S_{Enable} , phase selection circuit 71 determines the number of phase steps as indicated by Q' . The phase steps correspond to the fractional portion of T_{out1} or T_{out2} as provided by signal selection circuit 70. Circuit 71 can determine the correct number of phases by counting up, down, or by delaying for a predetermined amount of time. Once the correct number of phases has been determined, circuit 71 outputs this value to signal selection circuit 21 as $S_{Control}$ and, in response, circuit 21 outputs the correct phase shifted reference signal.

[0050] FIG. 8 illustrates a more detailed diagram of clock synthesis logic circuit 28. Signal selection circuit 70 includes an error register 41 clocked by S_{clock} . An output of register 41 is coupled to an adder 64 and a comparator circuit 43 through an adder 42. An output of comparator 43 is coupled to enables of signal selects 40

and 44. Signals $-Q' \cdot N$ and $(1-Q') \cdot N$ are provided to respective inputs of signal select 40 and signals P' and $P'+1$ are provided to respective inputs of signal select 44. An output of signal select 44 is coupled to phase circuit 71 and an output of signal select 40 is coupled to the input of register 41 through adder 64.

[0051] In operation, register 41 outputs its stored value during the current clock cycle, which can be zero at start-up. This value is added to $-Q' \cdot N$ (a negative number) by adder 42 to produce S_{Error} which is then compared to zero. If S_{Error} is less than zero, then signal select 40 outputs $(1-Q') \cdot N$ (a positive number) in response to S_{Select} . Signal $(1-Q') \cdot N$ is then added to the current stored value in register 41 and the result is stored in register 41 during the next clock cycle. The sequence is then repeated and S_{Error} becomes less negative until it is greater than zero. During the first clock cycle that S_{Error} is greater than zero, signal select 40 will output $(1-Q') \cdot N$ to adder 64 in response to S_{Select} . In this way, register 41 keeps a running total of the number of phase steps and adjusts the total so that $m \cdot M$ phase steps are provided for every N clock cycles.

[0052] Phase selection circuit 71 includes a phase step register 45 with an input coupled to the output of signal select 44. An output of register 45 is coupled to a delay register 46 and an adder 47. An output of register 46 is coupled to clock selection circuit 72. An output of adder 47 is coupled to an input of a phase select register 51. An output of register 51 is coupled to its input through adder 47 and also provides $S_{Control}$ to signal selection circuit 21 (See FIG. 3).

[0053] Register 45 receives P' or $P'+1$ from signal select 44 which are typically in digital form. The bits

in P' or $P'+1$ that correspond to the clock cycle are outputted by register 46 to clock selection circuit 72. Circuit 72 includes a signal select 57 with an output coupled to a clock select register 58. An output of register 58 is coupled to a comparator 60 and a subtractor 61. The output of register 46 and an output of subtractor 61 are coupled to respective inputs of signal select 57. An output of comparator 60 is coupled to an enable of signal select 57. The output of register 46 is also coupled to an input of an OR gate 63 through a comparator 59. The output of comparator 60 is coupled to another input to gate 63 through an enable register 62. Registers 58 and 62 are clocked by S_{Clock} .

[0054] Clock selection circuit 72 receives the bits in P' or $P'+1$ that correspond to the number of clock cycles and counts down to zero from this number during which time S_{Enable} is switched from low to high for one clock cycle. S_{Enable} is outputted to toggle circuit 21 (See FIG. 3) and is also coupled to the enables of registers 41, 45, and 46. In response to S_{Enable} being high, phase selection circuit 71 determines which phase step should be outputted by signal selection circuit 21 in response to S_{Control} .

[0055] Phase selection circuit 71 determines S_{Control} by receiving the bits that correspond to the phase steps in signals P' or $P'+1$ from register 45. These bits correspond to the phase step that is to be outputted by signal select circuit 21. This value is stored in register 51 so that it can be added to the phase steps in the next clock cycle when S_{Enable} is high again.

[0056] Adder 47 and register 51 form a phase select circuit 56 which can be substituted for by a phase select circuit 74, as indicated by substitution arrow 73. Circuit 74 can be used to reduce timing errors when

counting phase steps. Circuit 73 includes an adder 52 coupled to the output of register 51. The output of adder 52 and the input of register 51 are coupled to respective inputs of a signal select 53. The output of register 51 and the output of signal select 53 are coupled to respective inputs of a signal select 54. An output of signal select 54 is coupled to a phase delay register 55 which provides $S_{Control}$ at its output. The output of register 45 is also coupled to inputs of comparator 48 and a comparator 49. Outputs of comparators 48 and 49 are coupled to respective inputs of an OR gate 50. An output of gate 50 is coupled to an enable of signal select 53 and an enable of signal select 54 is coupled to S_{Enable} .

[0057] Phase selection circuit 74 determines $S_{Control}$ by receiving the bits that correspond to the phase steps in signals P' or $P'+1$ from register 45. These bits are compared to zero by comparator 48 and to $(m/2)-1$ by comparator 49. If the bits are equal to zero or greater than $(m/2)-1$, then gate 50 enables signal select 53 to output the input of register 51 to signal select 54. This value is then outputted by register 55 as $S_{Control}$ on the next clock cycle.

[0058] However, if the bits are between zero and $(m/2)-1$, then circuit 72 counts one fewer clock cycles in response to an indication from register 46. In these instances, gate 50 makes the enable of signal select 53 low so that $m/2$ phase steps (i.e. one-half a clock cycle) are added to $S_{Control}$ during the next clock cycle. The phase steps are then counted as before and $S_{Control}$ is outputted. For example, assume $m=32$ and it desired to provide 133 phase steps. This corresponds to four clock cycles and five phase steps. Circuit 72 will count three clock cycles which corresponds to 96 phase steps ($3 \cdot 32$

phase steps=96 phase steps). Adder 52 will then add 16 phase steps to give 112 phase steps and circuit 74 will count 21 more phase steps to give a total of 133 phase steps, as desired.

[0059] Hence, circuit 74 ensures that S_{Control} does not count by a number of phase steps less than $m/2$. This avoids timing errors which can result when counting between one or two phase steps, for example. The timing errors can occur because the probability of missing a clock edge increases as the number of phase-shifted reference signals increases. Hence, the timing errors are significantly reduced when counting a number of phase steps larger than $m/2$.

[0060] FIG. 9 illustrates another embodiment of pre-calculation logic circuit 27. FIG. 9 includes a logic circuit 120 which receives signal P' from the output of A/B divider 81 and logic circuits 121 and 122 which receive signals Q' and N . Logic circuit 120 provides values $P'+2$ and $P'-1$ to respective inputs of a signal select 123, $P'+1$ and P' to respective inputs of a signal select 124, and P' and $P'-1$ to respective inputs of a signal select 125. Logic circuit 122 provides $(2-Q') \cdot N$ and $(-1+Q') \cdot N$ to respective inputs of a signal select 126, $(1-Q') \cdot N$ and $-Q' \cdot N$ to respective inputs of a signal select 127, and $-Q' \cdot N$ and $(1-Q') \cdot N$ to respective inputs of a signal select 128.

[0061] Logic circuit 121 provides an enable signal S_{Enable1} to enable terminals of signal selects 123, 124, 125, 126, 127, and 128. When S_{Enable1} is high, signal selects 123, 124, and 125 can output $P'-1$, P' , and $P'+1$, respectively, and signal selects 126, 127, and 128 can output $(-1+Q') \cdot N$, $-Q' \cdot N$, and $(1-Q') \cdot N$, respectively. When S_{Enable1} is low, signal selects 123, 124, and 125 can output

$P'+2$, $P'+1$, and P' , respectively, and signal selects 126, 127, and 128 can output $(2-Q') \cdot N$, $(1-Q') \cdot N$, and $-Q' \cdot N$, respectively.

[0062] In operation, circuit 27 provides three signals to circuit 28 to dither between instead of two. The signals can be chosen based on how close $-Q'N$ is to P' or $P'+1$ as determined by logic circuit 121. For example, if signal $-Q'N$ is closer to P' , then $S_{Enable1}$ is high and the dithering is between $P'-1$, P' , and $P'+1$. However, if $-Q'N$ is closer to $P'+1$, then $S_{Enable1}$ is low and the dithering is between P' , $P'+1$, and $P'+2$. By dithering between three signals, low frequency fluctuations in $S(T_{out}, \phi_{out})$ are reduced. For example, if the period is close to P' and the dithering is only between P' and $P'+1$ as discussed in conjunction with FIG. 6, then the period will be P' for most of the M -th phase steps before it changes to $P'+1$ for a few phase steps towards the end. This change for only a few phase steps will cause low frequency fluctuation in the period which can increase the signal-to-noise ratio.

[0063] FIG. 10 illustrates another embodiment of signal selection circuit 70. In FIG. 10, circuit 70 is coupled to pre-calculation circuit 27 as illustrated in FIG. 9. Signal selection circuit 70 includes error register 41 clocked by S_{clock} with the output coupled to adder 64 and comparator circuit 43 through adder 42. The output of comparator 43 is coupled to enables of signal selects 40 and 44. The output of signal select 40 is coupled to an input of a signal select 75 and the output of signal select 75 is coupled to adder 64.

[0064] A D flip-flop 77 has an enable coupled to the enable of register 41 and a clock terminal coupled to S_{clock} . The inverting output of flip-flop 77 is coupled to

its D input and its non-inverting output is coupled to enables of signal select 75 and a signal select 76. The output of signal select 44 is coupled to an input of signal select 76 and the output of signal select 76 is coupled to circuit 71.

[0065] Respective inputs of signal select 44 receive signals $P'+2$ and $P'+1$ when $S_{Enable1}$ is low and receive $P'-1$ and P' when $S_{Enable1}$ is high. The other input of signal select 76 receives P' when $S_{Enable1}$ is low and $P'+1$ when $S_{Enable1}$ is high. Signals $(2-Q') \cdot N$ and $(1-Q') \cdot N$ are provided to respective inputs of signal select 40 when $S_{Enable1}$ is high and $(-1+Q') \cdot N$ and $-Q' \cdot N$ are provided when $S_{Enable1}$ is low. Signal $-Q' \cdot N$ is provided to the other input of signal select 75 when $S_{Enable1}$ is low and $(1-Q') \cdot N$ is provided when $S_{Enable1}$ is high.

[0066] In operation and assuming $S_{Enable1}$ is low, register 41 outputs its stored value during the current clock cycle, which can be zero at start-up. This value is added to $(1-Q') \cdot N$ by adder 42 to produce S_{Error} which is then compared to zero. If S_{Error} is less than zero, then a signal $S_{Select1}$ is low and signal select 40 outputs $(2-Q') \cdot N$ and signal select 44 outputs $P'+2$. Signal $(1-Q') \cdot N$ is then added to the current stored value in register 41 and the result is stored in register 41 during the next clock cycle.

[0067] When S_{Error} becomes greater than zero, $S_{Select1}$ will be high and signals selects 40 and 44 will output $(1-Q') \cdot N$ and $P'+1$, respectively, and the process will repeat. Flip-Flop 77 behaves as an oscillator which alternately makes a signal $S_{Select2}$ high and low. In this way, the value outputted to circuit 71 by signal select 76 is different for every clock cycle. Hence, the period

is moving between three sub-frequencies instead of two so that if the desired period is close to P' or $P'+1$, then the circuit will not output these values too many times in a row. It will instead alternate between outputting $P'-1$, P' , and $P'+1$ if the period is near P' or P' , $P'+1$, and $P'+2$ if the period is near $P'+1$. In this way, low frequency oscillations in T_{out} will be reduced because the jitter in $S(T_{out}, \phi_{out})$ is always changing.

[0068] FIG. 11 illustrates a simplified flow diagram 100 of a method of generating an output signal with a desired period. The method includes a step 102 of providing phase-shifted reference signals. The phase-shifted reference signals generally have the same period and an equal spacing across the reference signal period. A step 104 includes generating first and second signals in response to the phase-shifted reference signals. A step 106 includes a step of outputting one of the first and second signals so that an average period of an output signal is driven to within a predetermined number of phase steps of a desired period.

[0069] The first and second signals are typically generated by choosing edges of the reference signals so that the first and second signals have periods which are a certain number of phase steps from the desired period. The first and second signals can be generated by counting periods and/or phase steps in the phase-shifted reference signals. If counting phase steps, then step 104 can include a step of counting a predetermined minimum number of phase steps to reduce timing errors. This can be done if the phase steps are closely spaced to avoid missing a clock edge.

[0070] Step 106 can include a step of outputting one of the first and second signals in response to an error signal. The error signal can be proportional to the

difference between the average and desired periods. The first and second signals can be outputted with periods an integer multiple of the reference clock period or the multiple can be given by $P \cdot Q$. Hence, the first and second signals can be generated by counting a number of reference signal periods equal to P and a number of phase steps equal to $N \cdot Q$.

[0071] In step 106, the first and second signals can be alternately outputted in response to the error signal, where the error signal is typically chosen to drive $(P \cdot Q) \cdot m$ to be $M \cdot m / N$. Hence, the error signal can be adjusted in response to an indication that $M \cdot m / N$ does not equal $(P \cdot Q) \cdot m$. To do this, the error signal can be decreased by $N \cdot Q$ phase steps in response to an indication that $(P \cdot Q) \cdot m$ is greater than $M \cdot m / N$ or it can be increased by $(1 - Q) \cdot N$ phase steps in response to an indication that $(P \cdot Q) \cdot m$ is less than $M \cdot m / N$. The error signal is typically adjusted to drive the average period to be within one phase step of the desired period to minimize the jitter in the output signal.

[0072] FIG. 12 illustrates a simplified flow diagram 130 of another method of generating the output signal with a desired period. The method includes a step 132 of providing the phase-shifted reference signals. A step 134 includes generating first, second, and third signals in response to the phase-shifted signals. The first, second, and third signals can be generated as in method 100. A step 136 includes a step of outputting one of the first, second, and third signals so that the average period of the output signal is driven to within a predetermined number of phase steps of a desired period.

[0073] Step 136 can include a step of providing the second signal with a period greater than the first signal when the desired period is a non-integer multiple of the reference signal period. The period of the third signal can be chosen based on how close the desired period is to P' or $P'+1$ phase steps. If the desired period is closer to P' phase steps, then the third signal can have a period less than P' and if the desired period is closer to $P'+1$ phase steps, then the third signal can have a period greater than $P'+1$. In this way, the first, second, and third signals can be selectively outputted in step 136 so that the jitter is different in each sequential clock cycle. By changing the jitter, low frequency signals in the desired output signal can be minimized.

[0074] Step 136 can include a step of alternating between outputting the first, second, and third signals in response to the error signal. The error signal can be adjusted in response to an indication that $M \cdot m / N$ does not equal $P \cdot Q$ in a manner similar to method 100. Hence, the error signal can be decreased by $N \cdot Q$ or $(Q+1) \cdot N$ in response to an indication that $(P \cdot Q) \cdot m$ is greater than $M \cdot m / N$. The error signal can also be increased by $(1-Q) \cdot N$ or $(2-Q) \cdot N$ in response to an indication that $(P \cdot Q) \cdot m$ is less than $M \cdot m / N$.

[0075] If the desired period is close to P' , then step 136 can include a step of adjusting the error signal by one of $(Q+1) \cdot N$, $Q \cdot N$, and $(N-Q)$ in response to an indication that $M \cdot m$ is within a predetermined number of phase steps from $(P \cdot Q) \cdot m \cdot N$. If the desired period is close to $P'+1$, then step 136 can include a step of adjusting the error signal by one of $Q \cdot N$, $(1-Q) \cdot N$, and $(2-$

Q)·N in response to an indication that M·m is within a predetermined number of phase steps from (P+1)·N·m.

[0076] Thus, a frequency synthesizer that can provide an output signal with a period being a multiple of another signal period has been disclosed. The synthesizer can selectively output two or more signals with periods close to the desired period of the output signal. The periods of the signals can be provided by phase shifted reference signals. The signals can be selectively outputted so that the average period of the output signal is driven to the desired period. More than two output signals can be used and dithered between to minimize low frequency signals in the output signal. In this way, the frequency synthesizer can provide less jitter at a given reference frequency.

[0077] The embodiments of the invention described herein are exemplary and numerous modifications, variations and rearrangements can be readily envisioned to achieve substantially equivalent results, all of which are intended to be embraced within the spirit and scope of the invention as defined in the appended claims.

I CLAIM:

1. A frequency synthesizer, comprising:
a circuit which alternately outputs multiple output signals having different respective periods to drive the average period of the output signal to within a predetermined number of phase steps of a desired period, said phase steps being provided by a plurality of phase-shifted reference clock signals.
2. The synthesizer of claim 1, wherein said circuit provides said first and second output signals by counting periods and/or phase steps in said plurality of phase-shifted reference clock signals.
3. The synthesizer of claim 1, wherein said circuit counts a predetermined minimum number of phase steps to reduce timing errors.
4. The synthesizer of claim 1, wherein said circuit outputs one of said multiple output signals in response to an error signal which is equal to the difference between said average and desired periods.
5. The synthesizer of claim 4, wherein said multiple output signals include first and second output signals with periods which are multiples of said reference clock period, said multiples being given by $P.Q(1)$ and $P.Q(2)$, respectively, where P is an integer and Q is a decimal.

6. The synthesizer of claim 5, wherein said desired period is equal to Mm/N , where m is the number of phase steps in one reference clock period and M/N is a multiplier relating said output signal period to a period of an input signal provided to said synthesizer, in which M and N are natural numbers.

7. The synthesizer of claim 6, wherein said circuit counts a number of reference clock periods in response to P and a number of phase steps in response to Q .

8. The synthesizer of claim 6, wherein said circuit alternates between outputting said first and second signals in response to said error signal, and adjusts said error signal in response to an indication that Mm/N does not equal the average of $(P.Q(1))m$ and $(P.Q(2))m$.

9. The synthesizer of claim 8, wherein said circuit reduces said error signal by NQ phase steps in response to an indication that the average of $(P.Q(1))m$ and $(P.Q(2))m$ is greater than Mm/N .

10. The synthesizer of claim 8, wherein said circuit increases said error signal by $(1-Q)N$ phase steps in response to an indication that the average of $(P.Q(1))m$ and $(P.Q(2))m$ is less than Mm/N .

11. The synthesizer of claim 8, wherein said circuit adjusts said error signal to drive said average period to be within one phase step of said desired period.

12. The synthesizer of claim 5, wherein said second signal has a period greater than said first signal when said desired period is a non-integer multiple of said reference signal period.

13. The synthesizer of claim 12, wherein said multiple output signals further include a third signal with a period $P.Q(3)$ either smaller than $P.Q(1)$ or larger than $P.Q(2)$, said circuit alternating between outputting said first, second, and third signals in response to said error signal, and adjusting said error signal in response to an indication that M_m/N does not equal the average of $(P.Q(1))_m$, $(P.Q(2))_m$, and $(P.Q(3))_m$.

14. The synthesizer of claim 13, wherein said circuit reduces said error signal by NQ or $(Q+1)N$ phase steps in response to an indication that the average of $(P.Q(1))_m$, $(P.Q(2))_m$, and $(P.Q(3))_m$ is greater than M_m .

15. The synthesizer of claim 13, wherein said circuit increases said error signal by $(1-Q)N$ or $(2-Q)N$ phase steps in response to an indication that the average of $(P.Q(1))_m$, $(P.Q(2))_m$, and $(P.Q(3))_m$ is less than M_m .

16. The synthesizer of claim 13, wherein said circuit adjusts said error signal by $(Q+1)N$, QN , or $(1-Q)N$ phase steps in response to an indication that M_m is within a predetermined number of phase steps from $(P.Q(1))_mN$.

17. The synthesizer of claim 13, wherein said circuit adjusts said error signal by QN , $(1-Q)N$, or $(2-Q)N$ phase steps in response to an indication that M_m is

within a predetermined number of phase steps from $((P.Q(1))^{m+1})N$.

18. A pulse generator, comprising:

a circuit which provides multiple output signals in response to a predetermined number of reference signal periods and/or phase steps in a plurality of phase-shifted reference signals; and

said circuit dithering said multiple output signals to form a combined output signal with a desired period.

19. The generator of claim 18, wherein said circuit dithers between outputting said multiple output signals to drive said combined output signal period to within one phase step of said desired period.

20. The generator of claim 18, wherein said circuit dithers by alternating between outputting said multiple output signals so that the average period of said combined output signal is driven to said desired period.

21. The generator of claim 20, said circuit further providing an error signal equal to the difference between said average and desired periods, said error signal controlling said dithering.

22. The generator of claim 18, wherein said circuit counts at least the number of phase steps in one reference signal period to reduce timing errors.

23. The generator of claim 18, wherein each period of said multiple output signals is a multiple of one phase step.

24. The generator of claim 18, wherein said circuit generates said multiple output signals by counting periods and/or phase steps of said phase-shifted reference signals.

25. The generator of claim 18, wherein said multiple output signals are outputted in response to an indication that the number of phase steps in said plurality of phase-shifted reference signals is equal to a predetermined value.

26. The generator of claim 18, wherein said circuit dithers between said multiple output signals so that the jitter of said combined output signal is driven to be one phase step when said desired period is a non-integer multiple of said reference signal period.

27. The generator of claim 18, wherein said multiple output signals include first and second output signals, said second signal with a period larger than or equal to said first signal when said desired period is a non-integer multiple of or equal to said reference signal period, respectively.

28. The generator of claim 27, wherein said multiple output signals further include a third signal with a period either smaller than said first signal or larger than said second signal, said dithering occurring between said first, second, and third signals.

29. The generator of claim 28, wherein said circuit adjusts said dithering to reduce frequency fluctuations in said output signal.

30. A frequency synthesizer system, comprising:

a signal selection circuit which outputs a selected phase-shifted reference signal in a plurality of phase-shifted reference signals in response to a control signal;

a toggle circuit coupled to an output of said signal selection circuit, said toggle circuit alternately toggling between outputting multiple output signals in response to a select signal; and

a control circuit coupled to said output of said signal selection circuit, said control circuit providing said control and select signals to said signal selection and toggle circuits, respectively, so that said multiple output signals form a combined output signal with an average period driven to within a predetermined number of phase steps of a desired period.

31. The system of claim 30, further comprising electronic circuitry that operates together with said frequency synthesizer as a digital phase locked loop.

32. The system of claim 31, wherein said electronic circuitry includes a phase detector, said digital phase locked loop providing said combined output signal from said frequency synthesizer as a multiple of an input signal period provided to said phase detector.

33. The system of claim 31, further comprising a signal conditioning system which receives and processes data in response to said combined output signal.

34. The clock of claim 33, further comprising an analog phase locked loop coupled between said signal conditioning system and said digital phase locked loop,

said analog phase locked loop reducing high frequency noise in said combined output signal provided by said digital phase locked loop.

35. The clock of claim 33, wherein said signal conditioning system includes at least one of an analog-to-digital converter, a digital-to-analog converter, a data transmission system, and a display device.

36. The system of claim 30, further comprising electronic circuitry coupled to said frequency synthesizer so that said average period is a multiple of a period of an input signal provided to said electronic circuitry, said input and combined output signals being in phase.

37. A method of generating an output signal with a desired period with a frequency synthesizer, comprising:

outputting multiple output signals so that an average period of a combined output signal is driven to within a predetermined number of phase steps of a desired period; and

providing said phase steps by a plurality of phase-shifted reference signals.

38. The method of claim 37, wherein the step of providing said multiple output signals includes counting periods and/or phase steps in said plurality of phase-shifted reference signals.

39. The method of claim 37, wherein the step of providing said multiple output signals includes counting a predetermined minimum number of phase steps to reduce timing errors.

40. The method of claim 37, wherein the step of providing said multiple output signals includes outputting said multiple output signals in response to an error signal, said error signal being proportional to the difference between said average and desired periods.

41. The method of claim 40, wherein the step of providing said multiple output signals includes outputting first and second output signals with periods which are a multiple of said reference clock period, said multiples being given by $P.Q(1)$ and $P.Q(2)$, respectively, where P is the integer part and Q is the fractional part.

42. The method of claim 41, wherein the step of outputting said first and second signals includes making the average of $(P.Q(1))^m$ and $(P.Q(2))^m$ equal to Mm/N , where M is the period of an input signal to said frequency synthesizer, m is the number of phase steps per reference clock period, and N is a divisor which relates M to said desired period.

43. The method of claim 42, wherein the step of outputting said first and second signals includes counting a number of reference signals in response to P and a number of phase steps in response to Q .

44. The method of claim 42, wherein the step of outputting said first and second signals includes alternating between outputting said first and second signals in response to said error signal, and adjusting said error signal in response to an indication that Mm/N does not equal the average of $(P.Q(1))^m$ and $(P.Q(2))^m$.

45. The method of claim 44, wherein the step of outputting said first and second signals includes reducing said error signal by $N \cdot Q$ phase steps in response to an indication that the average of $(P \cdot Q(1))_m$ and $(P \cdot Q(2))_m$ is greater than M_m/N .

46. The method of claim 44, wherein the step of outputting said first and second signals includes increasing said error signal by $(1-Q)N$ in response to an indication that the average of $(P \cdot Q(1))_m$ and $(P \cdot Q(2))_m$ is less than M_m/N .

47. The method of claim 44, wherein the step of outputting said first and second signals includes adjusting said error signal to drive said average period to be within one phase step of said desired period.

48. The method of claim 41, wherein the step of outputting said first and second signals includes providing said second signal with a period greater than said first signal when said desired period is a non-integer multiple of said reference signal period.

49. The method of claim 48, wherein the step of outputting said multiple output signals includes outputting a third signal with a period $P \cdot Q(3)$ either smaller than $P \cdot Q(1)$ or larger than $P \cdot Q(2)$.

50. The method of claim 49, further including the step of alternating between outputting said first, second, and third signals in response to said error signal, and adjusting said error signal in response to an indication that M_m/N does not equal the average of $(P \cdot Q(1))_m$, $(P \cdot Q(2))_m$, and $(P \cdot Q(3))_m$.

51. The method of claim 50, wherein the step of alternating between outputting said first, second, and third signals includes reducing said error signal by $N \cdot Q$ or $(Q+1)N$ in response to an indication that the average of $(P.Q(1))_m$, $(P.Q(2))_m$, and $(P.Q(3))_m$ is greater than M_m/N .

52. The method of claim 50, wherein the step of alternating between outputting said first, second, and third signals includes increasing said error signal by $(1-Q)N$ or $(2-Q)N$ in response to an indication that the average of $(P.Q(1))_m$, $(P.Q(2))_m$, and $(P.Q(3))_m$ is less than M_m/N .

53. The method of claim 51, further including the step of adjusting said error signal by one of $(Q+1)N$, QN , and $(N-Q)$ in response to an indication that M_m is within a predetermined number of phase steps from $(P.Q(1))_m N$.

54. The method of claim 52, further including the step of adjusting said error signal by one of $Q \cdot N$, $(1-Q)N$, and $(2-Q)N$ in response to an indication that M_m is within a predetermined number of phase steps from $((P.Q(1))_m + 1)N$.

FIG. 1

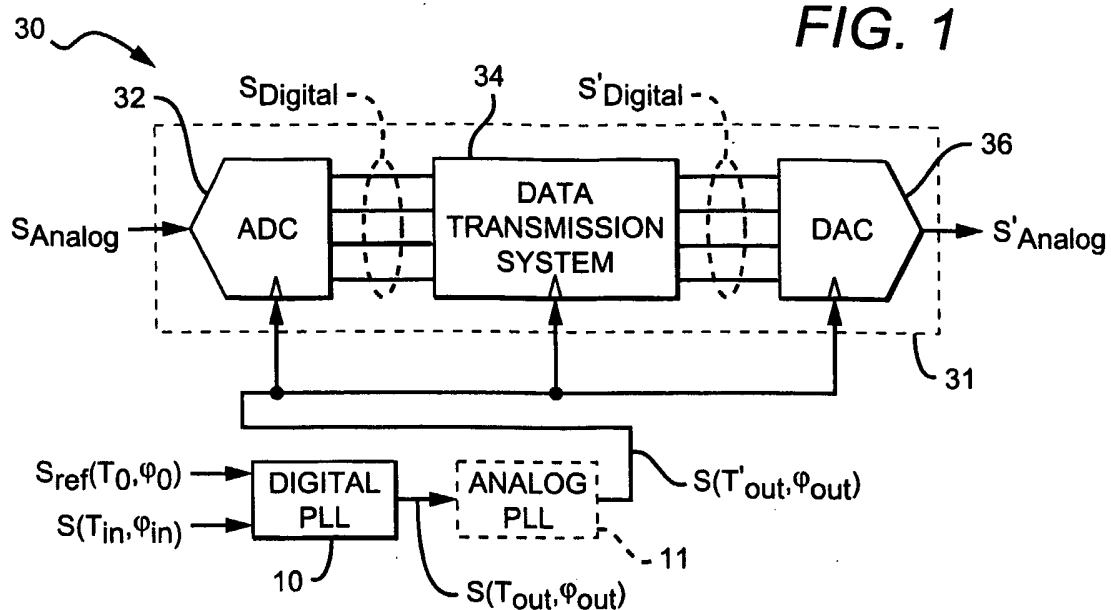
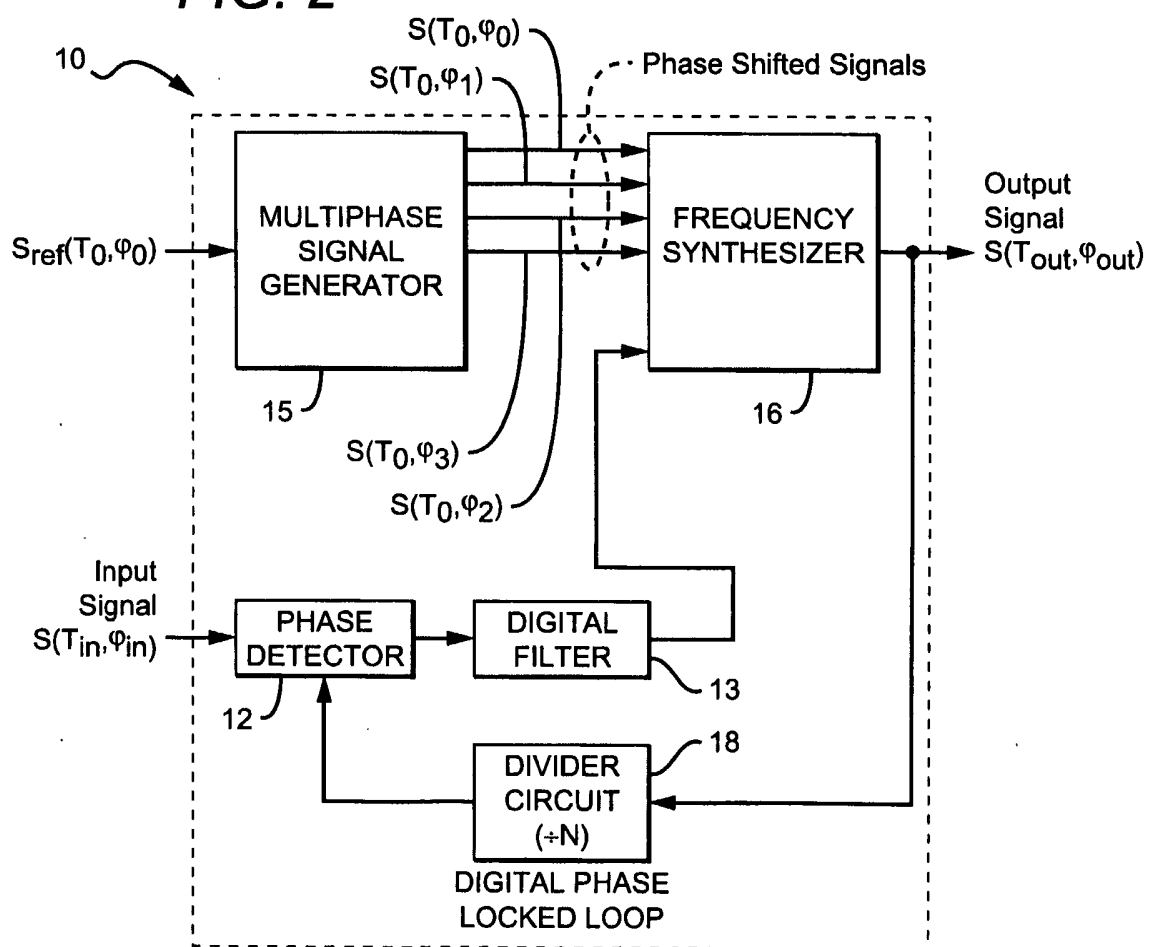


FIG. 2



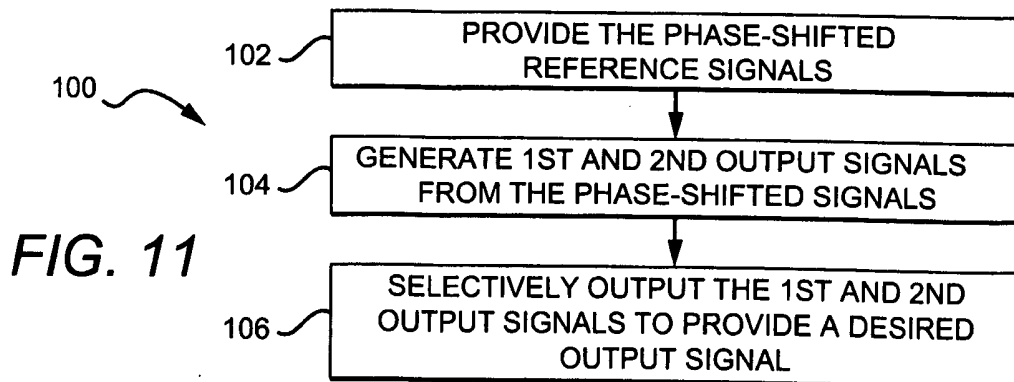
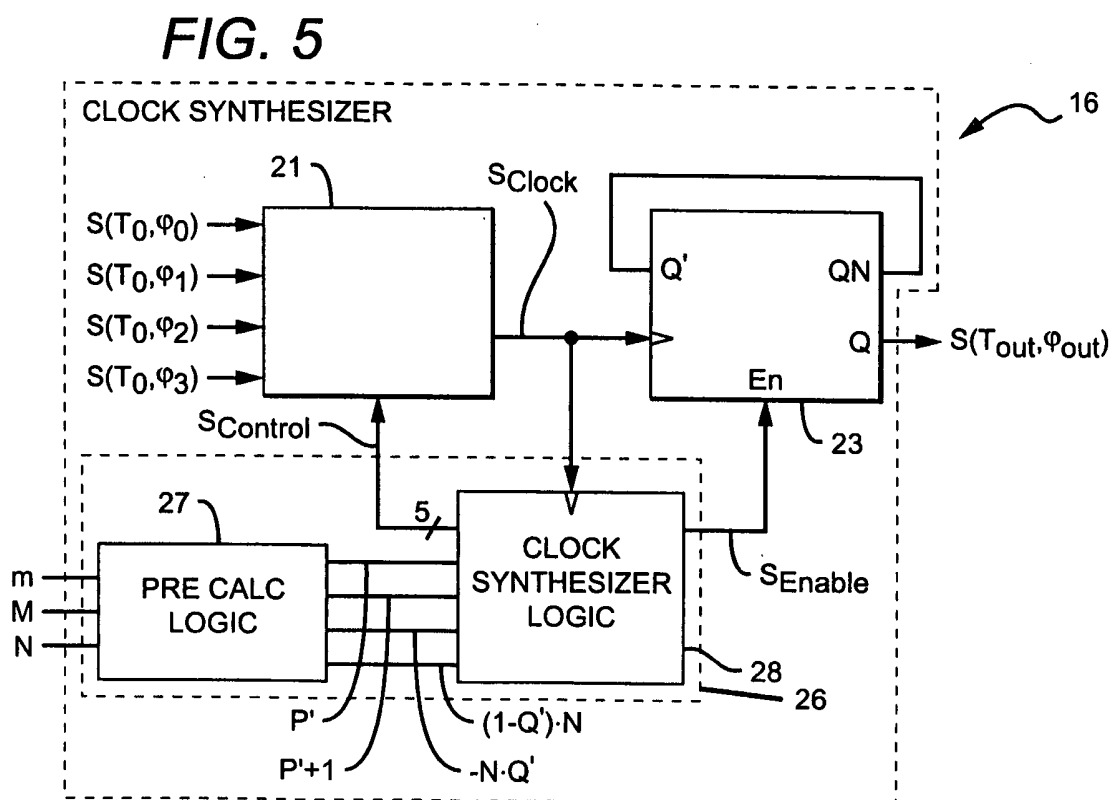
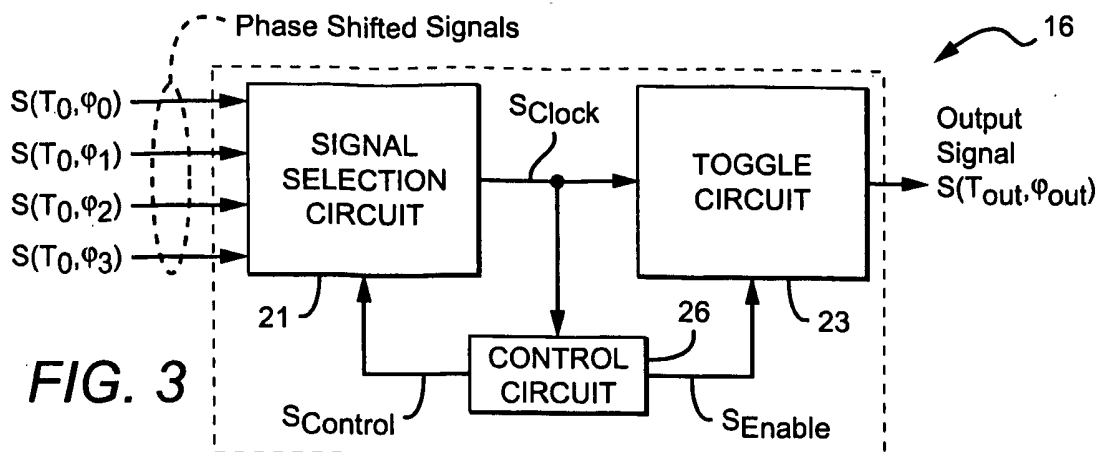
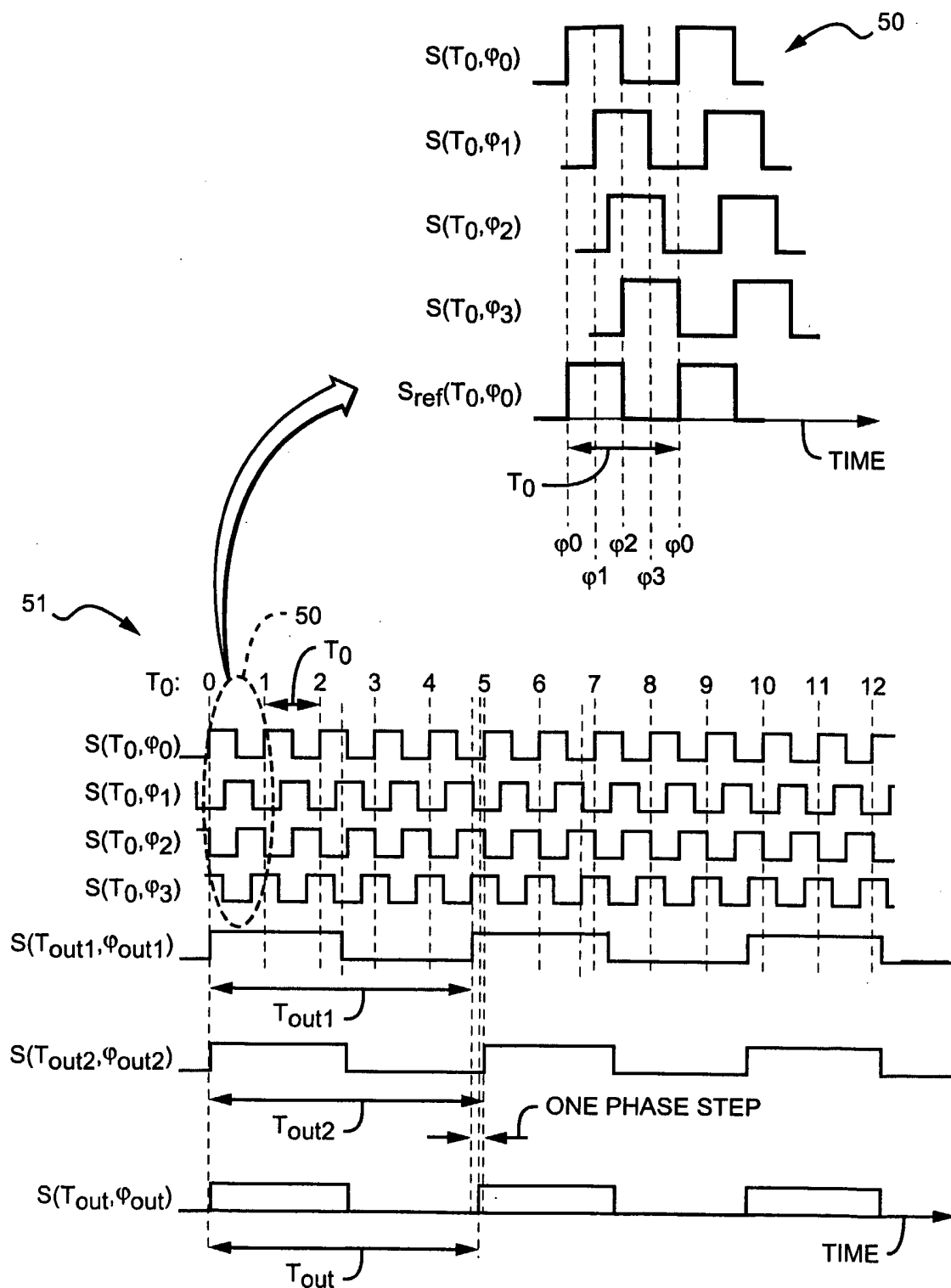


FIG. 4



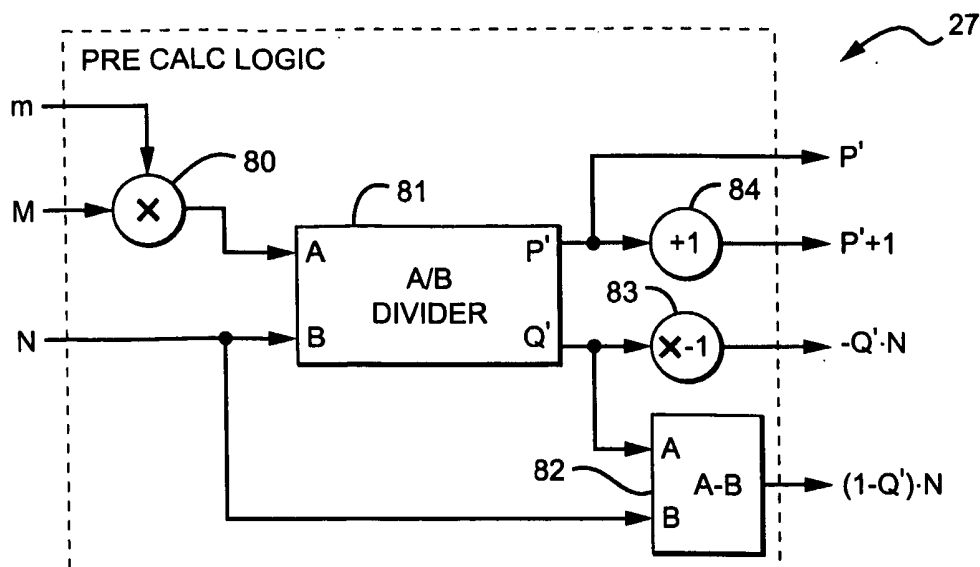


FIG. 6

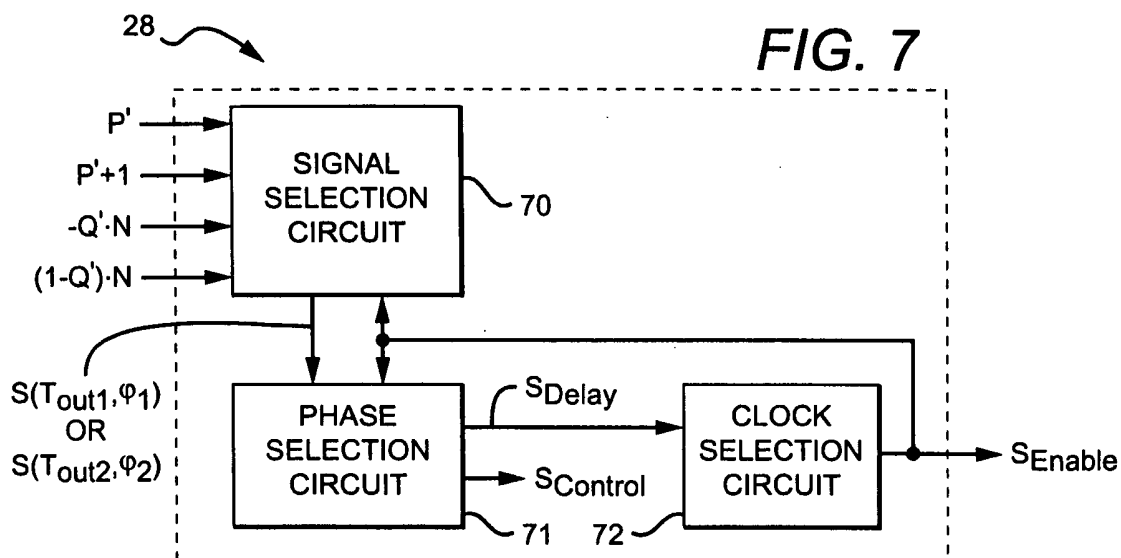


FIG. 7

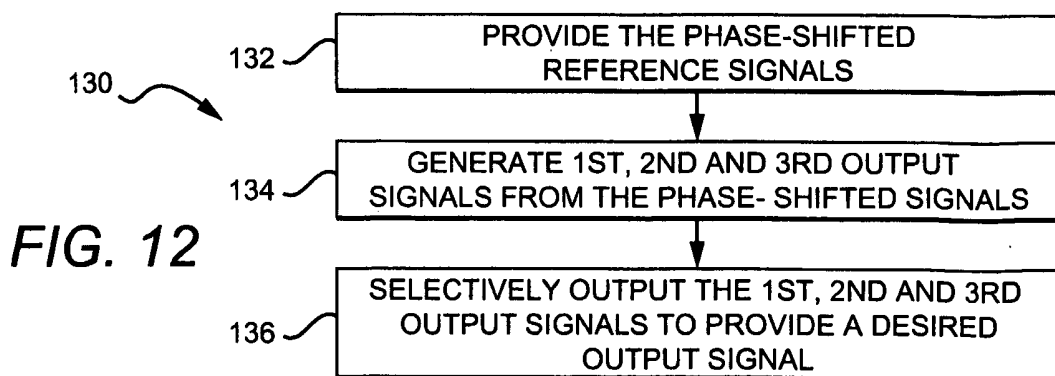


FIG. 12

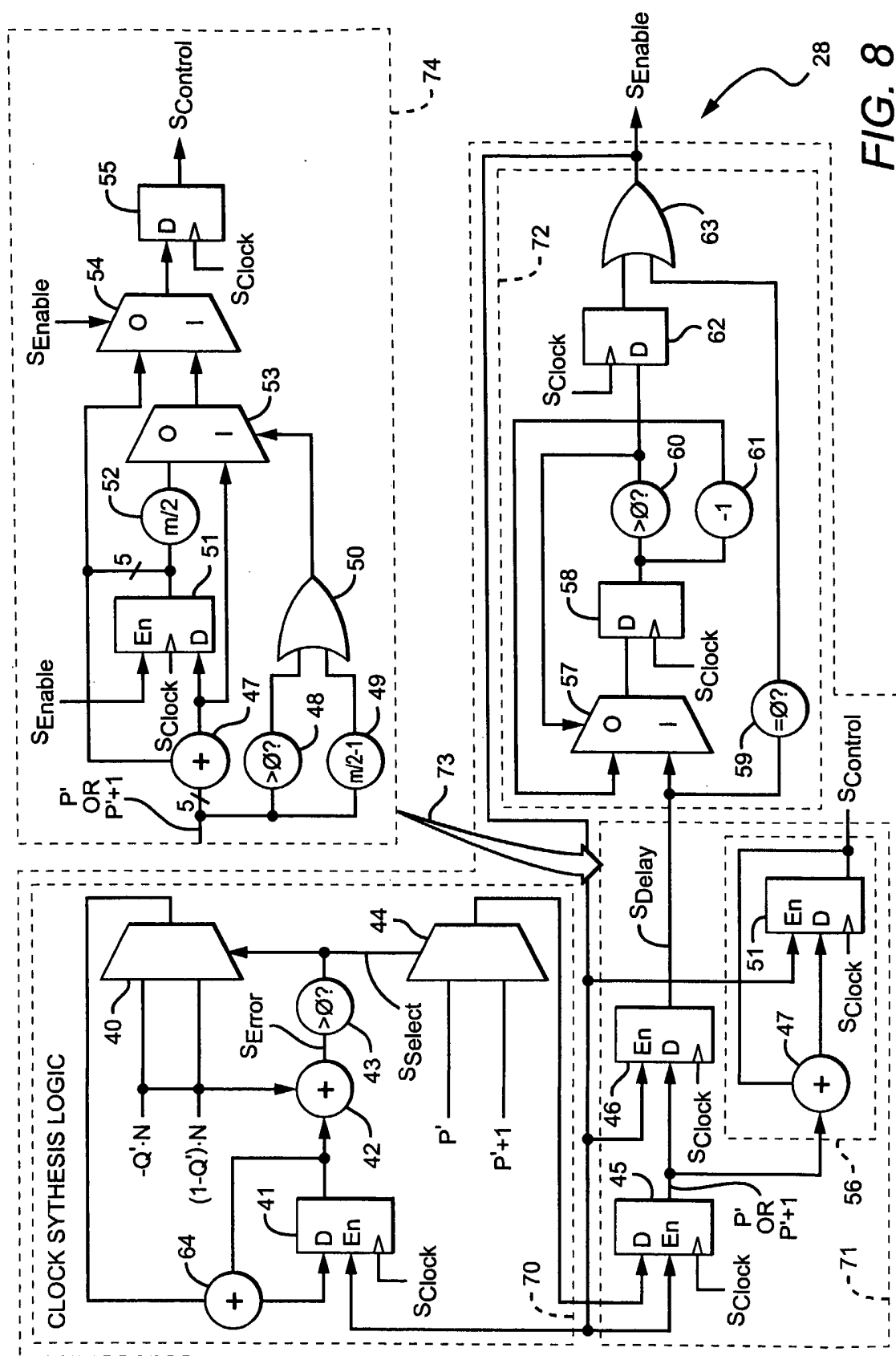


FIG. 8

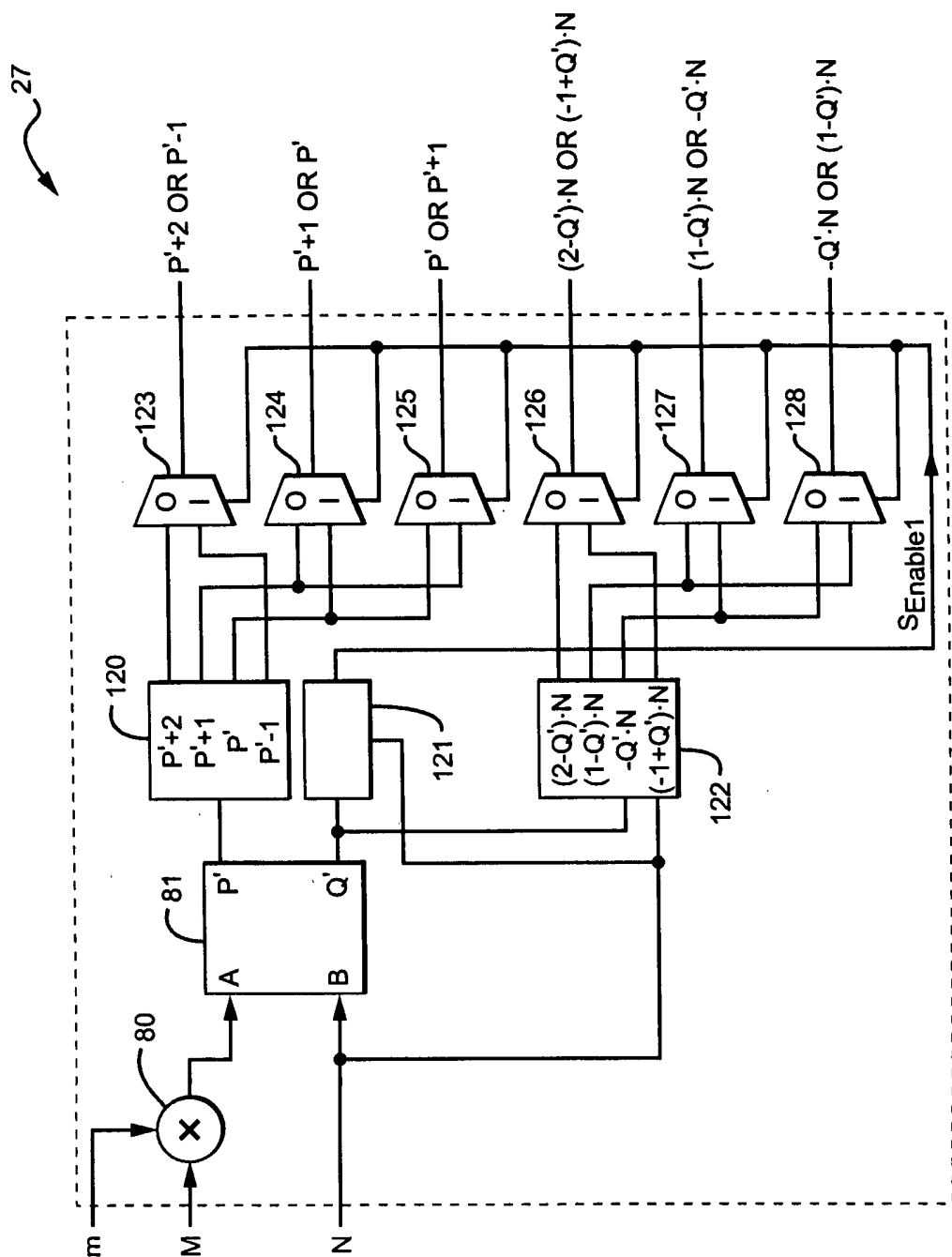
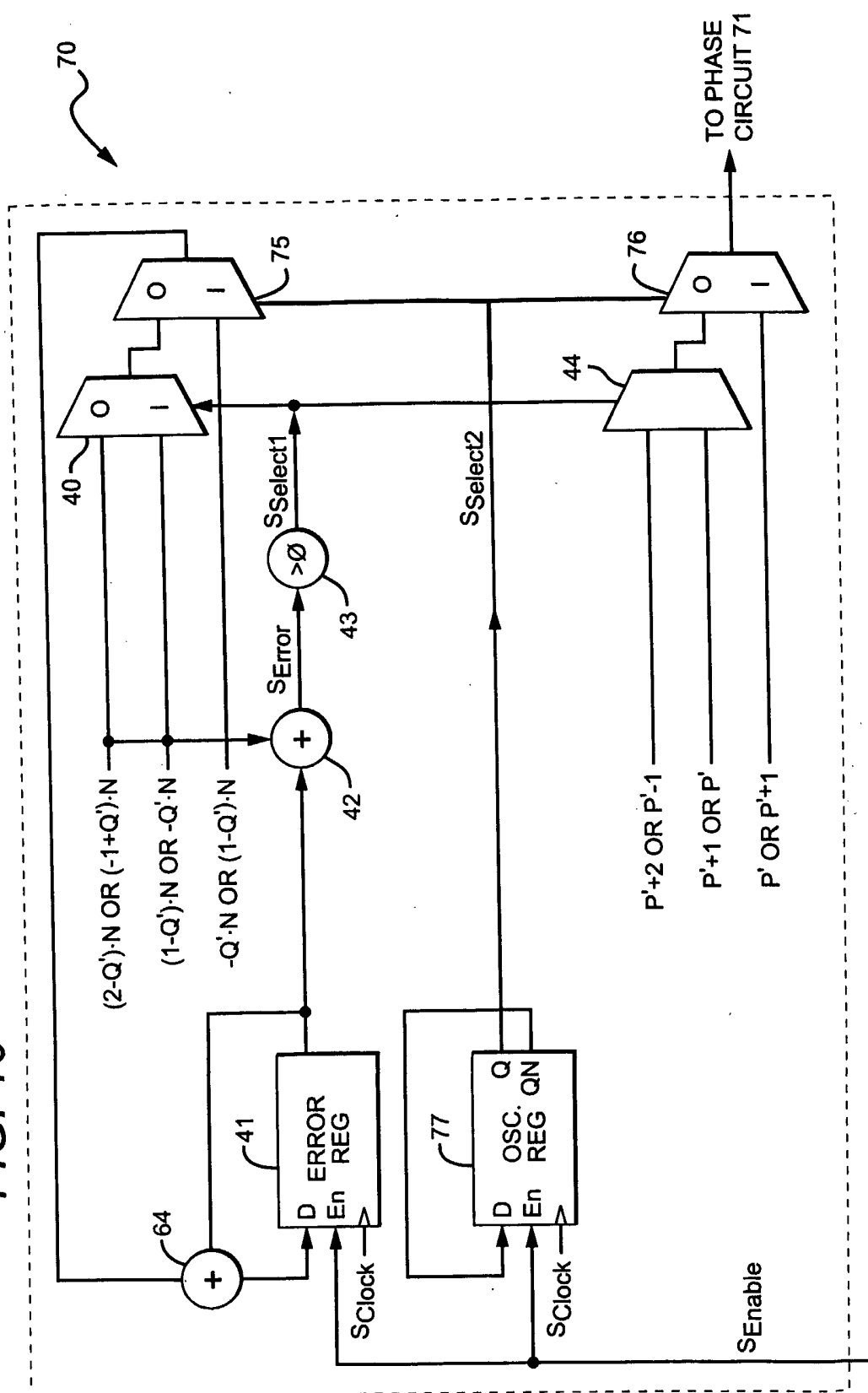


FIG. 9

FIG. 10



INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2005/011486

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H03K5/13 G06F1/025 H03L7/18 H03K23/68

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H03L H03K G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 970 110 A (LI ET AL) 19 October 1999 (1999-10-19) column 3, line 49 - column 6, line 44; figures 1-6 -----	1-3, 18-20, 22-27, 30-32, 36-39
X	US 6 353 649 B1 (BOCKLEMAN DAVID E ET AL) 5 March 2002 (2002-03-05) column 2, line 3 - column 4, line 56; figures 2,3 ----- -/--	1-3, 18-20, 22-27, 30-32, 36-39

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

- *A* document defining the general state of the art which is not considered to be of particular relevance
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- *O* document referring to an oral disclosure, use, exhibition or other means
- *P* document published prior to the international filing date but later than the priority date claimed

- *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- *&* document member of the same patent family

Date of the actual completion of the international search

27 June 2005

Date of mailing of the international search report

05/07/2005

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Aouichi, M

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2005/011486

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002/101955 A1 (POULLET FREDERIC) 1 August 2002 (2002-08-01) page 2, paragraph 34 - page 3, paragraph 47; figures 2,3 -----	1,18,30, 37
A	US 5 889 436 A (YEUNG ET AL) 30 March 1999 (1999-03-30) column 3, line 23 - column 6, line 25; figures 3-7 -----	1-54

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US2005/011486

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 5970110	A	19-10-1999	NONE	
US 6353649	B1	05-03-2002	NONE	
US 2002101955	A1	01-08-2002	FR 2820254 A1 JP 2002305440 A	02-08-2002 18-10-2002
US 5889436	A	30-03-1999	NONE	