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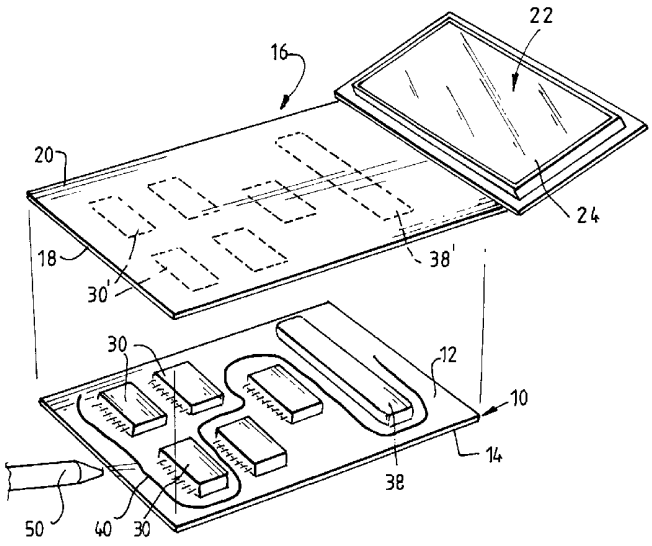
(54) Title: CIRCUIT BOARD ARRANGEMENT AND FUNDS TRANSACTION DEVICE



(57) Abstract: A circuit board assembly is disclosed which includes a first printed circuit board (10) and a second printed circuit board (16). First side (12) of the first board (10) includes security sensitive electronic circuits (30) together with security sensitive traces. The circuit boards include connectors (38) and (38') which couple together when the boards are connected together. Epoxy resin sufficient to entirely fill the space between the boards (12) and (14) is applied to the board from a dispenser so as to embed a security wire (40) and the circuits (30) within the epoxy resin and surround the signal traces on the sides (12) and (18). Each of the boards may be formed from a multi-layer construction in which one of the sides of one of the layers including a ground plane and the security trace being formed on an internal surface of the layer structure. Vias are provided in the layers which do not extend to an outsider of one of the layers.

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CIRCUIT BOARD ARRANGEMENT AND FUNDS TRANSACTION DEVICE

FIELD OF THE INVENTION

This invention relates to a circuit board arrangement and, in particular, but not exclusively, to a circuit board arrangement for a funds transaction device in which security sensitive transactions take place.

DESCRIPTION OF THE PRIOR ART

Products designed for use in security sensitive applications (eg banking applications) have often faced the requirement to mitigate their potential for miss-use, or the ability of a malicious third party to violate its secure functionality. Many options for such mitigation have thus arisen; initially it was deemed acceptable to merely encase the security sensitive components of the product (usually the internal Printed Circuit Boards) in epoxy resin. However, the judicious application of certain solvents would often prove this measure as ineffective. New integrated circuits were developed with added security features (such as the Dallas Semiconductor DS500X series of controllers), but work-arounds and loop-holes were found in the device security and exploited by attackers. Some devices used a combination of the epoxy and secure controller, with the added feature of embedding a loose wire in the epoxy resin, to "detect" any intrusion into the volume of the resin; if the wire was broken (or melted by solvent) a security violation would be detected and acted upon. However, careful solvent selection and application could still be used to penetrate such a device, as it could be applied slowly, with each layer of the epoxy removed before a subsequent application.

SUMMARY OF THE INVENTION

The object of the present invention is to provide a circuit board arrangement in which greater security is provided and which is applicable to a funds transaction device and

elsewhere where security sensitive applications are needed.

The invention may be said to reside in a circuit board assembly, including;

a first printed circuit board having a first side and a second side;

a second board having a first side and a second side;

circuit components mounted on the first side of the first printed circuit board and signal traces formed on the first side of the first board for interconnecting the circuit components;

the first and second boards being arranged adjacent one another and with the first sides facing one another; and

a filler material disposed between the first sides of the first and second boards, which adheres to the first sides of the first and second circuit boards and embeds the circuit components within the filler material and surrounds the signal traces to form a monolithic circuit board assembly.

Thus, since the circuit components are located in the interior of the assembly and encased between two circuit boards access to the circuit component is extremely difficult without destroying the assembly

Preferably the second board is a second printed circuit board.

Preferably the circuit components are arranged on both the first side of first circuit board and the first side of the second circuit board and the components on one of the circuit boards are staggered with respect to components on the other circuit board so as to sit within valleys formed by components on the other circuit board to ensure that the space between the first and second circuit boards is as

small as possible.

In one embodiment a security wire is provided between the first and second boards and embedded in the filler material for providing a violation signal indicative of an attempt to break through the first or second circuit boards.

The second sides of the first and second circuit boards may include circuit components and signal traces which are not security sensitive.

Preferably the first side of the first circuit board carries a connector component and the first side of the second circuit board carries a co-operating connector component so that the connector component and co-operating connector component are connected together to provide electrical communication between circuit components and traces on the first side of the first circuit board and circuit components and traces on the first side of the second circuit board.

Preferably the filler material comprises an epoxy resin.

According to one preferred embodiment of the invention, the first printed circuit board is formed from a plurality of circuit board layers, a first side of one of the layers forming the said first side of the first printed circuit board, and a second side of another of the layers forming the second side of the first printed circuit board, a ground plane being formed on a side of one of the plurality of layers other than the said first side and said second side, and a security detection trace being formed on another side of one of the plurality of layers other than the said first side, and said second side or side having the ground plane.

Preferably at least one via extends through the layer

having the security detection trace for electrical interconnection with signal traces on the first side of the first printed circuit board, the vias being shaded vias so that the said vias do not extend to the second side of the first circuit board.

Preferably additional vias extend from the first side of the first printed circuit board to the second side of the first printed circuit board for coupling non-secure circuit components on the second side of the first circuit board to security sensitive components on the first side of the first circuit board.

Preferably the second printed circuit board is formed of a plurality of layers in the same manner as the first printed circuit board.

The structure of forming the boards from a plurality of layers provide additional advantages. An attacker may attempt to drill into the circuit board assembly to gain access to certain pins of interest on the components within the filler material, after obtaining information on the exact locations of the component themselves (which could be obtained by destruction of an identical device). The pins of the components could be attacked directly, particulary as it is much simpler to attach a probe to a component pin than to a narrow track on the printed circuit board given the extra size of the volume of solder that attaches the pin to the printed circuit board. However, because of the formation of the security trace on one of the layers between the first and second sides and a ground plane of on another of the layers between the first and second sides, any attempt to drill through the board to gain access to components within the resin would sever the security trace enabling the activation of security mitigation protocols, such as deleting bank keys or the like from secure componentary. The attacker would also be prevented from

strapping out the security trace (i.e. attaching an external wire to provide continuity whilst the attacker drills through the circuit board assembly) as the vias connecting the trace to the security components are shaded and do not appear external to the epoxied interior of the circuit board assembly. Preferably, the security trace also activates a violation if the trace is connected to ground via the ground plane. This would provide an additional security measure of ensuring that even if the attacker were to somehow externally strap the security trace, and then attempt to drill through the circuit board assembly, a violation would still be caused by the conductive drill bit shorting out the two internal layers carrying the trace and ground plane as the drill passes through them to the components on the first side of the first board.

The invention may also be said to reside in a method of forming a circuit board assembly including the steps of;

locating a first printed circuit board having a first side and a second side, within a mould, the first side having circuit components mounted on the first side and signal traces on the first side;

applying a filler material;

applying a second board to the first side of the first printed circuit board to spread the filler material so that the circuit components and traces are embedded within the filler material and the filler material surrounds the traces, filler material adhering to the first and second boards to thereby form a monolithic circuit board assembly.

Preferably the mould comprises a casing of an article in which the circuit board assembly is to be used.

Preferably the casing is a casing of a funds transaction terminal.

Preferably the filler material is applied to the first side of the first printed circuit board.

The invention may also be said to reside in a printed circuit board including;

a first layer having a first side and a second side;

a second layer having a first side and a second side;

the first and second layers being coupled together with the second side of the first layer overlying and being adjacent to the first side of the second board so as to form a unitary structure;

a security trace formed on either the second side of the first board or the first side of the second layer; and

the security trace being connected to the first side of the first layer by at least one via which passes through the first layer but which does not extend to the second side of the second layer.

Thus, according to this aspect of the invention, two such circuit boards can be coupled together with security sensitive components arranged on the first side and embedded in filler material so as to be internal within the circuit board assembly formed from the two boards so that any attempt to drill into the assembly to gain access to the components will sever the security trace to enable a security signal to be generated.

Preferably a ground plane is formed on the other of the second side of the first layer or first side of the second layer. In accordance with this preferred aspect, if an attempt is made to strap out the security trace and then drill through the board hole the contact between the drill bit, trace and ground plane will cause a circuit to be

completed between the security trace and the ground plane thereby grounding the security trace to by enable generation of a security signal.

Preferably the security trace is connected to an invertor means for providing a predetermined signal indicative of the integrity of the circuit board and upon severing of the trace or grounding of the trace the predetermined signal is altered to thereby provide an indication of an attack on the circuit board.

Preferably a circuit board assembly is formed from two said circuit boards by coupling the two said circuit boards together so that the first sides of the first layers of the boards are adjacent and overlie one another and a filler material is interposed between the two boards, and circuit components being formed on the first side of at least one of the boards and embedded in the filler material.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the invention will be described, by way of example, with reference to the accompanying drawings in which;

Figure 1 is a schematic view of a circuit board assembly in exploded view according to one embodiment of the invention;

Figure 2 is a view of the assembled circuit board assembly of Figure 1;

Figure 3 is a cross-sectional view through a circuit board arrangement according to the preferred embodiment of the invention;

Figures 4, 5, 6 and Figure 7 are views showing first and second sides of the layers of the circuit board arrangement of Figure 3;

Figure 8 is a circuit diagram relating to the embodiment of Figures 3 to 8; and

Figure 9 is a view showing the method of forming

the circuit board assembly according to the preferred embodiment of the invention.

With reference to Figure 1 a first printed circuit board 10 has a first side 12 and a second side 14. A second printed circuit board 16 has a first side 18 and a second side 20. The second printed circuit board 16 may be connected to a display board 22 having a display panel 24. The board 22 may be physically connected to the board 16 or separate from the board 16 and connected by an electrical connection cable (not shown).

The first side 12 of the first printed circuit board 10 includes security sensitive electronic circuits 30 together with security sensitive traces (not shown) formed on the board 12 which interconnect the circuits 30.

The first side 18 of the second printed circuit board 20 may also be provided with security sensitive electronic circuits 30′ .The first side 18 of the second board 20 may also include traces for coupling the circuits 30 on the first side 18 of the board 20 together.

The first side 12 and the first side 18 also include connectors 38 and 38′ which couple together when the two boards 10 and 16 are bought together as shown in Figure 2 to form electrical interconnections between the circuits 30 on the side 12 and the circuits 30′ on the side 18.

A loose length of wire 40 (shown schematically in Figure 1) is located between the boards 10 and 16 for carrying a security detectable signal in the event of an attempt to interfere with the circuit board assembly shown in Figures 1 and 2. The wire 40 is quite long in comparison to the length of the board.

Before the board 10 is connected to the board 16 by the

connectors 38, an amount of epoxy resin sufficient to entirely fill the space between the boards 12 and 14 when they are connected together is applied to the board 10 (for example) from a dispenser shown schematically by reference numeral 50. When the board 16 is arranged over and adjacent to the board 10 so that the first side 12 faces the first side 18, and the connectors 38 and 38′ connect together, the epoxy resin is spread out to the edges of the boards 10 and 16 so as to embed the security wire 40 and also the circuits 30 within the epoxy resin and surround the signal traces on the sides 12 and 18. The epoxy resin adheres to the sides 12 and 18 to securely couple the boards 10 and 16 together. Once the epoxy resin has set, the two boards 10 and 16, together with their circuits 30 and 30′, and connectors 38 and 38′, become one integral mass with the security sensitive circuits 30 and their traces contained on the sides 12 and 18 interior of the circuit board assembly and therefore inaccessible to any attacker.

As shown in Figure 2, when the epoxy resin has set it forms a solid mass 52 which is adhered to the first sides 12 and 18 of the boards 10 and 16 respectively and which is embedded the circuits 30 and security wire 40 as previously described. Thus, in order to break into the circuit assembly it is necessary to destroy the boards 10 and 16 which in turn will destroy the security sensitive components on the boards thereby preventing access to the sensitive information contained within the circuits 30. Furthermore, any attempt to break the boards 10 and 16 to gain access to the circuits 30 or their traces on the sides 18 and 12 will most likely rupture the security sensitive wire 40. Rupture of the wire 40 can create a security signal, (as will be described in more detail hereinafter) to provide an indication of tampering with the circuit board assembly so that sensitive information in the circuits 30 can be deleted.

Figure 3 shows an embodiment of one of the circuit boards 10 or 16 (for example and for illustrative purposes the board 10 shown in Figure 1). Rather than form the board 10 as a single layered printed circuit board, in the embodiment of Figure 3 the board 10 is formed as a multi-layer board arrangement. Preferably the board 10 of Figure 3 comprises a first layer 64 and a second layer 66 each of which may comprises printed circuit boards. The first layer 66 has a first side 68 and a second side 70. The second side 70 forms the second side 14 of the board 10 shown in Figure 1. The second layer 66 has a first side 72 and a second side 74. The first side 72 forms the first side 12 of the circuit board shown in Figure 1. The circuits 30 are formed on the side 72 of the circuit board arrangement 10 shown in Figure 3. Thus, according to this embodiment the circuit board 10 has a first side 72 and a second side 70 which would form the first side 12 and second side 14 respectively of the circuit board 10 shown in Figure 1. As pervasively noted, the circuits 30 are located on the side 72 as would be the connector 38 (not shown in Figure 3). The arrangement shown in Figure 3 also has two intermediate sides formed by the side 74 of the layer 66 and the side 68 of the layer 64 which face one another and are adhered together to form the board 10 shown in Figure 3.

Figures 4 and 5 show the sides 72 and 74 respectively of the layer 66, and figures 6 and 7 show the sides 68 and 70 respectively of the layer 64. The side 72 of the layer 66 includes signal traces 80 and the circuits 30 (not shown in Figure 4 for ease of illustration). Vias 82 (which are holes through the layer 72 having a wall coated with conducting material which is generally the same as that from which the traces are formed) are formed in the layer 66 for conductively coupling the side 72 of the layer 66 to the side 74. The side 74 of the layer 66, as is shown in

Figure 5, is provided with a security signal trace 90 which forms a square shaped zig-zag type pattern on the side 74. As clearly shown in Figure 4 the security trace is formed over the entire surface of the side 74 and the trace lines 90 are quite close together. The vias marked 82' in Figure 5 and also in Figure 4 are electrically connected to the security trace 90 so that the security trace 90 can be connected to a circuit component formed on the side 72 shown in Figure 4 for security monitoring of the circuit board assembly. The other vias marked 82 in Figures 4 and 5 are provided for connection to other circuit components as will be described hereinafter.

Figure 6 shows the side 68 of the layer 64 and the side 68 is formed as a ground plane. Vias 83 pass through the layer 64 and are electrically insulated from the ground plane on the side 68 by the ground plane 68 not extending all of the way to the vias 83 as shown by the region 85 surrounding the vias 83. The ground plane shown cross hatched in Figure 6 occupies the entire surface of the side 68 apart from the regions 85 surrounding the vias 83 and the vias 83 themselves.

The side 70 of the layer 64 is provided with traces 87 which may interconnect non-secure circuit components (not shown in Figure 7) which may be formed on the second side 14 of the assembly shown in Figure 1 so that those components can be connected to the circuit components formed on the side 72 shown in Figure 4 by the vias 83 which register and contact the vias 82 (other than those labelled 82') shown in Figures 4 and 5. Thus, non-secure circuit components provided on the outside of the circuit board assembly shown in Figure 1 (that is on the side 70 shown in Figure 7) can be electrically connected to the security sensitive circuits 30 provided on the side 72 shown in Figure 4.

As described with reference to Figure 3, the side 68 of the layer 64 and the side 74 of the layer 66 are adhered together to form a unitary structure with the vias 82 shown in Figure 5 coupling with the vias 83 shown in Figures 6 and 7.

The vias 82' shown in Figures 4 and 5 are shaded vias, that is vias which do not extend all of the way through the circuit board 10 shown in Figure 3 so that they cannot be contacted from outside the circuit board assembly after the assembly has been constructed.

The circuit board 16 shown in Figure 1 can be formed in the same manner as that described with reference to Figure 3 and the assembly completed by bringing the two circuit boards together with the epoxy material between them so that the circuit components 30 provided on the side 72 of the first board 10 formed from the multi-layer configuration shown in Figure 3, and the circuit components 30' if provided on the first side 18 of a corresponding multi-layer circuit board 16 are embedded in the resin.

In this embodiment the security traces 90 are located in the interior of the board 10 being formed on the side 74 of the layer 66 and therefore are not assessable from outside of the circuit board assembly once constructed. It will be noted, as discussed above, that the security trace 90 is connected only to the side 72 and the components on the side 72 and not to the exterior of the circuit board assembly. Thus, if an attacker should attempt to break into the circuit board assembly by drilling through the assembly, the traces 90 will be broken and severing the security trace 90 enables the activation of a security mitigation code which can delete sensitive information from the circuits 30 such as bank keys or the like. The attacker is prevented from "strapping out" the security trace 90 by attaching an external wire to provide

continuity)whilst the attacker drills through the circuit board assembly) because the vias 82' connecting the trace 90 to the security components on the side 72 are shaded and do not appear external to the circuit board assembly. Furthermore, an attempt to drill through the board 10 will cause a circuit to be formed between the trace 90 and the ground plane formed on side 68 thereby grounding the trace 90. In the event of grounding the trace 90, a security mitigation code can also be activated in order to delete sensitive information in the circuits 30. Thus, even if an attacker is able to strap the security trace 90, the grounding of the security trace 90 by forming a circuit between a drill bit and the trace 90 and ground plane on the side 68 will still cause the violation to be notified so that the mitigation code can be implemented.

Figure 8 shows the circuit diagram illustrating how the trace 90 can generate a security signal. With reference to Figure 8, trace 90 is shown connected to a power supply 99 which supplies a voltage VCC to resistor 101 which is connected to the trace 90 by via 82'. The other end of the trace 90 is connected to the other via 82'. The via 82' connects to resistor 102 which is grounded, and also by trace 104 to a first invertor 105. The output of the first invertor 105 is connected to a second invertor 106 and also to trace 107. The output of the second inventor 106 is connected to trace 108.

When the trace 90 is not broken the resistor 101 overrides the resistor 102 and the input to the inverter 105 is high. The inverter 105 acts as an amplifier to this input, providing a low impedance output to trace 107 and invertor 106. If the input to the inverter 106 is low the output from the inverter 106 is high on trace 108. The traces 107, and inverter 106 and trace 108, are alternatives and the trace 107 can be used for active high inputs or the inverter 106 and trace 108 used for active low inputs.

If an attempt is made to drill through the circuit board one of two things occurs. Firstly, the trace 90 is severed by the cutting, removing the resistor 101 from the circuit. The input to the inverter 105 is then controlled only by the resistor 102 which is at ground potential. The output from the invertor 105 therefore goes high causing the trace 107 to go high and the trace 108 to go low thereby providing signals indicative of an attack on the circuit board assembly. Alternatively, if the trace 90 is not effectively broken, perhaps by being externally strapped, the trace 90 is nevertheless momentarily connected to ground as the drill cuts through the ground plane on side 68 shown in Figure 6 thereby temporarily grounding the trace 90. This connection overrides the resistor network and applies a ground potential to the input of the invertor 105 thereby causing the trace 107 to go high and the trace 108 to go low. The change in signal on the trace 107 or the trace 108 is received by a processor (not shown) which immediately initiates a security protocol to delete sensitive information from the circuits 30 in accordance with known standards.

The power supply 99, resistor 101, resistor 102 and inverters 105 and 106 together with the respective traces 104, 107 and 108 are formed on the side 72 shown in Figure 4 (that is the side 12 shown in Figure 1), as made clear above, connected to the trace 90 by the vias 82'.

Figure 9 shows the preferred embodiment of forming the circuit board assembly shown in Figure 1 either from single circuit boards as described with reference to Figure 1 or from multi-layer circuit boards as described with reference to Figures 3 to 7. In this embodiment the circuit board, such as the circuit board 10 is arranged within casing 92 of a funds transfer device in which the circuit board 10 is to be provided. Epoxy is then applied to the side 12 of

the circuit board 10 with the surrounds of the casing 12 acting as a mould to assist in retaining epoxy on the side 12. The second circuit board 16 is then located on the board 10 to spread out the epoxy and embed the circuit components 30 within the epoxy. Thus, in this embodiment the casing of the product in which the circuit board assembly is to be used, forms a mould for facilitating retention of the epoxy between the circuit boards 10 and 16.

The casing 92 forms one casing part of a funds transfer device which preferably a hand held device communicating with a central bank facility via an over the air network will generally include a pin pad for the input of information, a slot for enabling a card to be swiped through the device and read by the device and a transmitter for transmitting the information. Further details of the device are given in our co-pending application filed concurrently herewith and entitled Funds Transaction Terminal, the contents of which is incorporated into this specification by this reference.

Since modifications within the spirit and scope of the invention may readily be effected by persons skilled within the art, it is to be understood that this invention is not limited to the particular embodiment described by way of example hereinabove.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

1. A circuit board assembly, including;

a first printed circuit board having a first side and a second side;

a second board having a first side and a second side;

circuit components mounted on the first side of the first printed circuit board and signal traces formed on the first side of the first board for interconnecting the circuit components;

the first and second boards being arranged adjacent one another and with the first sides facing one another; and

a filler material disposed between the first sides of the first and second boards, which adheres to the first sides of the first and second circuit boards and embeds the circuit components within the filler material and surrounds the signal traces to form a monolithic circuit board assembly.

2. The assembly of claim 1 wherein the second board is a second printed circuit board.

3. The assembly of claim 1 wherein the circuit components are arranged on both the first side of first circuit board and the first side of the second circuit board and the components on one of the circuit boards are staggered with respect to components on the other circuit board so as to sit within valleys formed by components on the other circuit board to ensure that the space between the first and second circuit boards is as small as possible.

4. The assembly of claim 1 wherein a security wire is provided between the first and second boards and embedded in the filler material for providing a violation

signal indicative of an attempt to break through the first or second circuit boards.

5. The assembly of claim 1 wherein second sides of the first and second circuit boards include circuit components and signal traces which are not security sensitive.

6. The assembly of claim 1 wherein the first side of the first circuit board carries a connector component and the first side of the second circuit board carries a co-operating connector component so that the connector component and co-operating connector component are connected together to provide electrical communication between circuit components and traces on the first side of the first circuit board and circuit components and traces on the first side of the second circuit board.

7. The assembly of claim 1 wherein the filler material comprises an epoxy resin.

8. The assembly of claim 1 wherein the first printed circuit board is formed from a plurality of circuit board layers, a first side of one of the layers forming the said first side of the first printed circuit board, and a second side of another of the layers forming the second side of the first printed circuit board, a ground plane being formed on a side of one of the plurality of layers other than the said first side and said second side, and a security detection trace being formed on another side of one of the plurality of layers other than the said first side, and said second side or side having the ground plane.

9. The assembly of claim 8 wherein at least one via extends through the layer having the security detection trace for electrical interconnection with signal traces on the first side of the first printed circuit board, the vias

being shaded vias so that the said vias do not extend to the second side of the first circuit board.

10. The assembly of claim 9 wherein additional vias extend from the first side of the first printed circuit board to the second side of the first printed circuit board for coupling non-secure circuit components on the second side of the first circuit board to security sensitive components on the first side of the first circuit board.

11. The assembly of claim 9 wherein the second printed circuit board is formed of a plurality of layers in the same manner as the first printed circuit board.

12. A method of forming a circuit board assembly including the steps of;

locating a first printed circuit board having a first side and a second side, within a mould, the first side having circuit components mounted on the first side and signal traces on the first side;

applying a filler material;

applying a second board to the first side of the first printed circuit board to spread the filler material so that the circuit components and traces are embedded within the filler material and the filler material surrounds the traces, filler material adhering to the first and second boards to thereby form a monolithic circuit board assembly.

13. The method of claim 12 wherein the mould comprises a casing of an article in which the circuit board assembly is to be used.

14. The method of claim 12 wherein the casing is a casing of a funds transaction terminal.

15. The method of claim 12 wherein the filler

material is applied to the first side of the first printed circuit board.

16. A printed circuit board including;

a first layer having a first side and a second side;

a second layer having a first side and a second side;

the first and second layers being coupled together with the second side of the first layer overlying and being adjacent to the first side of the second board so as to form a unitary structure;

a security trace formed on either the second side of the first board or the first side of the second layer; and

the security trace being connected to the first side of the first layer by at least one via which passes through the first layer but which does not extend to the second side of the second layer.

17. The circuit board of claim 16 wherein a ground plane is formed on the other of the second side of the first layer or first side of the second layer.

18. The circuit board of claim 16 wherein the security trace is connected to an invertor means for providing a predetermined signal indicative of the integrity of the circuit board and upon severing of the trace or grounding of the trace the predetermined signal is altered to thereby provide an indication of an attack on the circuit board.

19. The circuit board of claim 16 wherein a circuit board assembly is formed from two said circuit boards by coupling the two said circuit boards together so that the first sides of the first layers of the boards are adjacent and overlie one another and a filler material is interposed

between the two boards, and circuit components being formed on the first side of at least one of the boards and embedded in the filler material.

Dated this 15th day of March 2001

MCOM SOLUTIONS INC
By their Patent Attorneys

GRIFFITH HACK
Fellows Institute of Patent and
Trade Mark Attorneys of Australia

FIG. 1.

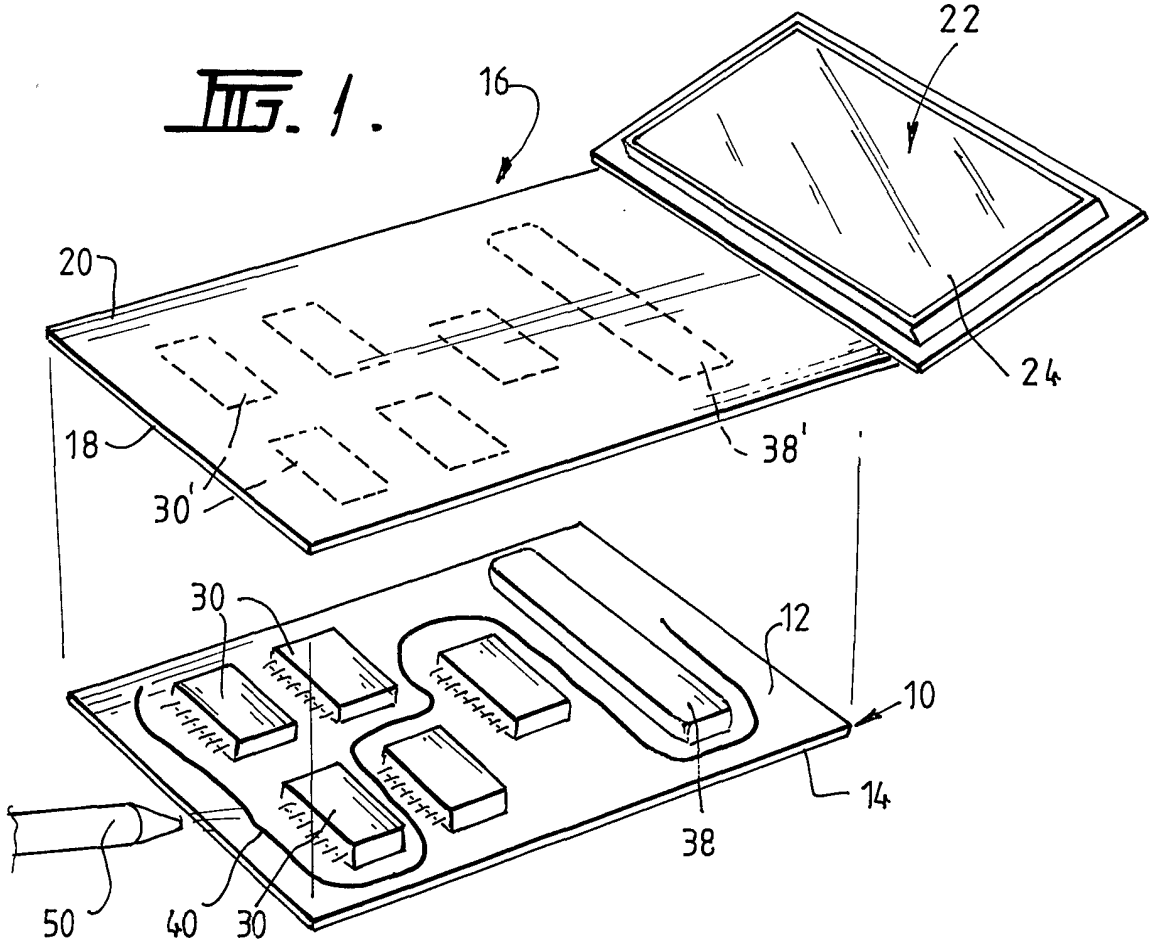
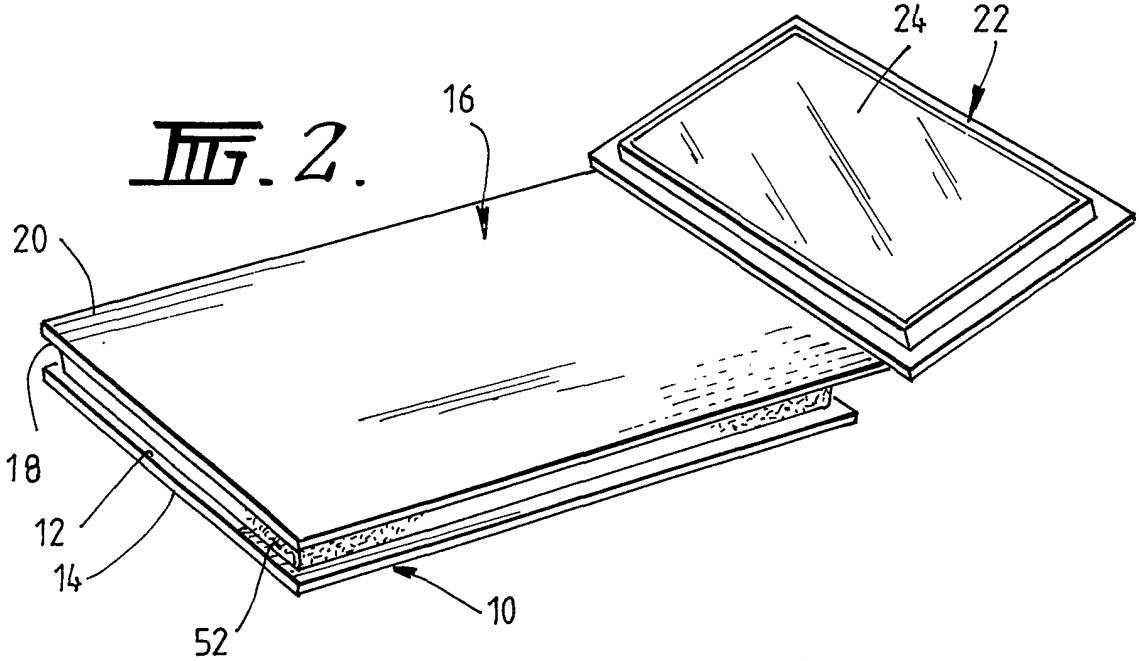


FIG. 2.



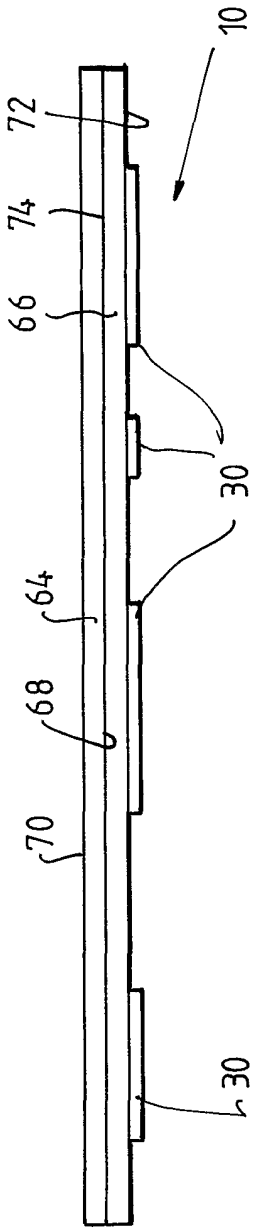
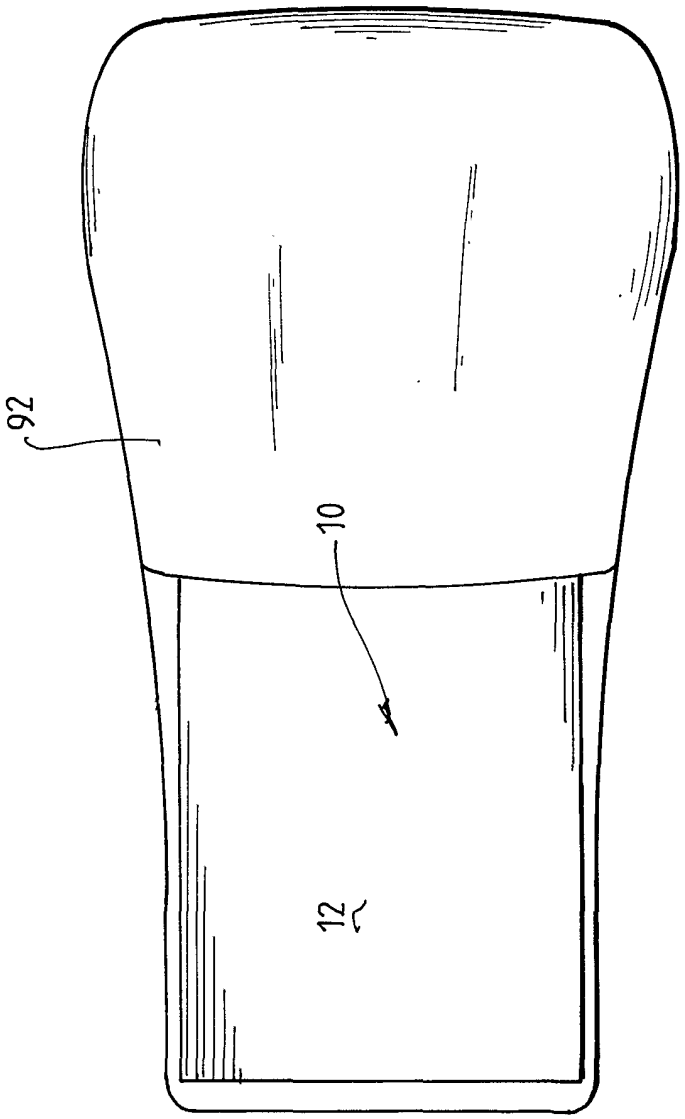


Fig. 3.

Fig. 9.



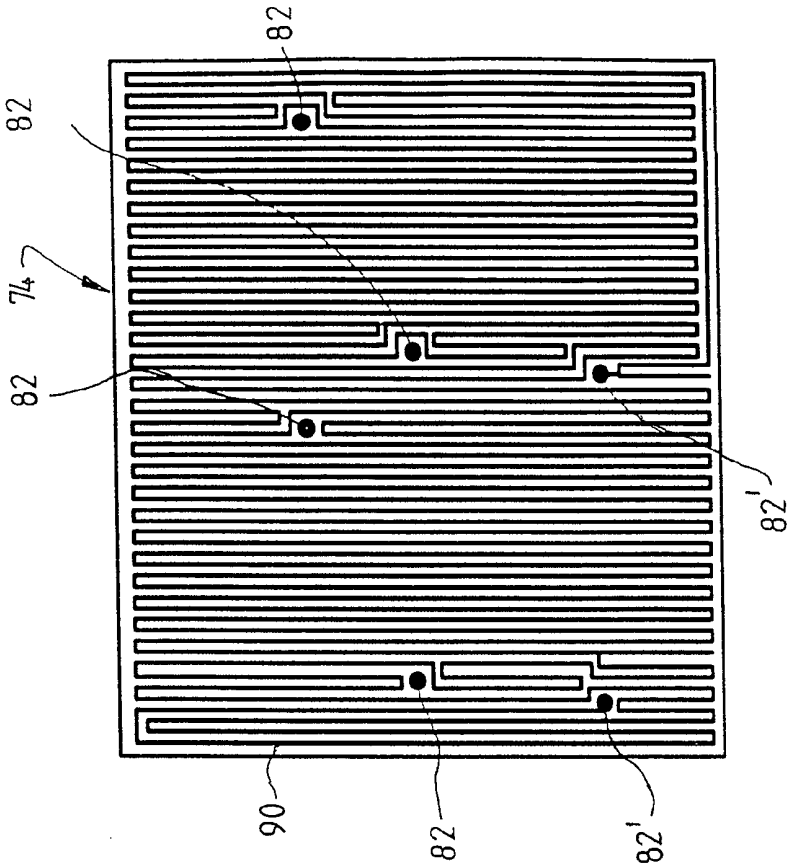


Fig. 5.

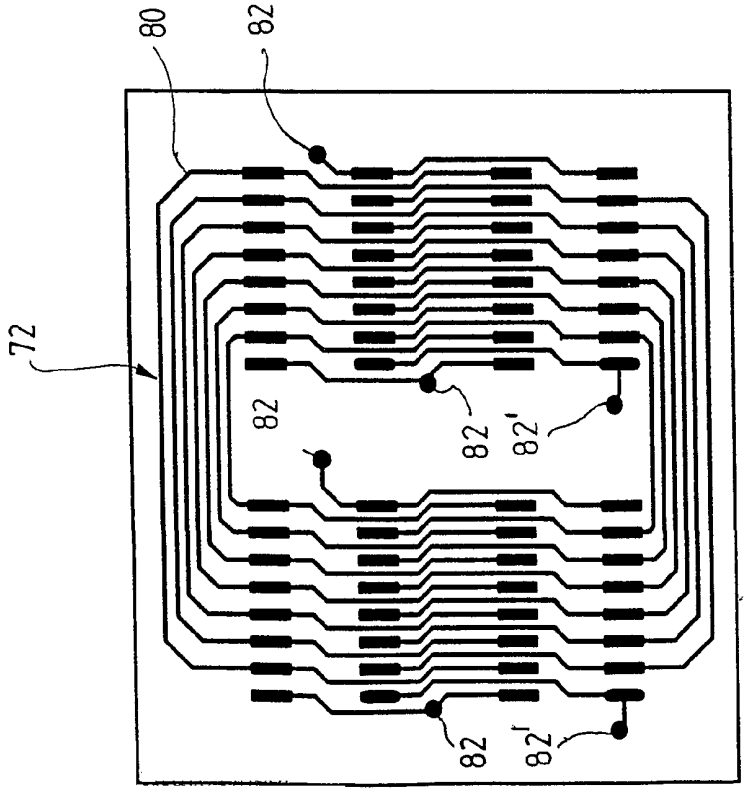


Fig. 4.

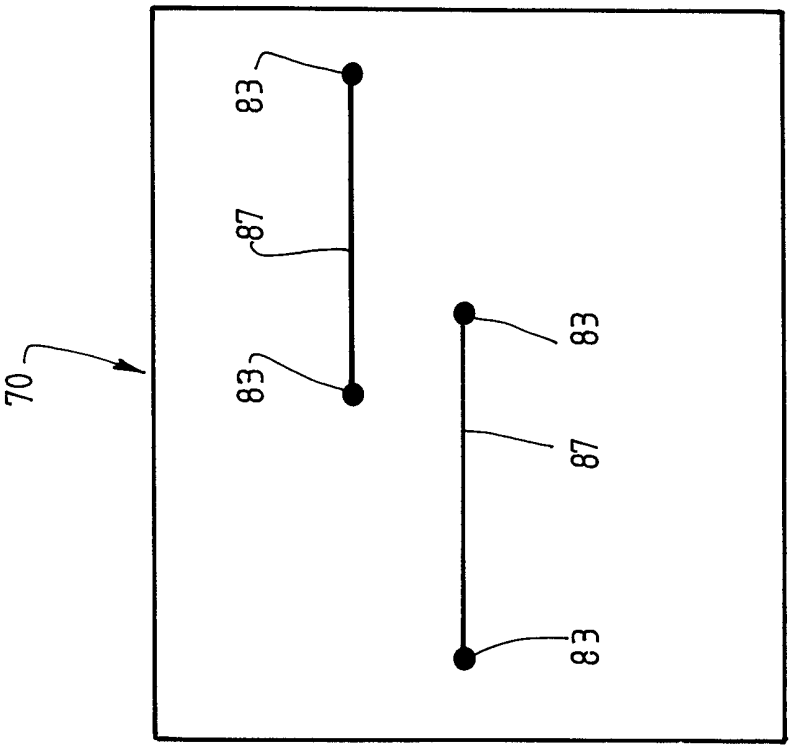


FIG. 7.

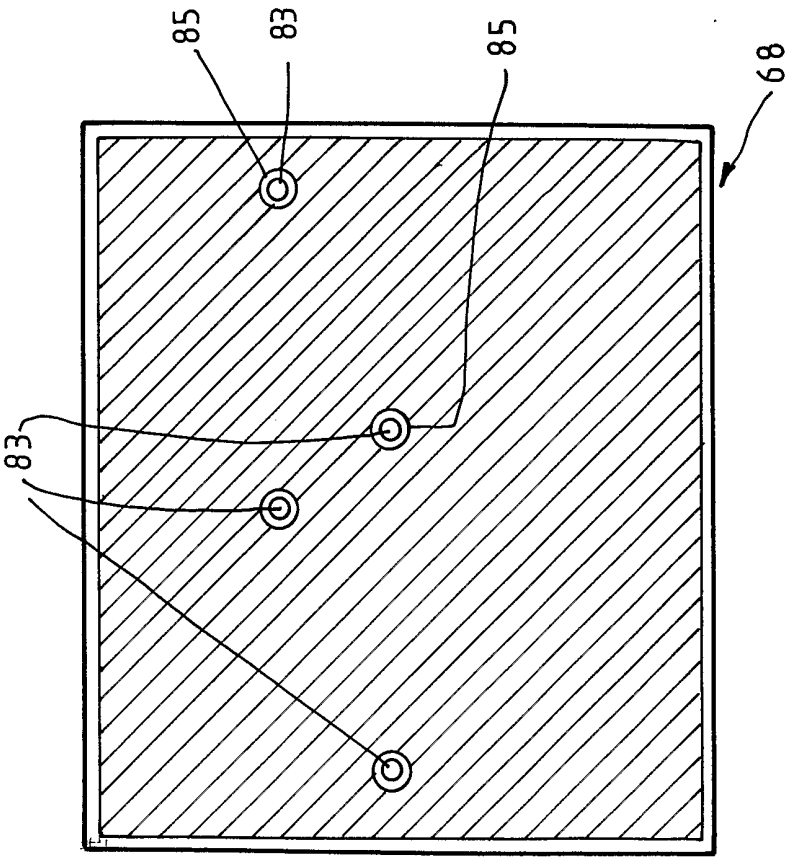


FIG. 6.

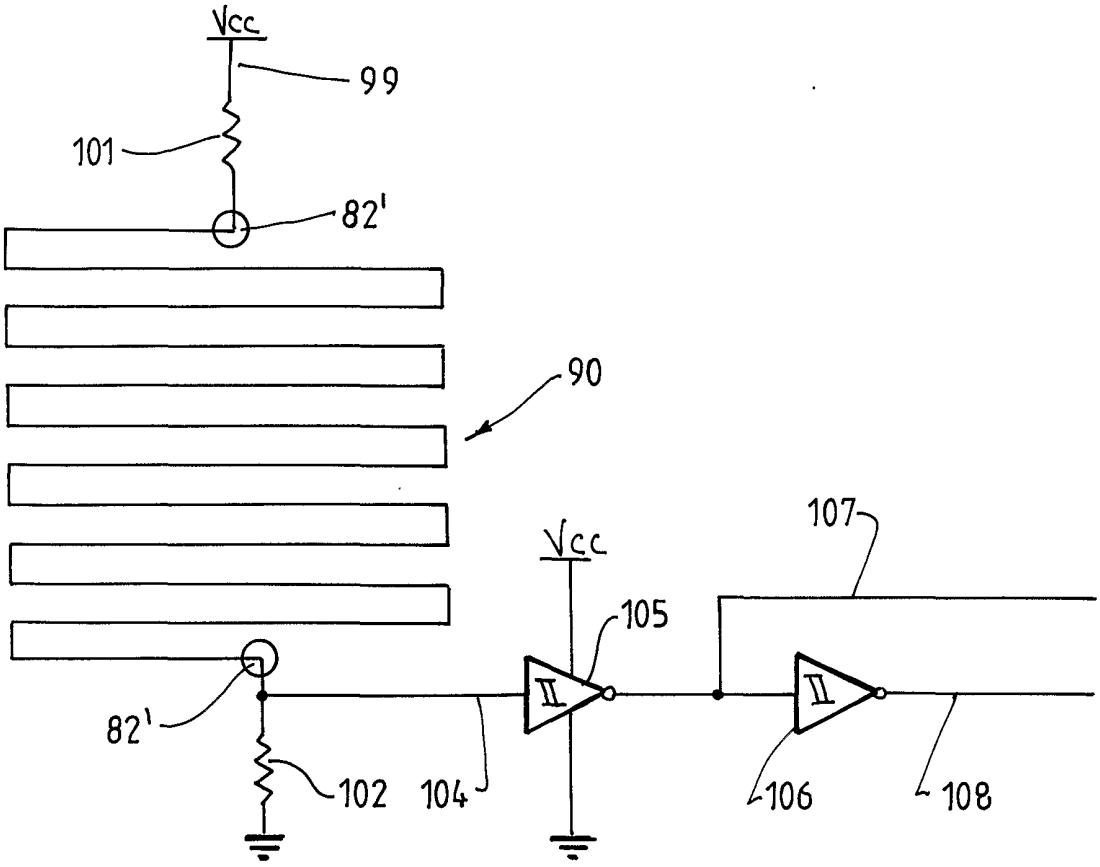


FIG. 8.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU01/00292

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl. [7]: H05K 3/36

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: G06K, H01L, H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPAT: circuit+, pcb+, monolithic+, epox+, resin+, filler+, encapsulat+

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5847650 A (Zhou et al.) 8 December 1998	1 - 19
A	US 5776796 A (Distefano et al.) 7 July 1998	1 - 19
A	US 5586389 A (Hirao et al.) 24 December 1996	1 - 19

[X] Further documents are listed in the continuation of Box C [X] See patent family annex

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
4 May 2001	10 May 2001
Name and mailing address of the ISA/AU	Authorized officer
AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. (02) 6285 3929	**R.W.J. FINZI** Telephone No : (02) 6283 2213

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU01/00292

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	GB 2279907 A (GEC Avery Limited) 18 January 1995	1 - 19
A	US 5371044 A (Yoshida et al.) 6 December 1994	1 - 19

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/AU01/00292

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
US	5847650	AU	11429/97	WO	9720292		
US	5776796	US	5663106	AU	20630/97	US	5834339
		WO	9733312	US	6107123		
US	5586389	EP	516149	JP	4354357	US	5408383
		US	5586388	US	5646827	US	5657203
		JP	4354362	JP	4354361	JP	4354354
		JP	4354360	JP	4354356	JP	4354359
GB	2279907	AU	70063/94	EP	706693	WO	9501612
US	5371044	JP	5190733				

END OF ANNEX