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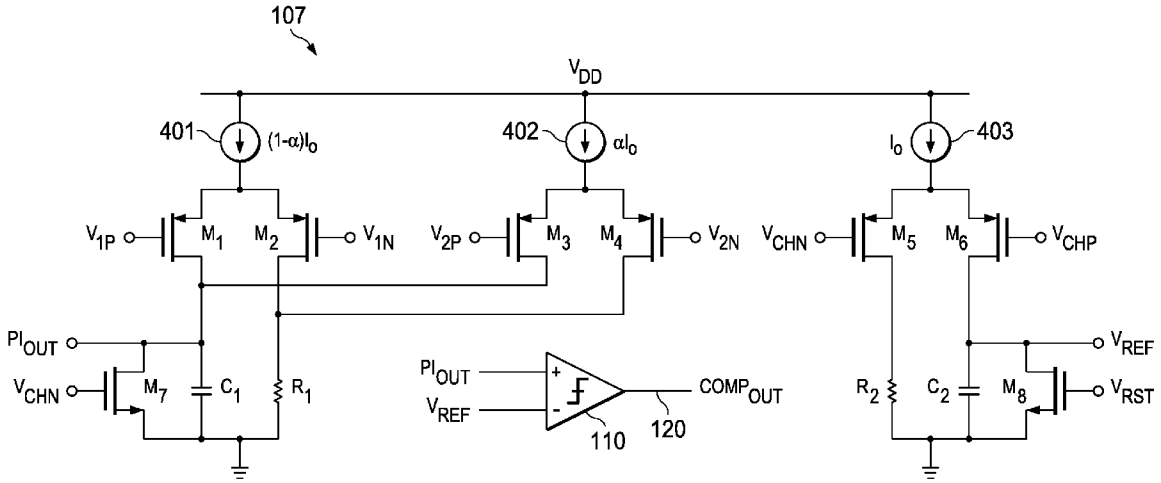

FIG. 4

(57) Abstract: In described examples of a high linearity phase interpolator (PI) (107), control logic may provide a phase value parameter (a) indicative of a desired phase difference between an output signal and an input clock signal edge. A first capacitor (CI) may be charged for a first period of time with a first current (401) that is proportional to the phase value parameter to produce a first voltage on the capacitor that is proportional to the phase value parameter. The first capacitor (CI) may be further charged for a second period of time with a second current (402) that has a constant value to form a voltage ramp offset by the first voltage. A reference voltage (Vref) may be compared (110) to the voltage ramp (Plout) during the second period of time. The output signal (120) may be asserted at a time when the voltage ramp equals the reference voltage.

[Continued on next page]

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HIGH LINEARITY PHASE INTERPOLATOR

[0001] This relates generally to phase interpolators, and more particularly to phase interpolators that have a high linearity over a full range of operation.

BACKGROUND

[0002] A phase interpolator (PI) may be used to generate a clock signal that is phase shifted from a reference clock signal by interpolating a specified amount of time from an edge of the reference clock signal.

[0003] For example, a phase interpolator may be used in the clock and data recovery (CDR) loop of a serializer/deserializer (SerDes) communication interface. The PI may be interposed between a phase locked loop (PLL) and the data samplers in order to shift a recovered clock phase to an appropriate position in the data sampling window. It may receive two clocks of the same frequency that are in-phase and quadrature phase (I-Q), respectively, and generate a clock output whose phase is the weighted summation of the two input phases. An ideal PI may be able to generate a number of equally spaced phase steps for a full cycle from 0 to 360 degrees.

[0004] Typically, SerDes applications do not require a highly linear PI to operate correctly.

SUMMARY

[0005] In described examples of a high linearity phase interpolator, control logic may provide a phase value parameter indicative of a desired phase difference between an output signal and an input clock signal edge. A first capacitor may be charged for a first period of time with a first current that is proportional to the phase value parameter to produce a first voltage on the capacitor that is proportional to the phase value parameter. The first capacitor may be further charged for a second period of time with a second current that has a constant value to form a voltage ramp offset by the first voltage. A reference voltage may be compared to the voltage ramp during the second period of time. The output signal may be asserted at a time when the voltage ramp equals the reference voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG. 1A is a block diagram and FIG. 1B is a timing diagram illustrating operation of an example fractional frequency divider.

[0007] FIG. 2 is a block diagram of an example clock generator system that includes multiple fractional frequency dividers.

[0008] FIG. 3 is a schematic of a conventional phase interpolator.

[0009] FIGS. 4-7 are schematics and timing diagrams that illustrate embodiments of improved phase interpolators.

[0010] FIG. 8 is a plot illustrating a further improvement in nonlinearity.

[0011] FIG. 9 is a schematic diagram illustrating another embodiment of a phase interpolator.

[0012] FIG. 10 is a timing diagram illustrating operation of the PI of FIG. 9.

[0013] FIGS. 11 is a plot illustrating operation of the PI of FIG. 9.

[0014] FIG. 12 is a flow chart illustrating operation of a high linearity phase interpolator.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0015] In the drawings, like elements are denoted by like reference numerals for consistency.

[0016] Example embodiments may provide a high resolution, high linearity phase interpolator for applications that require better linearity than a conventional SerDes application. For example, such application may include precision clock generators.

[0017] In example embodiments, an improved phase interpolator eliminates the need for quadrature input signals and common-mode feedback. Required input and control signals may be easily generated by digital logic.

[0018] In one embodiment, a phase interpolator may be provided that has a resolution of 11 bits across a period of 200ps (picosecond) to produce a time resolution of approximately 97.6fs (femtosecond). For example, such resolution may be 40x better than the integer nonlinearity (INL) of conventional phase interpolators used in SerDes applications.

[0019] FIG. 1A is a block diagram of an example fractional frequency divider (FFD) 100 that includes a high linearity phase interpolator 107. FFD 100 is operable to generate an output clock signal 120 that has a frequency equal to a specified fraction of an input clock signal 102. Input clock signal 102 may be selected to have a value that ranges between 10MHz up to 10GHz in this example embodiment. In other embodiments, a different range of input clock frequencies may be supported. Output clock signal 120 may be produced with a frequency that may be selected from a range of approximately 100 Hz to 1 GHz in this example.

[0020] Digital control circuitry 104 may be configured either in a hardwired manner or in a programmable manner to select a particular divider ratio between the output clock signal 120 and

the input clock signal 102. For example, control circuitry 104 may include registers that are loaded by software or firmware that is executed on a processor that is coupled to FFD 100.

[0021] FFD 100 operates by counting a specified number of clock periods of input clock 102 that is the desired approximate period of output clock signal 120, and then interpolating an amount of time between edges of clock signal 102 to produce the exact period length between edges of output clock signal 120. The operation of FFD 100 is described briefly herein; a detailed description of the operation of an FFD such as FFD 100 is provided in Patent Application No. US 15/281,617, "Fractional Frequency Clock Divider with Direct Division", Hoshyar etal, filed 2016-09-30, which is incorporated by reference herein.

[0022] FIG. 1B is a timing diagram illustrating operation of FFD 100 for an example divide ratio of 13.75. Frequency divider 103 is configured to count a number N of edges of input clock signal 102 in response to a control parameter N 105 provided by digital control logic 104 and to produce "Nth clock" signals V1P, V2P. In this embodiment, frequency divider counts both the rising and falling edges of input clock signal 102. Phase interpolator 107 is configured to interpolate between two edges of input clock 102 as specified by phase parameter α. For example, if a divider ratio of 13.75 is specified, then control logic 104 may instruct counter 103 to count 13 edges (N = 13) of input clock 102 and instruct PI 107 to then interpolate 0.75 (α = 0.75) of a period of input clock 102 before asserting intermediate clock signal CLKp 119. On the next output period, control logic may then instruct counter 103 to count thirteen input periods and instruct PI 107 to then interpolate between half of a period of input clock 102. Intermediate clock signal 119 may then be divided by two in frequency by 111 to form output clock signal 120 with a 50% duty cycle and with a period of 13.75 periods of input clock 102. This process is then repeated for each period of output clock signal 120. Usually, each period will require a different amount of phase interpolation because the fractional frequency ratio causes the edge relations between the output clock signal and the input clock signal to continually change.

[0023] In this example, parameter α is an 11-bit digital value (0-2047). In another example, α may have a higher or a lower resolution than 11-bits. Phase interpolator 107 generates a voltage PIout 109 that correlates to a requested phase shift amount indicated by parameter α. PIout 109 may be compared to a reference voltage Vref 108 by comparator 110. A transition on output clock signal 120 is produced by comparator 110 when PIout is equal to Vref, as described in more detail hereinbelow.

[0024] FIG. 2 is a block diagram of an example clock generator system 200 that includes one or more fractional frequency dividers 100(1) through 100(n). For example, system 200 may be fabricated on a single integrated circuit (IC) using known or later developed semiconductor processing techniques. Also, for example, a phase locked loop (PLL) circuit 210 may be used to generate a fixed frequency reference clock signal 202 under control of crystal 214 controlled oscillator 212. In some examples, crystal 214 may be located external to IC 200. In another embodiment, other types of known or later developed clock generation circuits may be used, such as an oscillator with MEMs resonator, multivibrator, ring oscillator, delay line oscillator, etc. In another example, reference clock 202 may be provided from an external source instead of from an on-chip source.

[0025] In this manner, a single IC may provide multiple clock signals of different frequencies that are all synthesized from a single reference clock signal.

[0026] As described in more detail hereinbelow, phase interpolator 107, referring again to FIG. 1, produces a phase shift in response to parameter α across a range of values in a highly linear manner. In this description, "nonlinearity" may be described in a similar manner as commonly used for analog to digital convertors (ADC). To express the non-linearity of an ADC in a standard way, manufacturers may draw a line through the ADC transfer function, called the best fit line. The maximum deviation from this line is called "integral nonlinearity (INL), which can be expressed in percentage of the full scale or in LSBs (Least Significant Bit). INL is measured from the center of each step to that point on the line, where the center of the step would be if the ADC was ideal. The term "differential" refers to the values an ADC takes between two consecutive levels. In response to a changing input signal, the ADC samples the signal and the output of the ADC is a stream of binary numbers. An ideal ADC will step up or down one Least Significant Bit (LSB), without skipping any level and without holding the same decimal number past two or three LSBs. Differential nonlinearity (DNL) is defined as the maximum deviation from one LSB between two consecutive levels, over the entire transfer function.

[0027] FIG. 3 is a schematic of a conventional phase interpolator (PI) 300. The general operation of phase interpolators is known, such as described in "Phase Interpolator with Improved Linearity," Soulioutis et al, May 2015. Conventional PIs may require quadrature control signals I, Iz, Q, and Qz to control the operation of summing circuits that provide a charging current to capacitor 304. Some implementations, such as this one, also require common

mode feedback (CMFB). However, a portion of the charging current may be lost to devices 302, 303 and thereby create nonlinearity. Simple PI circuits such as PI 300 may have an INL error of 60 LSB or more, which may be greater than 6000 fs when one LSB is 100 fs.

[0028] FIG. 4 is a schematic diagram that illustrates improved phase interpolator 400 that may be used for PI 107, referring again to FIG. 1, in more detail. FIG. 5 is a timing diagram that illustrates the operation of PI 400. As described hereinabove, parameter α may be provided by control circuitry, such as control circuitry 104 in FIG. 1. Parameter α may be loaded into a register within or coupled to control logic 104, such as by execution of instructions, by other control logic, by initialization circuitry, by hardwired control logic, etc. In this example, parameter α is a fractional value having a value in a range of 0.0 to 1.0 that represents a percentage of a time period to shift the phase of output clock signal 120 with respect to input clock signal 102.

[0029] During each interpolation cycle, a first current source 401 is configured to produce a current proportional to $(1-\alpha)$ and a second current source 402 is configured to produce a current proportional to (α). For example, current sources 401, 402 may be implemented using digital to analog converters (DAC). In this example, DACs with a resolution of twelve bits may be used; other embodiments may use DACs with a higher or a lower resolution. The current sources may be controlled by control circuitry, such as control circuitry 104, referring again to FIG. 1.

[0030] During a first time period 501, the current from current source 401 is provided to ramp capacitor C1 via MOS device M1 while the current from current source 402 is dissipated by resistor R1 via MOS device M4. The current from current source 401 charges ramp capacitor C1 and produces a voltage PIout that ramps up with a slope that is proportional to $(1-\alpha)$ during first period of time 501 to produce a PIout voltage at time 531 that is proportional to the requested phase shift.

[0031] During a second period of time 502, the current proportional to (α) from current source 402 is also provided to ramp capacitor C1 via MOS device M3, such that the total current provided to capacitor C1 during period 502 is proportional to $(\alpha) + (1-\alpha) = 1$. Thus, during period 502 a constant rate of charge is produced that is independent of parameter α. Thus, voltage PIout ramps up with a slope that is independent of parameter α during time period 502 and is offset by the PIout voltage at time 531. In this manner, a two step voltage ramp signal is produced in which the first step produces a voltage magnitude proportional to a requested phase

shift at time 531 and in which the second step allows an output signal that has the requested phase shift to be produced based on the voltage magnitude at time 531.

[0032] During a third period of time 503, the current from current source 401 may be diverted to resistor R1 by MOS device M2 so that ramp capacitor C1 charges at a rate proportional to (α) during time period 503. In this manner, ramp capacitor C1 is charged to a same full charge voltage level as indicated at 510 during each repetition of the interpolation cycle, regardless of the value of parameter α.

[0033] A reference voltage Vref may be provided that has a value of ½ of full charge voltage 510, which corresponds to the maximum voltage at 531. By comparing PIout to Vref during the second period of time 502, a clock signal 120 may be generated that has a phase shift relative to input clock 102 that is extremely linear with respect to parameter α. For example, when $\alpha = 0$, clock signal 120 is asserted at time 520, which has a phase shift of 0 degrees relative to input clock signal 102. When $\alpha = 0.5$, clock signal 120 is asserted at time 521, which has a phase shift of 180 degrees relative to input clock signal 102. Similarly, when $\alpha = 1.0$, clock signal 120 is asserted at time 522, which has a phase shift of 360 degrees relative to input clock signal 102. Thus, any phase shift amount between 0-360 degrees may be produced by a corresponding selection of parameter α.

[0034] During time period 504, ramp capacitor C1 may be discharged by MOS device M7.

[0035] In this example, reference voltage Vref is produced by a third current source 403 that is configured to charge capacitor C2 during time period 504. Capacitor C2 may be reset during a second half of time period 503. In this manner, reference voltage Vref is produced under the same conditions as the rest of the PI circuit 400 so that mismatches caused by process variation are eliminated.

[0036] FIG. 6 is a schematic diagram that illustrates another implementation of an improved phase interpolator 600 that may be used as PI 107, referring again to FIG. 1. FIG. 7 is a timing diagram that illustrates the operation of PI 600. PI 600 may be implemented with a set of switch devices 630-639 that are controlled as indicated in FIG. 7 by timing signals S1-S5. The operation of PI 600 is similar to that of PI 400 as described with regard to FIGS. 4, 5. Switches 630-639 may be implemented using known or later developed devices, such as bipolar semiconductor devices, field effect devices, etc.

[0037] During each interpolation cycle, a first current source 601 is configured to produce a

current proportional to (1-α) and a second current source 602 is configured to produce a current proportional to (α). During a first time period 701, the current from current source 601 is provided to ramp capacitor C2 via switch device 631 while the current from current source 602 is dissipated by resistor R2 via switch devices 637 and 638. The current from current source 601 charges ramp capacitor C2 and produces a voltage PIout that ramps up with a slope that is proportional to (1-α) during first period of time 701 to produce a PIout voltage at the end of period 701 that is proportional to the requested phase shift.

[0038] During a second period of time 702, the current proportional to (α) from current source 602 is also provided to ramp capacitor C2 via switch device 636, such that the total current provided to capacitor C2 during period 702 is proportional to (α) + (1-α) = 1. Thus, during period 702 a constant rate of charge is produced that is independent of parameter α. Thus, voltage PIout ramps up with a slope that is independent of parameter α during time period 702.

[0039] During a third period of time 703, the current from current source 601 may be diverted to resistor R1 by switch devices 632 and 633 so that capacitor C2 charges at a rate proportional to (α) during time period 703. In this manner, ramp capacitor C2 is charged to a same full charge voltage level as indicated at 710 during each repetition of the interpolation cycle, regardless of the value of parameter α.

[0040] A reference voltage Vref may be provided that has a value of ½ of full charge voltage 710. By comparing PIout to Vref during the second period of time 702, a clock signal 620 may be generated that has a phase shift relative to input clock 712 that is extremely linear with respect to parameter α. For example, when α = 0, clock signal 620 is asserted at time 720, which has a phase shift of 0 degrees relative to input clock signal 712. When α = 0.5, clock signal 620 is asserted at time 721, which has a phase shift of 180 degrees relative to input clock signal 712. Similarly, when α = 1.0, clock signal 620 is asserted at time 722, which has a phase shift of 360 degrees relative to input clock signal 712. Thus, any phase shift amount between 0-360 degrees may be produced by a corresponding selection of parameter α.

[0041] During time period 704, capacitor C2 is discharged by switch device 639.

[0042] In this example, reference voltage Vref is produced by current from both current sources 601 and 602 that is configured to charge capacitor C1 during time period 705 via switches 630 and 635. Capacitor C1 is reset during a second half of time period 704 by switch 634 in this example. In another example, capacitor C1 may be reset during the second half of

time period 703 and charged during time period 704. In this manner, reference voltage Vref is produced under the same conditions as the rest of the PI circuit 600, so that mismatches caused by process variation are eliminated.

[0043] FIG. 8 is a plot illustrating nonlinearity that may occur in PI circuit 107 of FIG. 4 and PI circuit 600 FIG. 6. Referring again to the timing diagram FIG. 5, glitch interference caused by signal switching at timing points 531 and 532 may cause nonlinear errors when parameter α has a value that is near its min or max, respectively. Plot line 801 represents an ideal linear response curve between timing points 531 and 532. Plot line 802 represents a possible response curve due to signal glitches around timing points 531 and 532. An INL magnitude indicated at 803 may result. Example embodiments allow a phase interpolator to be operated in a more linear region, such as the region between timing points 831 and 832. In this case, an ideal linear response 804 in this region will result in a much lower INL magnitude, as indicated at 805.

[0044] FIG. 9 is a schematic diagram illustrating another embodiment of a phase interpolator 900 that may be used as PI 107, referring again to FIG. 1. FIG. 10 is a timing diagram illustrating operation of the PI 900. PI 900 is similar to PI 400, referring again to FIG. 4, in that it has a first current source 901 configured to produce a current proportional to $(1-\alpha)$ and a second current source 902 is configured to produce a current proportional to (α). However, current source 901 and 902 each use a reference current that has a value of 0.5 I(0). To compensate for the lower current value, the first time period 1001 and the second time period 1002 span two periods of input clock 1012.

[0045] A second set of current sources 904, 905 are included to provide a "pedestal current" that shifts the voltage ramp of PIout produced by charging capacitor C1 by an additional constant amount. In this embodiment, current sources 904, 905 provide a constant current of 0.25 I(0).

[0046] During first time period 1001, the current from current source 901 and 904 is provided to ramp capacitor C1 via MOS device M1 while the current from current source 902 and 905 is dissipated by resistor R1 via MOS device M4. The current from current sources 901, 904 charge ramp capacitor C1 and produce a voltage PIout that ramps up with a slope that is proportional to $(1-\alpha)$ during first period of time 1001, which is two periods of input clock 1012, to produce a PIout voltage at time 1031 that is proportional to the requested phase shift.

[0047] During a second period of time 1002, the current proportional to (α) from current source 902 and the fixed current from current source 905 are also provided to ramp capacitor C1

via MOS device M3, such that the total current provided to ramp capacitor C1 during period 1002 is proportional to (α) + (1-α) = 1. Thus, during period 1002 a constant rate of charge is produced that is independent of parameter α. Thus, voltage PIout ramps up with a slope that is independent of parameter α during time period 1002.

[0048] A reference voltage Vref may be provided that has a value of approximately 0.5 of full charge voltage 1010. By comparing PIout to Vref during only sampling period 1030 that is only a central portion of the second period of time 1002, a clock signal 920 may be generated that has a phase shift relative to a falling edge of input clock 1012 that is extremely linear with respect to parameter α. For example, when α = 0, clock signal 920 is asserted at time 1020, which has a phase shift of 0 degrees relative to the falling edge of input clock signal 1012. When α = 0.5, clock signal 1020 is asserted at time 1021, which has a phase shift of 180 degrees relative to the falling edge of input clock signal 1012. Similarly, when α = 1.0, clock signal 920 is asserted at time 1022, which has a phase shift of 360 degrees relative to the falling edge of input clock signal 102. Thus, any phase shift amount between 0-360 degrees may be produced by a corresponding selection of parameter α. Furthermore, reduced sampling period 1030 avoids glitching that may be caused by switching of the control signals.

[0049] During time period 1003, capacitor C1 may be discharged by MOS device M7.

[0050] In this example, reference voltage Vref is produced by a third current source 903 that is configured to charge capacitor C2 during time period 1004. Capacitor C2 may be reset during time period 1003 by MOS device M8. In this manner, reference voltage Vref is produced under the same conditions as the rest of the PI circuit 900 so that mismatches caused by process variation are eliminated.

[0051] FIG. 11 is a plot illustrating simulated operation of PI 900 in which one LSB corresponds to 100 fs. In this example, PI 900 exhibits a maximum INL of only 120 fs, which corresponds to 1.2 LSB, as illustrated in FIG. 11. This compares to a max INL error of over 6000 fs in the conventional device illustrated in FIG. 3.

[0052] FIG. 12 is a flow chart illustrating operation of a high linearity phase interpolator, such as described hereinabove in connection with FIGS. 3-10. As described with regard to FIGS. 1-2, a high linearity phase interpolator may be used to generate accurate fractional frequency clock signals from a fixed reference frequency.

[0053] A phase value parameter indicative of a desired phase difference between an output

signal and an input clock signal edge may be produced 1202 by control logic coupled to the phase interpolator.

[0054] A first capacitor may be charged 1204 for a first period of time with a first current that is proportional to the phase value parameter to produce a first voltage on the capacitor that is proportional to the phase value parameter. As described in more detail hereinabove, a current source controlled by a DAC may be used to produce the first current. The phase value parameter may be used to control the DAC. For example, the phase value may be a 12-bit digital value that is provided to a 12-bit DAC.

[0055] The first capacitor may be further charged 1206 for a second period of time with a second current that has a constant value to form a voltage ramp offset by the first voltage. As described hereinabove, the second current source may also be implemented using a DAC for control.

[0056] A reference voltage may be compared 1208 to the voltage ramp during the second period of time. As described hereinabove, a comparator such as comparator 110 in FIG. 4 may be used for this comparison.

[0057] The output signal may then be asserted 1210 at a time when the voltage ramp equals the reference voltage to produce an output signal that is offset from the input clock by a phase amount specified by the phase value parameter.

[0058] As described hereinabove in more detail, a reference voltage may be produced 1212 by a current source that is configured to charge a second capacitor during another time period. The second capacitor may be reset at the end of each interpolation cycle. In this manner, a reference voltage may be produced under the same conditions as the rest of the PI circuit so that mismatches caused by process variation are eliminated.

Other Embodiments

[0059] Referring again to FIG. 4, in another example embodiment, current source 401 may have a value of $(\alpha)I_0$ and current source 402 may have a value of $(1-\alpha)I_0$.

[0060] In another embodiment, current source 401 may have a current value that is proportional to parameter α and current source 402 may have a constant current value of I_1. In this case, current from current source 401 may be directed to resistor R1 during time period 502 so that a ramp voltage with a fixed slope is produced by current source 402 alone during sample period 502.

[0061] In another embodiment, various combinations of current sources may be configured to produce a voltage slope proportional to requested phase shift amount during a first period of time and to produce an additional voltage slope having a fixed slope during a sampling period of time.

[0062] In various embodiments, the ramp capacitor may be implemented as a discrete capacitor, a MOS device, multiple devices, etc.

[0063] In another embodiment, a two step ramp signal for determining a phase shift may be produced using another type of device characteristic, such as producing a current that has a two step ramp using an inductive device.

[0064] A fractional frequency clock generator system is described herein, but other systems may embody the high linearity phase interpolator disclosed herein for functions, such as clock recovery for SerDes interfaces, frequency control of PLLs, etc.

[0065] In this description, the term "couple" and derivatives thereof mean an indirect, direct, optical, and/or wireless electrical connection. Thus, if a first device couples to a second device, that connection may be through a direct electrical connection, through an indirect electrical connection via other devices and connections, through an optical electrical connection, and/or through a wireless electrical connection.

[0066] Although method steps may be shown in the drawings and/or described herein in a sequential fashion, one or more of the steps shown and/or described may be omitted, repeated, performed concurrently, and/or performed in a different order.

[0067] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A method for performing phase interpolation, the method comprising:

producing a phase value parameter indicative of a desired phase difference between an output signal and an input clock edge;

charging a first capacitor for a first period of time with a first current that is proportional to the phase value parameter to produce a first voltage on the capacitor that is proportional to the phase value parameter;

charging the first capacitor for a second period of time relative to the input clock edge with a second current that has a constant value to form a voltage ramp offset by the first voltage;

comparing a reference voltage to the voltage ramp during the second period of time; and

asserting the output signal at a time when the voltage ramp equals the reference voltage.

2. The method of claim 1, further including resetting the first capacitor after the second period of time.

3. The method of claim 1, wherein the reference voltage is produced by charging a second capacitor for a third period of time with a third current that has a constant value; and

resetting the first capacitor and the second capacitor after the second period of time.

4. The method of claim 1, wherein the second current has a value of I-total and the first current has a value of (1-α)I-total, where α is proportional to the phase value parameter.

5. The method of claim 4, wherein the third current has a value that is a fraction of the second current value.

6. The method of claim 1, further including charging the first capacitor during the first period of time with an additional constant value pedestal current.

7. The method of claim 1, further including charging the first capacitor during the second period of time with an additional constant value pedestal current.

8. A phase interpolation circuit, comprising:

a first variable current source configured to produce a first constant current proportional to a phase value parameter;

a second variable current source configured to produce a second constant current, such that the sum of the first constant current and the second constant current is predefined fixed value;

a ramp capacitor coupled by a first switch device to the first current source and by a second switch device to the second current source; and

a comparator circuit with a first input coupled to receive a voltage produced on the ramp capacitor by the first current source and the second current source, a second input coupled to a reference voltage, and an output for providing a phase shifted output signal.

9. The phase interpolation circuit of claim 8, wherein the first current source is configured to produce a current equal to $(1-\alpha)I_0$, and wherein the second current source is configured to produce a current equal to $(\alpha)I_0$, where α is a phase value parameter indicative of a desired phase difference between the output signal and an input clock edge.

10. The phase interpolation circuit of claim 8, further including a reference capacitor coupled by a third switch device to a current source to generate the reference voltage.

11. The phase interpolation circuit of claim 8, further including another switch device coupled to the ramp capacitor and to a ground reference for periodically resetting the ramp capacitor.

12. The phase interpolation circuit of claim 8, further including another switch device coupled to the reference capacitor and to a ground reference for periodically resetting the reference capacitor.

3. The phase interpolation circuit of claim 8, further including a third current source coupled by another switch device to the ramp capacitor and configured to produce a constant pedestal current.

14. The phase interpolation circuit of claim 13, further including a fourth current source coupled by another switch device to the ramp capacitor and configured to produce another constant pedestal current.

15. A system comprising:

a fractional frequency divider (FFD) module configured to generate an output clock signal in which each phase of the output clock signal is equal to a fractional number of phases of an input clock signal, wherein the FFD includes:

control logic configured to provide a number N indicative of a number of full phases of the input clock signal required to define a phase of the output clock signal, and configured to provide a phase value parameter indicative of a fractional phase of the input clock signal required to define the phase of the output signal;

a counter coupled to receive the input clock signal and coupled to the control logic to receive the number N, the counter having an output configured to assert an Nth clock signal each time the counter counts N phases of the input clock;

a phase interpolator module (PI) coupled to receive the phase value parameter from the control logic and to receive the Nth clock signal from the counter, wherein the PI module includes:

a first variable current source configured to produce a first constant current proportional to the phase value parameter;

a second variable current source configured to produce a second constant current, such that the sum of the first constant current and the second constant current is predefined fixed value;

a ramp capacitor coupled by a first switch device to the first current source and by a second switch device to the second current source; and

a comparator circuit with a first input coupled to receive a voltage produced on the ramp capacitor by the first current source and the second current source, a second input coupled to a reference voltage, and an output for providing the phase shifted output clock signal.

16. The system of claim 15, further including an oscillator circuit with an output coupled to the counter to provide the input clock signal.

17. The system of claim 15, further including a plurality of the FFD modules coupled to receive the input clock signal.

18. The system of claim 17, wherein the system is formed on a single integrated circuit.

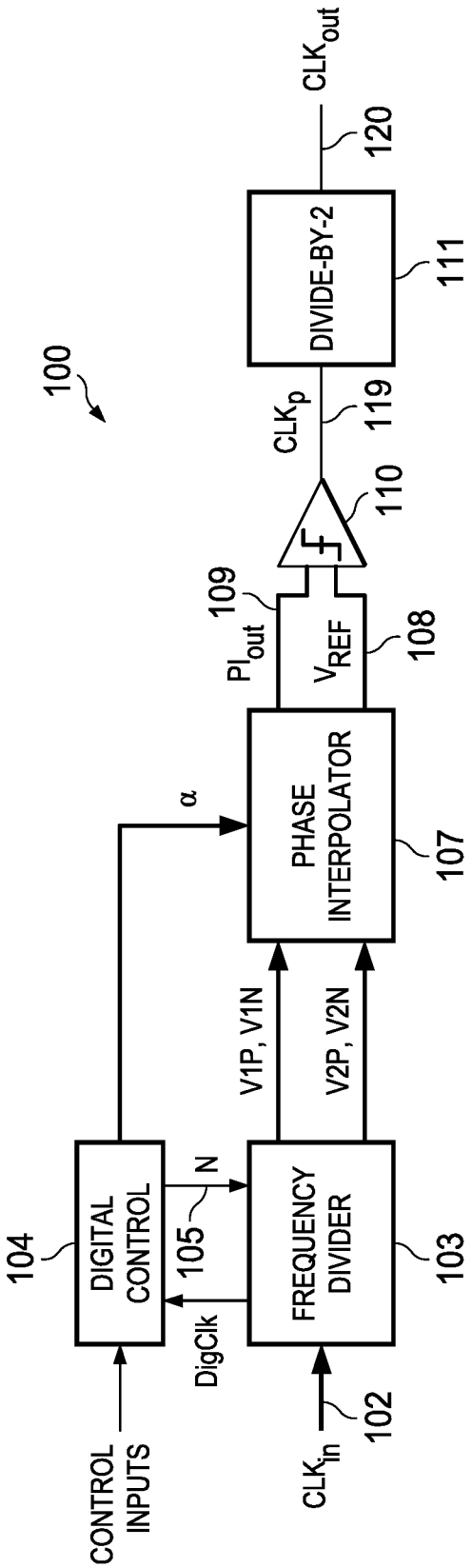

100
CONTROL INPUTS
104
DIGITAL CONTROL
105
N
DigClk
FREQUENCY DIVIDER
103
CLK$_{in}$
102
V1P, V1N
V2P, V2N
α
PHASE INTERPOLATOR
107
PI$_{out}$
109
V$_{REF}$
108
110
CLK$_p$
119
DIVIDE-BY-2
111
CLK$_{out}$
120

FIG. 1A

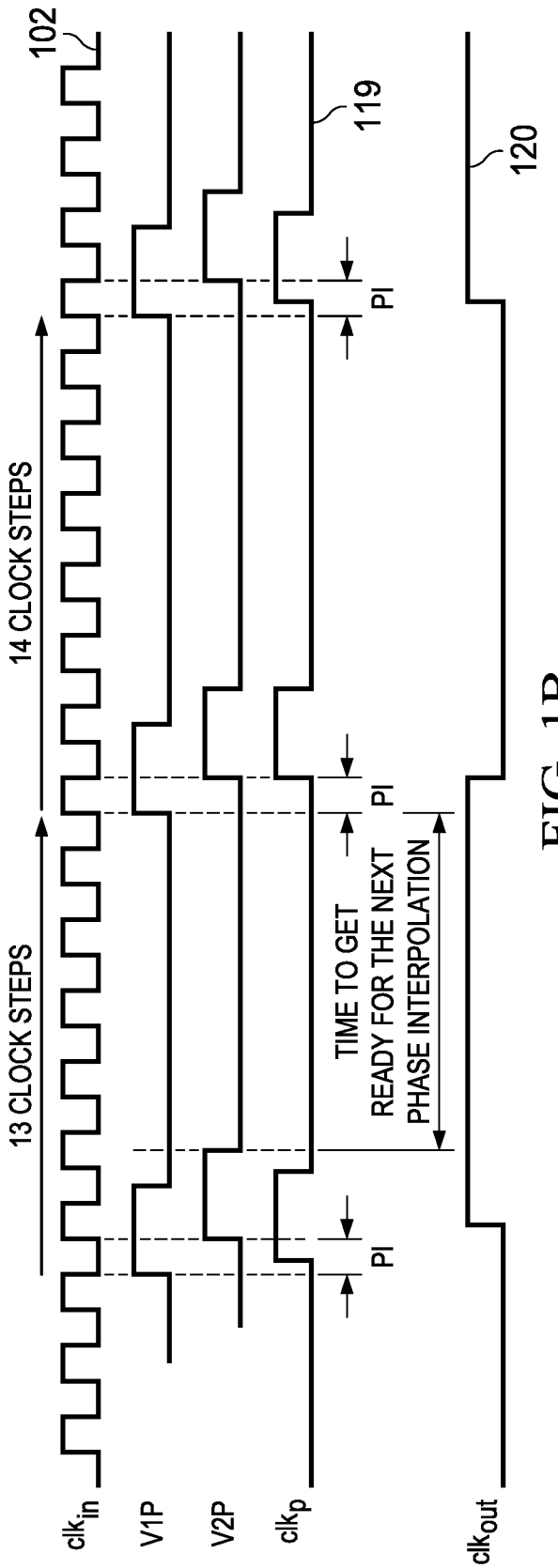

102
14 CLOCK STEPS
13 CLOCK STEPS
119
PI
PI
PI
TIME TO GET READY FOR THE NEXT PHASE INTERPOLATION
120
clk$_{in}$
V1P
V2P
clk$_p$
clk$_{out}$

FIG. 1B

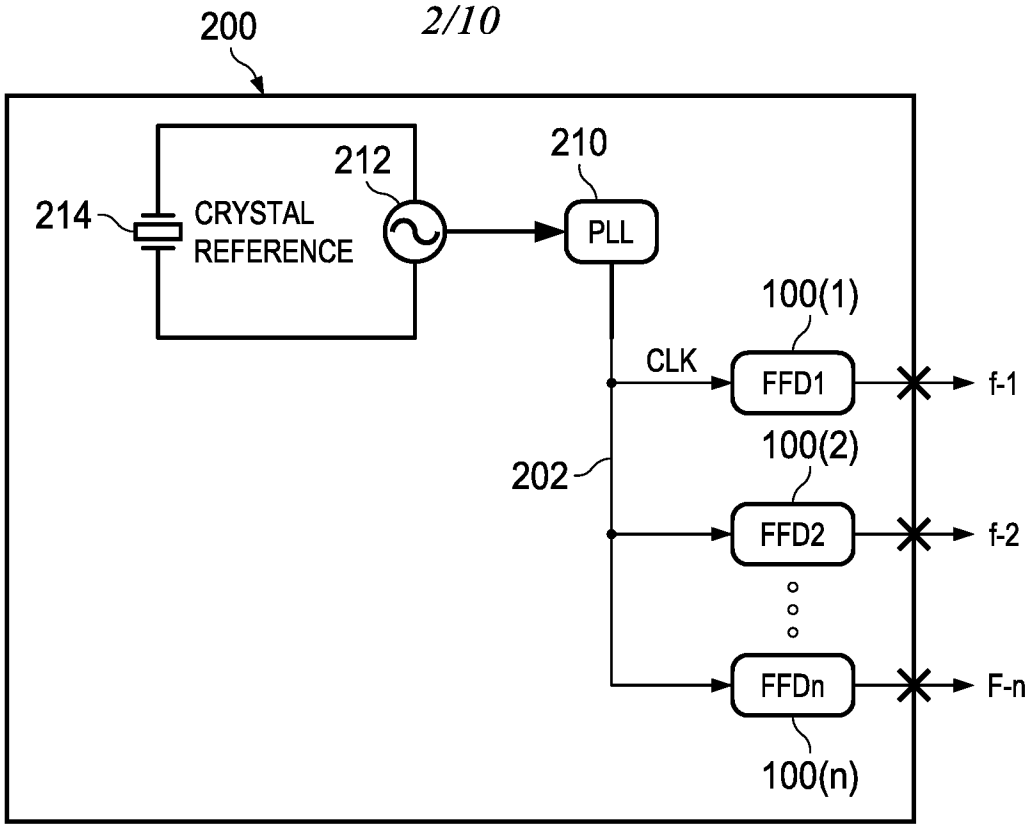


FIG. 2

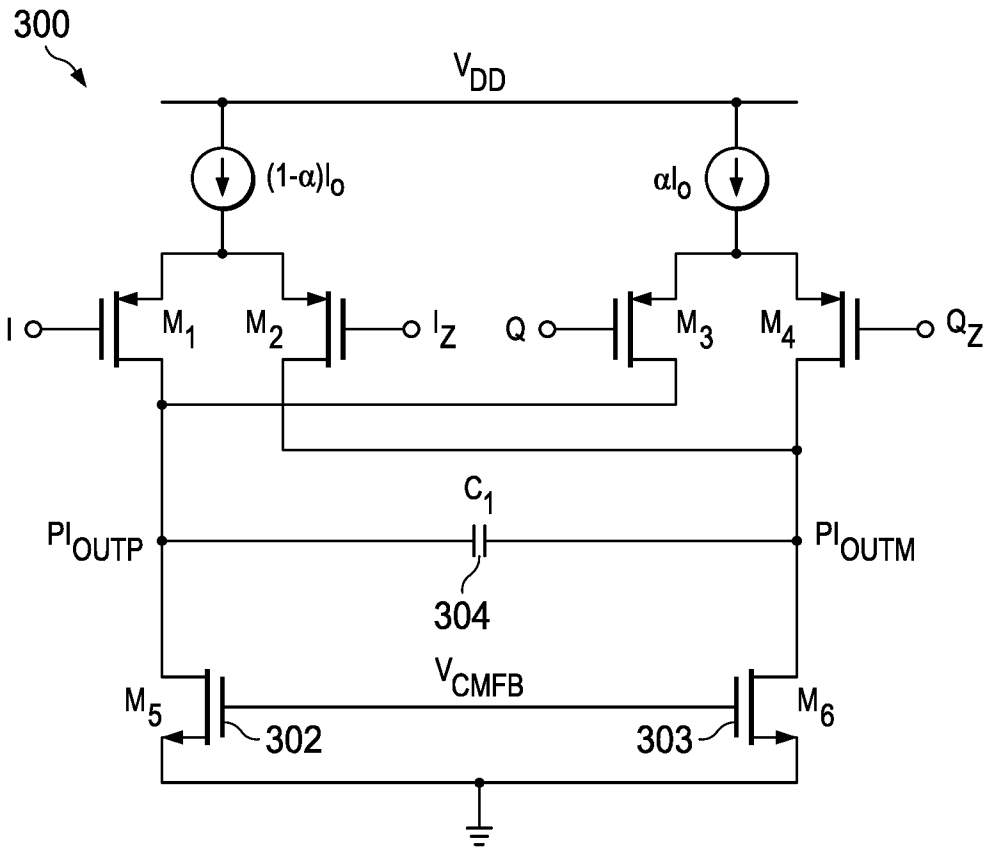


FIG. 3
(PRIOR ART)

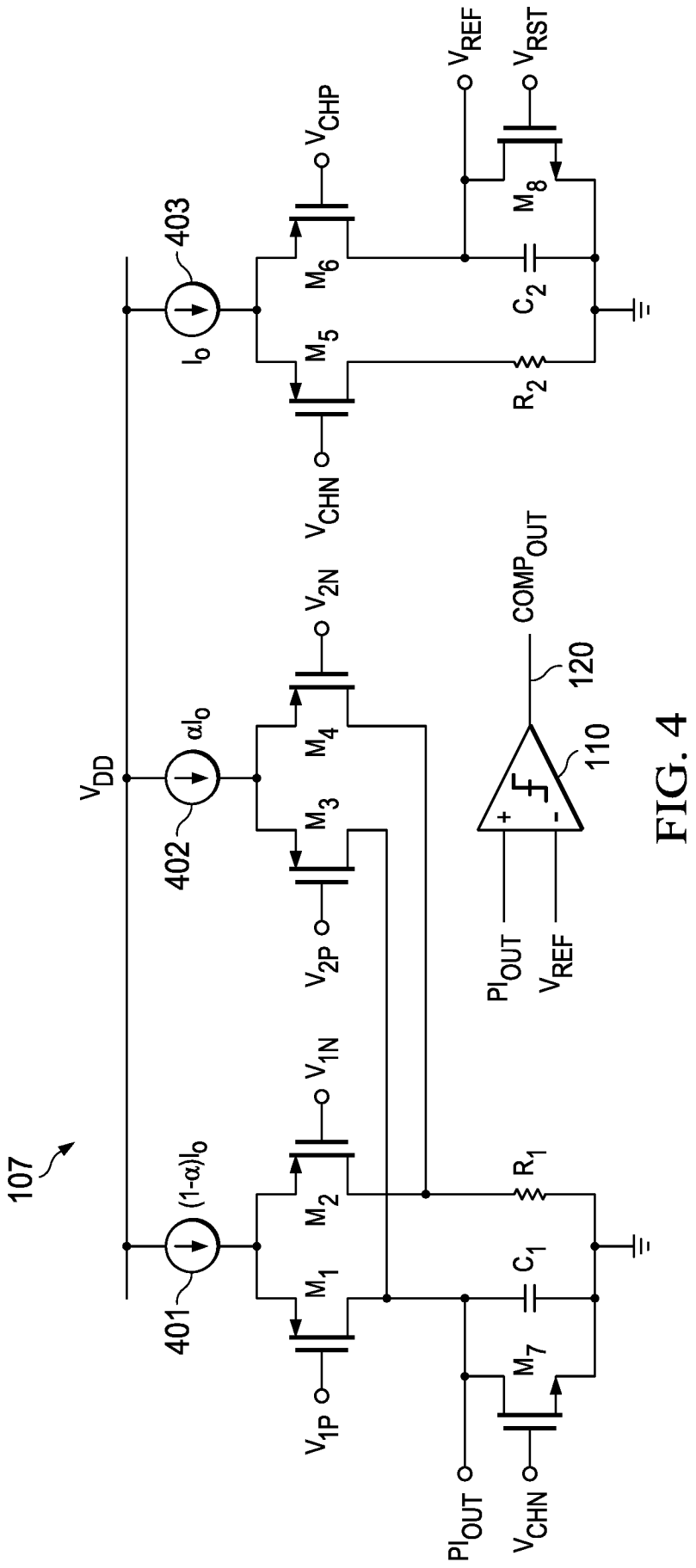

107
V_{DD}
401
$(1-\alpha)I_o$
402
αI_o
403
I_o
M_1
M_2
M_3
M_4
M_5
M_6
M_7
M_8
V_{1P}
V_{1N}
V_{2P}
V_{2N}
V_{CHN}
V_{CHP}
V_{RST}
V_{REF}
C_1
C_2
R_1
R_2
PI_{OUT}
V_{CHN}
PI_{OUT}
V_{REF}
110
120
$COMP_{OUT}$

FIG. 4

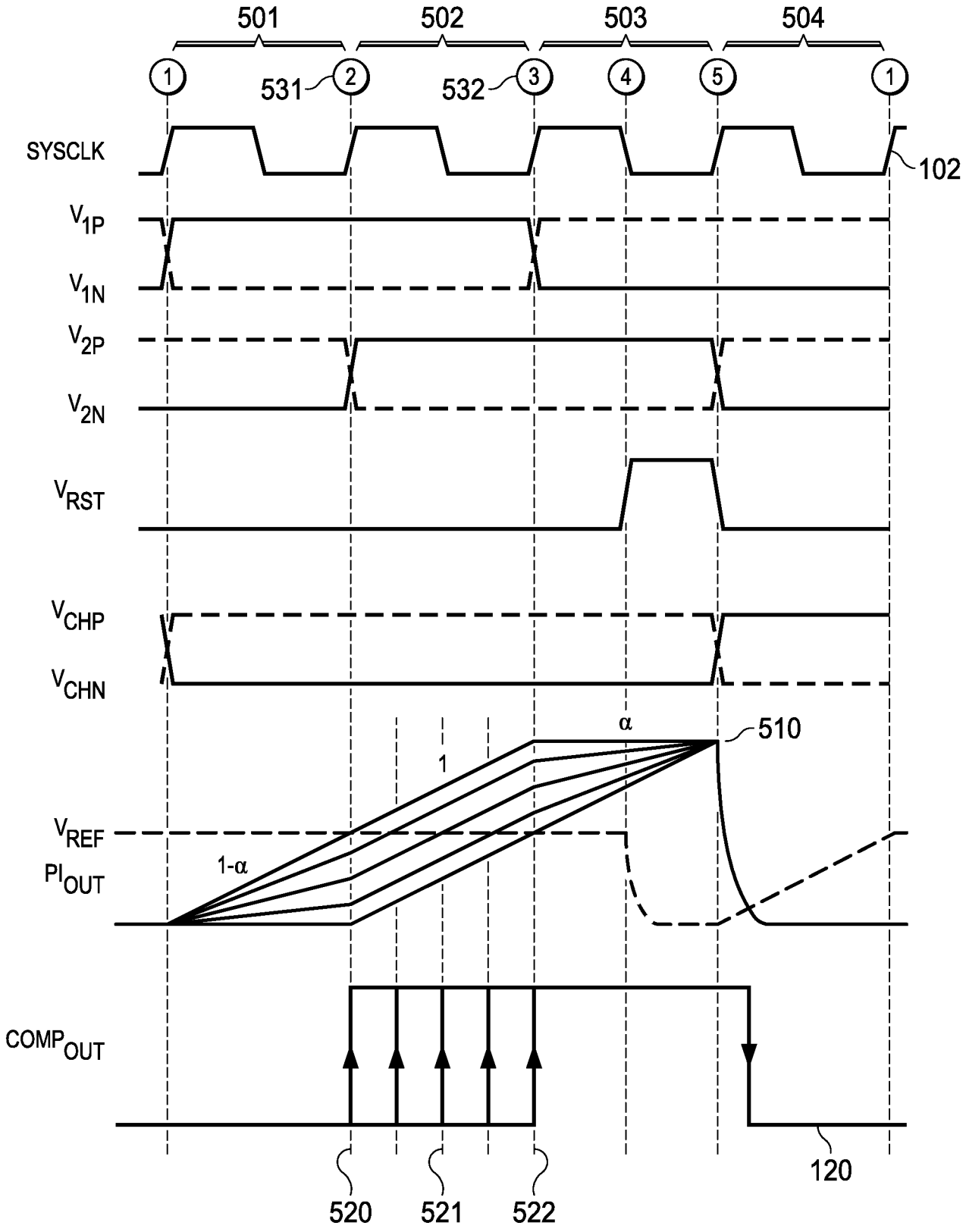

501
502
503
504
1
531
2
532
3
4
5
1
SYSCLK
102
V1P
V1N
V2P
V2N
VRST
VCHP
VCHN
α
510
1
VREF
PIOUT
1-α
COMPOUT
120
520
521
522

FIG. 5

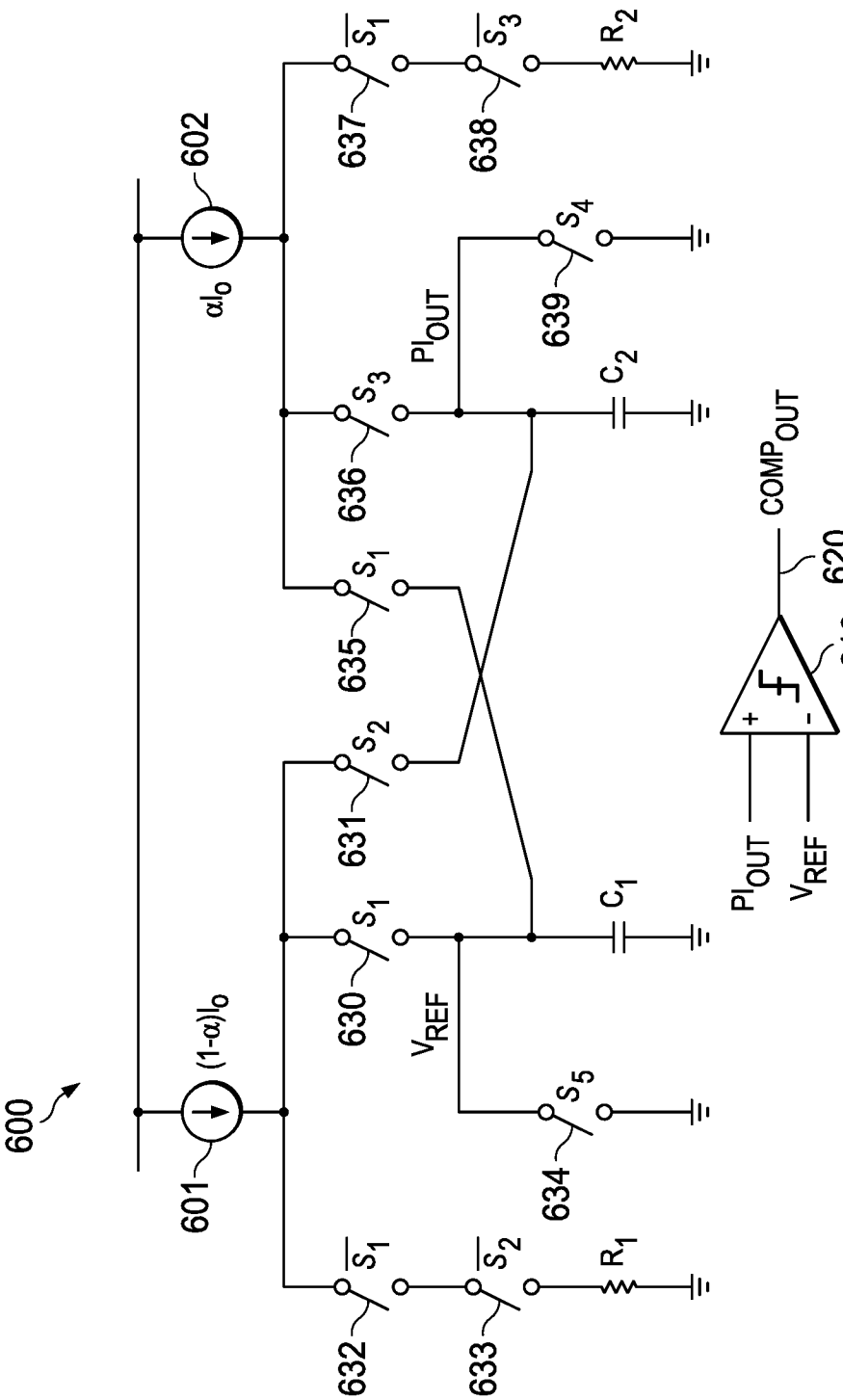

600
601
602
$(1-\alpha)I_0$
αI_0
630
631
632
633
634
635
636
637
638
639
S_1
S_2
S_3
S_4
S_5
$\overline{S_1}$
$\overline{S_2}$
$\overline{S_3}$
C_1
C_2
R_1
R_2
V_{REF}
PI_{OUT}
$COMP_{OUT}$
610
620
+
-

FIG. 6

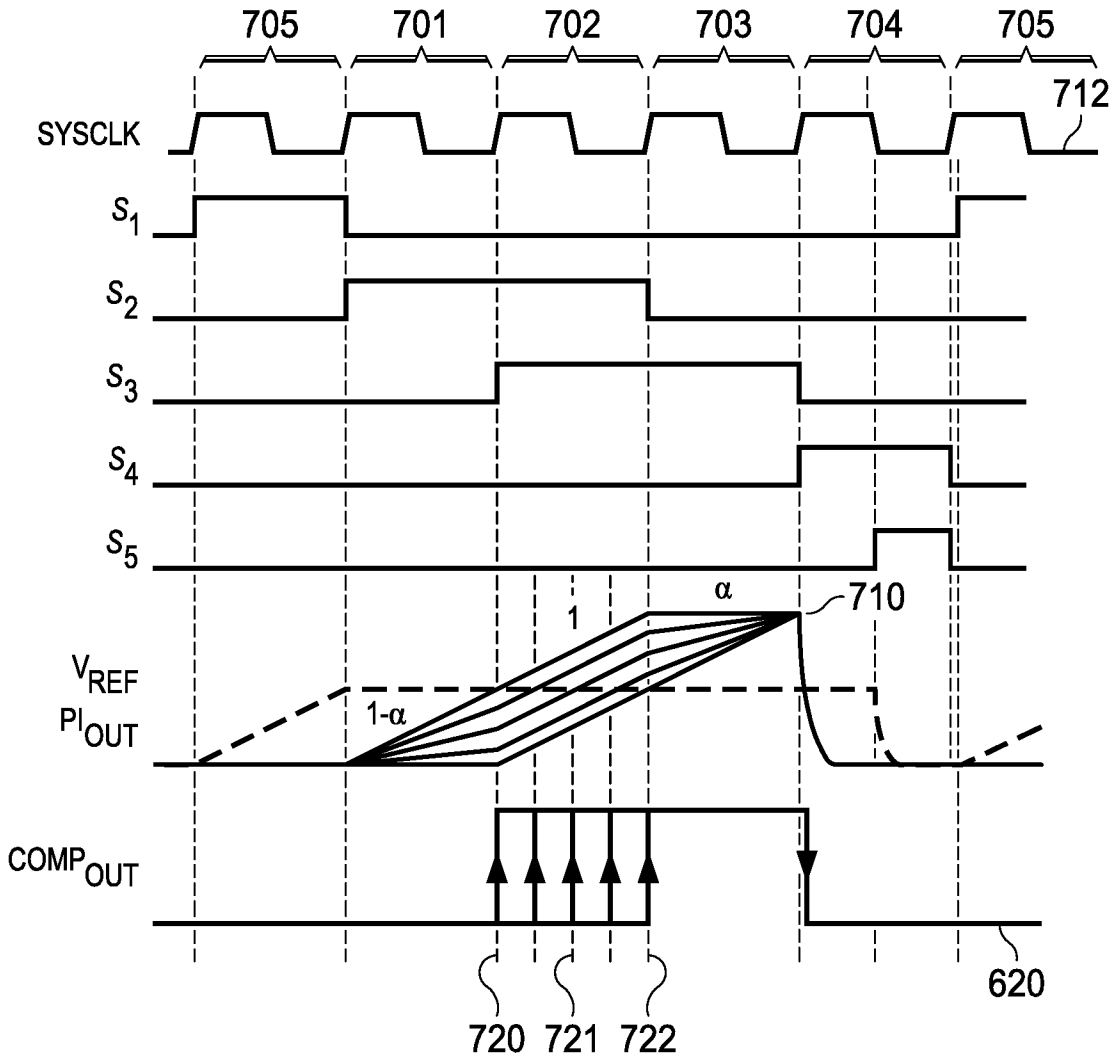
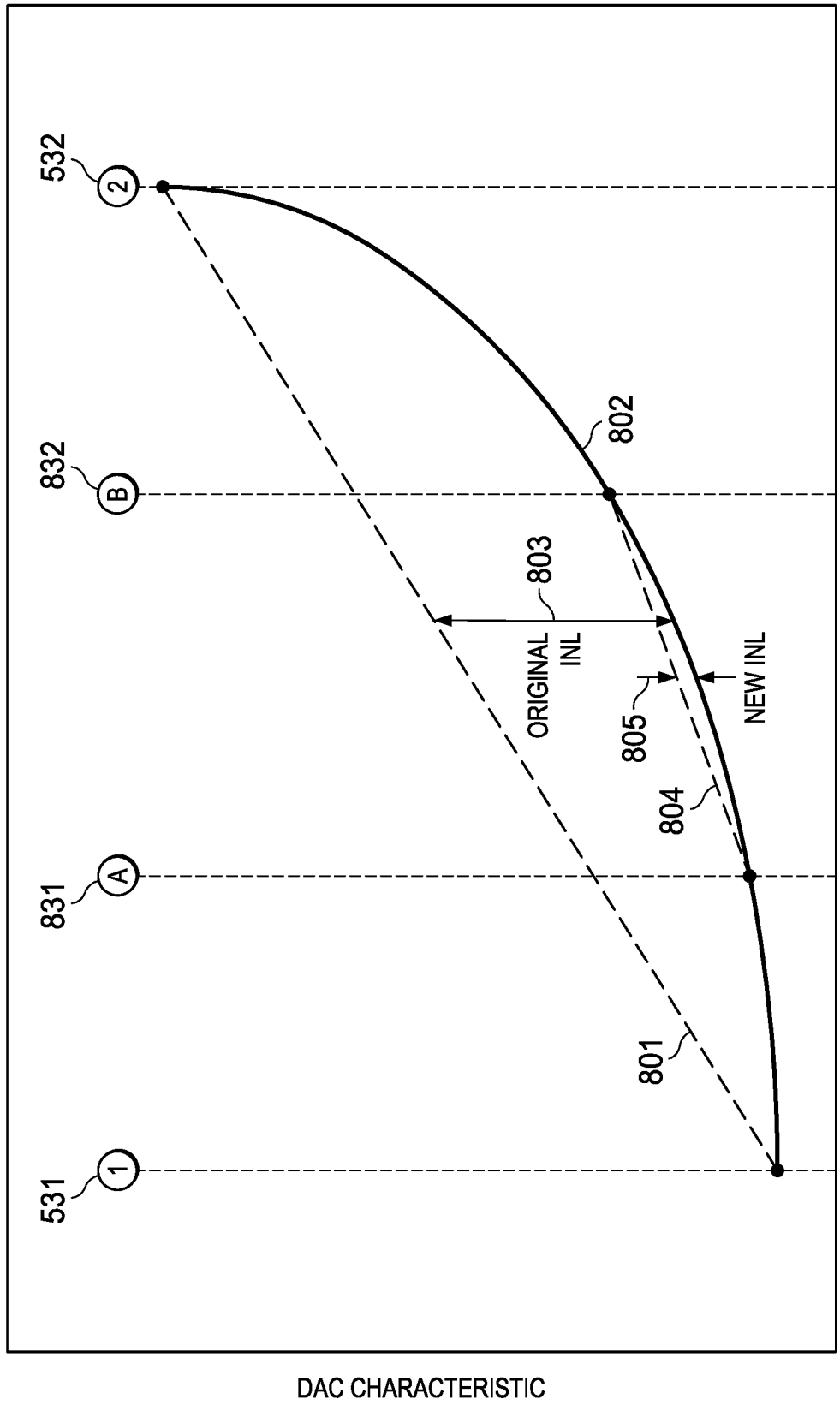

705
701
702
703
704
705
712
SYSCLK
S1
S2
S3
S4
S5
α
1
710
VREF
PIOUT
1-α
COMPOUT
620
720
721
722

FIG. 7

FIG. 8


532
2
832
B
831
A
531
1
802
803
ORIGINAL INL
805
NEW INL
804
801
DAC CODE
DAC CHARACTERISTIC

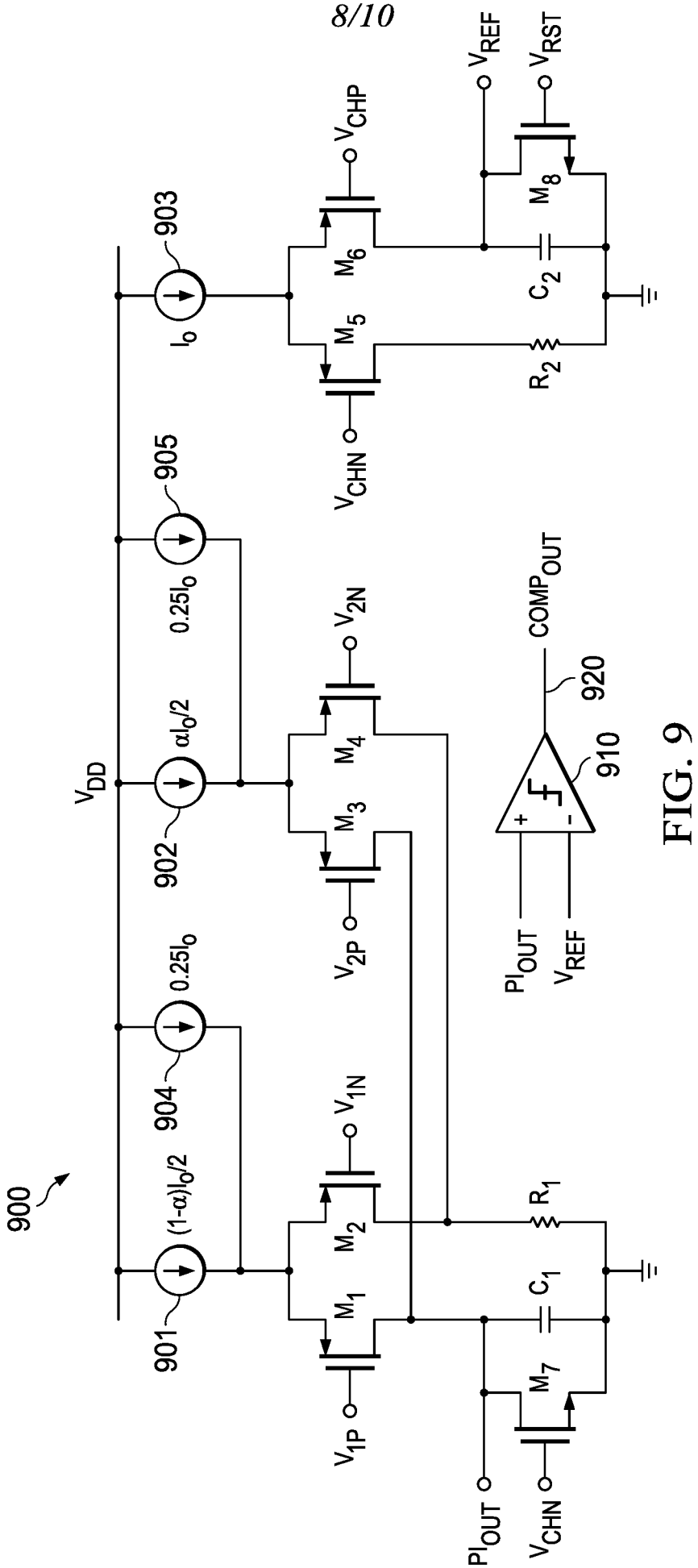

900
901
902
903
904
905
$(1-\alpha)I_0/2$
$\alpha I_0/2$
I_0
$0.25I_0$
$0.25I_0$
V_{DD}
M_1
M_2
M_3
M_4
M_5
M_6
M_7
M_8
V_{1P}
V_{1N}
V_{2P}
V_{2N}
V_{CHN}
V_{CHP}
V_{REF}
V_{RST}
C_1
C_2
R_1
R_2
PI_{OUT}
V_{CHN}
PI_{OUT}
V_{REF}
$COMP_{OUT}$
910
920

FIG. 9

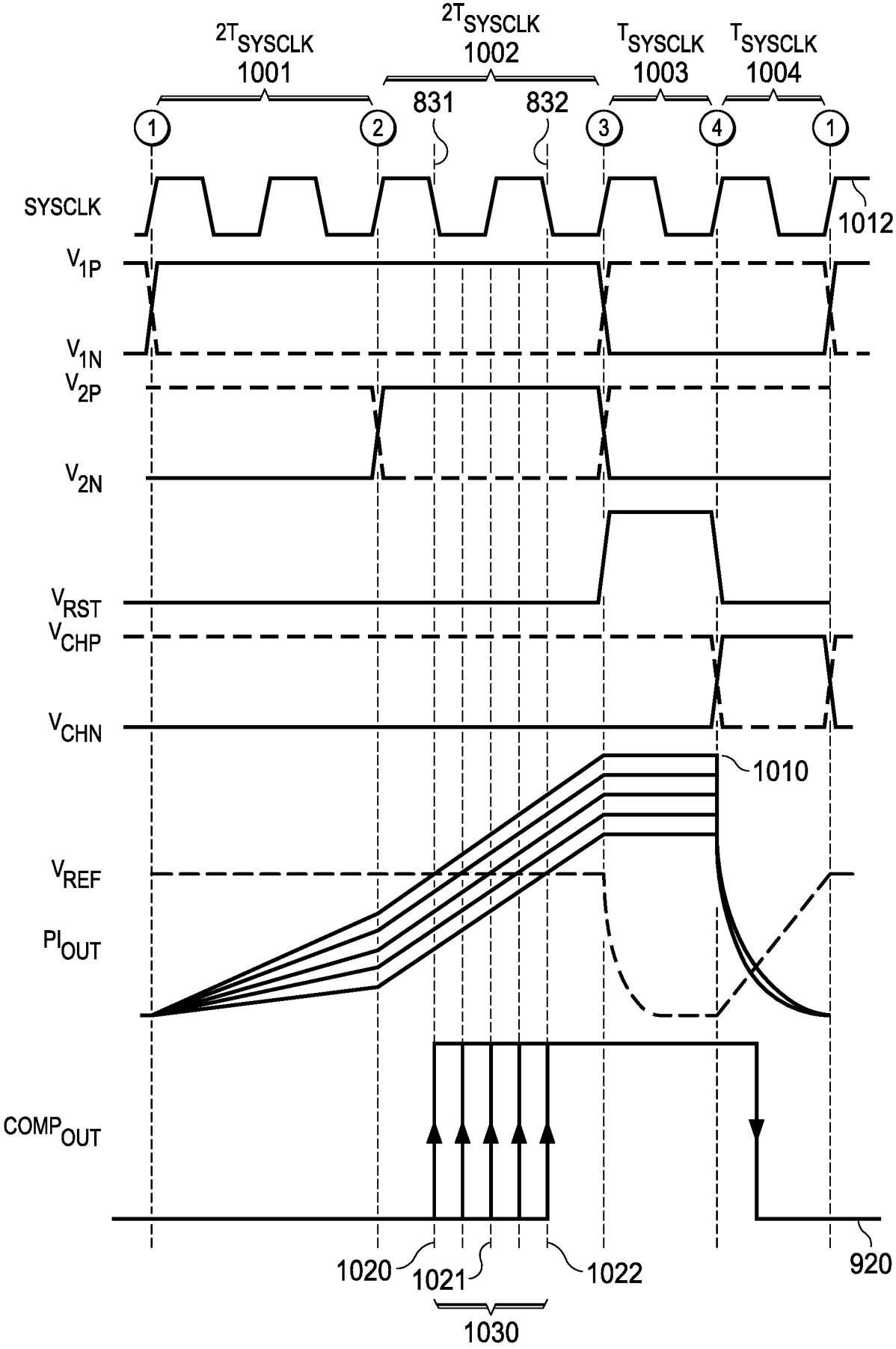

2TSYSCLK
1001
2TSYSCLK
1002
TSYSCLK
1003
TSYSCLK
1004
831
832
1
2
3
4
1
SYSCLK
1012
V1P
V1N
V2P
V2N
VRST
VCHP
VCHN
1010
VREF
PIOUT
COMPOUT
1020
1021
1022
1030
920

FIG. 10

FIG. 11

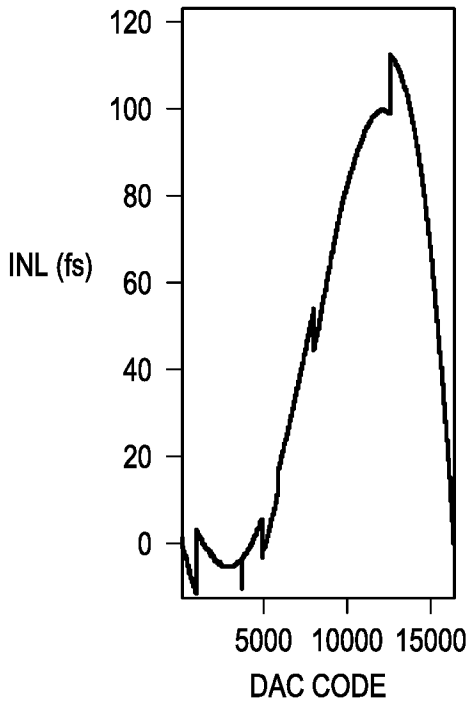
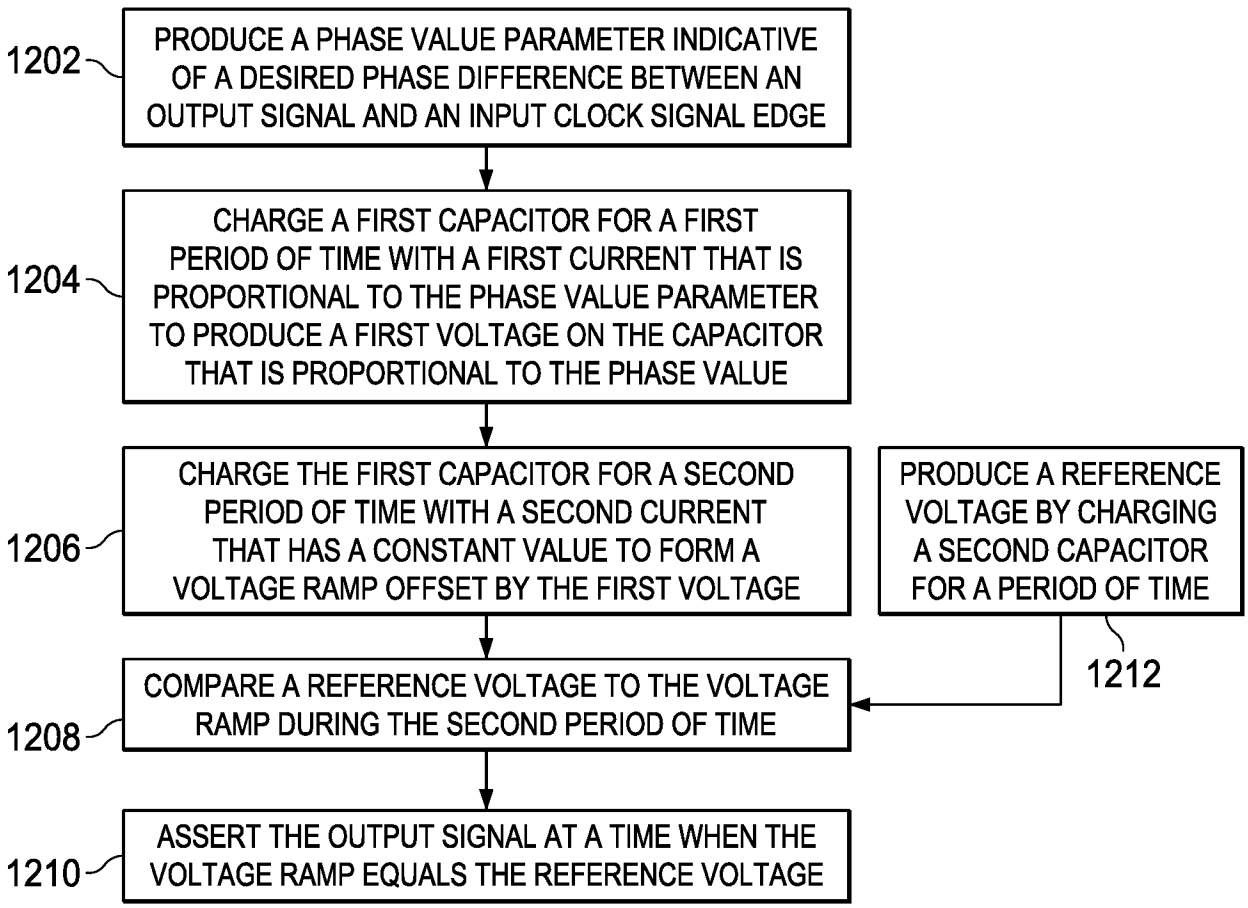

120
100
80
INL (fs)
60
40
20
0
5000
10000
15000
DAC CODE

FIG. 12


1202
PRODUCE A PHASE VALUE PARAMETER INDICATIVE OF A DESIRED PHASE DIFFERENCE BETWEEN AN OUTPUT SIGNAL AND AN INPUT CLOCK SIGNAL EDGE
1204
CHARGE A FIRST CAPACITOR FOR A FIRST PERIOD OF TIME WITH A FIRST CURRENT THAT IS PROPORTIONAL TO THE PHASE VALUE PARAMETER TO PRODUCE A FIRST VOLTAGE ON THE CAPACITOR THAT IS PROPORTIONAL TO THE PHASE VALUE
1206
CHARGE THE FIRST CAPACITOR FOR A SECOND PERIOD OF TIME WITH A SECOND CURRENT THAT HAS A CONSTANT VALUE TO FORM A VOLTAGE RAMP OFFSET BY THE FIRST VOLTAGE
PRODUCE A REFERENCE VOLTAGE BY CHARGING A SECOND CAPACITOR FOR A PERIOD OF TIME
1212
1208
COMPARE A REFERENCE VOLTAGE TO THE VOLTAGE RAMP DURING THE SECOND PERIOD OF TIME
1210
ASSERT THE OUTPUT SIGNAL AT A TIME WHEN THE VOLTAGE RAMP EQUALS THE REFERENCE VOLTAGE

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2017/060658

A. CLASSIFICATION OF SUBJECT MATTER

H03D 3/00 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03D 3/00, H03K 5/00-5/145

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PAJ, Esp@cenet, DWPI, Patentscope, USPTO DB, CIPO (Canada PO), SIPO DB, PatSearch (RUPTO internal), RUPAT, RUABRU, RUABEN, RUPAT_OLD, RUABU1

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2009/0103675 A1 (DIABLO TECHNOLOGIES INC.) 23.04.2009	1-18
A	US 2014/0037035 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD.) 06.02.2014	1-18
A	US 2011/0241746 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD.) 06.10.2011	1-18
A	US 2009/0108898 A1 (AGERE SYSTEMS INC.) 30.04.2009	1-18

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 February 2018 (15.02.2018)	06 March 2018 (06.03.2018)

Name and mailing address of the ISA/RU:	Authorized officer
Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	K. Afanasiev Telephone No. (495)531-64-81