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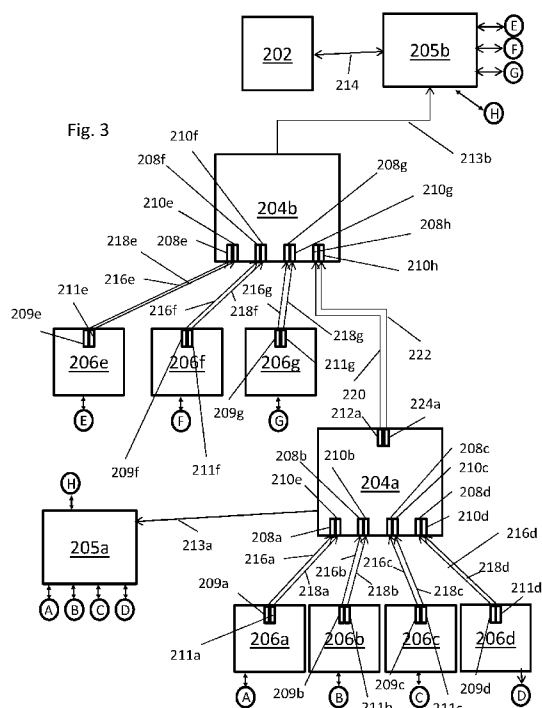
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(57) Abstract: A microprocessor comprises an interconnect system arranged to control access to a slave device (202). The interconnect system comprises: a plurality of first stage master devices (206a-d), wherein each master device 206a-d has a priority value for said slave associated therewith; a first stage arbiter (204a) connected to said plurality of first stage master devices 206a-d and arranged to: determine a first selected master device (206a-d) from the priority values (216a-d) of those of the first stage master devices (206a-d) wishing to connect to the slave (202); and produce a transaction including the priority value (216a-d) associated with the first selected master device (206a-d); and a second stage arbiter (204b) connected to said first stage arbiter (204a) to receive said transaction and further connected to at least one second stage master device (206e-g) having a priority value (216e-g) for said slave (202) associated therewith. The second arbiter (204b) is arranged to: determine a second selected master device (206a-g) from the priority values (216e-g) of any second stage master device (206e-g) wishing to connect to the slave and the priority value (216a-d) of the transaction from the first stage arbiter (204a).

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Interconnect System

The present invention relates to interconnect systems, particularly the arbitration of requests to interact with a slave device generated by multiple master devices
5 connected at different stages in a multi-stage interconnect system.

Modern electronic devices such as system-on-chip (SoC) devices may include an "interconnect system" to allow multiple master devices to access a given slave device. Typically an arbitration unit or "arbiter" is arranged to determine which
10 master device has priority access to the slave device in the event that more than one of them requests access or initiates a transaction involving the slave. However, the Applicant has appreciated that conventional interconnect systems typically suffer from timing issues and relatively high power consumption.

15 When viewed from a first aspect, the present invention provides a microprocessor comprising an interconnect system arranged to control access to a slave device, said interconnect system comprising:

- a plurality of first stage master devices, wherein each master device has a priority value for said slave associated therewith;
- 20 a first stage arbiter connected to said plurality of first stage master devices and arranged to: determine a first selected master device from the priority values of those of the first stage master devices wishing to connect to the slave; and produce a transaction including the priority value associated with the first selected master device; and
- 25 a second stage arbiter connected to said first stage arbiter to receive said transaction and further connected to at least one second stage master device having a priority value for said slave associated therewith, said second arbiter being arranged to: determine a second selected master device from the priority values of any second stage master device wishing to connect to the slave and the priority
30 value of the transaction from the first stage arbiter.

Thus it will be appreciated by those skilled in the art that an interconnect system in accordance with embodiments of the present invention provides a "multi-stage" system wherein different master devices are connected at different stages, and
35 each stage has an arbiter. The first stage arbiter determines from the priority

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values associated with its connected master devices that wish to connect to the slave which master device should be selected and passes this as a transaction which includes the priority value of the selected master to the second stage arbiter. The second stage arbiter compares the transaction priority value to the priority value(s) associated with any master device connected to the second stage arbiter that wishes to connect to the slave. If the master device selected by the first arbiter is determined to be of greater priority than any master device connected to the second arbiter that wishes to connect to the slave, the second arbiter will select the master device selected by the first arbiter.

Dividing the interconnect system into two or more stages can give a number of advantages. For example each stage can be designed with knowledge only of the number of masters that are connected to that stage, i.e. without needing to know the number of masters connected to other stages. Moreover the connection matrix required for each stage is simplified compared to a densely connected matrix as is required for a corresponding single-stage system. These benefits means that the individual stages can be developed and implemented more easily and independently than was previously the case.

An interconnect system in accordance with embodiments of the present invention also allows for the priority values associated with each master device to be set completely independently of the configuration of the interconnect system itself.

In a set of embodiments the first and second arbiters are located in different clock domains having respective lower and higher frequencies. This allows a further advantage of embodiments of the invention to be realised whereby improved and less critical timing paths, fewer gates and therefore less power is needed in the higher frequency clock domain. In one illustrative example the first stage arbiter is located in the lower clock domain – e.g. 16 MHz – and the second stage arbiter is located in the higher frequency clock domain – e.g. 64 MHz.

In a set of embodiments transactions originating from the first stage are always addressed to one particular slave. This means that no new address decoding is required in the second stage for these transactions which provides a saving in the number of gates needed in a digital integrated circuit implementation.

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In a set of embodiments the priority levels comprise a plurality of bits. This allows the system to support 'fine grain' priority levels rather than simpler 'high' or 'low' levels.

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The second stage arbiter could effect a connection between said second selected master device and said slave device. Alternatively the second stage arbiter could produce a second transaction including the priority value associated with the second selected master device. This could be passed to a third stage arbiter, thereby forming a cascade or hierarchy of arbiters. Alternatively it could be passed to another system to effect the connection between said second selected master device and said slave device.

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It is also envisaged that a downstream arbiter could receive transactions from more than one upstream arbiter.

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While it will be appreciated that the arbiters may apply any algorithm or metric in order to determine which master device connected to it should be the selected master device for that stage, in some preferred embodiments the first selected master device is determined to be the master device having the highest priority value associated therewith. In a set of potentially overlapping embodiments, the second selected master device is determined to be the master device having the highest priority value associated therewith (which may be connected to the second arbiter or associated with the transaction priority value).

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In some embodiments, the slave device is connected to the second arbiter. It will of course be appreciated that in the set of embodiments wherein the interconnect system comprises more than two arbiters, the slave device may, at least in some embodiments, be connected to a final arbiter, said final arbiter being an arbiter that does not produce a transaction with a priority value (although typically it will pass along a transaction without a priority value).

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The priority value assigned for each master device for the slave (or for each slave that the master can access) may be configured either during the design of the interconnect system or may, at least in preferred embodiments, be user-

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configurable. Such embodiments may allow the user to configure priorities for each master-slave pair without having to take into account the internal architecture of the interconnect system, which clock domain the master is in etc.

5 As mentioned above, in at least some embodiments the priority values are fixed during use. However in some alternative embodiments, at least some of the priority values are arranged to vary dynamically when said interconnect system is in use. Having the priority values vary dynamically may also be useful in systems having different modes of operation wherein different master devices are given different
10 priorities than would be the normal in other modes of operation.

In some embodiments, the interconnect system is arranged to control access to two or more slave devices. It may be arranged so that master devices at all stages have access to slave devices at all stages or there may only be a subset of possible
15 pairing that are permitted.

While it will be appreciated by those skilled in the art that there are numerous specifications for interconnect systems known in the art *per se*, in at least some preferred embodiments the interconnect system is implemented in accordance with
20 the Advanced Microcontroller Bus Architecture (AMBA®) specification. Those skilled in the art will appreciate that the AMBA® specification is an industry-standard outlined by ARM®. In such embodiments, the interconnect system may be implemented using the AMBA® high-performance bus lite (AHB-Lite) protocol.

25 Certain embodiments of the invention will now be described, by way of example only, with reference to the accompanying drawings in which:

Fig. 1 shows a block diagram of a conventional interconnect system;

Fig. 2 shows a block diagram of a typical implementation of the interconnect system of Fig. 1;

30 Fig. 3 shows a block diagram of a interconnect system in accordance with an embodiment of the present invention; and

Fig. 4 shows the implementation of Fig. 2 when adapted to incorporate the interconnect system of Fig. 3.

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Fig. 1 shows a block diagram of a conventional interconnect system 1. The interconnect system comprises: a slave device 2; an arbiter 4; a multiplexer 5 and four master devices 6a, 6b, 6c, 6d. The multiplexer 5 is connected to each of the master devices 6a-d through respective connections A – D and to the slave 2.

5 While only one slave device is shown in Fig. 1, it will be appreciated that a typical interconnect system may have a plurality of slaves connected to it. The slave device 2 can only serve one master device 6a, 6b, 6c, 6d at a time. For each connection between a master device 6a, 6b, 6c, 6d and the slave device 2, there is a priority value 16a, 16b, 16c, 16d which is output from a respective priority output
10 9a, 9b, 9c, 9d provided on each of the master devices 6a, 6b, 6c, 6d respectively. Each of these priority values 16a, 16b, 16c, 16d is input to a priority input 8a, 8b, 8c, 8d provided on the arbiter 4. Each of the master devices 6a, 6b, 6c, 6d is also arranged to provide a request signal 18a, 18b, 18c, 18d to the arbiter 4 via respective request outputs 11a, 11b, 11c, 11d that are connected to respective
15 request inputs 10a, 10b, 10c, 10d of the arbiter 4. Each of these request signals 18a, 18b, 18c, 18d is typically a binary "1" if the respective master module 6a, 6b, 6c, 6d is requesting access to the slave device 2 and is a binary "0" if not.

In the first phase of a transaction (i.e. an exchange of data between the master
20 devices 6a, 6b, 6c, 6d and the slave device 2), the arbiter 4 grants access to the slave device 2 to the master device 6a, 6b, 6c, 6d having the highest priority value 16a, 16b, 16c, 16d of the master devices 6a, 6b, 6c, 6d that are currently indicating via their respective request signals 18a, 18b, 18c, 18d that they wish to access the slave device 2.

25 Once the arbiter 4 has determined which of the master devices 6a, 6b, 6c, 6d should be granted access to the slave device 2, the arbiter 4 outputs, via its selector output 12, a selection signal 13 which is provided to a multiplexer 5 which is part of the interconnect system and which utilises the selector signal 13 to permit
30 a connection 14 between the slave device 2 and the appropriate master device 6a, 6b, 6c, 6d.

Fig. 2 shows a functional block diagram of a typical implementation of the interconnect system of Fig. 1. The implementation shown in Fig. 2 is typical of the
35 ARM® Advanced Microcontroller Bus Architecture (AMBA®), an open standard

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interconnect specification for the connection of functional blocks in a system on chip (SoC) design. In this particular implementation, a processor 100 and peripheral devices 102 are arranged to access a set of eight random access memory (RAM) units 110a-h using the AMBA®3 AHB-Lite Protocol.

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The processor 100 comprises: a central processing unit (CPU) core 104 such as an ARM® Cortex® M4 processor core; a set of parallel bridges 106 such as AHB-AHB (or "AHB2AHB") bridges, one for each master; and an arbiter 108 for each slave. Each arbiter 108 is connected to its respective slave 110 by a signal/bus set 120.

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The peripherals 102 include a number of direct memory access (DMA) master devices 112. While shown as a single functional block for illustrative purposes, the peripherals 102 in this particular example include twenty DMA master devices 112. These DMA master devices 112 are connected to the bridges 106 via buses 118.

15

The bridges 106 serve to convert transactions from the master devices 112 which operate in a first clock domain at 16MHz to the 64MHz used in the second clock domain in which the RAM unit slaves 110 reside. Similarly the bridges 106 convert read data and response signals from 64MHz to 16MHz.. The bridges 106 are

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connected to the arbiter 108 via further buses 116, corresponding in number to the buses 118 between the DMA master devices 112 and the bridges 106. The arbiter 108 is also connected to the CPU core 104 via other buses 114. There may, by way of example only, be three buses from the core 104 to the each of the eight arbiters 108 and thus each of the arbiters 108 accepts twenty-three busses 114, 116. The eight arbiters 108 are arranged to determine which of the twenty-three

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master devices should be given access to the eight slave devices, i.e. the eight RAM units 110a-h.

Fig. 3 shows a block diagram of an interconnect system in accordance with an embodiment of the present invention. The interconnect system depicted in Fig. 3 comprises: a slave device 202; a number of master devices 206a-g; two multiplexers 205a, 205b and two arbiters 204a, 204b compared to the single multiplexer and arbiter in the interconnect system shown in Fig. 1. This creates a two-stage interconnect system. In the first stage, which may for example be in a 16 MHz clock domain, four of the master devices 206a-d are connected to the first arbiter 204a so that their priority outputs 209a-d and request outputs 211a-d are

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connected to the respective priority inputs 208a-d and request inputs 210a-d of the first arbiter 204a. The master devices 206a-d are also connected to the first multiplexer 205a by respective connections A-D.

5 The other three master devices 206e-g are in the second stage, which may be in a 64 MHz clock domain, connected to the second arbiter 204b. Similarly, their respective priority outputs 209e-g and request outputs 211e-g are connected to the corresponding priority inputs 208e-g and request inputs 210e-g of the second arbiter 204b. These master devices 206e-g are also connected to the second
10 multiplexer 205b by respective connections E-G. The first stage multiplexer 205a is connected to the second stage multiplexer 205b by a connection H.

The first arbiter 204a is arranged to determine which of the four master devices 206a-d connected to it has the highest priority value 216a-d of the master devices
15 206a-d having their respective request signals 218a-d set to binary '1'. The first arbiter 204a then outputs via its priority output 212a a priority signal 220 corresponding to the priority value of the master devices 206a-d which has the highest priority value. The priority signal 220 is input to the fourth priority input 208h of the second arbiter 204b. Along with this a request signal 222 is output from the
20 request output 224a of the first arbiter 204a to the request input 210h of the second arbiter. Each instance of a request signal 222, priority signal 220 and corresponding control signals and data passed over connection H between the two multiplexers 205a, 205b comprise a transaction. The priority value of these transactions going
25 between the first stage and the second stage can change from one transaction to the next.

In addition, the first arbiter 204a passes a selector signal 213a to the first multiplexer 205a. This allows the corresponding master 206a-d to be connected to the slave 202 once access has been granted.

30

The second arbiter 204b is arranged to determine which master device 206e-g connected to it and requesting access has the highest priority value 216e-g. However the second arbiter 204b also compares these priority values 216e-g with the priority value 220 provided to it by the first arbiter 204a. Thus, in effect, the
35 master device selected by the second arbiter 204a will be the master device with

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the highest priority value 216a-g of all seven of the master devices 206a-g which want to connect to the slave 202. The second arbiter 204b passes a selector signal 213b to the second multiplexer 205b. As previously described with reference to Fig. 1, this will enable a connection between the slave device 202 and the appropriate master device 206. In accordance with the AHB Lite protocol, this is achieved by the multiplexer 205b sending a 'ready' signal, if necessary via the first stage multiplexer 205a using the connection H, to the master device which has been granted access. Any other requesting master devices 206 will not get such a 'ready' signal and will thus have to wait.

Fig. 4 shows the implementation of Fig. 2 when adapted to incorporate the interconnect system of Fig. 3. When compared to the implementation shown in Fig. 2, it will be readily seen that the peripherals 302 now also include a set of eight arbiters 308a (one for each end RAM slave 310a-h) to which the DMA master devices 312 are connected via twenty buses 322. This set of arbiters 308a is each arranged to determine which of the twenty DMA master devices 312 have the highest priority for a given slave 310a-h and produce outputs accordingly. Each master device 312 can request access to any of the slaves 310a-h by means of the corresponding arbiter, although a master can only request access to one slave via one arbiter at a time. The outputs from the arbiters 308a are passed to the eight bridges 306 via eight buses 318. The number of buses 316 connecting the bridges 306 to the second set of arbiters 308b need only be the same as the number of buses 318 connecting the bridges 306 to the first set of arbiters 308a, thus only eight buses are required here. It will be appreciated that the second set of arbiters 308b need only compare inputs from eleven buses - the three outputs produced by the CPU core 304 plus the eight buses from the bridges 306 - compared to twenty three in the arrangement of Fig. 2. The second set of arbiters 308b produce signals indicating which of its eleven masters should be granted access to each of the eight independent RAM units 310a-h

The second set of arbiters 308b in this case do not have to compare the priority values of all twenty DMA master devices 312 and only eight bridges are required in this domain compared to twenty. This is particularly advantageous as the second set of arbiters 308b are in the faster clock domain when compared to the first set of arbiters 308a. This means that fewer logic gates and flip-flops are required in the

5 faster clock domain which reduces the overall power consumption and complexity of the circuit as a whole. The complexity of the circuit is reduced as fewer input/output (IO) ports are required on the interface between the processor 300 and the peripherals 302. This also reduces the number of time critical paths in the faster processor clock domain, providing the possibility of using higher clock frequencies within the processor 300 than with conventional interconnect systems. Moreover much of the requirement for multiplexing is moved from the fast to the slow clock domain which means that the power is further reduced as the additional arbiter is not activated by transactions from the processor.

10 Thus it will be seen that the present invention provides a multi-stage interconnect system that can be readily scaled for any number of slave devices and master devices. Interconnect systems in accordance with embodiments of the present invention provide user-programmable priority settings that are independent of the physical configuration of the interconnect system and uses transactions carrying the priority levels between the stages. It will be appreciated by those skilled in the art that the embodiments described hereinabove are merely exemplary and are not limiting on the scope of the invention.

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Claims:

1. A microprocessor comprising an interconnect system arranged to control access to a slave device, said interconnect system comprising:
 - 5 a plurality of first stage master devices, wherein each master device has a priority value for said slave associated therewith;
a first stage arbiter connected to said plurality of first stage master devices and arranged to: determine a first selected master device from the priority values of those of the first stage master devices wishing to connect to the slave; and produce
10 a transaction including the priority value associated with the first selected master device; and
a second stage arbiter connected to said first stage arbiter to receive said transaction and further connected to at least one second stage master device having a priority value for said slave associated therewith, said second arbiter being
15 arranged to: determine a second selected master device from the priority values of any second stage master device wishing to connect to the slave and the priority value of the transaction from the first stage arbiter.
2. The microprocessor as claimed in claim 1 wherein the first and second
20 arbiters are located in different clock domains having respective lower and higher frequencies.
3. The microprocessor as claimed in claim 2 wherein the first stage arbiter is located in the lower frequency clock domain and the second stage arbiter is located
25 in the higher frequency clock domain.
4. The microprocessor as claimed in any preceding claim wherein transactions originating from the first stage are always addressed to one particular slave.
- 30 5. The microprocessor as claimed in any preceding claim wherein the priority levels comprise a plurality of bits.
6. The microprocessor as claimed in any preceding claim wherein the second stage arbiter is arranged to produce a second transaction including the priority
35 value associated with the second selected master device, said transaction being

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passed to another system to effect the connection between said second selected master device and said slave device.

5 7. The microprocessor as claimed in any preceding claim wherein the first selected master device is determined to be the master device having the highest priority value associated therewith.

10 8. The microprocessor as claimed in any preceding claim wherein the second selected master device is determined to be the master device having the highest priority value associated therewith.

9. The microprocessor as claimed in any preceding claim wherein the slave device is connected to the second arbiter.

15 10. The microprocessor as claimed in any preceding claim wherein the interconnect system comprises more than two arbiters and the slave device is connected to a final arbiter, said final arbiter being an arbiter that does not produce a transaction with a priority value.

20 11. The microprocessor as claimed in any preceding claim wherein the priority value assigned for each master device for the slave is user-configurable.

25 12. The microprocessor as claimed in any preceding claim wherein at least some of the priority values are arranged to vary dynamically when said interconnect system is in use.

13. The microprocessor as claimed in any preceding claim wherein the interconnect system is arranged to control access to two or more slave devices.

30 14. The microprocessor as claimed in any preceding claim wherein only a subset of possible pairings of master devices and slave devices is permitted.

35 15. The microprocessor as claimed in any preceding claim wherein the interconnect system is implemented in accordance with the Advanced Microcontroller Bus Architecture specification.

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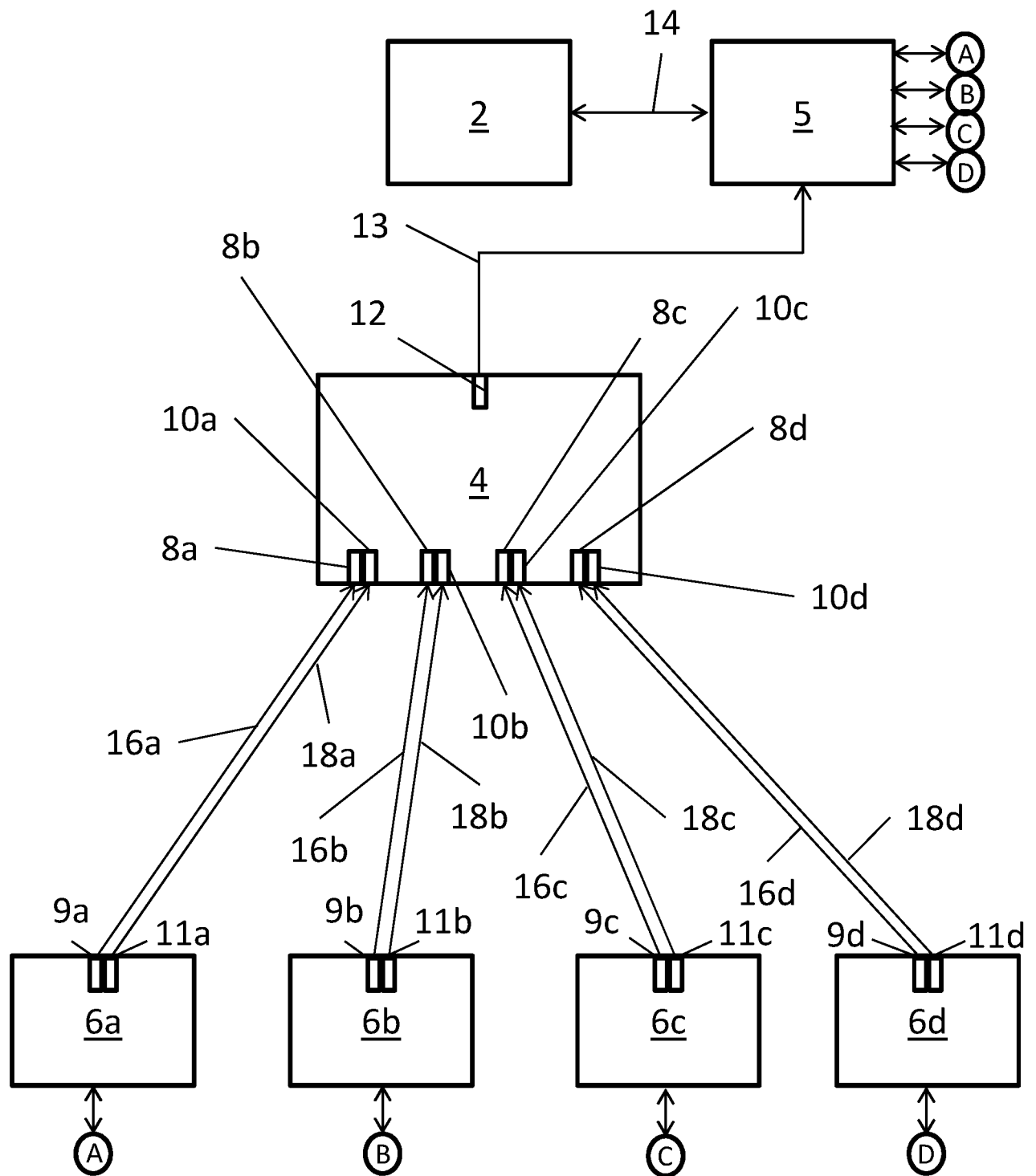


Fig. 1 Prior Art

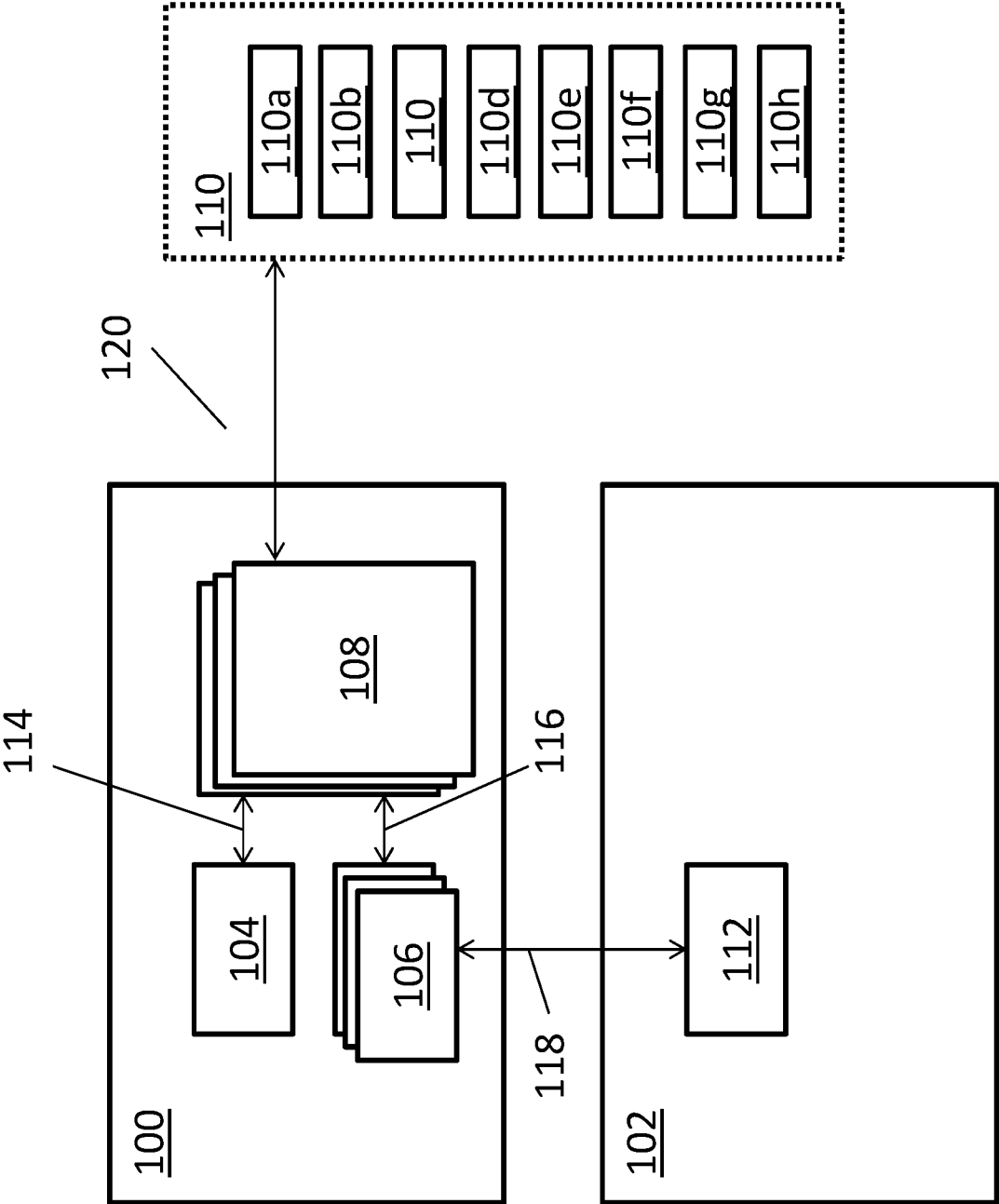
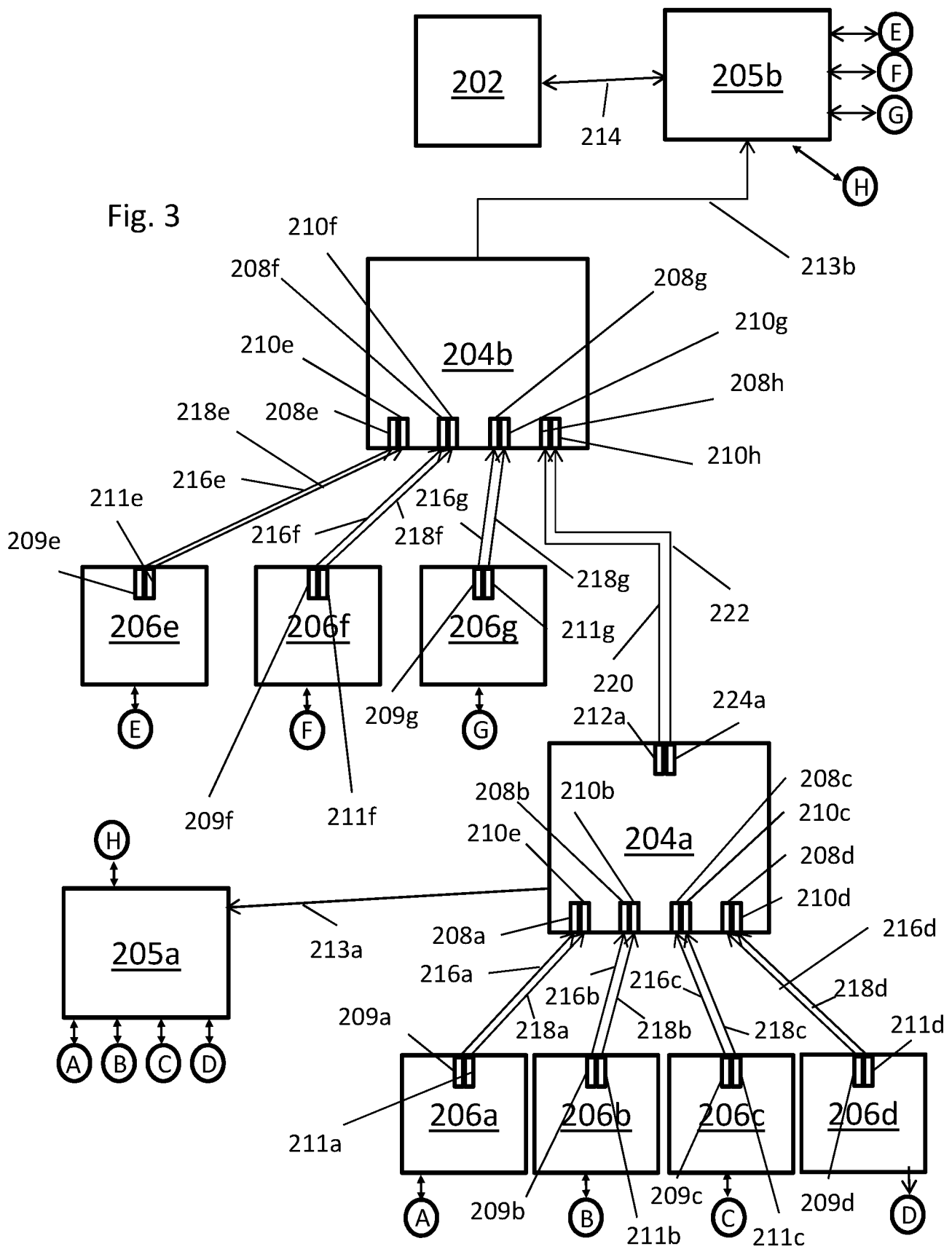


Fig. 2
Prior Art

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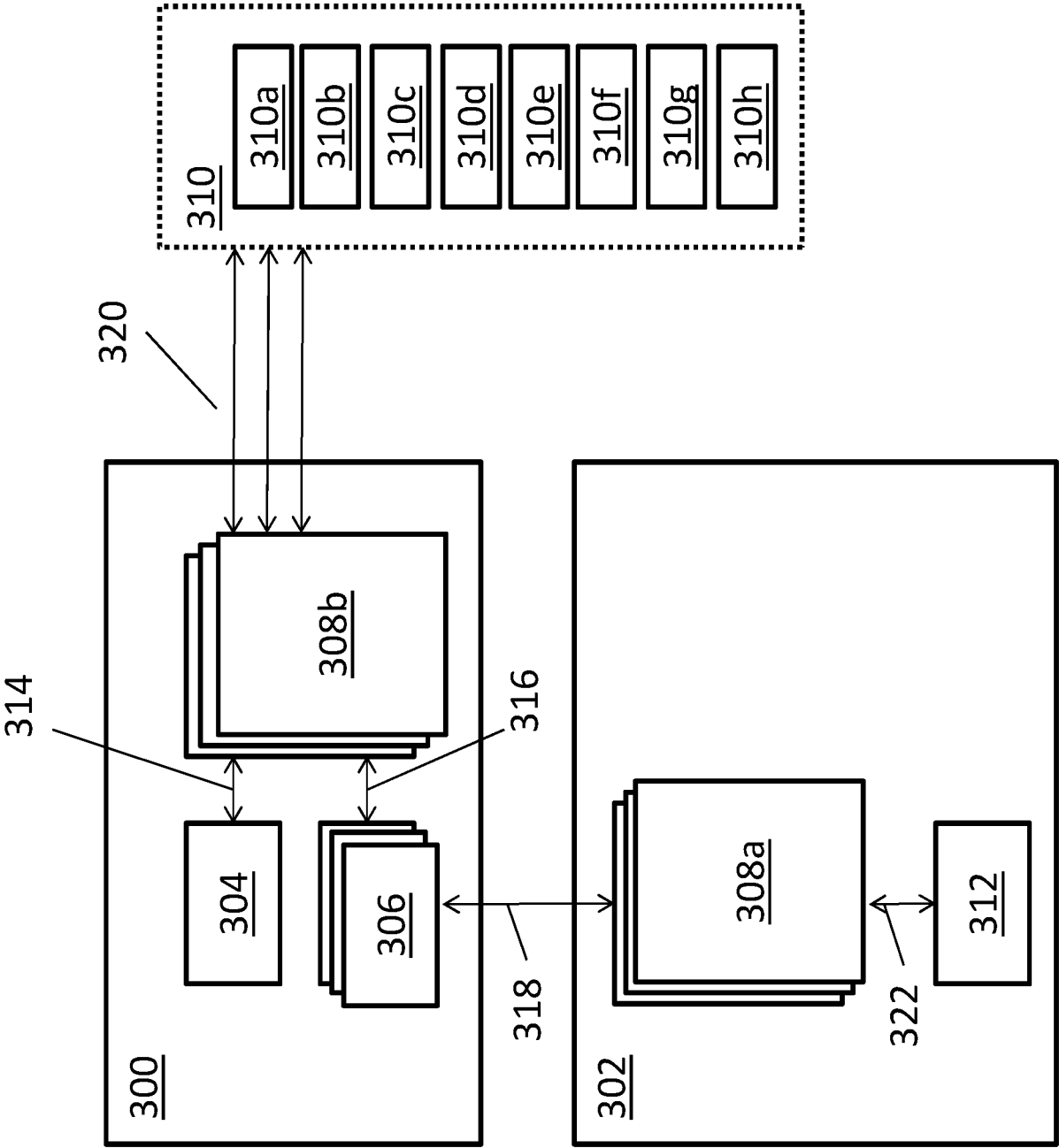


Fig. 4

INTERNATIONAL SEARCH REPORT

International application No
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A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F13/362
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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X A	US 2006/047873 A1 (BOSE BIJOY [US] ET AL) 2 March 2006 (2006-03-02) paragraph [0020] - paragraph [0061] figures 1-5	1,4-15 2,3
X A	US 2003/167294 A1 (NEUMAN DARREN [US]) 4 September 2003 (2003-09-04) paragraph [0004] - paragraph [0013] paragraph [0033] - paragraph [0047] paragraph [0079] - paragraph [0080] figure 8	1,4-15 2,3
X A	US 2008/059674 A1 (SHI JIAXIANG [SG] ET AL) 6 March 2008 (2008-03-06) paragraph [0017] - paragraph [0027] figures 1, 2	1,4-15 2,3
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Date of the actual completion of the international search

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22/02/2018

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Rudolph, Stefan

INTERNATIONAL SEARCH REPORT

International application No

PCT/GB2017/053609

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

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