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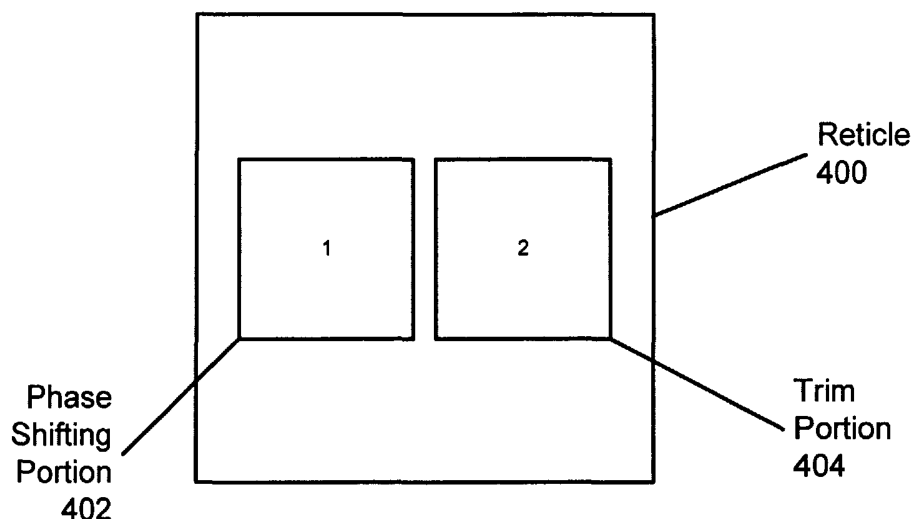

(57) Abstract: Mask and integrated circuit fabrication approaches are described to facilitate use of so called "full phase" masks. This facilitates use of masks where substantially all of a layout is defined using phase shifting. More specifically, exposure settings including relative dosing between the phase shift mask and the trim masks are described. Additionally, single reticle approaches for accommodating both masks are considered. In one embodiment, the phase shifting mask and the trim mask are exposed using the same exposure conditions, except for relative dosing. In another embodiment, the relative dosing between the phase and trim patterns is 1.0:r, 2.0< r <4.0. These approaches facilitate better exposure profiles for the resulting ICs and can thus improve chip yield and increase throughput by reducing the need to alter settings and/or switch reticles between exposures.

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EXPOSURE CONTROL FOR PHASE SHIFTING PHOTOLITHOGRAPHIC MASKS

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to manufacturing small dimension features of objects, such as integrated circuits, using photolithographic masks. More particularly, the present invention relates to the application of phase shift masking to complex layouts for integrated circuits and similar objects.

Description of Related Art

[0002] Phase shift masking has been applied to create small dimension features in integrated circuits. Typically the features have been limited to selected elements of the design, which have a small, critical dimension. See, for example, United States Patent No. 5,766,806.

[0003] Although manufacturing of small dimension features in integrated circuits has resulted in improved speed and performance, it is desirable to apply phase shift masking more extensively in the manufacturing of such devices. However, the extension of phase shift masking to more complex designs results in a large increase in the complexity of the mask layout problem. For example, when laying out phase shift windows on dense designs, phase conflicts will occur. One type of phase conflict is a location in the layout at which two phase shift windows having the same phase are laid out in proximity to a feature to be exposed by the masks, such as by overlapping of the phase shift windows intended for implementation of adjacent lines in the exposure pattern. If the phase shift windows have the same phase, then they do not result in the optical interference necessary to create the desired feature. Thus, it is necessary to prevent inadvertent layout of phase shift windows in phase conflict near features to be formed in the layer defined by the mask.

[0004] In the design of a single integrated circuit, millions of features may be laid out. The burden on data processing resources for iterative operations over such large numbers of features can be huge, and in some cases makes the iterative operation impractical. The layout of phase shift windows and the assignment phase shift values to

such windows, for circuits in which a significant amount of the layout is accomplished by phase shifting, is one such iterative operation which has been impractical using prior art techniques.

[0005] Another problem that is associated with the use of phase shift masking arises from the need for two different mask patterns for implementation of a layer of material having small dimension features. Existing systems expose the wafer using a binary mask pattern using a stepper having optical settings optimized for the binary mask pattern, and expose the wafer using the phase shift mask pattern using a stepper having optical settings optimized for the phase shift mask pattern. Typically, the optical settings are quite different. For example, a phase shift pattern is usually exposed using a highly coherent radiation source. However, binary masks achieve better results having less coherent radiation sources. Thus, between the two exposures, the wafer is required to sit while the settings and masks are changed within the stepper. During the time the wafer sits, the quality of the resist can degrade. Furthermore, the time involved in moving the wafer and adjusting a stepper slow down the manufacturing process. For background concerning optical lithography and the phase shift masking, see Wong, RESOLUTION ENHANCEMENT TECHNIQUES IN OPTICAL LITHOGRAPHY, SPIE Press, Bellingham, Washington (2001).

[0006] It is useful to understand the common stepper settings and parameters used in so called "gate shrink" phase shifting designs. A "gate shrink" design, or mask, is simply a layout, or mask, where significant portions of a pattern, usually field polysilicon, must still print properly using the corresponding binary trim mask, while portions such as transistor gates are formed using phase shifting, resulting in so-called "shrunk" gates.

[0007] Generally, phase shifting masks require a low partial coherence σ arrangement in the stepper, so that the light exposing the wafer is highly coherent.

[0008] In contrast, when working with a binary pattern on a mask that has densely packed and small features, high partial coherence σ stepper settings producing less coherent light, and/or off-axis-illumination (OAI), or other illumination configurations are employed.

[0009] For that reason, the binary trim pattern on a mask for a gate shrink-type design would commonly be exposed using low coherency (high σ) or off-axis illumination. But, the phase shifting pattern on a mask for such a gate shrink-type

design would use high coherency (low σ) illumination. This requires an adjustment of the projection system in the stepper, typically a change in size of an aperture, between the phase shifting pattern and trim pattern exposures.

[0010] Because of these and other complexities, implementation of a phase shift masking technology for complex designs will require improvements in the approach to the design of phase shift masks.

SUMMARY OF THE INVENTION

[0011] Mask and integrated circuit fabrication approaches are described to facilitate use of so called "full phase shift" masks, where substantially all of a layout is defined using phase shifting. Definitions of other patterns, layouts, and mask types for which the invention is suitable are described below.

[0012] For the masks used by embodiments of the invention, the optical settings of a stepper are maintained constant, except for dosing in some embodiments, between exposure with the phase shifting pattern and the binary trim pattern. Optical settings that are not changed between the exposures of the phase shifting and trim patterns include one or more members of a set of optical parameters including numerical aperture (N.A.), wavelength (λ) of light, coherency (such as measured by partial coherence σ), illumination configuration (single spot source, dipole source, quadrapole source, annular source), axis of illumination, and defocus, in various combinations.

[0013] In various embodiments, the relative dosing between the exposure of the phase shifting pattern and the trim pattern is expressed by a ratio $1.0{:}r$, where $r > 0.0$. In some embodiments, $2.0 < r < 4.0$, so that the exposure dosing of the binary pattern is from 2 to 4 times greater than the dosing of the phase shifting pattern. One embodiment uses a 1:2 ratio, another a 1:3 ratio. The greater exposure of the trim pattern facilitates clearing of cuts, or openings, while preventing exposure of the features defined by the phase shifting pattern. In some embodiments, r is determined from simulation results for a particular optical lithography model, e.g. stepper, wavelength, resist measurements, etc.

[0014] Additionally, both patterns are provided on a single reticle in one embodiment of the present invention. A single reticle with multiple patterns can increase mask manufacturing costs. However, the cost of the mask is justified because the use of the single reticle can improve yield, and save manufacturing steps and time.

A multiple pattern reticle can allow more rapid exposure of the layer of material using both the phase shifting pattern and the trim pattern. The layout of patterns on the single reticle can be simple (one of each) or more complex (multiple phase patterns; multiple binary patterns; one-dimensional; two-dimensional; etc.) The dosing ratio r for a layer to be exposed can be implemented, for example using constant exposure doses to each pattern with the ratio of the number of phase shifting patterns and to the number of trim patterns on the mask set equal to the dosage ratio $1.0{:}r$. In this example, the exposure dosage is another parameter that is not changed between exposures of the phase shift and trim patterns.

[0015] A method for manufacturing an integrated circuit is provided according to the present invention, which includes forming a layer of resist on a semiconductor wafer, moving the wafer to a stepper system including a radiation source and a reticle having a phase shifting pattern and a trim pattern; positioning the wafer and the reticle for exposure of a phase shifting pattern in the reticle; applying a dose of radiation to the wafer through the phase shifting pattern using stepper settings including a set of optical parameters including numerical aperture (N.A.), wavelength (λ) of light, coherency (such as measured by partial coherence σ), illumination configuration (single spot source, dipole source, quadrapole source, annular source), axis of illumination, and defocus; positioning the wafer and the reticle for exposure of a trim pattern in the reticle; applying a dose of radiation to the wafer through the trim pattern using stepper settings including said set of parameters for the trim exposure, wherein all or some of the members of said set of parameters are substantially the same as those used for the phase shifting exposure. The phase shifting and trim patterns may be exposed in any order that results in the die on the wafer being exposed using both, and receiving proper dosages of radiation for the phase shifting and trim patterns. After exposing both patterns, the wafer is removed from the stepper, and available for subsequent steps to complete the integrated circuit. Then, the stepper is available for a next wafer in the line.

[0016] In one embodiment, all of said stepper settings are the same, in the sense that the stepper settings are not altered, or in other embodiments, settings of parameters that involve changing or moving an optical device such as an aperture stop setting or a lens position are not changed, between the phase shifting and trim exposures. In some embodiments, one reticle carries the phase shifting pattern and another carries the trim

pattern, and the steps of positioning the reticle and the wafer include selecting the appropriate reticle.

[0017] In one embodiment, after exposing both patterns, the photoresist is developed, and the resulting pattern of developed photoresist is used for formation of a layer of polysilicon on the wafer, including elements of circuits being formed thereon. Such elements include transistor gates, interconnect structures, and the like.

[0018] Resulting ICs produced according to embodiments of the invention can include a large number of subwavelength features due to the use of phase shifting and those features will tend to be extremely well defined because of the high quality energy profile achieved, and the ability to rapidly develop the photoresist by using embodiments of the invention (shorter and more uniform time intervals between exposures; fewer mistakes in lithography settings, fewer mistakes in optical settings; etc.)

BRIEF DESCRIPTION OF THE FIGURES

[0019] Fig. 1 illustrates a pattern of features and phase shift regions for defining those features.

[0020] Fig. 2 illustrates a simulated exposure of the layout of Fig. 1 according to a 1:2 dosage ratio between the phase shifting mask and the trim mask.

[0021] Fig. 3 illustrates a simulated exposure of the layout of Fig. 1 according to a 1:1 dosage ration between the phase shifting mask and the trim mask.

[0022] Fig. 4 illustrates a single reticle having both a phase shifting and trim patterns.

[0023] Fig. 5 illustrates a portion of a wafer after a first exposure by the reticle of Fig. 4.

[0024] Fig. 6 illustrates the wafer of Fig. 5 after a second exposure by the reticle of Fig. 4.

[0025] Fig. 7 illustrates a portion of a wafer after a first exposure by the reticle of Fig. 4 with blading.

[0026] Fig. 8 illustrates the wafer of Fig. 7 after a second exposure by the reticle of Fig. 4 with blading.

[0027] Fig. 9 illustrates a single reticle having phase shifting pattern and two trim patterns.

[0028] Fig. 10 illustrates a portion of a wafer after a first exposure by the reticle of Fig. 9.

[0029] Fig. 11 illustrates a portion of a wafer after a second exposure by the reticle of Fig. 9.

5 **[0030]** Fig. 12 illustrates a portion of a wafer after a third exposure by the reticle of Fig. 9.

DETAILED DESCRIPTION

Overview

10 **[0031]** First, exposure settings for use in conjunction with phase shifting masks that produce substantial portions of a pattern of a layer on an integrated circuit (IC) using phase shifting will be considered. Next, relative dosing considerations between the phase shifting pattern exposure and the binary, trim pattern exposure will be considered. Finally, approaches for using a single reticle in the production of ICs using phase 15 shifting will be considered. (As used herein, the terms "mask" and "reticle" are synonyms, generally referring to a device carrying patterns, also called layouts, for photolithographic exposure used in manufacture of semiconductor wafers or other workpieces.)

20 ### Exposure Settings

[0032] In one embodiment of the invention, an optical lithography exposure system, generally referred to as a stepper, has a setting of members of a set of one or more optical parameters that control characteristics of exposures, the settings used to expose the phase shifting pattern and the complementary trim pattern used to produce an IC 25 using phase shifting are unchanged, or otherwise kept substantially the same, between the exposures. This is applied for example when all, or substantially all portions, of a pattern are being defined using a phase shifting pattern on a mask, because there is minimal need to print small features using the trim pattern. Thus the trim pattern consists of features that have greater design latitude in exposure settings that do the 30 features formed using the phase shifting pattern, and can be exposed with key optical settings such as one or more members of a set of optical parameters including numerical aperture (N.A.), wavelength (λ) of light, coherency (such as measured by partial

coherence σ), illumination configuration (single spot source, dipole source, quadrapole source, annular source), axis of illumination, and defocus, in various combinations.

[0033] Masks having a phase shift pattern that results in all, or substantially all portions, of a pattern on the layer of material being exposed being defined using the phase shifting pattern, are sometimes referred to as "full phase" masks. In one embodiment, the masks are defined according to the process described in United States Patent Application Serial No. 09/932,239 filed 16 Aug 2001, entitled "Phase Conflict Resolution for Photolithographic Masks" having inventors Christophe Pierrat and Michel Côté; and assigned to the assignee of the present invention, which is incorporated herein by reference as if fully set forth herein.

[0034] In another embodiment, a phase shifting mask that produces substantial portions of a pattern of an IC using phase shifting comprises a phase shifting pattern on the mask where substantially all features for a particular layer are defined using phase shifting. In another embodiment, a phase shifting mask that produces substantial portions of a pattern of an IC using phase shifting comprises a pattern on a mask such that only features that are non-critical for the binary exposure are non-phase shifted. In such an embodiment, a non-critical feature is a feature where there is greater latitude in critical dimension control such that when the non-critical feature is exposed according to the conditions more fully described below the resulting critical dimension variances are acceptable.

[0035] In other embodiments, the relevant layout comprises a layout where phase shifting is used to define at least one of:

- eighty percent (80%) of non-memory portions in one layer of material in the layout;
- eighty percent (80%) of a part of the floorplan in one layer of material;
- eighty percent (80%) of cells in a given area;
- ninety percent (90%) of a layer of material;
- ninety five percent (95%) of a layer of material;
- ninety nine percent (99%) of a layer of material;
- one hundred percent (100%) of a layer of material;
- one hundred percent (100%) of a in a functional unit of the chip (e.g. ALU) in one layer of material;

- one hundred percent (100%) of features in a layer of material that are in the critical path of the design;
- one hundred percent (100%) of features in a layer of material above or below certain dimensions, e.g. all features with a critical dimension 50 μm < CD < 100 μm;
- everything in a layer of material except those features that cannot be phase shifted due to phase conflicts that cannot be resolved;
- everything in a layer of material except test structures; and
- one hundred percent (100%) of all non-dummy features, e.g. features providing structural support for processing purposes, and non-electrically functional features in a layer of material.

[0036] By maintaining a high coherency illumination setting (low partial coherence σ) for both the phase shifting and binary trim pattern on a mask, it is possible to more quickly, and accurately, produce ICs where all or substantially of the pattern features are defined using phase shifting. In one embodiment, the percentages are determined based on the number of edges, or edge segments, within the pattern defined using phase shifting.

[0037] In one embodiment, one or more of the numerical aperture (NA) of the radiation exposing the wafer, the coherency setting (σ), the illumination configuration (on/off axis, dipole, quadrapole, annular, etc.), and defocus are kept unchanged between the phase shifting and trim exposures. In one embodiment, all optical settings that require mechanical adjustment of items in the optical path to change, such as an aperture stop setting, or a lens position, are left unchanged between the phase shifting and trim pattern exposures.

[0038] In one embodiment, keeping the stepper settings unchanged facilitates the use of the single reticle approach described below. In another embodiment, keeping the stepper settings unchanged facilitates the use of a single stepper for exposure of both the phase shifting pattern and the corresponding trim pattern, whether such patterns are on the same mask or on separate masks.

<u>Dosing</u>

[0039] Turning to Fig. 1, a pattern of features and phase shift regions for defining those features is shown. The phase shifting design shown in Fig. 1 was manually

defined. The pattern includes the feature 100 and the feature 102. Of interest is the proximity of the end cap of the feature 100 with the top edge of the feature 102. The phase shift regions have been defined with the shifter 104, the shifter 106, the shifter 108, and the shifter 110. Here, the shifter 106 and the shifter 110 share a single phase, e.g. 0, as do the shifter 104 and the shifter 108, e.g. π.

[0040] Turning to Fig. 2 and Fig. 3, simulation results for the pattern of Fig. 1 are shown with stepper settings maintained constant, but the relative dosing between pattern exposures changed. Fig. 2 shows a simulation output 200 where the relative dosing between the phase shift pattern and the corresponding trim pattern was 1:2 ($r = 2$). Fig. 3 shows a simulation output 300 where the relative dosing was 1:1 ($r = 1$).

[0041] Looking more closely at the simulation output 200 and the simulation output 300, the outputs include black contour lines (contour line 202, contour line 204, contour line 302, and contour line 304) that indicate where the feature 100 and the feature 102 will print. As can be seen from the figure, with a 1:1 ratio, Fig. 3, the end cap of the feature 100 and the edge of the feature 102 come extremely close. In contrast, with a 1:2 ratio, Fig. 2, the end cap and edge are better defined, and therefore less likely to improperly print as a single connected feature.

[0042] More generally, higher values of r in the ratio 1.0:r, where $r > 1.0$ are useful in printing ICs when phase shifting masks of the type discussed here are used. In one embodiment, $2.0 < r < 4.0$. In another embodiment, a 1:3 ratio is used. Most generally, r can have a real numbered value as the stepper/scanner exposure setting will be set in an absolute number of millijoules per square centimeter per exposure, e.g. 10 mJ/cm^2 and 20mJ/cm^2, etc.

[0043] In some embodiments, one or more simulations are performed using the actual and/or test layouts to select r for a particular optical/stepper model. However, the selected ratio reflects a balance between "hard" or over exposure for cut regions (necessary and desirable) versus exposure of areas under the trim (undesirable).

Single Reticle

[0044] Fig. 4 illustrates a single reticle having both a phase shifting and trim patterns. In this example, the reticle 400 includes a phase shifting pattern 402 and a trim pattern 404. The phase shifting pattern 402 shows a pattern "1" and the trim

pattern 404 a pattern "2" for convenience of explanation of the wafer exposures described below.

[0045] The phase shifting pattern 402 and the trim pattern 404 are separated by a small gap. In some embodiments, the gap is dependent on the blading capabilities and accuracy for the stepper. In one embodiment, the separation is 5 mm.

[0046] A given stepper/scanner system will have a usable area of a mask, e.g. an *n* by *m* millimeter field. Thus, the number of mask patterns that can be accommodated on a single reticle will depend on the size of the design and the usable reticle area.

[0047] In one approach, the dosing will be maintained at equal levels for the trim and binary exposures. Turning to Fig. 5, a wafer 500 is shown after the first exposure. The wafer 500 has the alternating 1-2 pattern caused by the exposure of some regions to the phase shifting pattern and the exposure of other regions to the trim pattern 404. A second exposure, shown in Fig. 6, of the wafer 500 completes the process once the reticle and/or wafer has been repositioned within the stepper. Fig. 6 illustrates the pattern as 12 or 21 depending on the order of exposure for a region.

[0048] In another approach, dosing can be at a user selected ratio, e.g. 1.0:*r*, between patterns through the use of blading. By blading, or covering, one region of the reticle 400, an exposure of the type shown in Fig. 7 on a wafer 700 will result after all of the fields on the wafer are exposed. A second exposure after repositioning the reticle and/or wafer in the stepper is shown in Fig. 8 where the exposure with the phase shifting pattern 402 is complete. The blades could then be adjusted to cover the other patterns of the reticle and allow exposures to be made with the trim pattern 404 exposing the wafer.

[0049] Fig. 9 illustrates a single reticle having phase shifting pattern and two trim patterns. In this example, the reticle 900 includes a phase shifting pattern 902, a trim pattern 904 and a trim pattern 906. In this embodiment, the trim pattern 904 and the trim pattern 906 are designed to produce the same pattern. Accordingly, by triple exposing the wafer a 1:2 dosing ration between the phase shifting pattern and the trim patterns can be accomplished. The results are depicted in Figs. 10-12 showing a portion of the wafer after the first exposure 1000, after the second exposure 1100, and after the third exposure 1200, respectively.

[0050] More complex reticle patterns are possible. For example, two phase shifting patterns could be used, e.g. with one phase shifting pattern having structures in one

orientation and another pattern with structures in another orientation. In other embodiments, a two-dimensional pattern of the mask patterns on the reticle is used.

[0051] The present invention also provides method for manufacturing an integrated circuit. Method includes forming a layer of resist on a wafer at a first process station. The resist is cured and prepared for exposure using a stepper or scanner. The wafer with a layer of resist is transported to the stepper. The stepper includes a radiation source, a mask and an optical path for exposing the wafer to radiation. The optical path is characterized by a set of optical parameters including one or more of a wavelength λ of illumination, numerical aperture NA, coherency, illumination configuration and defocus. In the stepper, the layer of resist is exposed to a first dosing radiation to a phase shifting pattern in said mask using a first setting of the set of optical parameters. Next, the layer of resist is exposed to a second dose of radiation through the trim pattern in said mask using said first setting. Thus, the setting of the optical parameters is not changed between the exposures of the phase shift pattern and the trim pattern. As mentioned above, the mask may have more than one trim pattern and more than one phase shift pattern implemented thereon. In this case, the wafer may be subject to additional exposure steps, in which the settings of the optical parameters are not changed. The order of exposure of the phase shift pattern or patterns and trim pattern or patterns can be changed as suits a particular processing situation.

[0052] As can be seen, according to this process both the phase shift and trim exposures are carried out in the same stepper, using the same settings. Thus, the wafer does not wait for changing of optical parameters, or to be moved from one stepper to the next, between exposures. This reduces the possibility for error in manufacturing of the device, and reduces the time required to complete the exposure step.

[0053] After the exposure, the resist is developed using the techniques that are adapted for use with a particular resist involved. A pattern is left on the wafer which is used for a deposition and/or etching step to form of features an integrated circuit. For example, the pattern may be used for etching an underlying layer of polysilicon to form interconnect, gate, capacitor, resistor and other circuit features on integrated circuit.

Process Advantages

[0054] Maintaining the stepper settings as a constant can significantly improve throughput as well as lead to better critical dimension uniformity. Accordingly, if too

much time passes between the first exposure and the second exposure and/or the amount of time is not maintained constant the results may be poorer than expected.

[0055] More specifically, current generation photoresist materials are chemically amplified so that exposure to light produces a very small number of acid molecules, that then continue to react. The passage of time and exposure to air may cause carbon dioxide, and other chemicals, to take up the acid and neutralize it. Using the single reticle approach, the photoresist should maintain its properties throughout both exposures and the timing between exposures can be shorter and more closely controlled the effect of exposure. Additionally, over time, the acid diffuses into the polymer.

[0056] The better effects from different dosing can be implemented while maintaining other stepper settings constant.

[0057] The increased throughput and yield possible should readily make up for the increase in reticle costs; although, the cost should be comparable, or less than, the cost of a dual reticle approach using separate masks for phase shifting and binary patterns.

Representative Alternative Embodiments

[0058] Additionally, although the description has primarily focused on examples of defining a polysilicon, or "poly", layer within an IC, phase shifting can be used to define other layers of material.

[0059] Some embodiments of the invention include computer programs for simulating stepper exposures using phase shift and trim patterns to compute appropriate relative dosing between phase and trim/binary exposures. In one embodiment, the ICWorkbench(TM) software produced by Numerical Technologies, Inc., San Jose, California is used to simulate the exposure conditions, e.g. as seen in Figs. 2-3. In other embodiments, computer programs are used to develop a pattern of layouts on a single reticle and a corresponding exposure pattern for exposure of wafers by the reticle.

[0060] As used herein, the term optical lithography refers processes that include the use of visible, ultraviolet, deep ultraviolet, extreme ultraviolet, x-ray, and other radiation sources for lithography purposes.

Conclusion

[0061] The foregoing description of embodiments of the invention has been provided for the purposes of illustration and description. It is not intended to be

exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations will be apparent. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, thereby enabling others to understand the invention for various embodiments and with various
5 modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the following claims.

[0062] What is claimed is:

CLAIMS

1. A method of fabricating a layer of material in an integrated circuit (IC), the layer including a pattern, the layer defined by a layout data, the method comprising:

5 analyzing the layout data to determine whether substantial portions of the pattern are to be defined using a phase shifting pattern; and

responsive to the analyzing, configuring an optical lithography exposure system to have a setting of a set of one or more optical parameters that control characteristics of exposures, to expose at least a first mask pattern and a second mask pattern for use in 10 defining the layer of material to use said setting for exposing each mask pattern, and wherein the first mask pattern comprises an alternating aperture phase shifting pattern and wherein the second mask pattern comprises a trim pattern.

2. The method of claim 1, wherein the analyzing comprises determining if all of the pattern on the layer is defined using phase shifting.

15 3. The method of claim 1, wherein the layout data comprises a "full phase" design such that the first mask pattern comprises a "full phase" mask pattern.

4. The method of claim 1, wherein the analyzing comprises determining if one or more of all of the pattern is defined using phase shifting, wherein a pattern is exposed on the layer which can be characterized by one or more of the following: at least eighty 20 percent (80%) of the non-memory portions of the pattern are defined by the phase shift pattern; at least eighty percent (80%) of a part of the floorplan in the pattern is defined by the phase shift pattern; at least ninety percent (90%) of the pattern is defined by the phase shift pattern; all of the features in the critical path of the pattern are defined by the phase shift pattern; all features in the pattern except those features that are not phase 25 shifted due to phase conflicts are defined by the phase shift pattern; everything in the pattern except test structures are defined by the phase shift pattern; and everything in the pattern except dummy structures are defined by the phase shift pattern.

5. The method of claim 1, wherein a pattern is exposed on the layer which can be characterized by having at least ninety-five (95%) of the pattern defined by the phase 30 shift pattern.

6. The method of claim 1, wherein the optical lithography exposure system comprises at least one of a stepper and a scanner.

7. The method of claim 1, wherein the first mask pattern and the second mask pattern are on a single reticle.

8. The method of claim 1, wherein said set of optical parameters consists of the numerical aperture (N.A.), wavelength (λ) of radiation, partial coherency (σ),
5 illumination configuration, and defocus.

9. The method of claim 1, wherein said set of optical parameters comprise one or more of the numerical aperture (N.A.), wavelength (λ) of radiation, partial coherency (σ), illumination configuration, and defocus.

10. The method of claim 1, further comprising exposing the layer of material in the
10 optical lithography exposure system using a first dosing for the first mask pattern and a second dosing for the second mask pattern, the first dosing and the second dosing in a ratio of 1.0 to r, $r > 0.0$.

11. The method of claim 10, wherein $2.0 <= r <= 4.0$.

12. The method of claim 10, wherein the first mask pattern and the second mask
15 pattern are on a single reticle.

13. The method of claim 12, wherein the exposing further comprises blading the first mask pattern and second mask pattern during the exposing to permit different dosing.

14. The method of claim 12, and wherein the single reticle further includes a second
20 instance of the second mask pattern and wherein the exposing comprises exposing the layer of material to the single reticle in a pattern to cause a 1:2 exposure ratio between the first mask pattern and instances of the second mask patterns.

15. A reticle for use in defining a pattern in a layer of material of an integrated circuit (IC) production using optical lithography in an optical lithography exposure
25 system having a set of one or more optical parameters that control characteristics of exposures, the reticle for defining a layer of material in an IC, the reticle comprising at least two patterns:

a first pattern comprising a phase shifting mask; and

a second pattern comprising a trim mask,

30 the first pattern defining a sufficient amount of the layer of material using phase shifting to allow the use of substantially the same settings of said set of one or more optical parameters for both the first pattern and the second pattern.

16. The reticle of claim 15, wherein a pattern is exposed on the layer which can be characterized by one or more of the following: at least eighty percent (80%) of the non-memory portions of the pattern are defined by the phase shift pattern; at least eighty percent (80%) of a part of the floorplan in the pattern is defined by the phase shift pattern; at least ninety percent (90%) of the pattern is defined by the phase shift pattern; all of the features in the critical path of the pattern are defined by the phase shift pattern; all features in the pattern except those features that are not phase shifted due to phase conflicts are defined by the phase shift pattern; everything in the pattern except test structures are defined by the phase shift pattern; and everything in the pattern except dummy structures are defined by the phase shift pattern.

17. The reticle of claim 15, wherein a pattern is exposed on the layer which can be characterized by having at least ninety-five (95%) of the pattern defined by the phase shift pattern.

18. The reticle of claim 15, wherein said set of optical parameters consists of the numerical aperture (N.A.), wavelength (λ) of radiation, partial coherency (σ), illumination configuration, and defocus.

19. The reticle of claim 1, wherein said set of optical parameters comprise one or more of the numerical aperture (N.A.), wavelength (λ) of radiation, partial coherency (σ), illumination configuration, and defocus.

20. The method of claim 15, wherein substantially the same comprises within plus or minus 10%.

21. The reticle of claim 15, wherein the reticle further includes a third pattern substantially identical to the second pattern, such that the layer defined by a triple exposure comprising one exposure by the first pattern, one exposure by the second pattern, and a third exposure by the third pattern.

22. The reticle of claim 15, wherein the reticle further includes a third pattern comprising a phase shifting pattern, and wherein the first pattern for defining features oriented in a first direction in the pattern and the third pattern for defining oriented in a second direction features in the pattern, such that the layer defined by a triple exposure comprising one exposure by the first pattern, one exposure by the second pattern, and a third exposure by the third pattern.

23. An method of manufacturing an integrated circuit (IC) product comprising:

defining at least one layer of material in the IC using at least two mask patterns, the layer of material comprising a pattern, the first mask pattern comprising a phase shifting pattern and the second mask pattern comprising a trim pattern, the first pattern defining substantially all of the pattern of the layer of material and the second pattern
5 for protecting the pattern and clearing phase shifting artifacts;

exposing layer of material in an optical lithography exposure system having a setting of a set of one or more optical parameters that control characteristics of exposures, to the first mask pattern and the second mask pattern, where said setting is substantially the same while exposing the first and second mask patterns.

10 24. The method of manufacturing an IC product of claim 23, wherein the first mask pattern comprises a "full phase" mask.

The method of manufacturing an IC product of claim 0, wherein the pattern on the layer of material can be characterized by one or more of the following: at least eighty percent (80%) of the non-memory portions of the pattern are defined by the
15 phase shift pattern; at least eighty percent (80%) of a part of the floorplan in the pattern is defined by the phase shift pattern; at least ninety percent (90%) of the pattern is defined by the phase shift pattern; all of the features in the critical path of the pattern are defined by the phase shift pattern; all features in the pattern except those features that are not phase shifted due to phase conflicts are defined by the phase shift pattern;
20 everything in the pattern except test structures are defined by the phase shift pattern; and everything in the pattern except dummy structures are defined by the phase shift pattern.

25. The method of manufacturing an IC product of claim 23, wherein the pattern on the layer of material can be characterized by having at least ninety-five (95%) of the pattern defined by the phase shift pattern.

25 26. The method of manufacturing an IC product of claim 23, wherein the optical lithography exposure system comprises at least one of a stepper and a scanner.

27. The method of manufacturing an IC product of claim 23, wherein the first mask pattern and the second mask pattern are on a single reticle.

28. The method of manufacturing an IC product of claim 23, wherein said set of
30 optical parameters consists of the numerical aperture (N.A.), wavelength (λ) of radiation, partial coherency (σ), illumination configuration, and defocus.

29. The method of manufacturing an IC product of claim 23, wherein said set of optical parameters comprise one or more of the numerical aperture (N.A.), wavelength (λ) of radiation, partial coherency (σ), illumination configuration, and defocus.

30. The method of manufacturing an IC product of manufacturing an IC product of
5 claim 23, wherein substantially the same comprises within plus or minus 10%.

31. The method of manufacturing an IC product of claim 23, wherein the exposing further comprises using a first dosing for the first mask pattern and a second dosing for the second mask pattern, the first dosing and the second dosing in a ratio of 1.0 to r, $r >$ 0.0.

10 32. The method of manufacturing an IC product of claim 31, wherein $2.0 <= r <=$ 4.0.

33. The method of manufacturing an IC product of claim 23, wherein the first mask pattern and the second mask pattern are on a single reticle.

34. The method of manufacturing an IC product of claim 33, and wherein the
15 exposing further comprises blading the first mask pattern and second mask pattern on the reticle during the exposing to permit different dosing.

35. The method of manufacturing an IC product of claim 33, and wherein the single reticle further includes a second instance of the second mask pattern and wherein the exposing comprises exposing the layer of material to the instances of the mask patterns
20 on the single reticle in a sequence to cause a 1:2 exposure ratio between the first mask patterns and instances of the second mask pattern.

36. A method for manufacturing an integrated circuit, comprising:

forming a layer of resist on a wafer;

exposing the layer to a first dose of radiation through a phase shifting pattern in
25 a mask, the radiation characterized by set of one or more parameters selected for exposure of the phase shifting pattern; and

exposing the layer to a second dose of radiation through a trim pattern in a mask, the radiation characterized by said set of parameters.

37. The method of claim 36, wherein said set of parameters includes a parameter
30 indicating partial coherence σ of the radiation at the layer.

38. The method of claim 36, wherein said set of parameters includes a parameter indicating the numerical aperture NA of the radiation at the layer.

39. The method of claim 36, wherein said set of parameters includes a parameter indicating an axis of propagation of the radiation at the layer.

40. The method of claim 36, wherein said set of parameters includes a parameter indicating an illumination configuration of the radiation.

5 41. The method of claim 36, wherein said set of parameters includes a parameter indicating defocus of the radiation at the layer.

42. The method of claim 36, wherein said set of parameters includes parameters indicating numerical aperture NA of the radiation at the layer, partial coherence σ of the radiation at the layer, an axis of propagation of the radiation at the layer, an illumination

10 configuration of the radiation, and defocus of the radiation at the layer.

43. The method of claim 36, wherein said first dose and said second dose are different.

44. The method of claim 36, wherein said phase shift pattern and said trim pattern are on a single mask.

15 45. The method of claim 36, wherein a pattern is exposed on the layer which can be characterized by one or more of the following: at least eighty percent (80%) of the non-memory portions of the pattern are defined by the phase shift pattern; at least eighty percent (80%) of a part of the floorplan in the pattern is defined by the phase shift pattern; at least ninety percent (90%) of the pattern is defined by the phase shift pattern;

20 all of the features in the critical path of the pattern are defined by the phase shift pattern; all features in the pattern except those features that are not phase shifted due to phase conflicts are defined by the phase shift pattern; everything in the pattern except test structures are defined by the phase shift pattern; and everything in the pattern except dummy structures are defined by the phase shift pattern.

25 46. The method of claim 36, wherein a pattern is exposed on the layer which can be characterized by having at least ninety-five (95%) of the pattern defined by the phase shift pattern.

47. The method of claim 36, wherein said set of parameters comprises parameters that are changed by a mechanical adjustment of an optical element.

30 48. A method for manufacturing an integrated circuit, comprising:

forming a layer of resist on a wafer in a first process station;

moving the wafer to a second process station including a radiation source, a mask and an optical path for exposing the wafer to radiation, the optical path being

characterized by a set of optical parameters including one or more of a wavelength λ of illumination, numerical aperture NA, coherence, illumination configuration, and defocus;

exposing, in the second process station, the layer to a first dose of radiation through a phase shifting pattern in said mask using a first setting of set of optical parameters; and

exposing, in the second process station, the layer to a second dose of radiation through a trim pattern in said mask using said first setting.

49. The method of claim 48, wherein said set of optical parameters includes the numerical aperture and partial coherence σ.

50. The method of claim 48, wherein said set of optical parameters includes the numerical aperture NA, partial coherence σ, the illumination configuration, and the defocus.

51. The method of claim 48, wherein said set of optical parameters includes partial coherence σ as the coherence parameter.

52. The method of claim 48, wherein said first dose and said second dose have different dosage levels.

53. The method of claim 48, wherein a pattern is exposed on the layer which can be characterized by one or more of the following: at least eighty percent (80%) of the non-memory portions of the pattern are defined by the phase shift pattern; at least eighty percent (80%) of a part of the floorplan in the pattern is defined by the phase shift pattern; at least ninety percent (90%) of the pattern is defined by the phase shift pattern; all of the features in the critical path of the pattern are defined by the phase shift pattern; all features in the pattern except those features that are not phase shifted due to phase conflicts are defined by the phase shift pattern; everything in the pattern except test structures are defined by the phase shift pattern; and everything in the pattern except dummy structures are defined by the phase shift pattern.

54. The method of claim 48, wherein a pattern is exposed on the layer which can be characterized by having at least ninety-five (95%) of the pattern defined by the phase shift pattern.

55. The method of claim 48, wherein said set of parameters comprises parameters that are changed by a mechanical adjustment of an optical element.

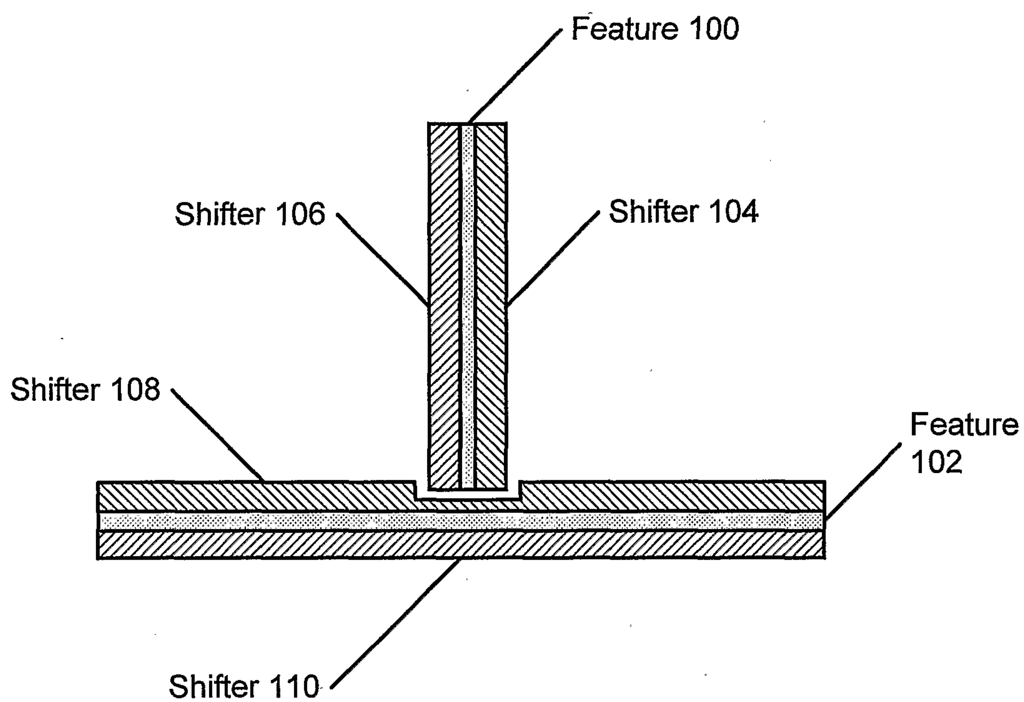

Fig. 1

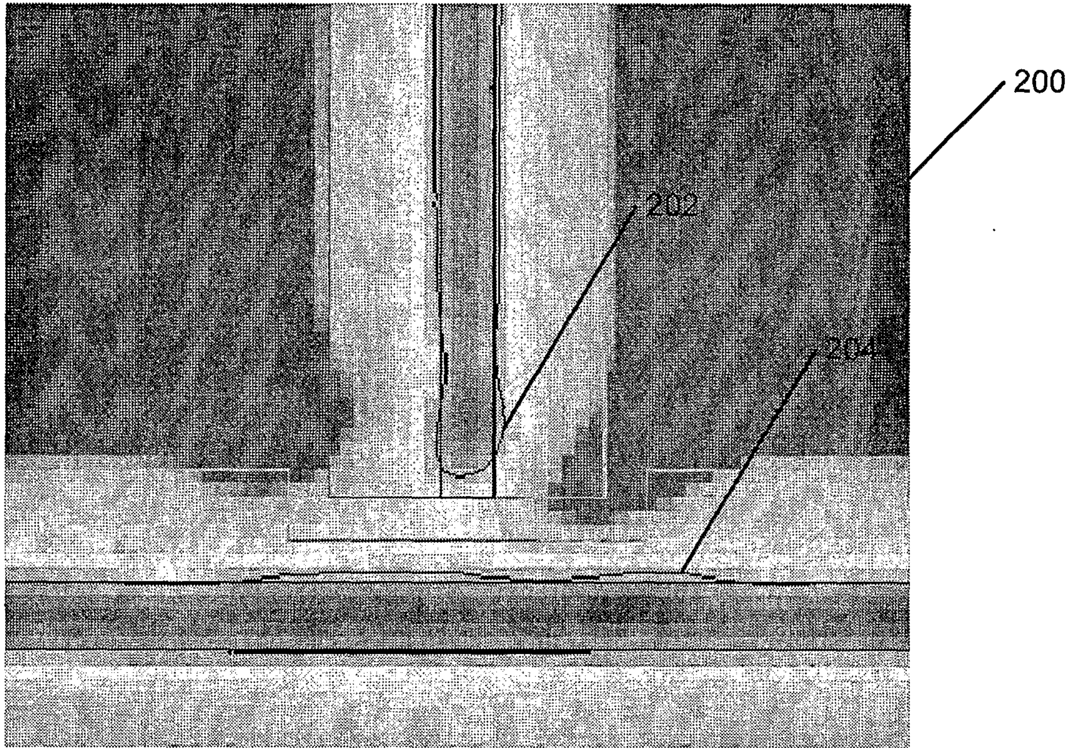

Fig. 2

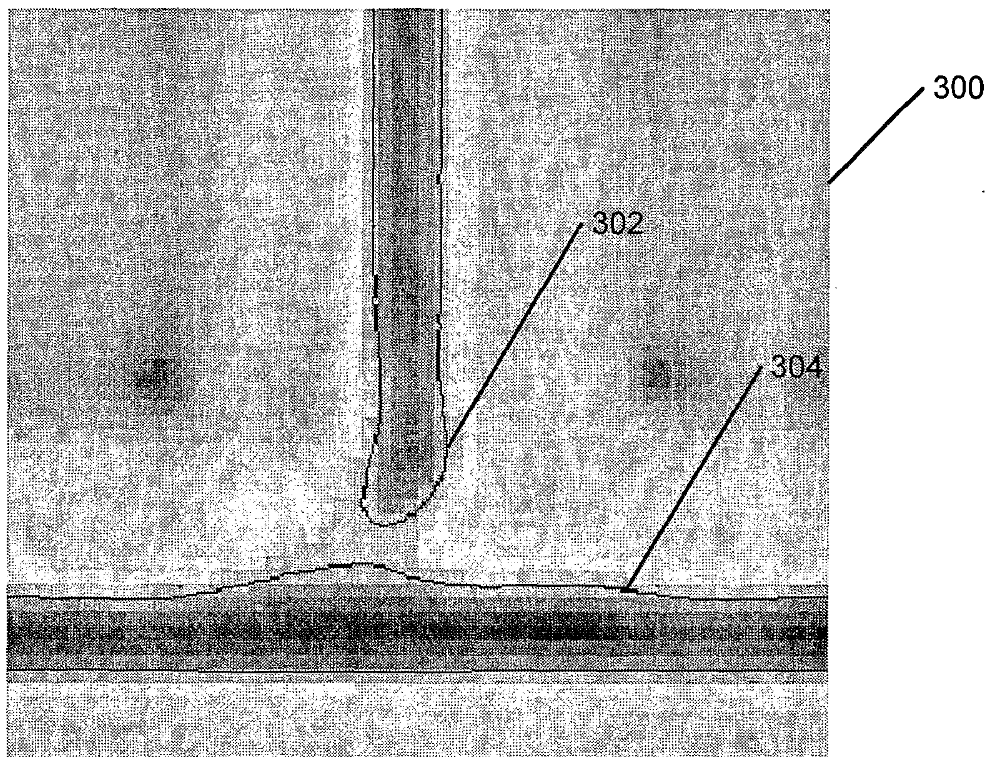

Fig. 3

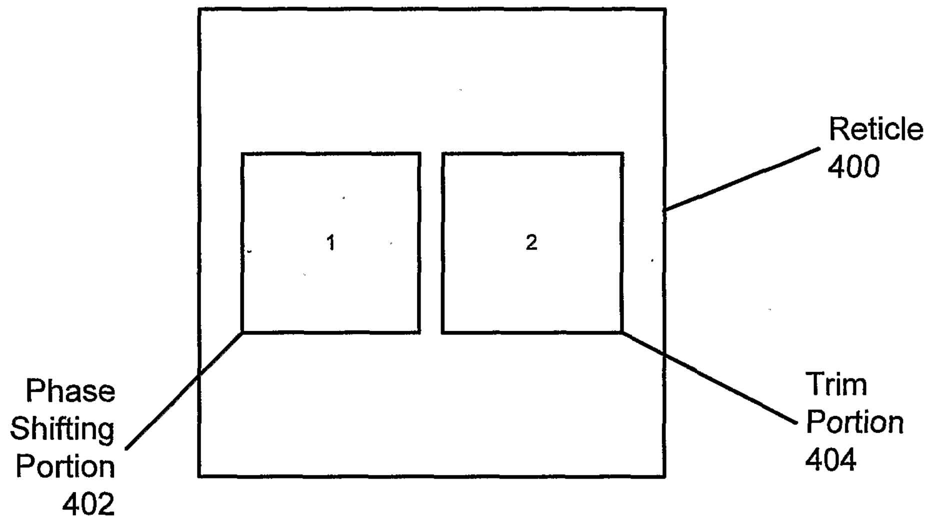

Fig. 4

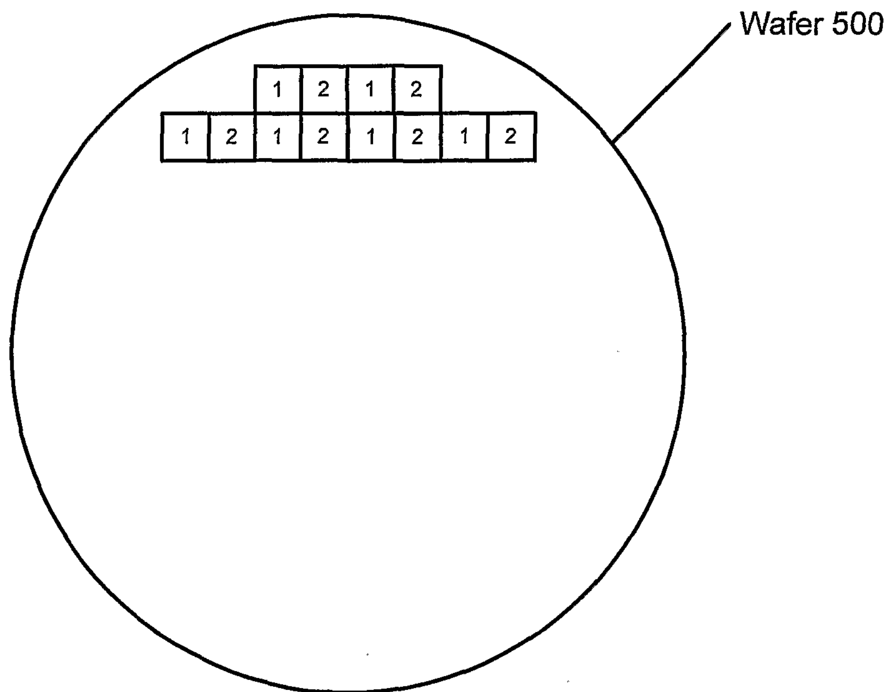

Fig. 5

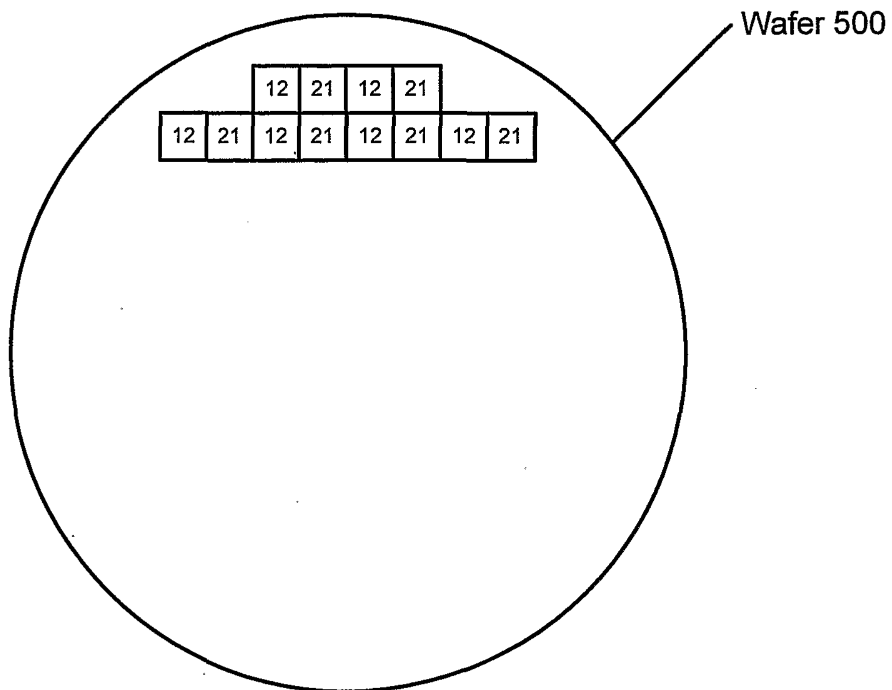

Fig. 6

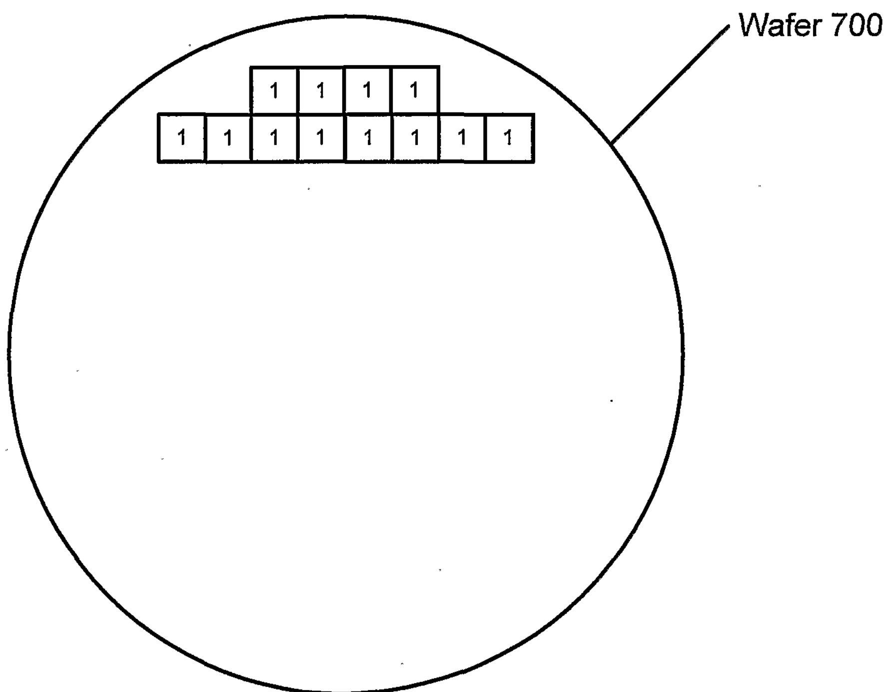

Fig. 7

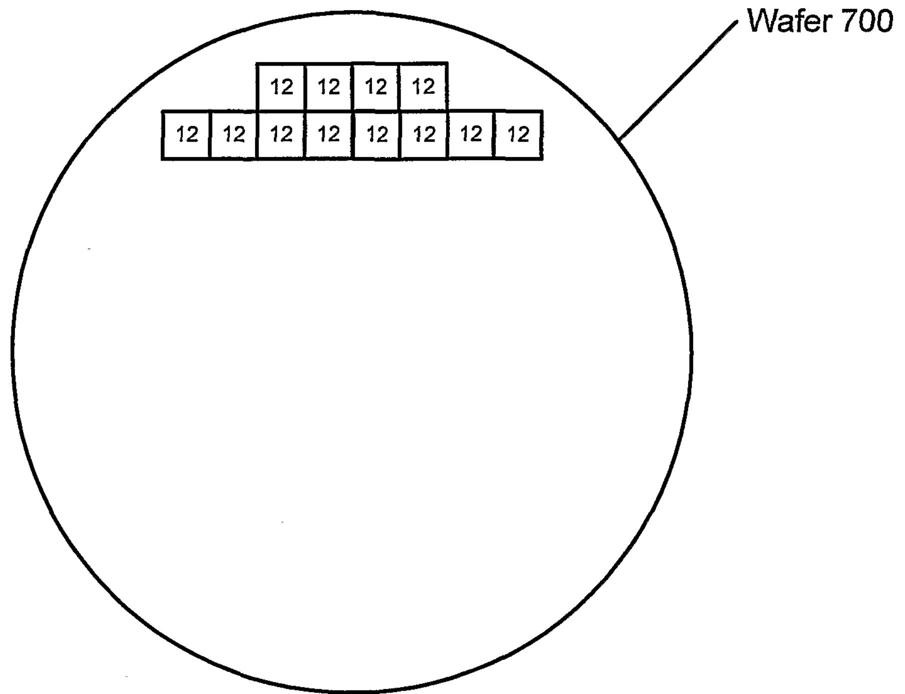

Fig. 8

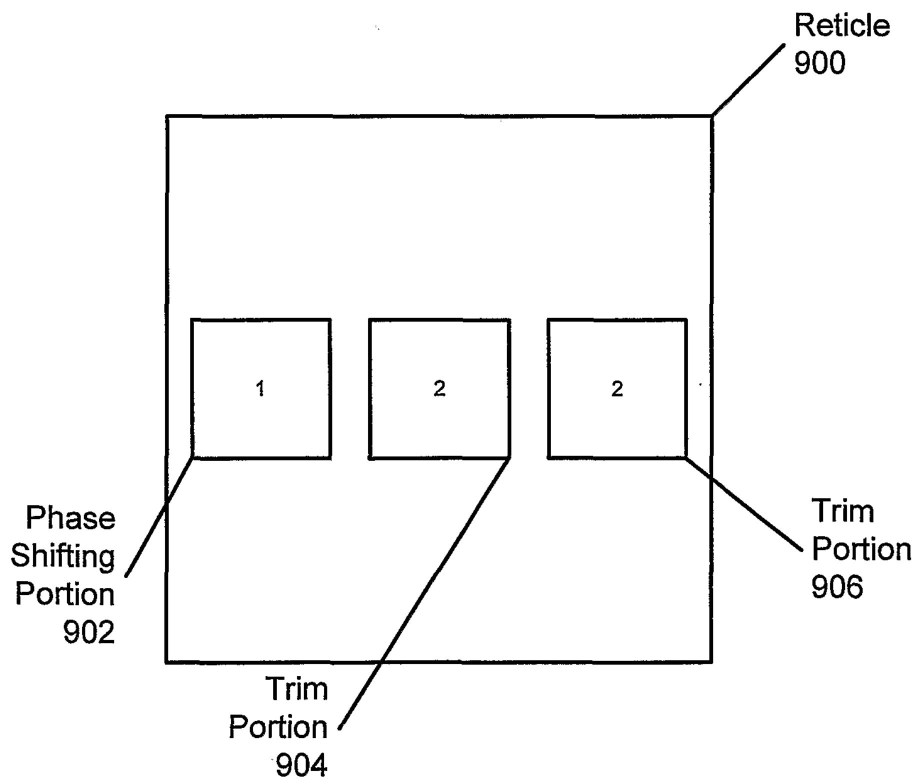

Fig. 9

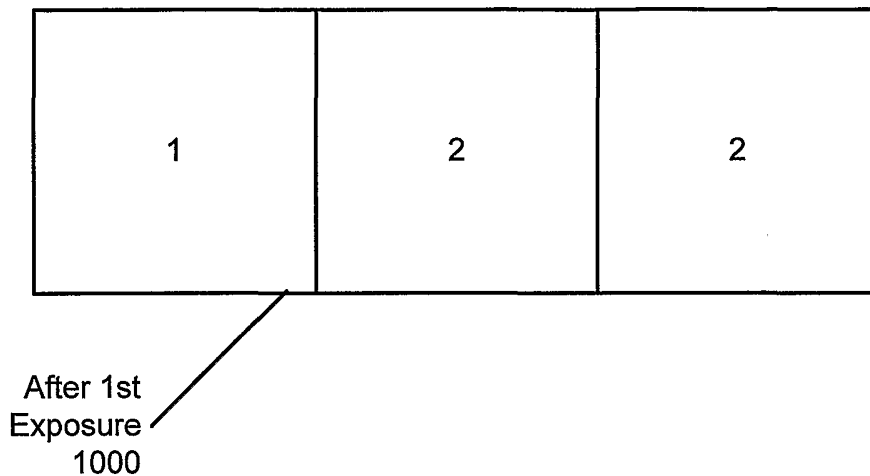

Fig. 10

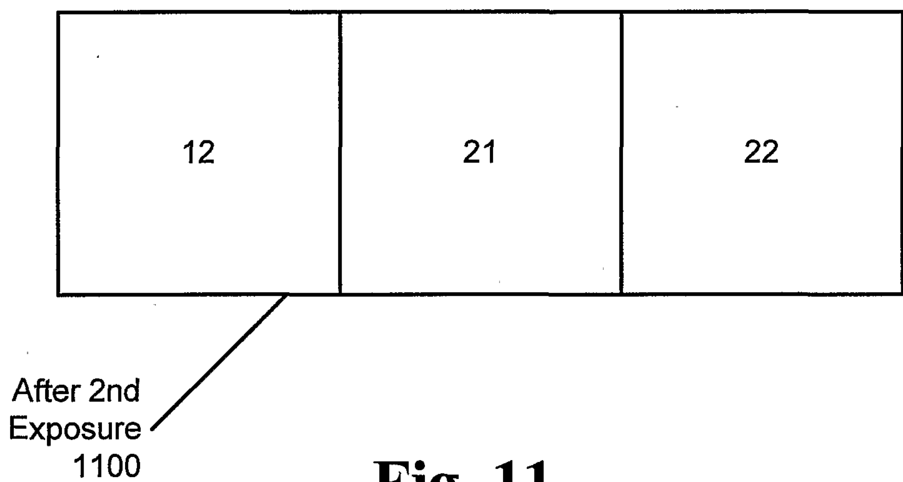

Fig. 11

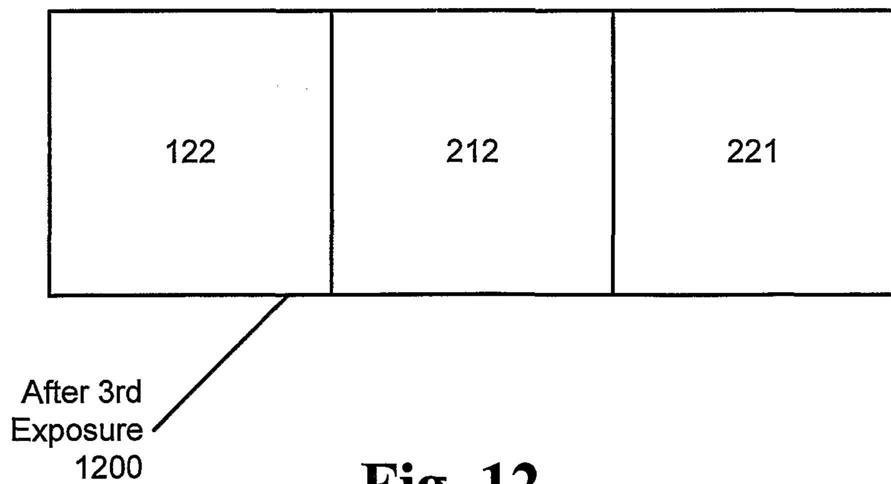

Fig. 12