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- [73] Assignee **The United States of America as**
represented by the Secretary of the Navy

[56]

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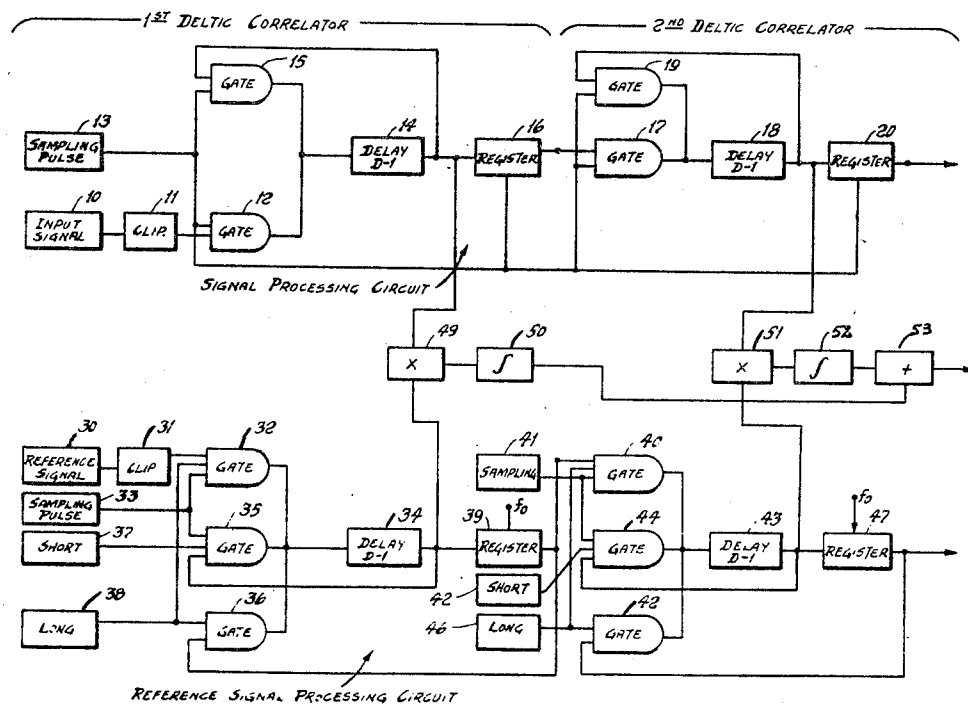
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- [54] **EXTENDED APERTURE DELTIC CORRELATOR**
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- [52] U.S. Cl. **235/181,**
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340/173
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ABSTRACT: There are disclosed arrangements for extending the aperture of Deltic correlators which involve (1) cascading the delay line loops each of which has a time delay approximately equal to the maximum sampling period, and (2) increasing the sampling period by making it a multiple of the basic sample period.



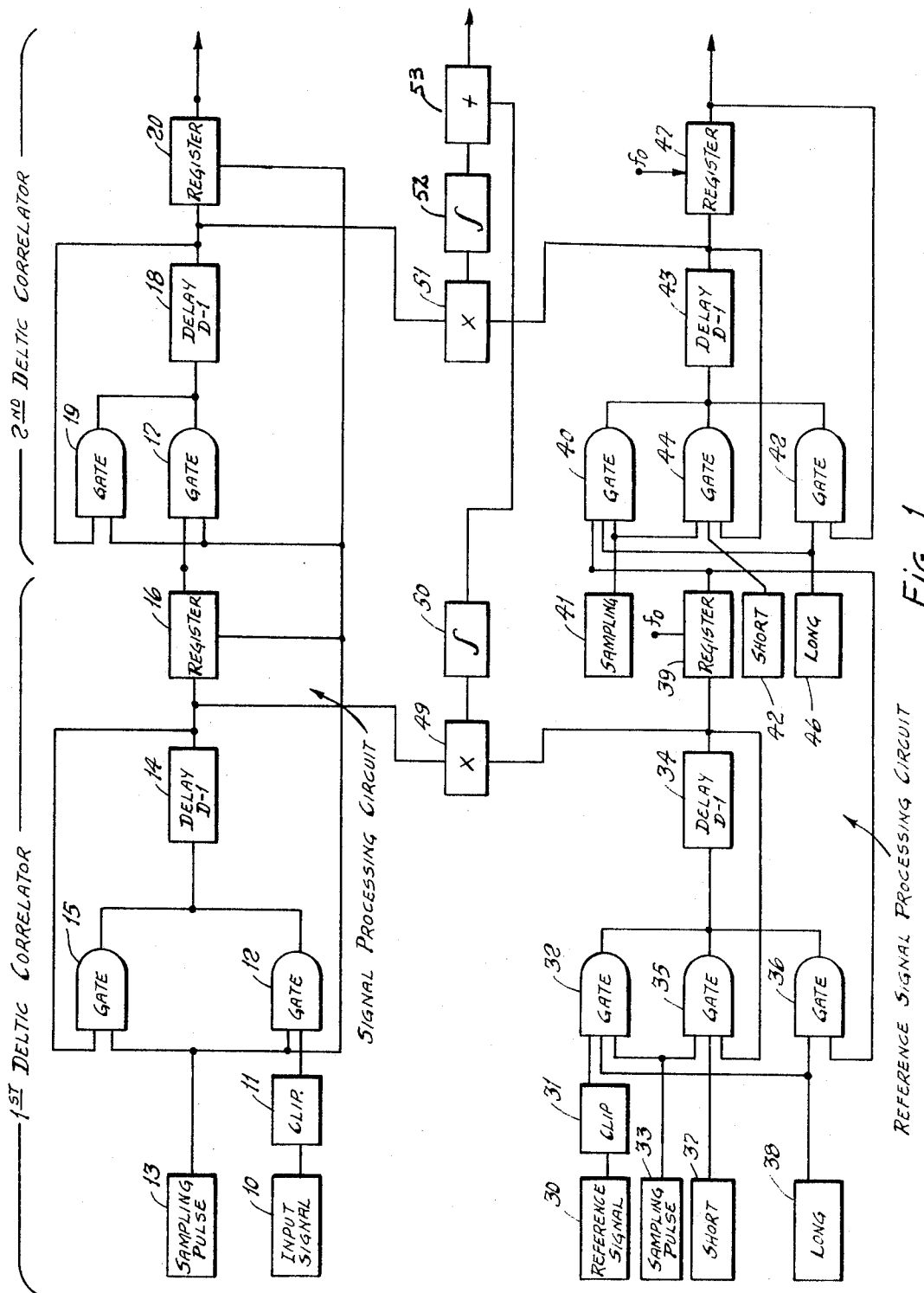


Fig. 1

REFERENCE SIGNAL PROCESSING CIRCUIT

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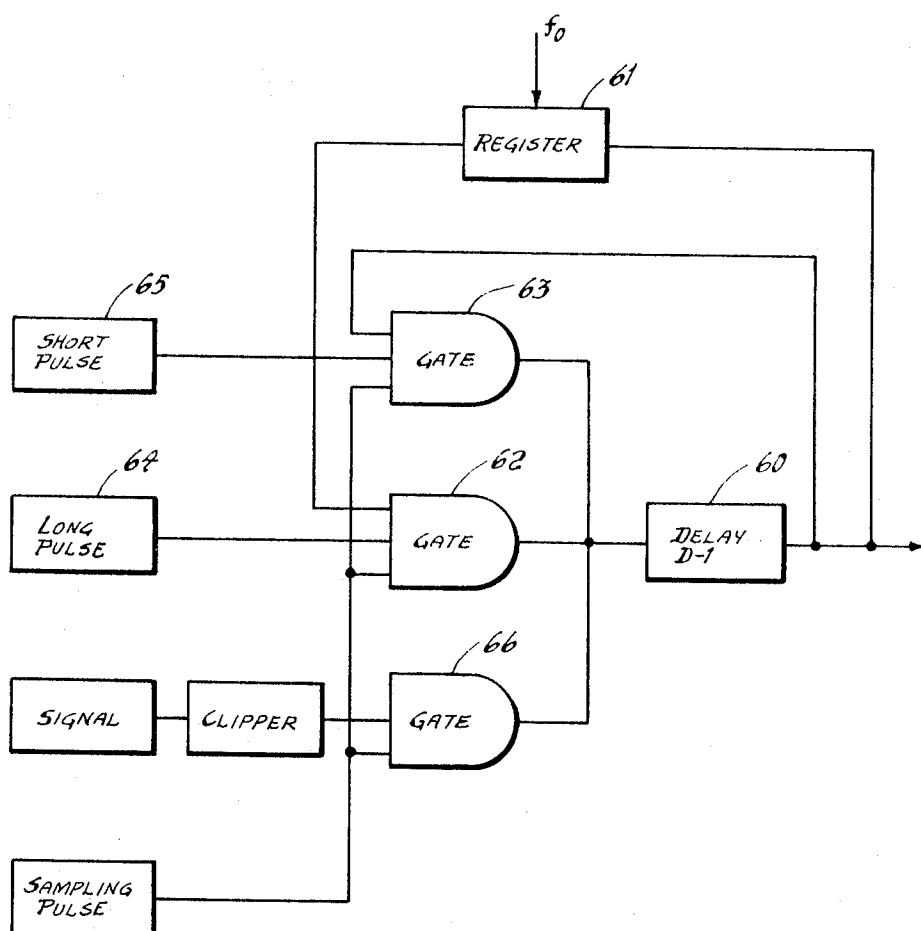


Fig. 2

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EXTENDED APERTURE DELTIC CORRELATOR

The invention described herein may be manufactured and used by or for the Government of the United States of America for governmental purposes without the payment of any royalties thereon or therefor.

The present invention relates generally to Deltic correlators and, more particularly, to arrangements for and methods of extending the aperture of these correlators beyond the limits previously imposed on the system by the finite length and operating frequency of the delay apparatus.

In a standard correlator, digital techniques are usually used to determine the correlation function given by the expression

$$(1) \quad \rho(\tau) = \frac{1}{T} \int_0^T f(t-\tau)g(t)dt$$

where

$f(t)$ = signal being processed

$g(t)$ = replica of signal

T = length of replica (aperture) Thus, the signal being processed must be multiplied by its replica or the reference signal and integrated for each value of the time delay.

In the Deltic correlator, the signal being processed, $f(t)$, is hard clipped and periodically sampled before being applied to the input of a delay line that has the capacity of being able to store sequentially $D-1$ bits, where D is the number of bits the delay apparatus could store if its time delay were equal to the sampling period. The output of the delay apparatus is fed back to the input through an inhibiting circuit which prevents recirculation of this signal when a sampling pulse is present. Since the of the delay apparatus in real time is one bit time less than the sampling period, the first sample loaded into the line travels down the line, is fed back to the input and travels back down the line for one bit time before the next sample occurs and enters the line. For each subsequent sample, the process is repeated with the last sample being loaded into the line one bit time following the preceding sample until the line is filled with $D-1$ bits. The first sample has now precessed down the line by $D-1$ bit times. When the next sampling pulse occurs, this precession amounts to D bits and the first sample is therefore in time coincidence with this sampling pulse. Recirculation of this first sample is consequently rejected in the inhibiting circuit and its place in the delay line storage apparatus taken by the D th signal sample. This mode of operations is continued with each succeeding signal sample replacing the oldest sample then stored in the delay line.

At the output of the delay line, starting at the time of the D th sampling pulse, there appears a pulse train corresponding to the sample version of $f(t)$, the signal being processed but compressed in time to one sample period. During each ensuing period, the pulse train is presented to the output but each time it is shifted in time by one sample period.

The arrangement for storing the replica of the signal $g(t)$ or a reference signal operates in essentially the same manner for D sample pulses. At this time, the $D-1$ most recent samples are sequentially stored in the delay line but the oldest sample, which is prevented from reentering the delay line, is not dropped but stored in a one-bit shift register which is clocked at a rate equal to the bit rate or operating frequency of the delay line. Thereafter, the feedback loop includes this register, and the output of this new loop is a sample time-compressed version of $g(t)$, repeating itself once a sampling period. Consequently, the output of the reference storage is a stationary time series of bits corresponding to a sampled time-compressed version of $g(t)$.

In the correlator, the time-compressed signal $f(t)$ and replica $g(t)$ are multiplied together, and the resultant serves as the input to an integrator whose output is the desired correlation function.

The delay line in the Deltic correlator, it will be appreciated, accomplishes two purposes, namely, it time com-

presses the signal being processed, $f(t)$, so that a repeat correlation with a replica, $g(t)$, can be performed, and it provides the means for obtaining $f(t)-\tau$ by representing a signal delayed progressively in increments equal to the sampling period.

The number of samples that can be stored in the delay line is dependent on the length of this line and the minimum time spacing between stored samples that the frequency response of the line will permit. The delay of the line cannot exceed the maximum allowable sampling period less one sample spacing. Thus, the duration of the real time signal that can be stored becomes limited by the number of samples that can be accommodated in a line having that length.

In the standard Deltic correlator, the electrical specifications of the delay line, as mentioned above, are determined by two main parameters, the period T_s of the sampling pulses $s(t)$ and the duration T of real time signal to be compared against a reference or replica signal of the same length for various values of τ . The electrical length of both the signal and replica delay lines is equal to T_s (minus one bit time for the case of the $f(t)$ signal line which will be neglected for the purpose of this discussion). The number of bits or samples that must be stored in a line is equal to the ratio T/T_s . The operation frequency of the delay line (f_o) is equal to the number of stored bits divided by its length or T/T_s^2 .

In many cases, especially when the correlator is to be used for signal enhancement, it is advantageous to make T , the aperture of the correlator, as large as possible. Since $T=f_o T_s^2$, the technique is to use as large a sampling period as is permitted by the bandwidth of the signal and to operate the line at its maximum reliable frequency. If, however, the sampling rate cannot be reduced because of other considerations and the storage cannot be made to circulate any faster, the aperture cannot be extended in the conventional circuit.

Referring again to the expression,

$$(1) \quad \rho(\tau) = \frac{1}{T} \int_0^T f(t-\tau)g(t)dt,$$

the correlation function, the aperture in real time is T . If the aperture is increased by a factor of N , then equation (1) becomes

$$(2) \quad \rho N(\tau) = \frac{1}{NT} \int_0^{NT} f(t-\tau)g(t)dt$$

This new integral can be broken up into N parts resulting in

$$(3) \quad \rho N(\tau) = \frac{1}{NT} \left\{ \int_0^T f(t-\tau)g(t)dt + \int_T^{2T} f(t-\tau)g(t)dt + \dots + \int_{(N-1)T}^{NT} f(t-\tau)g(t)dt \right\}$$

It will be seen that the first integral in the brackets is exactly of the same form as before aperture extension. The second integral is the same except integration is performed from T to $2T$. All subsequent integrals are also the same with the exception that the location of the integration interval progresses in real time.

From a study of the summed integrals, it may be seen that the aperture of a recirculating delay line correlator operating at a given sampling rate may be increased in the following manner: N correlator sections, each equivalent in length to the sampling interval, may be employed. The reference and signal lines in each section store a part of the signal and replica T seconds long in real time. Each part of the replica and signal are allowed to recirculate in each individual loop section where they are stored. This permits multiplication of the part of the replica and signal associated with each interval of integration. For a given value of τ , the signal is also split up into the individual recirculating signal lines. However, after each recirculation, a τ shift of one bit is achieved in each line by dumping out its oldest bit into a line that is performing integration in the succeeding integration time interval. The individual section performing integration between 0 and T has its signal line updated each recirculation period by the oldest bit from

the T to $2T$ section. It, in turn, discards its oldest bit. The component which integrates from $(N-1)T$ to T is updated by the latest sample of the signal being analyzed. Multiplication and integration of the signal and replica outputs of each individual line are performed as in a conventional correlator, and the summation yields $\rho_N(\tau)$.

It is, accordingly, a primary object of the present invention to provide a Deltic correlator of increased aperture.

Another object of the present invention is to provide a Deltic correlator wherein the aperture is extended without increasing the delay line length.

Another object of the present invention is to provide a Deltic correlator utilizing interconnected delay lines, each of which has a time delay approximately equal to the basic sampling period.

Another object of the present invention is to provide a Deltic correlator whose sampling period is a multiple of the basic sampling frequency.

Other objects, advantages and novel features of the invention will become apparent from the following detailed description of the invention when considered in conjunction with the accompanying drawings wherein:

FIG. 1 is a schematic drawing of a cascaded Deltic correlator arrangement embodying one form of the present invention wherein the aperture is increased by a factor of two; and

FIG. 2 illustrates an arrangement for use in the Deltic correlator for extending the sampling period by multiples of the basic sampling frequency.

Referring to FIG. 1 of the drawings, the arrangement illustrated consists of a pair of cascaded Deltic correlators which cooperate to provide an aperture twice the length of that of each correlator in the system. Each correlator has an input signal processing circuit in the upper portion thereof and a replica or reference signal processing circuit in the lower portion thereof.

The input signal $f(t)$, which may be a binary signal obtained from a suitable source 10, is fed first to a clipper 11 which hard clips this signal and then is sent to a gate 12 controlled by sampling pulses $s(t)$ from a suitable source 13. Each sample of signal $f(t)$ is fed to a delay line 14 whose length is $T_s \times 1$ bit times long. The output of delay line 14 is fed back to its input through a gate 15 also controlled by sampling pulses obtained from source 13.

The operation of this portion of the Deltic correlator has been described hereinbefore in general terms. Each sample enters the delay line through gate 12 and is stacked one bit time apart because of the length of delay line 14 with respect to T_s , the period of sampling pulses 13. When the line is filled with $D-1$ bits, the first sample in the next cycle appears at gate 15 in time coincidence with a sampling pulse. Gate 15 inhibits the circulation of this first sample. It is consequently rejected from the system and a new sample is fed into the delay line through gate 12 to replace it. Thereafter, each new succeeding sample replaces the oldest sample and, at the output of delay line 14, there appears a pulse train corresponding to the sampled version of $f(t)$ but compressed in time to one sample period, T_s . The output of delay line 14 in the first correlator goes to a one bit register 16 which is controlled by sampling pulses from source 13. This register is coupled to a gate 17 also controlled by sampling pulses from this same source. Connected to this gate is a second delay line 18 having a time delay equal to delay line 14. This delay line, too, has a feedback path through a gate 19 controlled by sampling pulses.

In the operation of the input signal processing circuit, when a sample is discarded from delay line 14 by the inhibiting action of gate 15, this same sample enters register 16 and thereafter passes into delay line 18 of the second Deltic correlator when the next sampling pulse occurs. Thus, each successive oldest sample from the first correlator is selected from the compressed pulse train in successive cycles and enters the delay line in intervals T_s , duplicating the loading of delay line 14 in the first Deltic correlator. This loading continues with each sample now being stacked in delay line 18 during succes-

sive recirculations through gate 19 until the oldest of these samples appears at this gate in time coincidence with a sampling pulse from source 13. This particular sample is now rejected by the gate and a new sample enters the loop through gate 17 from the first correlator. The rejected sample enters register 20, and this register controlled by sample pulses provides an output which may be used in a third cascaded, Deltic correlator, if desired. In such a case, it would be followed by gates similar to 17 and 19 and a third delay line.

From what has been described hereinbefore, it will be appreciated that the input signal processing circuit accommodates two D bit of the input sample. The first D bits are in the second correlator in delay line 18, having a capacity of $D-1$, and register 20 having a 1-bit capacity. Likewise, the second D bits are in the first correlator in delay line 14 and register 16. As the system operates, the oldest of these bits or samples is dropped out of the system at the output of register 20 of the second correlator and a replacement for this sample enters the first correlator, representing a new portion of the input signal. Thus, twice the length of the input signal which could be accommodated in one of the Deltic correlators progresses through the cascaded arrangement.

Turning now to the reference signal processing circuit of the system, a reference signal $g(t)$ obtained from a suitable source 30 is fed first to a clipper 21 which hard clips it and then to a gate 32 controlled by sampling plus $s(t)$ from source 33. Gate 32 is also controlled by long pulses obtained from a source 38. These pulses, when present at gate 32, effectively block the gate and prevent samples of the reference signal from entering the system. Each sample of signal $g(t)$ is fed to a delay line 34 whose length equals that of delay line 14 in the signal processing circuit. The output of delay line 34 is fed back to its input through a first loop which contains a gate 35. This gate is controlled by sampling pulses from source 33 and is also controlled by a short pulse from source 37. When a short pulse is present, gate 35 is opened and the samples of $g(t)$ circulate around the first loop and are properly stacked, duplicating the performance of delay line 14 and gate 15 in the signal processing circuit.

The output of delay line 34 is applied to a single bit register 39 clocked at the bit rate or the operating frequency f_o of the delay lines. This register is included in a second feedback loop of delay line 34 which contains a gate 36 controlled by a long pulse from source 38.

In the operation of a conventional Deltic correlator, the input signal is progressively shifted through the input signal processing circuit by finite amounts corresponding to a sampling period during the correlation operation, but the replica or reference signal remains, in effect, stationary in the reference signal processing circuit. The second loop, mentioned above, is closed when it is desired to render stationary that portion of the reference signal which is accommodated within the first Deltic correlator of the cascaded pair.

Register 39 is connected to a gate 40 which is controlled by sampling pulses from a suitable source 41 and also controlled by a long pulse from source 36. Connected to this gate is a delay line 43 similar to the other delay lines hereinbefore described. This delay line, like its counterpart in the first Deltic correlator, has a first feedback loop which contains a gate 44 and a second feedback loop which includes a register 47 and a gate 45. Gate 44 is also controlled by short pulses from source 42, while gate 45 is controlled by long pulses from source 46.

In the operation of the reference signal processing circuit, samples of the reference signal enter delay line 34 through gate 32 and circulate through the first loop containing gate 35 until $D-1$ bits are in delay line 34. In the next cycle, it will be appreciated, gate 35 duplicates the performance of gate 15, rejecting the oldest bit and allowing a new sample to enter the loop through gate 32.

This oldest sample enters register 39 and subsequently passes into delay line 43 through gate 40 in a manner similar to that previously described in connection with the signal

processing circuit. The pulses which so enter delay line 43 from the first correlator are stacked in the proper sequence and, when $D-1$ bits are in delay line 43, gate 44 acts to remove the oldest sample and allow a new sample to enter the line through gate 40. However, this oldest sample is now in register 47 and may be sent to a third cascaded Deltic correlator if desired.

When two D pulses are present in the reference signal processing circuit, that is, when delay line 43 and register 47 of the second correlator and delay line 34 and register 39 of the first correlator are filled, gates 44 and 35 are blocked by the termination of the short pulses from sources 42 and 37 and gates 45 and 36 opened by the appearance of the long pulses from sources 46 and 38. Likewise, at this same time, gates 40 and 32 are blocked by long pulses so that the second correlator is isolated from the first correlator and the first correlator is disconnected from the reference signal source 30. As a result of this switching action, the D bits present in the second correlator now remain stationary in their second loop, completing a circulation through delay line 43, register 47 and gate 45 once each sampling period T_s . And, by the same token, the D bits present in the first Deltic correlator remain stationary, completing a circulation through delay line 34, register 39 and gate 36 once each same sampling period. Consequently, the cascaded system accommodates two D bits of the reference signal, twice the number normally handled by a single Deltic correlator, and these two D bits appear, in effect, as a stationary compressed series corresponding to an extended length of the reference signal.

It should be understood that a third or fourth Deltic correlator may be cascaded to the system for further extending the aperture. Also, different portions of the reference signal may be selected for correlation by simply controlling the application of the long pulses to gates 32, 36, 40 and 45. Until these gates are blocked, the reference signal, like the input signal, will progress through the reference signal processing circuit and the selection can be made whenever desired.

The time-compressed input signals appearing in the output of delay line 14 are multiplied by those appearing in the output of register 39 in an appropriate multiplication circuit 49. This may be done in a mutually exclusive "AND" circuit arrangement. The results of this multiplication are integrated in circuit 50.

In the same manner, the time-compressed input signals appearing in the output of delay line 18 and those appearing in the output of register 47 are also multiplied in circuit 51 and then integrated in circuit 52. The outputs of both integrators are added in circuit 53 to provide the desired correlation function $\rho(\tau)$.

It would be pointed out that the reason for adding the registers 16 and 20 in the signal processing circuit is to compensate for the registers needed in the reference signal processing circuit. If it were not for the extra bit of storage provided by register 16, for example, the first bit out of the signal processing circuit of the first correlator would be the D th bit, while that coming out of the reference signal processing circuit of the same correlator would be the $D \times 1$ th bit corresponding to a τ shift of 1-bit. The register remedies this situation.

In Figure 2 there is illustrated a technique for effectively increasing the sampling period of the Deltic correlator without resorting to unreasonably long delay lines. This system may be employed to obtain sample periods which are integral multiples of the basic delay line length. In the cascaded correlator previously described, the sample period, T_s , was equal to the number of bit times accommodated within each delay line plus 1-bit time. This extra bit time, it will be recalled, allowed the contents of the line to precess by one sample for each circulation. In the arrangement of FIG. 2 a provision is included which prevents the delay line contents from precessing on every circulation. It is therefore possible with this mode of operation to load samples at intervals that are multiples of the basic sample period, T_s .

For a sample period of kT_s , the apparent length of the delay line must be $kD-1$ bit times, where k corresponds to any integer, 1, 2, 3, etc. In the circuit of FIG. 2, there are two feedback paths around the delay line 60 which are rendered effective during mutually exclusive periods of time. During each extended sample interval, the contents of the delay line first circulates $k-1$ times around the long feedback path which includes register 61 and control gate 62. Thereafter, it circulates once around the short feedback loop including gate 63. This is accomplished by applying a first long pulse to gate 62 for the requisite time related to K and then a short pulse from source 65 to gate 63.

Since the long feedback loop includes register 61, this loop is D bit times long. With the recirculating feature, it increases to $k-1$ times D bit times long. The short loop is only $D-1$ bit times long. Thus, the effective line length is equal to $(k-1)D \times (D-1)$ bit times. This quantity simplifies to $kD-1$ bit times. The aperture for a correlator operating in the mode described above will therefore be $T = kf_s T_s^2$, again showing an increase by a factor k as compared to the basic Deltic correlator. This method of extension is advantageous, as mentioned above, when the desired sample period would otherwise dictate excessively long delay lines.

It should be appreciated that the two features hereinbefore described may be advantageously combined in the same system to provide an aperture extension which is the product of N and k , for example, $T = Nkf_s T_s^2$. The values of both N and k have no theoretical limit. However, enlarging the value of k involves a corresponding increase in the sampling period whose upper limit is set by the bandwidth of the signals to be processed.

Although the invention has been discussed in terms of recirculating delay lines which store only two levels of the input signal, if the storage apparatus does hold more levels, the same restrictions are applicable to the standard correlator and may be overcome with the cascaded arrangement described. The multiplication algorithm must be changed to one appropriate to the storage medium, be it digital or analog.

One major advantage of the cascaded arrangement resides in the fact that the extension is accomplished without regard to improvements in the storage medium operating frequency or length. Also, since long, high frequency delay lines are not only expensive but unstable, with the second feature of the invention, a number of shorter, lower frequency lines may be employed to obtain the same aperture. Thus, one achieves more dependable operation at a lower cost. Also, the present invention provides a degree of flexibility missing in previous correlators since, in the standard correlator, the delay line is a fixed piece of apparatus which must be reconstructed for each different application. The present invention allows a large, multipurpose correlator to be constructed out of subsections where the individual units may be cascaded to provide any desired length of aperture or used as separate or groups of separate correlators to provide multichannel capability. Also, a failure of one section decreases the maximum aperture by $1/N$ instead of resulting in the complete breakdown of the system.

It should be appreciated that the invention may employ any type of signal storage medium in which the information is cyclically available including, for example, magnetic drums, shift registers, cores, magnetostrictive delay lines and acoustic delay lines. Furthermore, if the storage medium is inherently multilevel or is capable of being employed in this fashion, the same advantages still accrue. For multilevel or analog operation, the 1 bit or one digit storage need only be made appropriate and the multiplication algorithm changed to one fitting true multilevel or analog multiplication.

What we claim is:

1. A system of cascaded Deltic correlators having an aperture of increased size comprising, in combination, a first and second Deltic correlator, each Deltic correlator having a first delay line, a first gate connected to the input of said first delay line, a second

gate connected in a first feedback circuit of said delay line, and a first 1-bit register connected to the output of said first delay line,

each Deltic correlator also having a second delay line, a third gate connected to the input of said second delay line, a fourth gate connected in a first feedback circuit of said second delay line, a second 1-bit register connected to the output of said second delay line, and a fifth gate in series with said second register in a second feedback circuit of said second delay line,

each Deltic correlator also having means for coupling sampling pulses to the first, second, third, fourth gates so as to periodically open each first and third gate and close each second and fourth gate;

means for connecting the output of the first 1-bit register of said first Deltic correlator to the first gate of said second Deltic correlator;

means for coupling a binary input signal to the first gate of said first Deltic correlator;

means for also coupling sampling pulses to the first 1-bit register of said first Deltic correlator so as to periodically transfer the count stored therein to the first gate of said second Deltic correlator as an input signal to this Deltic correlator,

each of said delay lines having a time delay slightly shorter than the time interval between sampling pulses, whereby pulse length portions of said binary input signal are fed into the first delay line of said first Deltic correlator with each of these pulses thereafter circulating around its first feedback path until a particular pulse coincides with a sampling pulse at said second gate,

each of these pulses also passing into the first register of said first Deltic correlator and then, at the time of occurrence of the next sampling pulse, through the first gate of said second Deltic correlator into the first delay line of said second Deltic correlator and thereafter circulating around its first feedback until a particular pulse coincides with the appearance of a sampling pulse at the first gate of said second Deltic correlator, said pulses being time compressed because of the length of the delay lines compared to the time interval between sampling pulses whereby complementary time compressed input signal pulse trains representing adjacent portions of said input signal appear in the output of the first delay lines of said Deltic correlators;

means for connecting a reference signal to the third gate of said first Deltic correlator;

means for connecting the output of the second 1-bit register of said first Deltic correlator to the first gate of said second Deltic correlator;

means for additionally controlling the operation of the third, fourth and fifth gates and said second 1-bit registers

such that either a first mode of operation is obtained wherein the time compressed reference signal pulse trains which appear in the output of the second delay of said Deltic correlators represent the same adjacent portions of said reference signal or a second mode of operation is obtained wherein these signal pulse trains represent changing adjacent portions of said reference signal,

each Deltic correlator also having means for multiplying the time compressed pulse trains appearing in the output of its first and second delay lines and for integrating the results thereof to obtain an output signal whose amplitude is indicative of the correlation between those portions of the input and reference signal which are represented by these pulse trains; and

means for combining the output signals from each Deltic correlator to give an overall output signal for the cascaded system.

2. In an arrangement as defined in claim 1 wherein said means for controlling the operation of said second 1-bit registers comprises

a source of clock pulses coupled to said registers and having a frequency corresponding to the time interval between the time compressed reference signal pulses appearing in the output of the second delay lines of said first and second Deltic correlators.

3. In an arrangement as defined in claim 1 wherein said means for additionally controlling the operation of each third, fourth and fifth gate includes

a source of relatively short pulses coupled to the fourth gates for maintaining these gates open and

a source of relatively long pulses coupled to the third and fifth gates for maintaining the third gates open and the fifth gates closed, whereby

whenever said third and fourth gates are open, pulse samples of said reference signal may be fed into the second delay line of said first Deltic correlator and circulate around its first feedback path and the output from the second 1-bit register in the second feedback circuit of this delay line may be fed into the second delay line of said second Deltic correlator and circulate around its first feedback path to produce said second mode of operation, and

whenever said third and fourth gates are closed and said fifth gates open, pulse samples of said reference signal cannot be fed into the second delay line of said first Deltic correlator nor can the output of the second 1-bit register that is connected in its output circuit be fed to the second delay line of said second Deltic correlator so that the time compressed reference signal pulse trains in the output of said second delay lines circulate around the second feedback path of these delay lines to produce said first mode of operation.