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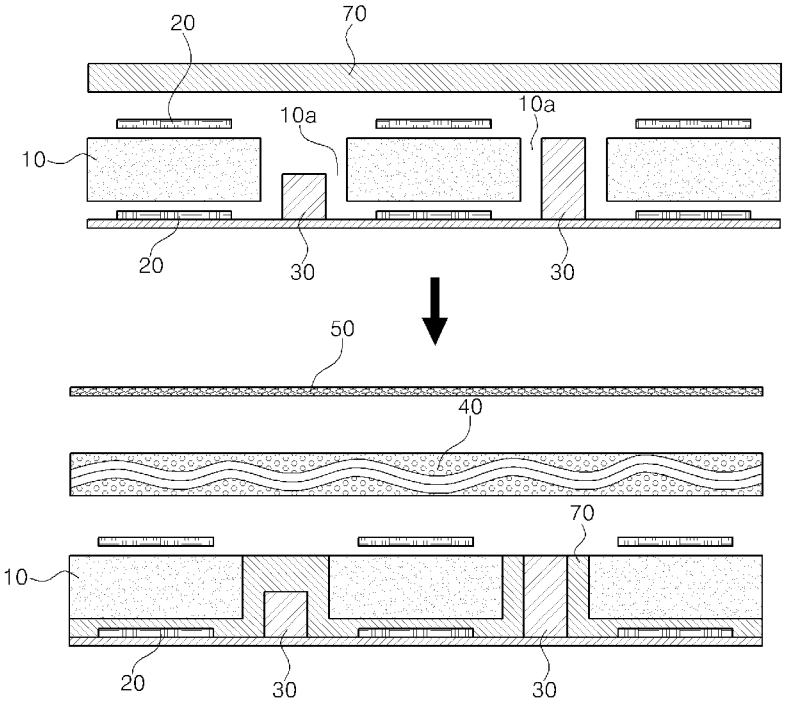
(54) Title: PRINTED CIRCUIT BOARD FOR MOUNTING CHIP AND METHOD OF MANUFACTURING THE SAME



(57) Abstract: Provided is a method of manufacturing a printed circuit board for mounting a chip, the method including: providing a chip mounting cavity in a core layer; mounting the chip to the chip mounting cavity forming a first insulating material layer on one surface of the core layer to fill a space formed between the chip mounting cavity and the chip and forming a second material layer of a different kind from that of the first insulating material layer on the one surface of the core layer.

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(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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Description

Title of Invention: PRINTED CIRCUIT BOARD FOR MOUNTING CHIP AND METHOD OF MANUFACTURING THE SAME

Technical Field

[1] The present invention relates to a method of manufacturing a printed circuit board for mounting a chip.

[2]

[3] This application claims priority to Korean Patent Application No. 10-2012-0121205, filed on 30 Oct 2012, in the Korean Intellectual Property Office, the entire contents of which are hereby incorporated by reference.

Background Art

[4] As the miniaturization and high functionalization of electronic components have been realized according to the development of the electronics industry, a demand for the miniaturization and high density of a printed circuit board has been increasing steadily. According to the trend of lightened, thinned, shortened and small-sized electronic products, the printed circuit board has been also micro-patterned, miniaturized and packaged. A chip including an active device such as an IC and a passive device such as a condenser, resistor and the like was mounted on the surface of a conventional printed circuit board for packaging using a device such as a chip mounter.

[5] However, in the past, the number of the chip mounted on a surface of the printed circuit increased in a certain number, and thus an area in which the chip is mounted was reduced from the surface of the printed circuit board. Accordingly, it was problematic that the printed circuit board is restricted by a mounting space of the chip mounted to the surface of the printed circuit board. Accordingly, an embedding process for equipping the chip in the printed circuit board has been recently developed and widely used.

[6] FIG. 1 and FIG. 2 are cross-sectional views illustrating a printed circuit board for mounting a chip according to a conventional art.

[7] Referring to FIG. 1, a printed circuit board for mounting a chip is configured such that a circuit pattern layer 20 is formed by forming Cu on both surfaces of a core layer 10 of an epoxy-based resin, and a chip mounting cavity, which passes through the core layer 10 and a circuit pattern layer 20, is formed. When a chip 30 is mounted to the chip mounting cavity, an insulating material layer 40 and a second circuit pattern layer 50 are formed on one surface of the core layer 10.

[8] However, when the chip embedded in the printed circuit board for mounting the chip

accounts for an increasing volume compared to a volume of the printed circuit board, it is problematic that a total volume increases because a resin material should be filled in an inner part of the chip mounting cavity.

[9] Also, as shown in FIG. 2, in the printed circuit board for mounting the chip, the insulating material layer 40 formed on one surface of the core layer 10 generates a difference in thickness according to its positions A, B thereof wherein 'A' is an area in which the chip 30 is mounted to the chip mounting cavity and 'B' is an area in which the insulating material layer 40 is in contact directly with the circuit pattern layer 20. Even after the chip 30 is mounted to the chip mounting cavity, a little space 10a is left in the chip mounting cavity. Accordingly, a difference in thickness is not generated from the areas A, B until the insulating material layer 40 is hardened (200) after the insulating material layer 40 is formed, but after the insulating material layer 40 is hardened (220), a difference in thickness is generated from the area A, B.

[10] The reason why is because a phenomenon in which a total volume is reduced is generated when the insulating material layer 40 is formed on one surface the core layer 10 through a high temperature and a high pressure, and resin molecules of the insulating material layer 40 are aggregated to each other. When the difference in thickness of the insulating material layer 40 is generated, a warpage problem is generated due to the generation of stress.

Disclosure of Invention

Technical Problem

[11] An aspect of the present invention provides a printed circuit board for mounting a chip, and a method of manufacturing the same, which is configured such that a first insulating material layer is formed on a core layer, and a second material layer of a different kind from that of the first insulating material layer is formed on one surface of the core layer so that the second insulating material layer is prevented from being non-uniformly formed on the surface of the core layer, thereby minimizing the generation of warpage.

[12] Another aspect of the present invention provides a printed circuit board for mounting a chip, and a method of manufacturing the same, which is configured such that a first insulating material layer composed of only resin without glass fabric is thermal-compressed on one surface of a core layer so that a second material layer formed on the core layer can be uniformly formed on the surface of the core layer.

[13] Still another aspect of the present invention provides a printed circuit board for mounting a chip, and a method of manufacturing the same, which is configured such that a first insulating material layer is formed on one surface of a core layer in advance so that a first insulating material layer is filled in a space formed between the chip and

a chip mounting cavity in a core layer, whereby thicknesses from a second insulating material to another surface of the core layer in an area in which the chip mounting cavity is formed and an area in which the chip mounting cavity is not formed are formed to be substantially identical to each other.

[14] Still another aspect of the present invention provides a printed circuit board for mounting a chip, and a method of manufacturing the same, which is configured such that a first insulating material layer is formed on one surface of a core layer in advance so that the first insulating material layer is filled in inner areas of a via hole and a chip mounting cavity in the core layer, thereby enabling shapes of the chip mounting cavity and the via hole to be maintained.

Solution to Problem

[15] According to an aspect of the present invention, there is provided a method of manufacturing a printed circuit board for mounting a chip, the method including: providing a chip mounting cavity in a core layer; mounting the chip to the chip mounting cavity; forming a first insulating material layer on one surface of the core layer to fill a space formed between the chip and the chip mounting cavity; and forming a second material layer of a different kind from the first insulating material layer on the one surface of the core layer.

[16] According to another aspect of the present invention, there is provided a printed circuit board for mounting a chip, including: a core layer in which a chip mounting cavity is formed; a chip mounted to the chip mounting cavity; a space formed between the chip and the chip mounting cavity a first insulating material layer filled in the space; and a second insulating material layer formed on one surface of the core layer, wherein the first insulating material layer and the second insulating material layer are different kinds of members.

Advantageous Effects of Invention

[17] According to one exemplary embodiment, the first insulating material layer is formed on one surface of the core layer, and the second material layer of a different kind from that of the first insulating material layer is formed on a surface of the core layer so that the second insulating material layer is prevented from being non-uniformly formed on the surface of the core layer, thereby minimizing the generation of warpage.

[18] According to one exemplary embodiment, the first insulating material layer composed of only resin without glass fabric is thermal-compressed on one surface of the core layer so that the second material layer formed on the core layer can be uniformly formed on the surface of the core layer.

[19] According to one exemplary embodiment, the first insulating material layer is formed on one surface of the core layer in advance so that the first insulating material layer is

filled in the space formed between the chip and the chip mounting cavity in the core layer, whereby the thicknesses from a second insulating material to another surface of the core layer in the areas in which the chip mounting cavity is formed and in which the chip mounting cavity is not formed are formed to be substantially identical with each other.

[20] According to one exemplary embodiment of the present invention, the first insulating material layer is formed on one surface of the core layer in advance so that the first insulating material layer is filled in the inner areas of the via hole and the chip mounting cavity in the core layer, thereby enabling the shapes of the chip mounting cavity and the via hole to be maintained.

Brief Description of Drawings

[21] The accompanying drawings are included to provide a further understanding of the present invention, and are incorporated in and constitute a part of this specification. The drawings illustrate exemplary embodiments of the present invention and, together with the description, serve to explain principles of the present invention. In the drawings:

[22] FIG. 1 and FIG. 2 are cross-sectional views illustrating a structure of a printed circuit board for mounting a chip according to a conventional art;

[23] FIG. 3 is a flow chart illustrating the process order of a method of manufacturing a printed circuit board for mounting a chip according to one exemplary embodiment of the present invention;

[24] FIG. 4 is a flow chart showing process 360 of FIG. 3 in detail; and

[25] FIG. 5 is a cross-sectional view illustrating a structure of the printed circuit board for mounting the chip according to the one exemplary embodiment of the present invention.

Best Mode for Carrying out the Invention

[26] Exemplary embodiments according to the present invention will now be described more fully hereinafter with reference to the accompanying drawings. In the explanation with reference to the accompanying drawings, regardless of reference numerals of the drawings, like numbers refer to like elements through the specification, and repeated explanation thereon is omitted. Terms such as a first term and a second term may be used for explaining various constitutive elements, but the constitutive elements should not be limited to these terms. These terms is used only for the purpose for distinguishing a constitutive element from other constitutive element.

[27] FIG. 3 is a flow chart illustrating a process order of a method of manufacturing a printed circuit board for mounting a chip according to one exemplary embodiment of the present invention.

[28] Referring to FIG. 3, in step 310, a method of manufacturing a printed circuit board for mounting a chip includes forming circuit pattern layers 20 on one surface and another surface of a core layer 10, and forming a via hole 10b for connecting the circuit pattern layers 20 formed on the one surface and the another surface to each other. The method of manufacturing the printed circuit board for mounting the chip may include forming the circuit pattern layers 20 by performing an etching process.

[29] In step 320, the method of manufacturing the printed circuit board for mounting the chip includes forming a cavity mounting cavity 10a in the core layer 10. the method of manufacturing the printed circuit board for mounting the chip includes forming the chip mounting cavity 10a using a router process or a drilling process to be consistent with a size of the chip to be mounted.

[30] The method of manufacturing the printed circuit board for mounting the chip includes performing chemical treatment on one surface of the core layer 10 (330), and attaching an insulating film 60 to the another surface opposed to the one surface of the core layer 10 (340).

[31] In step 350, the method of manufacturing the printed circuit board for mounting the chip includes mounting a chip 30 to the chip mounting cavity 10a.

[32] In step 360, the method of manufacturing the printed circuit board for mounting the chip includes filling a space formed between the chip mounting cavity 10a and the chip 30 by forming a first insulating material 70 on the one surface of the core layer 10. Also, the method of manufacturing the printed circuit board for mounting the chip includes filling the inner areas of the chip mounting cavity 10a and the via hole 10b by forming the first insulating material layer 70 on the one surface of the core layer 10.

[33] Even after the chip is mounted to the chip mounting cavity 10a, a void is bound to generate in the chip mounting cavity 10a. Furthermore, a void is also generated in the via hole 10b, thereby enabling the void to be filled with the first insulating material layer 70.

[34] FIG. 4 is a flow chart showing process 360 of FIG. 3 in detail.

[35] Referring to FIG. 4, the method of manufacturing the printed circuit board for mounting the chip includes forming the first insulating material layer 70 with a resin material including non glass fabric so as to be filled in the inner area of the chip mounting cavity 10a and the via hole 10b. The first insulating material layer 70 is formed to fill a void. If a resin material including glass fabric is used, resin and glass fabric are left on surfaces other than the inner part of the cavity due to the glass fabric, so a warpage problem, and bulge and dell problems are generated. Accordingly, in the present invention, the first insulating material layer 70 composed of only the resin material is formed on the one surface of the core layer 10.

[36] Accordingly, the first insulating material layer 70 may not protrude to an outer part

of the core layer 10, and may be filled to be present only in the inner areas of the chip mounting cavity 10a and the via hole 10b. At this time, the method of manufacturing the printed circuit board for mounting the chip may include thermal-compressing the first insulating material layer 70 on the one surface of the core layer 10 so that the first insulating material layer 70 can be inserted into the inner areas of the chip mounting cavity 10a and the via hole 10b in the core layer 10 (before being hardened). After the thermal-compressing (after being hardened), the method of manufacturing the printed circuit board for mounting the chip may include removing the first insulating material layer 70 remaining on the surface of the core layer 10.

[37] Accordingly, thicknesses from the second insulating material layer 40 to another surface of the core layer 10 in the areas in which the chip mounting cavity 10a is formed and in which the chip mounting cavity 10a is not formed are substantially identical to each other.

[38] The method of manufacturing the printed circuit board for mounting the chip is performed in such a manner that the insulating film 60 attached in step 340 is released (370), and the second insulating material layer 40 of a different kind of the first insulating material layer is formed on the surface of the core layer 10 (380). In the method of manufacturing the printed circuit board for mounting the chip, a second circuit pattern layer 50 may be formed on the second insulating material layer 40 (390).

[39] FIG. 5 is a cross-sectional view illustrating a structure of the printed circuit board for mounting the chip according to the one exemplary embodiment of the present invention.

[40] Referring to FIG. 5, the printed circuit board for mounting the chip includes: the core layer 10 in which a chip mounting cavity is formed; the chip 30 mounted to the chip mounting cavity the space 30 formed between the chip and the chip mounting cavity the first insulating material layer 70 filled in the space; and the second insulating material layer 40 formed on one surface of the core layer 10, wherein the first insulating material layer 70 and the second insulating material layer 40 are different kinds of members.

[41] The printed circuit board for mounting the chip may further include: circuit pattern layers 20 formed on the one surface and the another surface of the core layer 10; and the via hole for connecting the circuit pattern layers 20 formed on the one surface and the another surface to each other. At this time, the via hole may be filled with the first insulating material layer.

[42] In a conventional printed circuit board for mounting a chip, the insulating material layer 40 formed on the one surface of the core layer 10 generates a difference in thickness according to positions between the areas in which the chip mounting cavity

is formed and in which the chip mounting cavity is not formed. Accordingly, the difference in thickness is not generated according to the positions until the insulating material layer 40 is hardened 210 after the second insulating material layer 40 is formed, but after the second insulating material layer 40 is hardened, the difference in thickness is generated according the positions because the second insulating material layer 40 is filled in the void.

[43] To solve this problem, in the present invention, the first insulating material layer 70, which is a different member from the second insulating material layer 40, is formed on the one surface of the core layer 10 in advance before the second insulating material layer 40 is formed so the first insulating material layer 70 can be filled in the void in the core layer 10. For this, the first insulating material layer 70 may be composed of the resin material including non glass fabric. If the resin material including glass fabric is used, resin and fabric are left on surfaces other than the inner part of the cavity due to the glass fabric, thereby generating a warpage problem and bulge and dell problems.

[44] Accordingly, in the present invention, the first insulating material layer 70 composed of only a resin material is formed on the one surface of the core layer 10. The first insulating material layer 70 may be configured such that upper surface and lower surfaces thereof are formed smaller than upper and lower planes of the chip mounting cavity and the via hole. That is, the first insulating material layer 70 may be formed not to protrude to the outer part of the core layer 10. Accordingly, the first insulating material layer 70 may be completely removed from the surface of the core layer 10.

[45] Accordingly, the thicknesses from the second insulating material 40 to the another surface of the core layer 10 in the areas in which the chip mounting cavity 10a is formed and in which the chip mounting cavity 10a is not formed are substantially identical with each other.

[46] As an example, the printed circuit board for mounting the chip may further include the second circuit pattern layer 50 formed on the second insulating material layer 40.

[47] As previously described, in the detailed description of the invention, having described the detailed exemplary embodiments of the invention, it should be apparent that modifications and variations can be made by persons skilled without deviating from the spirit or scope of the invention. Therefore, it is to be understood that the foregoing is illustrative of the present invention and is not to be construed as limited to the specific embodiments disclosed, and that modifications to the disclosed embodiments, as well as other embodiments, are intended to be included within the scope of the appended claims and their equivalents.

[48]

[49]

Claims

[Claim 1] A method of manufacturing a printed circuit board for mounting a chip, the method comprising:
providing a chip mounting cavity in a core layer;
mounting a chip to the chip mounting cavity;
forming a first insulating material layer on one surface of the core layer to fill a space formed between the chip mounting cavity and the chip; and
forming a second material layer of a different kind from that of the first insulating material layer on the one surface of the core layer.

[Claim 2] The method of claim 1, further comprising: forming circuit pattern layers on the one surface and another surface of the core layer; and forming a via hole for connecting the circuit patterns formed on the one surface and the another surface of the core layer to each other, wherein the filling of the space formed between the chip mounting cavity and the chip comprises filling inner areas of the chip mounting cavity and the via hole.

[Claim 3] The method of claim 2, wherein the filling of the inner areas of the chip mounting cavity and the via hole is filling the inner areas of the chip mounting cavity and the via hole with a resin material including non glass fabric.

[Claim 4] The method of claim 2, wherein the filling of the inner areas of the chip mounting cavity and the via hole is filling only the inner areas of the chip mounting cavity and the via hole of the first insulating material layer so that the resin material is present only in the inner areas.

[Claim 5] The method of claim 2, wherein the filling of the inner areas of the chip mounting cavity and the via hole is thermal-compressing the first insulating material layer on the one surface of the core layer so that the first insulating material layer is inserted into the inner areas of the chip mounting cavity and the via hole in the core layer.

[Claim 6] The method of claim 5, further comprising removing the first insulating material layer remaining on the surface of the core layer after the thermal compressing.

[Claim 7] The method of claim 1, further comprising forming a second circuit pattern layer on the second insulating material layer.

[Claim 8] A printed circuit board for mounting a chip, comprising:
a core layer in which a chip mounting cavity is formed;

a chip mounted to the chip mounting cavity;
a space formed between the chip mounting cavity and the chip;
a first insulating material layer filled in the space; and
a second insulating material layer formed on one surface of the core layer,
wherein the first insulating material layer and the second insulating material layer are different kinds of members.

[Claim 9] The printed circuit board of claim 8, wherein the first insulating material layer is composed of a resin material including non-glass fabric.

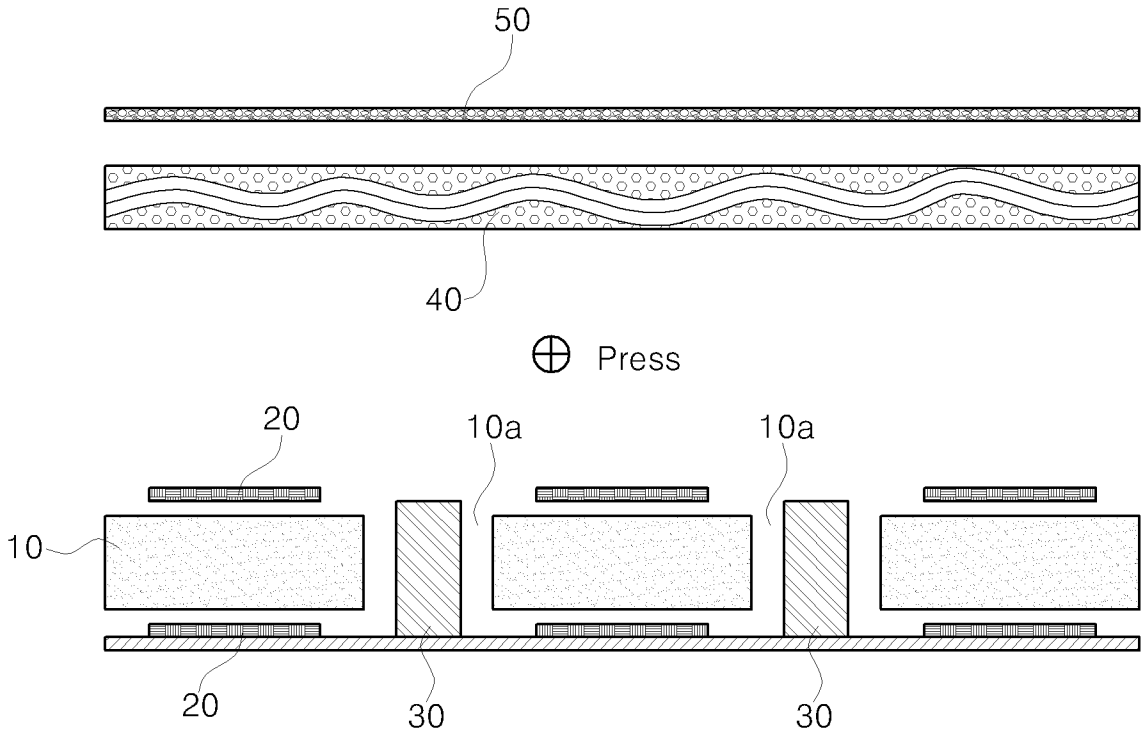
[Claim 10] The printed circuit board of claim 8, wherein the first insulating material layer does not protrude to an outer part of the core layer.

[Claim 11] The printed circuit board of claim 8, further comprising: circuit pattern layers formed on one surface and another surface of the core layer; and a via hole for connecting the circuit pattern layers formed on the one surface and the another surface to each other, wherein the via hole is filled with the first insulating material layer.

[Claim 12] The printed circuit board of claim 8, wherein thicknesses from the second insulating material layer to the another surface of the core layer in areas, in which the chip mounting cavity is formed and in which the chip mounting cavity is not formed, are substantially identical to each other.

[Claim 13] The printed circuit board of claim 8, further comprising a second circuit pattern layer formed on the second insulating material layer.

[Fig. 1]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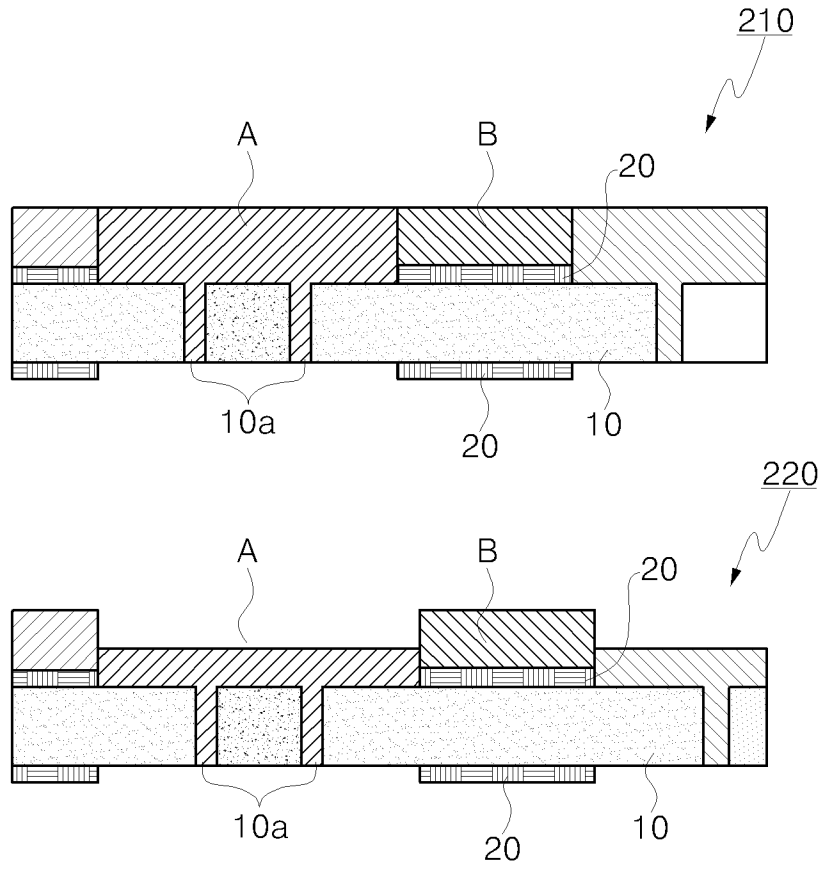
[Fig. 2]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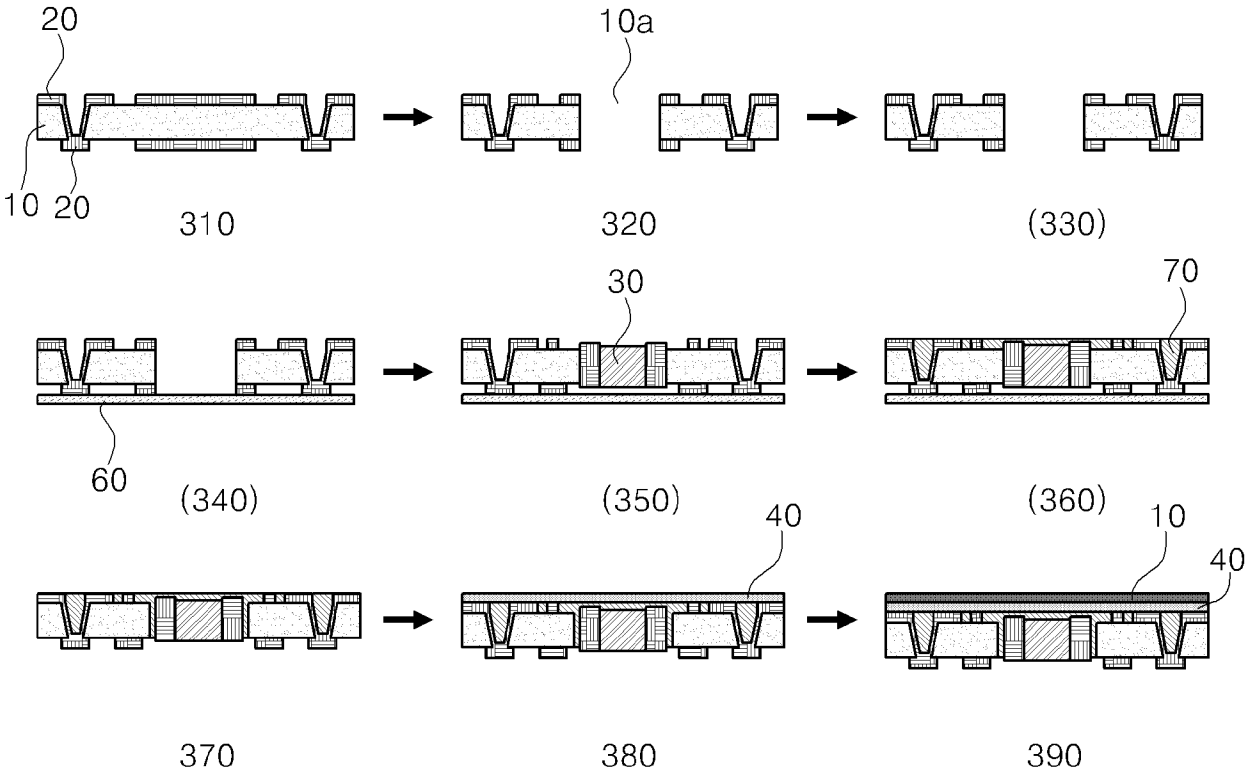
[Fig. 3]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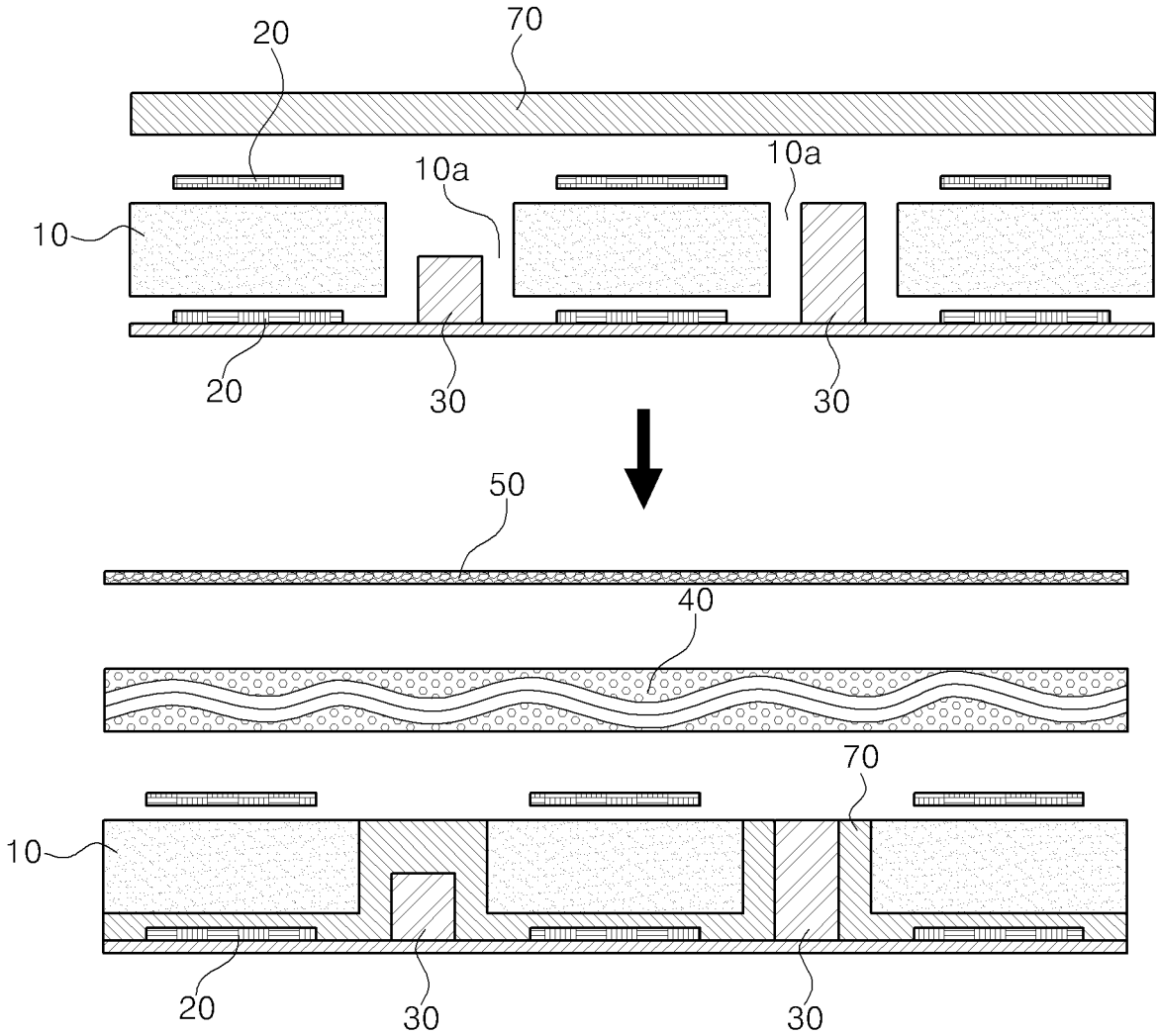
[Fig. 4]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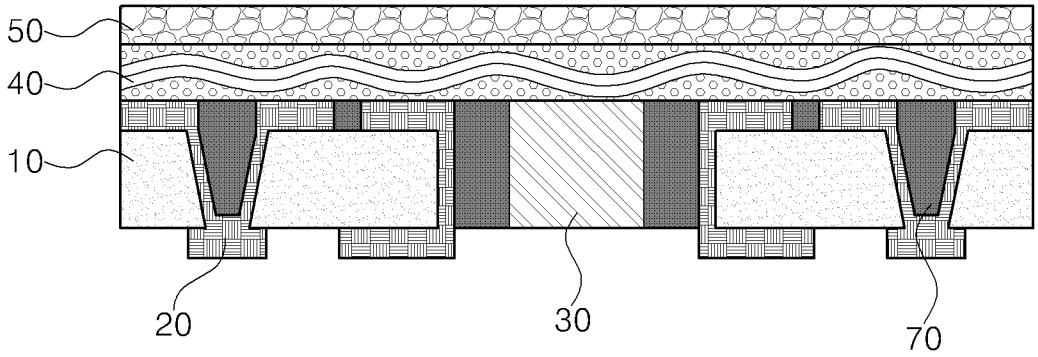
[Fig. 5]



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2013/004106

A. CLASSIFICATION OF SUBJECT MATTER

H05K 3/46(2006.01)i, H05K 1/18(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H05K 3/46; H05K 1/18; H05K 3/42; H05K 3/30; H01L 23/48; H05K 3/32; H01L 23/495; H01L 23/28

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: printed circuit board, chip, core layer, cavity, via hole, resin, insulating material layer, thermal compressing

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010-0031503 A1 (SAKAMOTO HAJIME et al.) 11 February 2010 See paragraphs [0100]-[0120], and figures 1-6.	1-2,7-8,10-13
Y		3-6,9
Y	US 2009-0206471 A1 (SUNOHARA MASAHIRO et al.) 20 August 2009 See paragraphs [0038]-[0051], and figures 1A-1I.	3-6,9
A	KR 10-2009-0062070 A (SEJONG METAL CO., LTD.) 17 June 2009 See abstract, paragraphs [0031]-[0060], and figures 1-5.	1-13
A	KR 10-2009-0111380 A (DAE DUCK ELECTRONICS CO., LTD.) 27 October 2009 See abstract, paragraphs [0013]-[0021], and figures 1A-2C.	1-13
A	US 2008-0308917 A1 (PRESSEL KLAUS et al.) 18 December 2008 See abstract, paragraphs [0026]-[0045], and figures 1-8.	1-13

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
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Date of the actual completion of the international search	Date of mailing of the international search report
27 August 2013 (27.08.2013)	**27 August 2013 (27.08.2013)**

Name and mailing address of the ISA/KR
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/KR2013/004106

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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