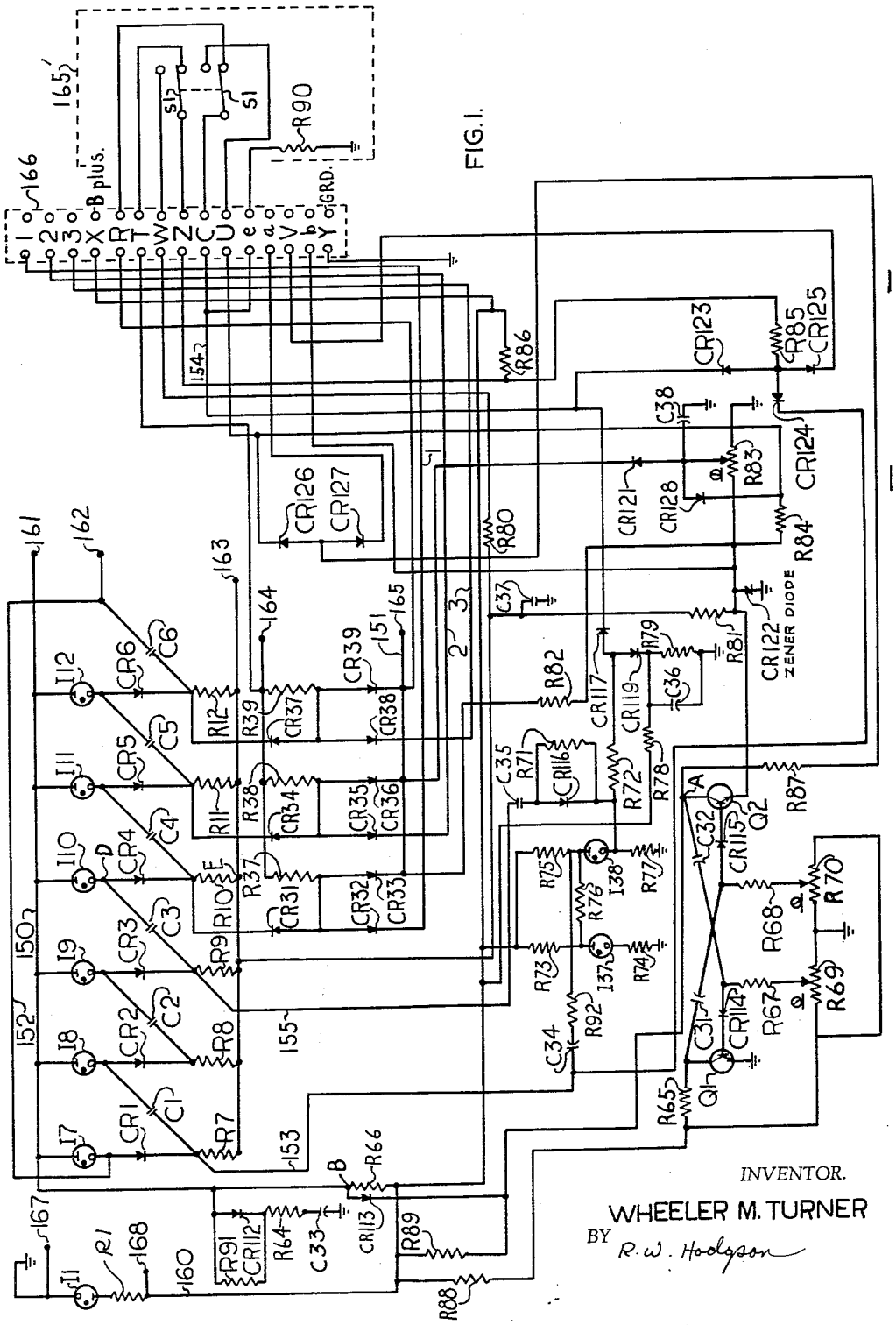
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TIME DIVISION MULTIPLEXING SYSTEM

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TIME DIVISION MULTIPLEXING SYSTEM

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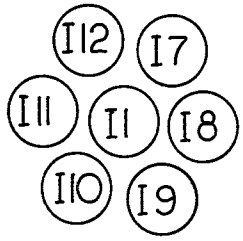


FIG. 2.

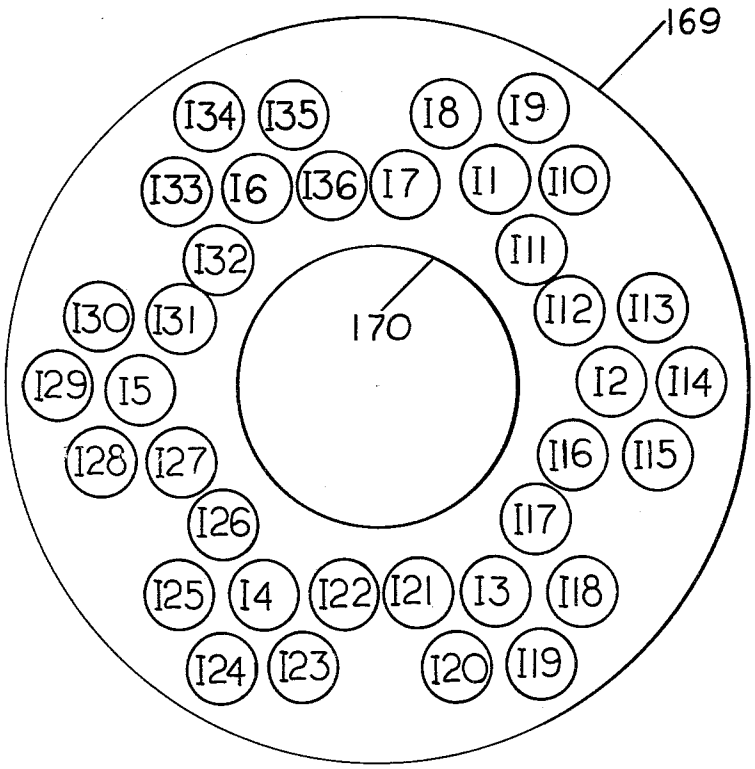


FIG. 3.

INVENTOR.
WHEELER M. TURNER
BY R. W. Hodgson

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TIME DIVISION MULTIPLEXING SYSTEM

Wheeler M. Turner, Whittier, Calif., assignor to Arnoux Corporation, Los Angeles, Calif., a corporation of California

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6 Claims. (Cl. 179—15)

Generally speaking, the present invention relates to the commutator art and, more particularly, to an electronic commutator for commutating a large number of information channels of individual information signal input circuits into a common output lead usually for the purpose of transmitting information out of these information channels on a single carrier. The electronic commutator of the present invention comprises improved apparatus for time division multiplexing, which is presently considered to be the best means for extending the number of information channels that can be telemetered from a device or vehicle under test.

I am aware of the fact that various commutators have been invented and developed heretofore. However, all such prior art commutators, known to me, have major disadvantages of one type or another.

For example, most such prior art commutators, known to me, are of the mechanical type which limits the maximum rate of sampling and which, therefore, has resulted in the prior art design and use of low-rate receiving equipment.

Furthermore, certain of said prior art mechanical commutators employ a switch element adapted to relatively rotate with respect to, and sequentially contact, a plurality of switch elements whereby to sequentially connect a plurality of input circuits to a common output circuit. It is obvious that this prior art type of mechanical commutator is necessarily limited to quite low commutation rates. Furthermore, electrically speaking, it is a "noisy" and otherwise undesirable arrangement. Also, the contacts wear away rapidly. These are only a few of the disadvantages of this prior art type of mechanically driven commutator.

Most prior art electronic commutators, known to me, are of relatively complex, difficult to maintain, costly and/or fragile construction—often employing cathode ray tubes, or the like, having a plurality of independent electrodes therein adapted to be sequentially impinged by a cathode ray beam cyclically swept over the plurality of electrodes. This type of construction has a very limited field of use because of its complexity, cost, and fragility.

Also, other types of prior art electronic, magnetic and non-mechanical commutators have been invented and developed heretofore, but all such known to me have major disadvantages of one type or another which limit the general use thereof in high rate commutating by time division multiplexing.

Generally speaking, the apparatus of the present invention comprises: a sequential counter including a plurality of electrically sequential counter circuit portions connected in parallel between an intermittently positive timing voltage and a negative potential point, each of said counter circuit portions including a similarly electrically conductively directed voltage-time responsive electrical discharge device which is non-conductive until the potential applied thereacross rises to a firing value, after which it is conductive in one direction until said potential drops to an extinction value, after which it again becomes non-conductive, each of said counter circuit portions including a preference voltage-producing means cooperable, in response to current conduction through said electrical discharge device, to produce a preference voltage; a plurality of sequentially operative preference voltage-transfer circuits, each including coupling means and

each being connected between different immediately electrically adjacent and sequential ones of said plurality of electrically sequential counter circuit portions in preference voltage transferring relationship whereby termination of current conduction through a counter circuit portion will cause transfer of said preference voltage to the electrically sequentially next counter circuit portion and effectively across the electrical discharge device in said next counter circuit portion and in additive relation to said intermittently rising positive timing voltage applied thereto and will cause preferential firing and conduction of said electrical discharge device in said next counter circuit portion; a plurality of information signal gates provided with a common output circuit, each of said gates being provided with an individual information signal input circuit normally effectively electrically isolated from said common output circuit, each of said gates being coupled with respect to the corresponding counter circuit portion and being gatingly responsive to conduction therethrough in a gate-opening direction whereby to effectively electrically connect the corresponding information signal input circuit with respect to said common output circuit and to provide therein an intermittently sampled information output signal corresponding in magnitude, within a predetermined range of magnitudes, to an information input signal carried by said information signal input circuit; said intermittently positive timing voltage having a rising leading edge waveform upper portion beginning at a potential less than the firing potential of any of said electrical discharge devices and which slopes upwardly therefrom in a manner providing optimum values of voltage and rise time to fire and initiate conduction through that particular electrical discharge device having said preference voltage thereacross.

In a preferred general form of the present invention, said intermittently positive timing voltage is supplied by clock means (usually electronic clock means) which is further provided with waveform shaping means operative at a predetermined positive level of said intermittently rising timing voltage less than the firing potential of any of said electrical discharge devices to control the remainder of the rise time thereof in a manner providing optimum values of voltage and rise time to fire and initiate conduction through that particular electrical discharge device having said preference voltage thereacross.

Also, in a preferred general form of the present invention, certain of said counter circuit portions which are not coupled to said information signal gates may comprise synchronization signal gating means effectively connected with respect to said common output circuit and operative in response to an input signal to provide in said common output circuit an intermittent repetitive synchronization signal distinguishably differing from any of the intermittently sampled information output signals.

In one preferred form of the present invention, each of the voltage-time responsive electrical discharge devices referred to generically above may take the form of a gaseous diode having a cathode, an anode, and an ionizable gas therebetween. This form of the present invention may also include means limiting conduction current through any of said electrical discharge devices, thereby limiting the degree of ionization of the gas contained therein, and correspondingly reducing the deionization time thereof—for example, the conduction current limiting action may be to an extent such as to cause electrode glow over substantially less than the full area of the anode of the gaseous diode.

In one preferred form of the present invention, said timing voltage may consist of an alternating intermittent series of positive pulses and negative pulses. In this specific form of the present invention, each of the intermittent negative pulses of said intermittent timing voltage

is applied to the anode of that particular gaseous diode which has just been conducting during the preceding positive pulse of said intermittent timing voltage, which rapidly deionizes the gas in said gaseous diode by attracting closely adjacent ions to the negatively charged anode thereof.

One preferred form of the present invention may also include semiconductor means effectively isolating negative transients, caused by the firing of any of said electrical discharge devices, from said electronic clock means.

In one preferred form of the present invention, the gas in each of said gaseous diodes may be exposed to non-varying excitation (such as radiation or the like) for stabilization of the degree of pre-firing ionization in all of said gaseous diodes.

It should also be noted that the present invention is additionally directed to subcombinations of the above complete inventive combination, such as the sequential counter individually, the electronic clock means individually, the waveform shaping means individually, the synchronizing pulse-producing means individually, and/or any one of the information signal gates individually, or to various combinations thereof.

From the above description of basic and preferred forms of the present invention, it will be apparent to those skilled in the art that the prior art disadvantages mentioned hereinabove are virtually entirely eliminated and overcome in and through the use of the apparatus of the present invention.

For example, since the present invention does not employ mechanically movable switch elements in the commutator, it is capable of extremely high commutation rates.

Furthermore, because of the above, the commutator of the present invention is not subject to mechanical wear, nor is it characterized by undesirable electrical qualities of the type hereinbefore mentioned in connection with mechanically driven prior art commutators.

Furthermore, the present invention is of exceedingly small, lightweight configuration and is of such simple construction as to be virtually foolproof and to require virtually no maintenance.

With the above points in mind, it is an object of the present invention to provide apparatus for commutation at extremely high rates.

It is a further object of the present invention to provide a commutator without mechanically movable commutator elements.

It is a further object of the present invention to provide a commutator without commutator brushes or commutator segments.

It is a further object of the present invention to provide commutation by sequentially firing individual ones of a plurality of gaseous diodes, or the like, in an arrangement wherein the firing of each gaseous diode applies a preference voltage to the electrically sequentially next diode, and wherein the firing of any given gaseous diode applies a gate-opening voltage to a corresponding information signal gate whereby to connect an information input circuit through said gate to a common output circuit.

It is a further object of the present invention to provide commutation of the type set forth in the preceding object wherein a rising voltage having a controlled slope in the region of the firing voltage of any of the plurality of gaseous diodes is applied to all of said gaseous diodes—said rising slope having a rise time such that the voltage applied to that particular one of the gaseous diodes having the preference voltage thereacross, will fire.

It is a further object of the present invention to provide apparatus of the character set forth in the two preceding objects wherein conduction current through a discharging gaseous diode is limited whereby to limit the degree of ionization of the gas contained therein and to correspondingly reduce the deionization time thereof.

It is a further object of the present invention to provide apparatus of the character set forth in the preceding object wherein the anode of a discharging gaseous diode is swung negative immediately after conductive discharge therethrough whereby to rapidly deionize the gas in said gaseous diode by attracting closely adjacent ions to the negatively charged anode.

It is a further object of the present invention to provide a commutator of the type set forth hereinabove including semiconductor means effectively isolating negative transients caused by the firing of any of said electrical discharge devices, from said electronic clock means.

It is a further object of the present invention to provide a commutator of the type set forth hereinabove wherein the gas in each of said gaseous diodes is exposed to non-varying excitation (such as radiation or the like) for stabilization of the degree of pre-firing ionization in all of said gaseous diodes.

It is a further object of the present invention to provide a small, compact, light, foolproof commutator adapted to both low speed and high speed commutation by time division multiplexing.

Other and allied objects will be apparent to those skilled in the art after a careful persual, examination, and study of the accompanying illustrations, the present specification, and the appended claims.

To facilitate understanding, reference will be made to the hereinbelow described drawings, in which:

FIG. 1 is a fragmentary electrical schematic circuit illustrating one specific form of the present invention;

FIG. 2 is a fragmentary diagrammatic view illustrating one specific physical configuration whereby the gas in each of the gaseous diodes comprising the electrical discharge means are exposed to non-varying radiation for stabilization of the degree of pre-firing ionization in all of said gaseous diodes; and

FIG. 3 is another fragmentary diagrammatic view of a thirty channel form of the present invention and illustrates another specific physical configuration wherein thirty counter gaseous diodes are exposed to non-varying radiation from six illuminating gaseous diodes for stabilization of the degree of pre-firing ionization of all of said thirty counter gaseous diodes.

The specific form of the present invention illustrated in FIGS. 1 and 2 may be said to comprise an electronic clock or frequency determining means taking the form of the multivibrator shown at the lower left of FIG. 1, the multichannel sequential counter shown at the top of FIG. 1 (exclusive of the illuminating gaseous diode at the top left of FIG. 1), the information matrix or plurality of information signal gates shown positioned directly below the sequential counter in FIG. 1, and a master pulse or frame synchronization pulse generating means positioned to the right of the electronic clock in FIG. 1 and effectively connected with respect to the three left gaseous diodes in the sequential counter at the top of FIG. 1.

In the specific example illustrated in FIG. 1, the unit is adapted to be supplied with electric power from a floating 150 volt power supply with its negative, or ground, return applied to a constant voltage dropping device such as a zener diode and with its positive lead applied to the B plus terminal of the unit indicated by the marking B plus in FIG. 1. The power supply and the ground return zener diode mentioned above are not shown since such arrangements are well known. An internal zener diode CR122 returns to ground. Therefore, there are three effective voltages effective in the unit. They are approximately plus 143 volts, ground, and minus 7 volts.

In the specific form of the invention illustrated in FIG. 1, the electronic clock is a modified multivibrator circuit, although the invention is not limited to this specific construction.

In the sequential counter shown in FIG. 1, the gaseous diodes take the form of a neon diode type NE76, al-

though the invention is not limited to this specific component.

Referring to FIG. 1, point A normally will be at a negative 6 volt potential during the normally conducting state of the clock, and at a positive 100 volt potential during the normally open state. Point B will be at a minus 3 volt potential when point A is at that potential; however, point B will never reach the positive 100 volt potential due to the action of the single-polarity integrator comprised of semiconductor or rectifier CR112, resistor R91, resistor R64, and condenser C33, and the firing of one of the gas diodes in the sequential counter.

To illustrate the operation of the counting circuit, assume that point A is positive and that gas diode I10 corresponding to the first information segment or gate is conducting. Point A will be at plus 100 volts and point B will be at approximately plus 90 volts. Point D will be at approximately positive 14 volts and point E will be at approximately minus 3 volts. At the instant of firing of gas diode I10, a 17 volt positive pulse will be applied to the junction of rectifier CR4, condenser C4, and load resistor R10. The 17 volt pulse will be coupled through C4 and thence to point E, thereby charging C4 to a 17 volt positive potential.

Point A now returns to its minus 6 volt potential, driving the anode of gas diode I10 to negative 6 volts and extinguishing the bulb. At the instant of bulb extinction, point D returns to the same potential as point E. Therefore, a negative 17 volt potential is applied to the anode of rectifier CR5 and to the cathode of gas diode I11. At this point, all of the gas diodes, except I11, will have a negative 3 volt potential applied to their respective cathodes, while I11 will have the negative 17 volt potential applied to its cathode.

Point A now, according to the normal operation of the clock, returns to a positive 100 volts, point B rises from its negative value towards a positive value, and when point B reaches a positive potential great enough to cause the firing potential to be applied across gas diode I11, said diode will fire, and will have fired because of its 17 volts preference over the remaining bulbs. When gas diode I11 fires, its normal regulating action causes a limiting of the final positive potential that point B can reach. Capacitor C33 is charged to approximately the same value of positive voltage that point B reaches during the maintaining state of diode I11. During the "Off" cycle, capacitor C33 discharges according to a rate determined by the value resistor R91. This rate is selected in normal operation to allow C33 to discharge to a point approximately 3 volts below the firing potential of the counter gas diodes.

The operation of this circuit, therefore, is to cause the sharp leading edge of the pulse being applied to the counter bus 150 to break and rise at a controlled slow rate at a predetermined point—which point is always about 3 volts below that of the firing voltage. The values of resistor R66, resistor R64, and condenser C33 are so selected that during this charging cycle, the slope of the wave form will be at a rate that will assure the firing of the proper neon tube. Point A according to the normal operation of the clock will return to a negative 6 volts; gas diode I11 will extinguish; the junction of CR5, load resistor R11, and C5 will return to a negative 3 volt potential, and the junction of gas diode I12 and rectifier CR6 will assume a minus 17 volt potential. During this "Off" cycle, C33 is discharging at the aforementioned predetermined rate, point A switches to the positive state, point B rapidly rises until C33 starts being charged again. Point B then slowly increases until gas diode I12 fires, etc. It should be understood that any desired number of counter circuit portions similar to the first three containing gaseous diodes I10, I11, and I12 may be similarly connected by means of terminals 161, 162, and 163—it being understood that the lead 152 is always connected to only the sequentially last one of the counter circuit portions controlling information signal gates, which, in the particular example illustrated, is the counter circuit portion containing the gaseous diode I12. This will provide virtually any desired number of counting channels. Additional gaseous diodes in excess of I10, I11, and I12 are not shown in FIG. 1 since the showing of I10, I11, and I12 quite adequately illustrates the inventive concept involved and no useful purpose would be served in adding to the complexity of the drawing by adding additional gaseous diodes.

When a potential only slightly greater than that required to fire a gas diode is applied, the firing will not occur immediately but will be delayed. That delay will be a function of the ambient light level, temperature, the presence of radio activity, and other ionization causing mechanisms. This delay is a real number and is variable for any given bulb. The purpose of the controlled rise is to enable the preferred neon tube to have more than its minimum firing potential applied for more than the maximum time required for ignition before the potential applied to any other neon tube reaches that tube's minimum firing level. For clarity, referring to the basic counter circuit, when a neon tube fires, it causes a positive potential to be developed across its associated load resistor through its coupling diode. The positive pulse is coupled through the coupling condenser through the next stage's diode in the forward direction, thus charging the coupling capacitor to the full potential developed across the load resistor. Upon the extinguishing of a neon tube, the potential across its load resistor returns to zero which places an equal negative potential across the coupling diode of the next succeeding stage. Due to the fact that this potential is negative and is applied to the anode of that diode, the potential will remain there for a relatively long time. When the positive bus of the counter rises, that tube with a negative voltage applied to its cathode will fire in preference to the others. Therefore, a very long counting chain is possible.

In the data commutator application described, the voltage developed across the respective load resistor such as R10, R11, R12, etc., is used as an enabling voltage for a corresponding plurality of information signal gates each in the form of a diode matrix, to cause successive sampling of a plurality of information signals; said signals being applied to a common output bus in time sequence.

To describe the action of this circuit, assume that all neon tubes are extinguished and point E is at a negative 3 volt potential. A relatively high positive potential is applied to resistors R37, R38, R39, etc. This positive potential causes a current to flow through rectifiers CR31, CR34, CR37, etc., and through their respective counter load resistors R10, R11, R12, etc. Since point E is at a negative potential and since the ratio of R10 to R37 is quite high, even though the positive potential applied to R37 may be quite high, the voltage developed across R10 will be relatively small, never allowing the potential across R10 to exceed 1 volt.

Therefore, the potential at the junction of CR31 and R10 never rises above minus 2 volts. This condition exists, in the absence of a firing potential on the counter bus, on all of the information channels. Therefore, the common output bus will be at that approximately negative 2 volt potential. When neon tube I10 fires, the voltage across its load resistor R10 will rise to at least a positive 6 volts with respect to ground, therefore, enabling the voltage at the junction of CR31, R37, CR32, and CR33 to rise to a possible 6 volts.

Assume in this instance, that the information voltage applied to this channel is 5 volts. The aforementioned junction is capable of rising to 6 volts; however, as soon as it exceeds the 5 volt information level, CR32 conducts and limits the voltage to that value. The output bus, while normally at a negative potential, is raised to that 5 volt level due to the conduction of CR33. The junction of the three matrix diodes (similar to CR31, CR32, and CR33 in the gate) and their resistor (similar to the

resistor R37 in the first gate) on all of the other channels are at a negative potential; this one only being positive. Therefore, this 5 volt information level present on the output bus looks backwards into all of the other matrix diodes which present a high impedance load to the information signal.

Assume for another instance that the information signal applied to the first channel is zero volts. The junction of said first channel's three diodes and matrix resistor starts to rise to a positive 6 volts but when it reaches zero volts, CR32 conducts and limits the voltage at zero and since the output bus is at a negative potential, CR33 conducts and causes a zero volt potential to be applied in the output bus. In the event a highly negative signal is applied to the input of the channel, CR32 will conduct; however, CR33 will not, and no signal will be applied to the output bus. In the event a highly positive signal is applied to the input of the channel, CR32 will remain cut off due to the fact that the junction point cannot rise above 6 volts, therefore, the output bus will see a potential of 6 volts and no more.

In the circuit described, the output bus **151** is held at a negative potential by R82. This negative potential is limited to a controlled and adjustable value by the limiting action of CR121, C38, R83; however, upon the application of an information pulse to the bus, the limitor ceases to function and presents a very high impedance to the positive voltage applied to the bus, and the current flow is only that required to develop the positive voltage across R82—a relatively high value resistor.

It should be understood that any desired number of information signal gates, similar to the first three information signal gates shown in FIG. 1 and described in detail immediately hereinabove, may be similarly connected by means of terminals **164** and **165** and by the provision of additional information signal input circuits similar to the first three already described and indicated by the reference numerals **1**, **2**, and **3**. Thus by the provision of additional counter circuit portions as described hereinabove and by the provision of corresponding additional information signal input circuits and gates (or diode matrices) it is possible to provide commutation of virtually any desired number of information channels.

As an example illustrative of a typical application of the commutator of the present invention, it might take the form of a 27 channel standard P.A.M. FM-FM commutator for telemetering use by time division multiplexing. In such a specific embodiment the counter circuit may employ a ring of 30 gaseous diodes of the type shown at I10, I11, and I12, all of which may be similarly sequentially connected in the same manner as I10, I11, and I12, as indicated hereinabove. Such a typical 27 channel commutator may also have additional information signal gates similar to the three information signal gates shown in FIG. 1 and connected as indicated hereinabove. Each of such additional information signal gates being adapted to include three rectifiers and a resistor corresponding to and connected in the manner of those contained in the first information signal gate, for example as indicated at CR31, CR32, CR33, and R37. Twenty-seven of the counter circuit portions beginning with I10, I11, I12, etc., and the corresponding 27 information signal gates connected thereto may be used for information and the remaining three counter circuit portions including the gaseous diodes I7, I8, and I9 may be used for the generation of a standard channel synchronizing pulse which is normally equal in length to three information "On" periods, and two information "Off" periods. In sequence of operation, after the last gaseous discharge diode in the sequence of such tubes beginning with I10, I11, I12, etc., has fired, a preference voltage is applied to the first gaseous diode I7 through the lead **152**, which causes said gaseous diode I7 to be fired during the next application of a positive pulse to the anode thereof, in the manner hereinbefore described. This causes a positive pulse to be applied from the junction of the diode rectifier CR1, load resistor R7, and coupling condenser C1 through the lead 153 and through capacitor C34 and resistor R92 to the junction of resistor R75 and gaseous diode I38.

The gaseous diode I38 is normally extinguished, its anode being held below firing potential by the voltage dividing action of resistor R75 and resistor R76. The positive pulse from the first counting circuit portion of the counter containing the gaseous diode I7 raises the anode of the gaseous diode I38 above its firing potential, which causes it to fire, thereby causing a positive voltage to appear at the junction of gaseous diode I38 and resistor R77. This positive voltage is applied through resistor R72 to the master pulse limiter consisting of resistors R78 and R79, condenser C36 and diode rectifier CR119. The clipped voltage is then applied through diode rectifier CR117 to the output bus **154**. The condition just described can be maintained indefinitely.

However, upon current conduction through the gaseous diode I9, which is the sequentially last of the three gaseous diodes I7, I8, and I9 involved in producing a synchronizing pulse, a positive pulse is applied through lead **155** to the cathode of the gaseous diode I38, which causes it to extinguish. Although the diode I38 is extinguished on the leading edge of the counter pulse produced when I9 conducts, that pulse is also applied to the master pulse limiter previously specifically described and to the output bus causing said bus to remain at a positive level through said last pulse produced as a result of conductive discharge through the gaseous diode I9, and causing return to the negative blanking level only at the end of said last pulse.

It should be noted that at the right of FIG. 1 a plurality of exterior connection terminals for connection of exterior leads with respect to interior leads of the unit are indicated and that these would normally comprise any standard type of electrical connector means, the assembly of which is indicated in broken line form at **166**. Certain of the connections are thought to be obvious and will not be specifically described in detail. It will be noted that an external control is indicated generally within the confines of the broken line box indicated at **165'** and that this includes leads connected as indicated and a switch S1 normally positioned in the position shown when the apparatus is to operate as multiple channel commutator means in the manner described hereinbefore. It should be noted that when the switch S1 is moved from the position shown in FIG. 1 to its other extreme, this acts to remove the positive voltage from the respective summing matrix resistors in each of the information signal gates; therefore, effectively disabling the commutator with regard to the normal input channels and substituting the output of the clock through a single matrix circuit, in summation with the master pulse circuit, to derive a pulse train substantially the same in appearance to that which is derived through normal operation but which has as its information output an amplitude value proportionate to the input of the aforementioned single matrix.

The leads connected with terminals **1**, **2**, and **3** indicate the input leads carrying information input signals which are adapted to be commutated and gated by the first three channels indicated in FIG. 1 and described hereinbefore. It should be noted that any desired additional number of additional information input circuits are within the scope of the present invention—it only being necessary to add additional counting and additional gating circuits to correspond therewith. It should also be noted that the output terminal is indicated at C. The reference character *a* indicates a calibration terminal which may be used for calibration purposes. The reference character V indicates a 5 volt reference terminal. The reference character *b* indicates the B minus power supply terminal, and the reference character X indicates the B plus power supply terminal.

The anode of the diode I1 is connected through the resistor R1 to positive lead 160 while the cathode of said gaseous diode is connected to ground; therefore, causing said gaseous diode I1 to conduct current in a steady manner and to emit stable non-varying radiation which is adapted for use in exposing the gas within all of the gaseous diodes I7, I8, I9, I10, I11, and I12 in the counter to non-varying radiation for stabilization of the degree of pre-firing ionization in all of said gaseous diodes. In this connection, FIG. 2 is a typical diagrammatic representation of the physical placement of said illuminating gaseous diode I1 within an arrangement of the counter gaseous diodes I7, I8, I9, I10, I11, and I12 in a manner whereby steady state radiation from the illuminating gaseous diode I1 will be received equally by all of the surrounding counter diodes I7, I8, I9, I10, I11, and I12. It should be understood that normally the arrangement of seven gaseous diodes shown in FIG. 2 would be completely enclosed in an opaque housing whereby the only illumination would be that steady state illumination emanating from the illuminating gaseous diode I1.

It should be understood that any desired number of illuminating gaseous diodes (and accompanying resistors) similar to the illuminating gaseous diode I1 (and its resistor R1) may be similarly connected in parallel with the illuminating gaseous diode I1 (and resistor R1) by means of terminals 167 and 168.

FIG. 3 illustrates one such arrangement (similar to that shown in FIG. 2) modified to provide for a 27 information channel commutator of the type hereinbefore referred to. In this structure there are 27 information channel counter tubes, I10 through I36, in numerical sequence and three master synchronizing pulse producing counters I7, I8, and I9. In this arrangement there are six illuminating gaseous diodes I1, I2, I3, I4, I5, and I6, all similar to the gaseous diode shown in FIG. 1 and all connected in parallel thereto in the manner described hereinabove. The 30 counter gaseous diodes I7 through I36 are each arranged in a circular arrangement of five counter diodes with an illuminating diode in the center thereof, and with each arrangement of five counter diodes and one illuminating diode being circularly arranged as shown in FIG. 3 and being adapted to be positioned within a circular exterior housing closed at the top and bottom thereof so as to exclude all light but that emanating from the illuminating gaseous diodes I1, I2, I3, I4, I5, and I6. Also it should be noted that the assembly of gaseous diodes shown in FIG. 3 has a transparent acrylic resin interior cover 169 which acts to evenly distribute light to all of the counter diodes and that the physical configuration of the assembly of diodes and said interior cover is such as to provide a hollow center recess 170, which may be used to house remaining components of the commutator, to provide a very compact unit.

For the purpose of providing a full and complete disclosure of aspects of the present invention which are of major importance, the following brief summation is set forth:

The counter circuit employed requires no reset means to prevent its getting into a condition, or state, wherein it will not count. Due to the fact that the potential applied to the positive counting bus can, in time, reach a value far in excess of that required to cause ignition of a neon tube, it is assured that a neon tube will be fired. Therefore, no means is required to establish a condition to enable counting.

No reset signal is required to prevent the counter from getting into a condition wherein more than one count progresses through the chain at any one time. Due to the fact that the counter positive bus is limited to a value which is a function of the regulating potential, or maintaining voltage of a neon tube, it is evident that it is unlikely that another neon tube can be fired. In the event of such spurious firing, a voltage will be developed across the two respective succeeding neon tube anodes which will cause them to tend to fire in preference to any of the remaining neon tubes. However, upon the firing of one of the two preferred tubes, the counter bus will assume a value determined by the regulating potential of that neon tube, and it is very unlikely that the second preferred neon tube will fire. In the event that the second one should fire, the process will simply be repeated until only one is fired.

The counter circuit employs current values that cause the anodes to be only partially covered with glow. This partial electrode glow characteristic results in the generation of a small number of ions during the maintaining time, therefore, there is a relatively short time required for deionization. In the event a larger current value is used, complete electrode glow will result, a substantially larger number of ions will be generated, and the deionization time for any given tube will be substantially increased.

The unit described utilizes a negative potential applied to the neon tube anodes as a means of accomplishing deionization rapidly. The mechanism is as follows: Upon the firing of a neon tube, a number of ions are formed which form a cloud physically adjacent to the anode. When the applied potential is reduced to a value less than that required to sustain the glow, ions are no longer generated. Under these conditions, that cloud of ions adjacent to the anode will travel to the cathode and there be dissipated. In this circuit, when the potential applied to the neon tube is reduced to the value less than that required for maintenance of the glow, it is quickly brought to a value that causes the cathode to be positive in respect to the anode. Therefore, the ion cloud has only to travel the relatively short distance to the anode to be dissipated, resulting in a substantially reduced deionization time.

The action of the previously described integrating circuit which causes a controlled slope of the pulses applied to the positive counter bus is such that upon the firing of any neon tube, the bus is regulated at a voltage which is held substantially constant by the integrator. This state allows a relatively large variation in load to be applied to the normal load resistor associated with the counter with minimized effect.

This device employs a novel charge transfer circuit from counter segment to counter segment as exemplified in the preceding description and in the figures.

The device employs a controlled pulse amplitude rise time to insure miscount proof operation. Reference to the preceding theory of operation discloses that through the application of a sloping pulse to the counter positive bus, the preferred neon tube must fire before any other tube. It is though the utilization of this controlled slope that the effect of the firing time variable characteristic of gas diodes can be eliminated. This is the particular unique feature that makes this counting circuit reliable in operation as opposed to all previous attempts.

This device uses a diode coupled clock multivibrator with one side common to the counter bus to conserve parts. The diode referred to in the attached schematic diagram is disclosed to be CR113 and enables the clock to be disconnected from the counting bus at the instant of neon tube firing and, therefore, removes the resultant negative transient associated with the neon tube firing from the clock circuit. If, in the absence of this diode, that transient were allowed to manifest itself at the collector of the multivibrator transistor, it would be coupled through the multivibrator time determining capacitor to the base of the opposite stage and cause immediate recycling of the multivibrator and consequent instability.

Normal sequential counter circuits employ short dif-

ferentiated pulses as their drive or control means. The resultant counter output is a series of pulses with a minimum spacing between pulses. In the counter described, the input wave form is coupled to the counter, as opposed to differentiation and the resulting counter output pulse spacing is substantially equal to the spacing determined by the input wave shape. For example, if the clock multivibrator employs a 50–50 duty cycle, then the spacing between the sequential output pulses will be substantially equal to the individual pulse widths.

The counter circuit described employs a plurality of neon tubes with a D.C. steady state voltage applied thereto for the generation of light. Said light being nonfluctuating and of relatively constant intensity. Said light is applied to the counter neon tubes as a "keep alive" means. This enables the counter to be operated in total darkness. The counter will be normally housed in a totally enclosed container, therefore, the only light ambient to the counter bulbs will be that generated by the "keep alive" neons with the result that a high degree of stability is achieved.

This commutator device employs a counter which generates output pulses that swing from a negative voltage to a positive voltage in combination with a D.C., high voltage, high impedance summing source that allows the output of each individual information matrix to swing from a small desired negative level to a positive level only slightly in excess of the maximum anticipated information level.

The device uses a D.C. summing source. In previous electronic commutator devices, it has been necessary to apply pulses to the individual information matrices which have as their width or time duration the quantity desired. This has been necessitated because of the substantially 100% duty cycle of the counter output. In the case of a 50–50 duty cycle output requirement such as is commonly encountered in P.A.M. FM–FM applications, that aforementioned controlled duration pulse is the means by which the 50–50 duty cycle is achieved. In the subject device, the normal counter output pulse width can be made equal to that desired, therefore, a D.C. source can be used in the summing matrix.

A low voltage counter output pulse only slightly greater in amplitude than the maximum anticipated information amplitude is utilized only to enable a gate which derives its internally generated signal level from a high impedance, high voltage D.C. source. The result of this technique is that the signal input impedance requirement is minimized. In other words, due to the high impedance of the internally generated voltage, proper limiting can be achieved into a relatively high signal source impedance.

The subject device employs a counter that generates the proper width output pulse which negates the requirement for signal source pulse summation.

The subject device employs a high impedance negative voltage bias source applied to the output bus across which source all information pulses are generated. Under these conditions, a minimum current which has a real value flows through both matrix diodes at all information levels including zero volts. The effect of this is to insure near perfect linearity from absolute zero voltage information up.

The subject device through the use of a negative output level clamping, or limiting circuit in association with the information matrices ensures that no negative input signal can cause the output to drop below a prescribed level. Said level always being more positive than the normal negative blanking level.

The subject device through the utilization of a low impedance, low level counter output pulse, insures that the information output will never rise above a nominal and controlled level resulting from an excessively high positive input signal.

The subject device has provision for the application of a full information, normally 5 volt signal to be applied to the master pulse circuit which will result in the generation of a full scale reference pulse which will occur during the first nominal ⅛ of the total width—or time duration—of the master channel synchronizing pulse. Said reference pulse having as its time duration a quantity substantially the same as all normal information pulses.

The subject device has provision for the application of information to one point which results in the generation of a normal pulse train, including the master synchonizing pulse, said normal pulse being of substantially the same amplitude and being a known function of the single input, and being normally used for calibration purposes.

The subject device employs means for providing a negative "blanking level" between information pulses, said "blanking level" being of a known and adjustable quantity.

It is frequently convenient to be able to apply an information signal to one point of these commutators and derive therefrom a normal output pulse train which has as its pulse amplitudes a quantity proportionate to the input. In the circuit described, this characteristic is achieved through the removing of the positive voltage to the respective summing matrix resistors, therefore effectively disabling the commutator with regard to the normal input channels, and substituting the output of the clock through a single matrix circuit, in summation with the master pulse circuit, to derive a pulse train substantially the same in appearance to that which is derived through normal operation but which has as its information output an ampitude value proportionate to the input of the aforementioned single matrix.

It should be noted that the commutator of the present invention is not limited to any specific commutation rate or to any specific number of channels, although the 27 information channel version (30 total channels) referred to hereinbefore and having component values as set forth hereinafter is intended for sampling each individual channel ten times per second or, in other words, sampling all 30 of the channels (including the three master pulse producing channels) so as to produce 300 samples per second in the common output lead. Furthermore, the commutator of the present invention may be of the P.A.M. or the P.D.M. type. For example, converting the commutator hereinbefore described for P.D.M. use will simply require the removal of the master pulse circuit. Extending the number of channels requires only the addition of the required counter stages and information signal gates (or diode matrices). The commutation rate can be changed to include all of the standard rates used throughout industry by merely changing the values of nine of the components used—these nine components being resistor **R31**, capacitor **C33**, resistor **R66**, resistor **R89**, capacitor **C31**, capacitor **C32**, capacitor **C34**, resistor **R92**, and capacitor **C35**. This makes it possible to very easily and simply adjust the commutation rate of the cummutator of the present invention.

For the purpose of providing a full disclosure of one illustrative form of the present invention, the values of the componnets used in the hereinbefore mentioned **30** channel commutator adapted to commutate **27** information signal input channels will be set forth. It should be noted that these are not to be construed as limiting the invention but are merely to illustrate one specific operative form of the present invention. In said version each of the counter circuit load resistors such as **R7**, **R8**, **R9**, **R10**, **R11**, **R12**, and all of the rest of the load resistors used in the remaining 24 channels of counter circuit portions has a resistance of 60,000 ohms. Each of the counter circuit coupling condensers, such as **C1**, **C2**, **C3**, **C4**, and **C5** and all of the rest of the similar coupling condensers of the remaining counter circuit portions has a value of 33 micromicrofarads. Each of the information signal gate resistors such as **R37**, **R38**, **R39**, and all of the rest of the similar resistors in the remaining 24 information

signal gates has a value of 2.2 megohms. The resistor R1 connected in series with the illuminating gaseous diode I1 and each of the similar resistors connected in series with each of the five other gaseous diodes in the 27 information channel commutator hereinbefore referred to has a resistance of 100,000 ohms. The remaining components in said 30 channel commutator having an output of 300 p.p.s. are tabulated hereinbelow:

R31 is 470,000 ohms	R64 is 33,000 ohms
C33 is 0.03 microfarad	R88 is 15,000 ohms
R66 is 186,000 ohms	R65 is 43,000 ohms
R89 is 240,000 ohms	C32 is 0.0022 microfarad
C31 is 0.0047 microfarad	R68 is 430,000 ohms
R67 is 430,000 ohms	R70 is 50,000 ohms
R69 is 50,000 ohms	C34 is 0.01 microfarad
R87 is 2.2 megohms	R74 is 110,000 ohms

R92 has zero resistance in the 300 p.p.s. output version of the present invention although it has finite value at other commutation rates

R73 is 3.3 megohms	R75 is 3.3 megohms
R76 is 560,000 ohms	R78 is 3.9 megohms
R77 is 1 megohm	R79 is 47,000 ohms
C36 is 20 microfarads	R71 is 1 megohm
R72 is 220,000 ohms	R80 is 47,000 ohms
C35 is 0.02 microfarad	R81 is 1,500 ohms
C37 is 0.004 microfarad	R84 is 680,000 ohms
R82 is 750,000 ohms	C38 is 20 microfarads
R83 is 500,000 ohms	R86 is 39,000 ohms
R85 is 2.2 megohms	R90 is 500,000 ohms

Numerous modifications and variations of the present invention will occur to those skilled in the art after a careful study hereof and all such properly within the basic spirit, scope, and/or teachings of the present invention are intended to be included and comprehended herein as fully as if specifically described, illustrated, and claimed herein.

For example, it should be apparent that the electronic clock, the waveform shaping means, the counter means, the information gates, the master pulse producing circuit, and/or the arrangement of stabile illumination of the gaseous diodes may be individually modified and in certain cases some of said portions of the complete inventive combination set forth herein may be eliminated—and all within the basic scope of the present invention. For example, the clock means may take a number of different forms and, under some circumstances, an exterior timing signal may be applied to the present invention—in which case no interior clock will be needed. Furthermore, said exterior timing signal may have its waveform modified by the waveform shaping means of the present invention, or it may initially have the proper waveform shape in the region of firing potential for any of the gaseous diodes, in which case the waveform shaping means will not be needed. Furthermore, the specific type of information gates may be modified substantially from the embodiment shown herein since the counter means of the present invention may be employed to oeprate a number of different types of information gates.

The means for producing the synchronizing pulse may also be modified substantially.

The charge transfer circuit and/or the individual counter circuit portions may be modified within the spirit of the present invention. Furthermore, electrical discharge devices of a type other than those specifically described and illustrated herein may be employed.

In those forms of the present invention wherein the gaseous diodes are to be provided with a steady state excitation, means other than the illuminating gaseous diodes specifically disclosed herein, may be employed. In fact, any means capable of producing a desired stabilized degree of ionization by means of excitation of the gas within the counter gaseous diodes may be employed.

The exact compositions, configurations, constructions, relative positionings, and cooperative relationships of the various component parts of the present invention are not critical, and can be modified substantially within the spirit of the present invention.

The embodiments of the present invention specifically described and illustrated herein are exemplary only, and are not intended to limit the scope of the present invention, which is to be interpreted in the light of the prior art and the appended claims only, with due consideration for the doctrine of equivalents.

I claim:

1. Time division multiplexing apparatus comprising: a sequential counter including a plurality of electrically sequential counter circuit portions connected together in parallel for connection between intermittently positive timing voltage pulses and a negative potential, each of said counter circuit portions including a similarly electrically conductively directed voltage-time responsive electrical discharge device, each of said counter circuit portions including a preference voltage-producing means responsive to current conduction through said electrical discharge device and similarly electrically conductively directed semi-conductor means connected in series with said electrical discharge device and said preference voltage-producing means; a plurality of electrically sequentially operative preference voltage-transfer circuits, each including coupling means between different immediately electrically adjacent and sequential ones of said plurality of counter circuit portions in preference voltage transferring relationship, each of the preference voltage-transfer circuits and the coupling means comprising same having first end means connected to the preference voltage-producing means in the electrically sequentially first one of two electrically adjacent and sequential counter circuit portions and having second end means connected to the electron inflow end of said electrical discharge device between said semi-conductor means and said electrical discharge device; and a plurality of information signal gates provided with a common output circuit and individual information signal input circuits having the corresponding gates effectively electrically interposed therebetween when closed, each of said gates being coupled with respect to the corresponding counter circuit portion in gate-opening relationship in response to current conduction therethrough.

2. Time division multiplexing apparatus comprising: a sequential counter including a plurality of electrically sequential counter circuit portions connected together in parallel for connection between intermittently positive timing voltage pulses and a negative potential, waveform shaping and pulse-rise-time modifying means connected to said plurality of electrically sequential counter circuit portions for receiving and modifying the leading edge waveform of said intermittently positive timing voltage pulses, each of said counter circuit portions including a similarly electrically conductively directed voltage-time responsive electrical discharge device comprising a similarly electrically conductively directed voltage-time responsive diode having a cathode, an anode, and an ionizable medium therebetween, each of said counter circuit portions including a preference voltage-producing means connected to the cathode of said electrical discharge device for producing a preference voltage in response to current conduction through said electrical discharge device and similarly electrically conductively directed semi-conductor means connected in series with said electrical discharge device and said preference voltage-producing means and electrically positioned between the cathode of said electrical discharge device and said preference voltage-producing means; a plurality of electrically sequentially operative preference voltage-transfer circuits, each including coupling means between different immediately electrically adjacent and sequential ones of said plurality of electrically sequential counter circuit portions in preference voltage transferring rela-

tionship, the coupling means of each of the preference voltage-transfer circuits comprising coupling condenser means, and each of said preference voltage-transfer circuits having first end means connected between the preference voltage-producing means and the semi-conductor means device in the electrically sequentially first one of two electrically adjacent and sequential counter circuit portions and having second end means connected to the second one of said two counter circuit portions between the cathode of its electrical discharge device and its semi-conductor means; and a plurality of normally closed information signal gates provided with a common output circuit and individual information signal input circuits having the corresponding normally closed gates effectively electrically interposed therebetween when closed, each of said gates being coupled with respect to the corresponding counter circuit portion in gate-opening relationship in response to current conduction therethrough.

3. Apparatus of the character defined in claim 1, including means for applying said intermittently positive timing voltage pulses and said negative potential, respectively, to similar opposite ends of said plurality of parallel connected electrically sequential counter circuit portions.

4. Apparatus of the character defined in claim 1, including means for effectively applying said intermittently positive timing voltage pulses and said negative potential, respectively, to similar opposite ends of said plurality of parallel connected electrically sequential counter circuit portions; and waveform shaping and pulse-rise-time-modifying means effectively electrically interposed between opposite ends of said plurality of parallel connected electrically sequential counter circuit portions and said applying means for receiving from said applying means and modifying the leading edge waveform of said intermittently positive timing voltage pulses to have appreciable leading edge waveform rise time.

5. Apparatus of the character defined in claim 1, including positive pulse producing oscillator-clock means for producing said intermittently positive timing voltage pulses of a selected frequency and of appreciable rise time, said oscillator-clock means being provided with output means effectively coupled with respect to said plurality of electrically sequential counter circuit portions at the opposite ends thereof from said negative potential.

6. Apparatus of the character defined in claim 1, including positive pulse producing oscillator-clock means for producing said intermittently positive timing voltage pulses, said oscillator-clock means being provided with waveform shaping and pulse-rise-time-modifying means connected between said plurality of parallel connected electrically sequential counter circuit portions and said oscillator-clock means for receiving from said oscillator-clock means and modifying the leading edge waveform of said intermittently positive timing voltage pulses to have appreciable leading edge waveform rise time.

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