US 20030119281A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2003/0119281 A1

Suzuki et al. (43) Pub. Date: Jun. 26, 2003

(54) METHOD FOR MANUFACTURING SEMICONDUCTOR POWER DEVICE

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(21) Appl. No.: **10/310,021**

(22) Filed: **Dec. 5, 2002**

(30) **Foreign Application Priority Data**

Dec. 12, 2001 (JP) 2001-378725
Apr. 9, 2002 (JP) 2002-106327
Sep. 10, 2002 (JP) 2002-264135

Publication Classification

(51) **Int. Cl.**[7] **H01L 21/301**; H01L 21/46; H01L 21/78

(52) **U.S. Cl.** **438/460**

(57) **ABSTRACT**

A semiconductor device, which has a relatively low ON resistance, is manufactured using the following steps. First, a semiconductor wafer that includes a semiconductor layer and a semiconductor element layer, which is located on the semiconductor layer, is formed. Then, the wafer is ground evenly to a predetermined thickness from the side where the semiconductor layer is located. Next, the wafer is etched to a predetermined thickness from the side where the semiconductor layer is located while the periphery of the wafer is masked against the etchant to form a rim at the periphery. The wafer is reinforced by the rim at the periphery, so even if the wafer is relatively large, the wafer is prevented from breaking or warping at the later steps after the wafer is thinned by etching.

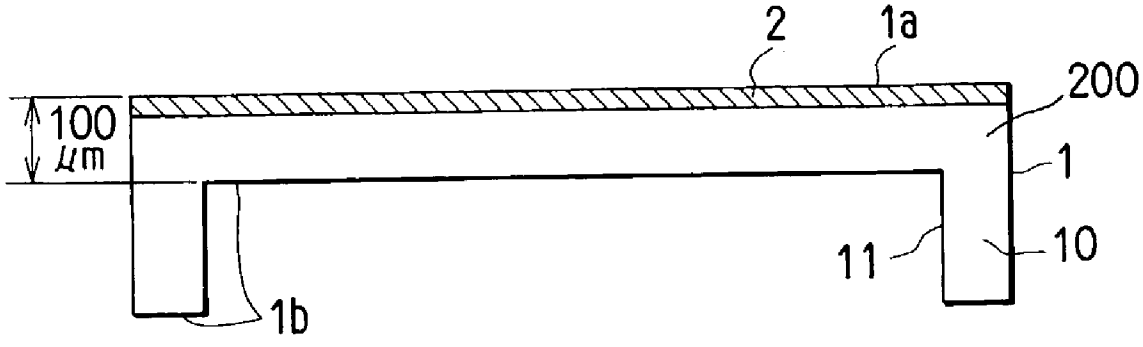


FIG. 1A

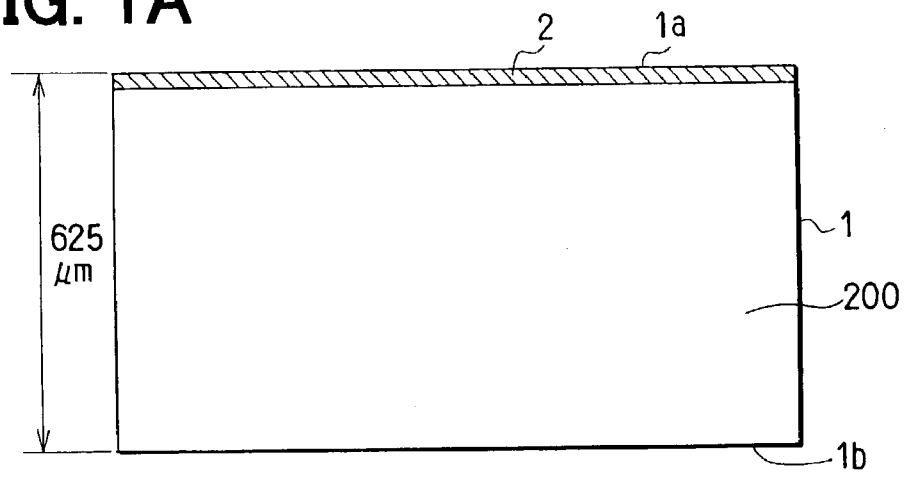


FIG. 1B

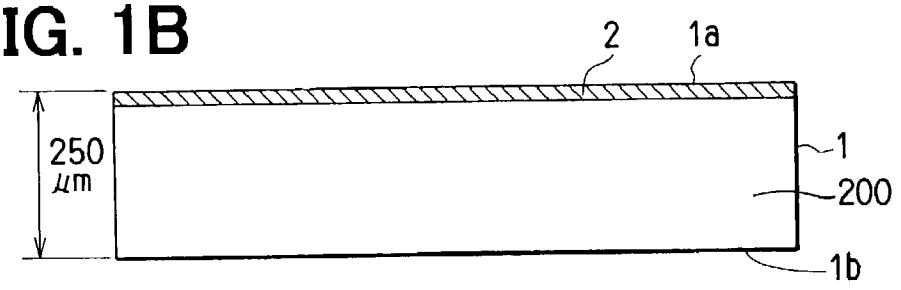


FIG. 1C

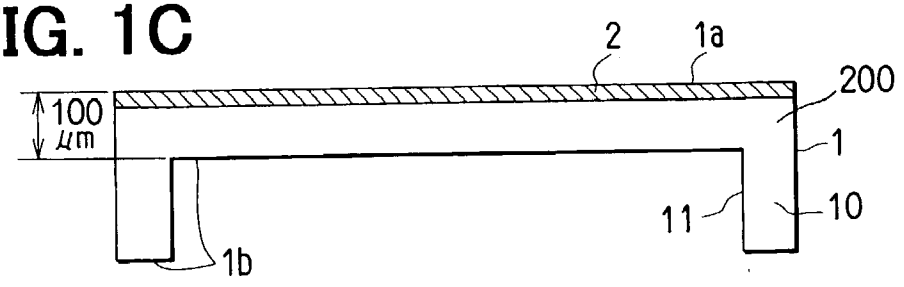


FIG. 1D

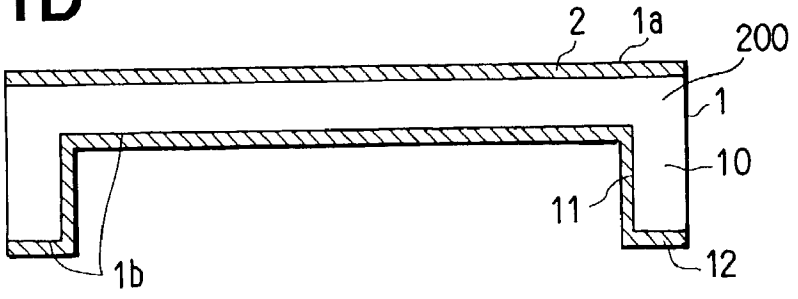


FIG. 2

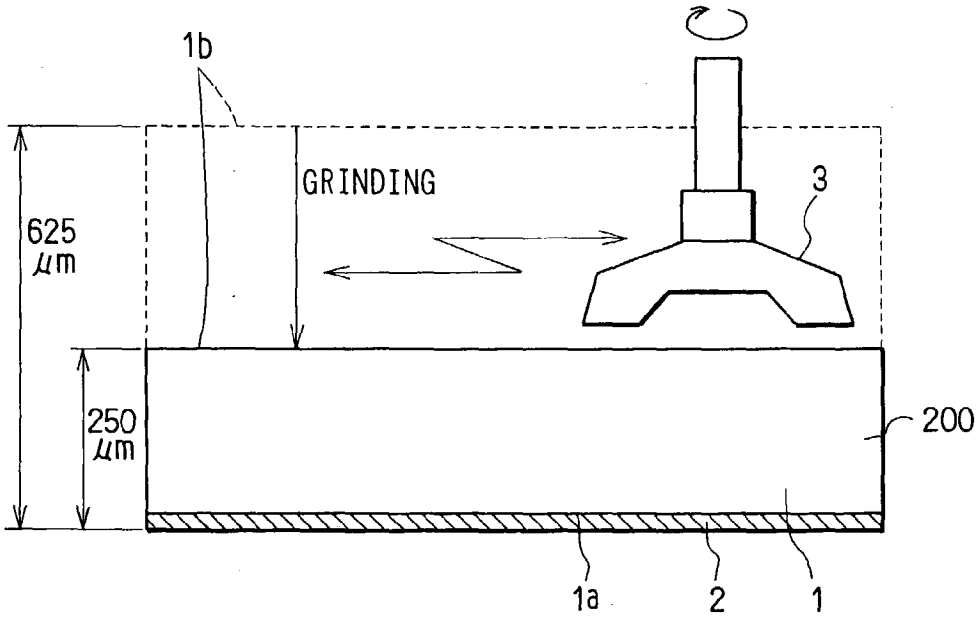


FIG. 3

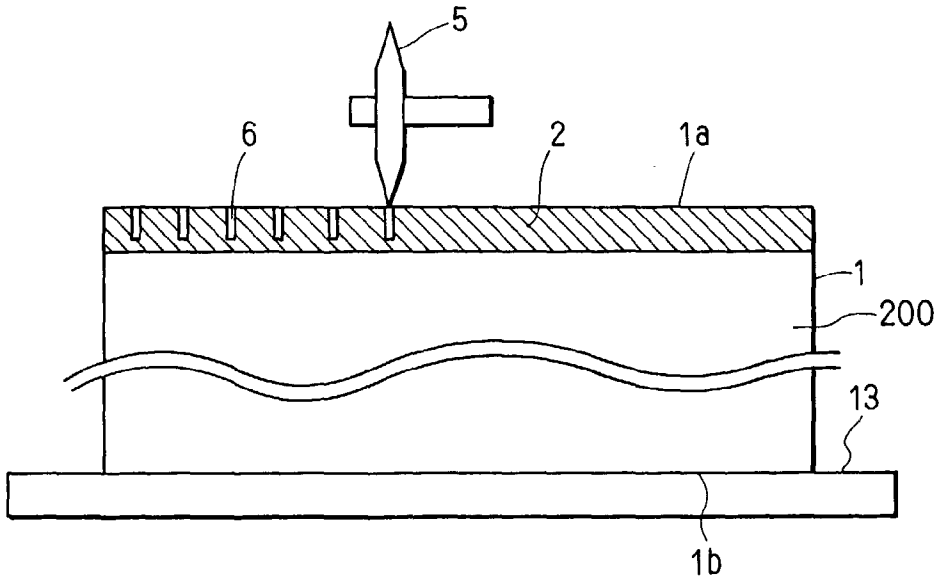


FIG. 4

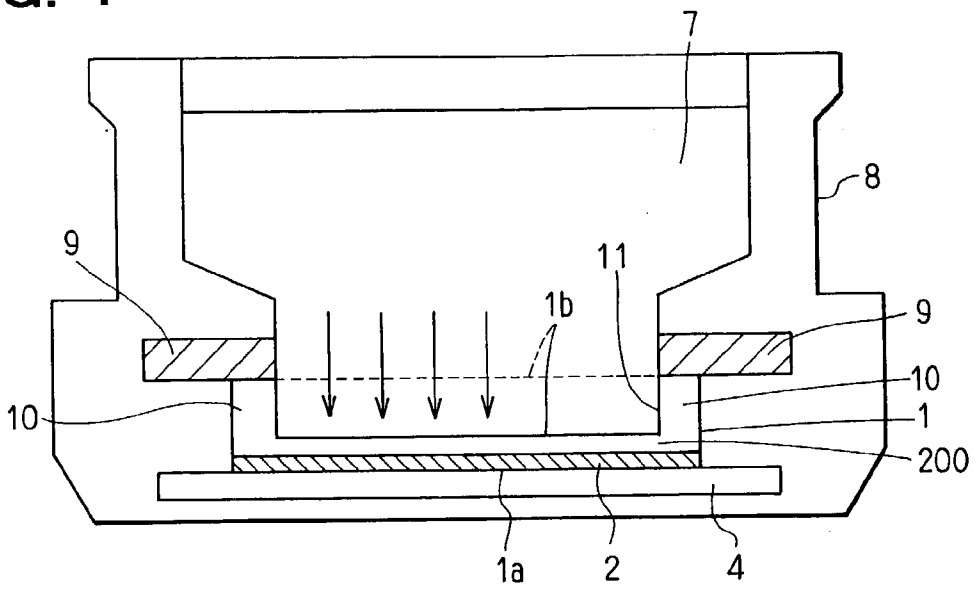


FIG. 5

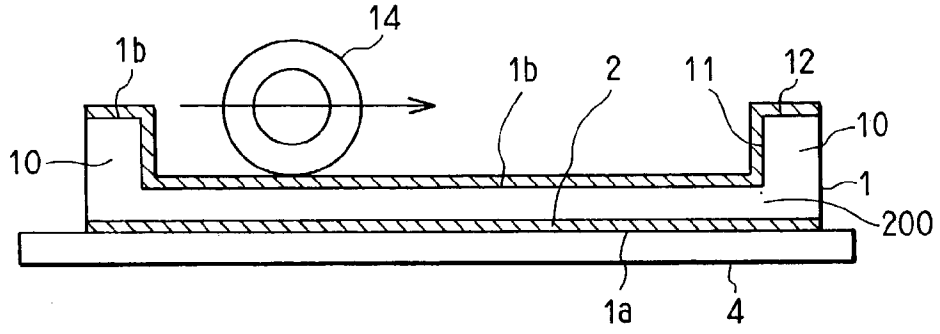


FIG. 6

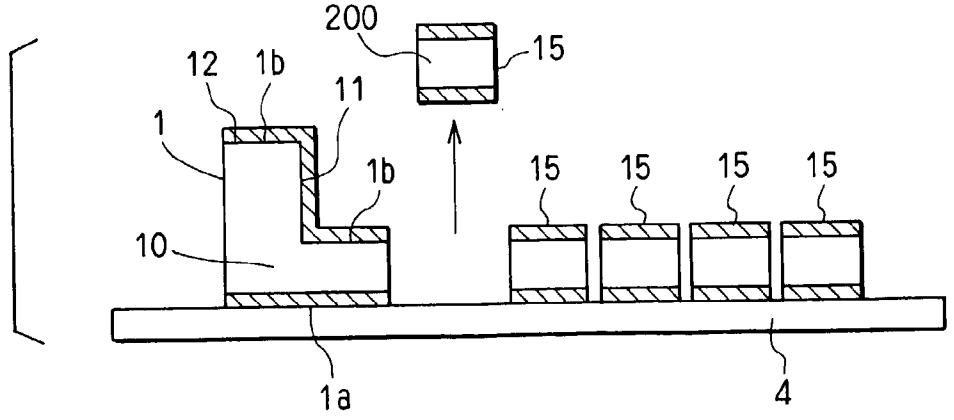


FIG. 7A

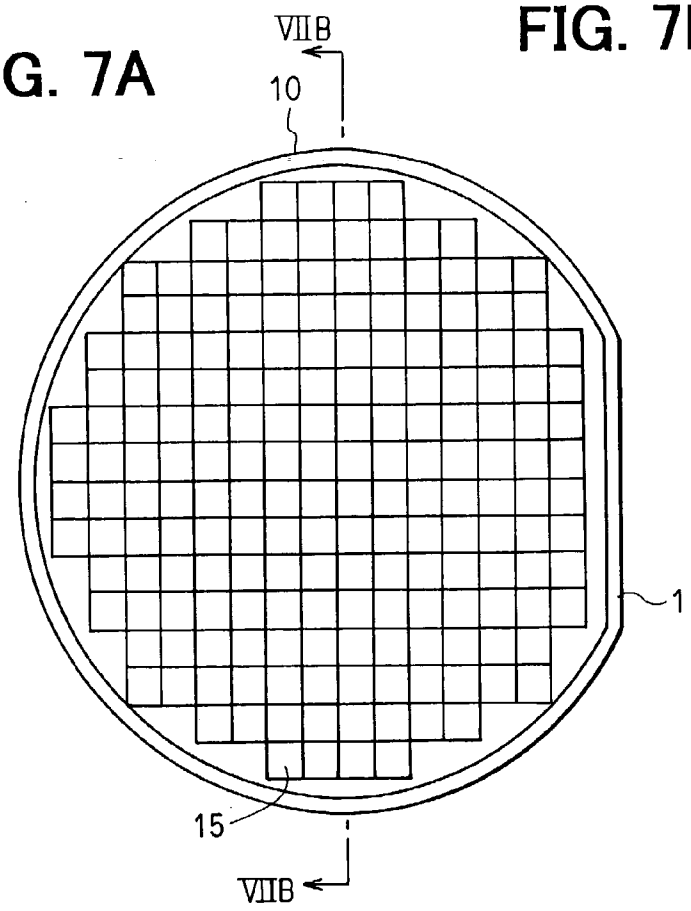


FIG. 7B

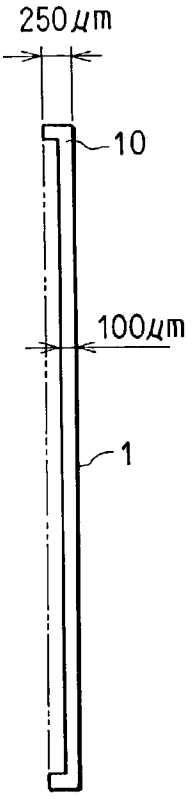


FIG. 8

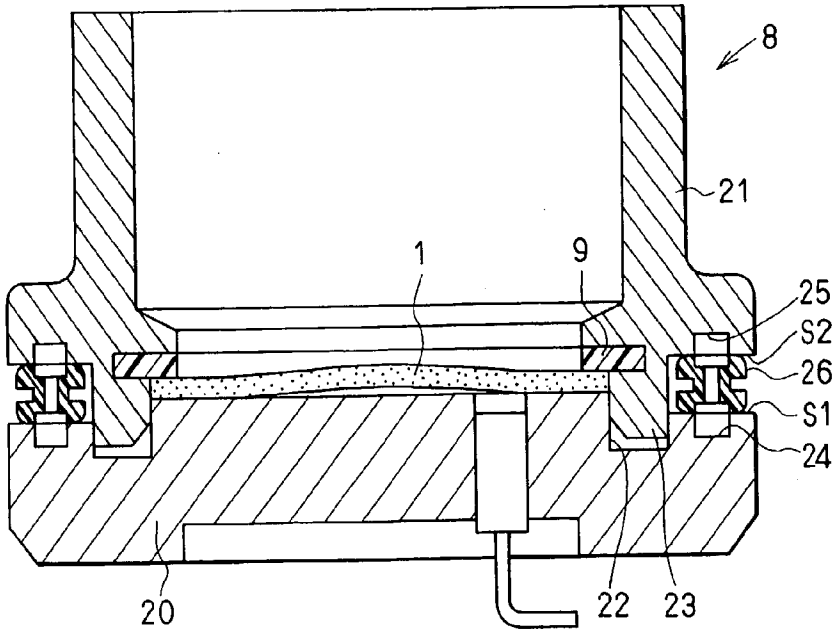


FIG. 9

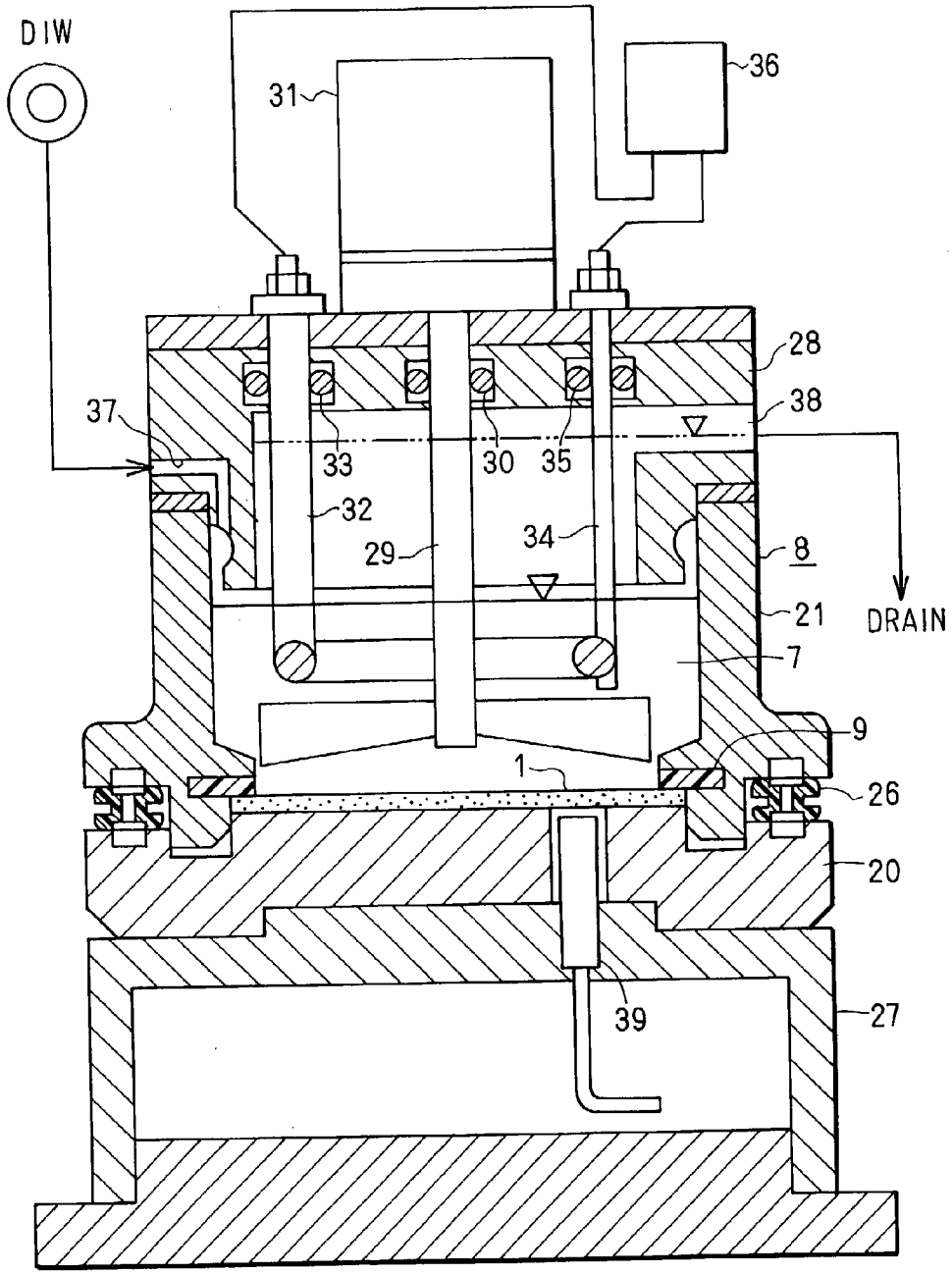


FIG. 10

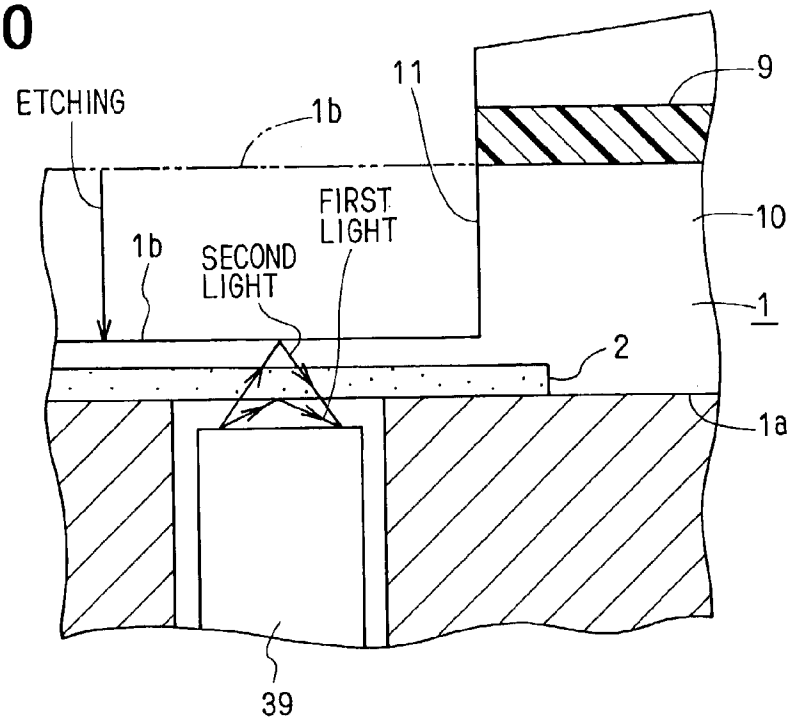

ETCHING
1b
11
9
10
1b
SECOND LIGHT
FIRST LIGHT
1
2
1a
39

FIG. 11

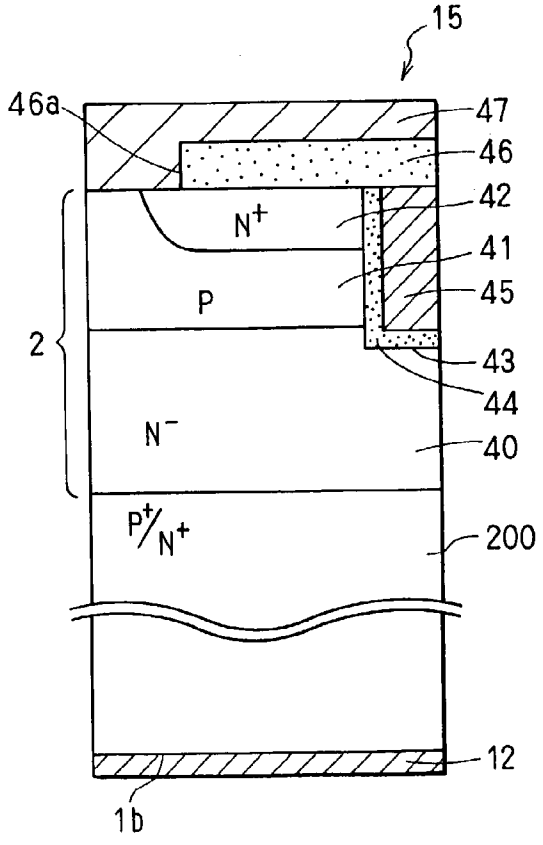

15
46a
47
46
42
N+
41
P
45
2
43
44
N−
40
P+/N+
200
12
1b

FIG. 12

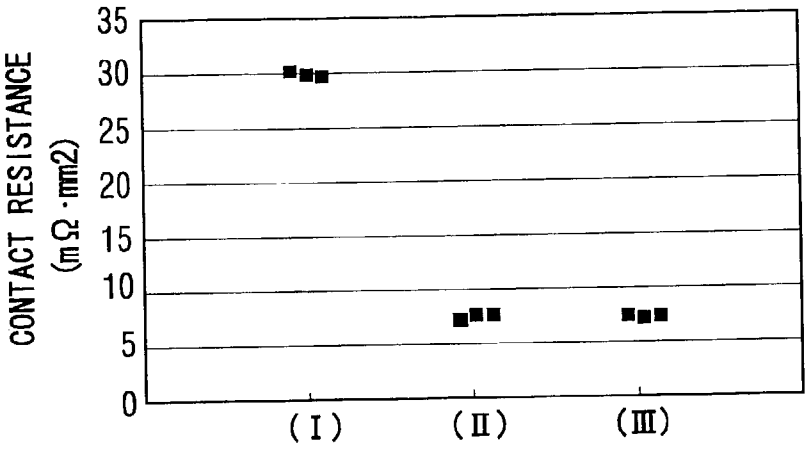

CONTACT RESISTANCE
(mΩ·mm2)
35
30
25
20
15
10
5
0
(I)
(II)
(III)

FIG. 13

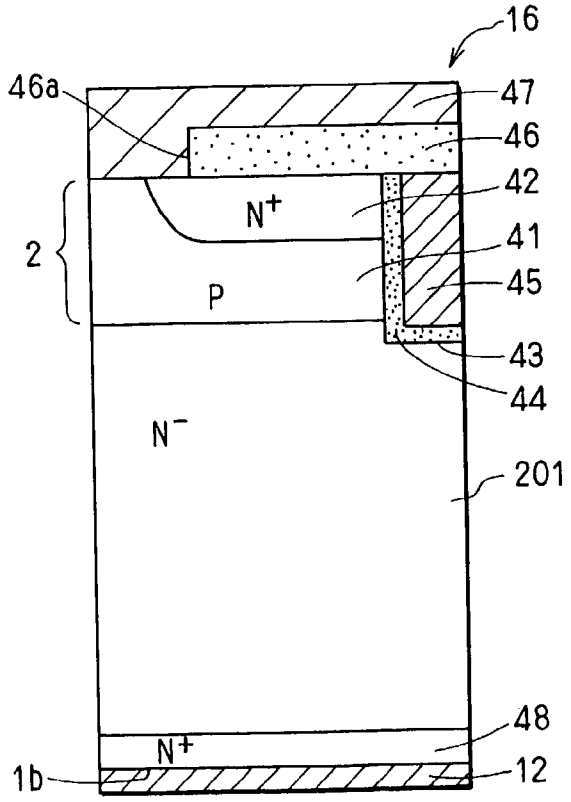

16
46a
47
46
42
N+
41
2
P
45
43
44
N−
201
48
N+
1b
12

FIG. 14

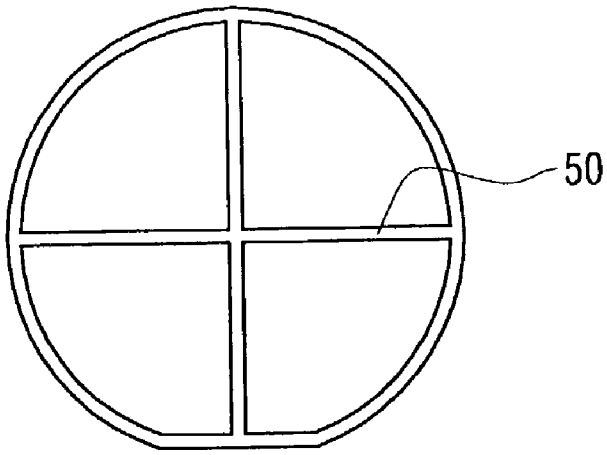


FIG. 15

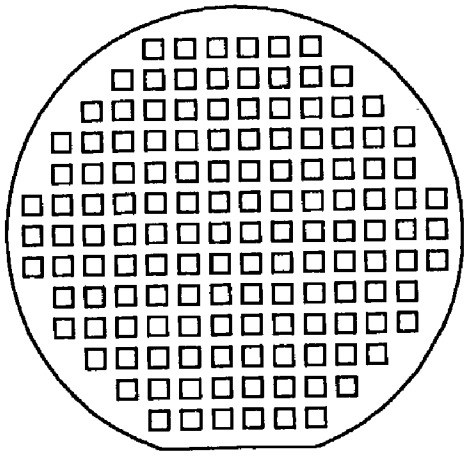


FIG. 16A

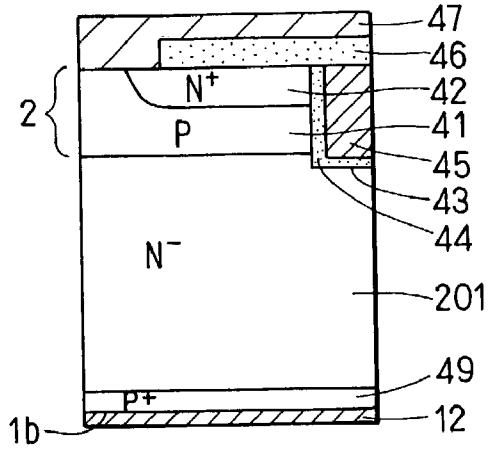


FIG. 16B

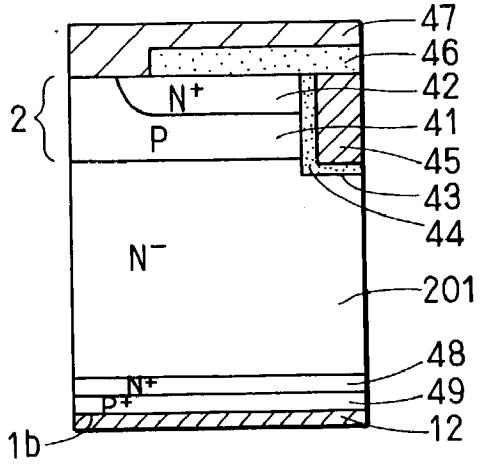


FIG. 16C

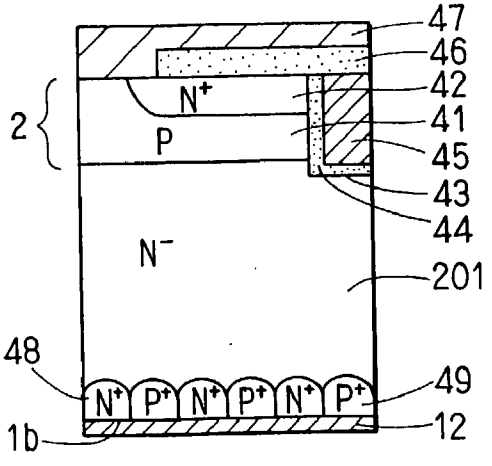


FIG. 17A

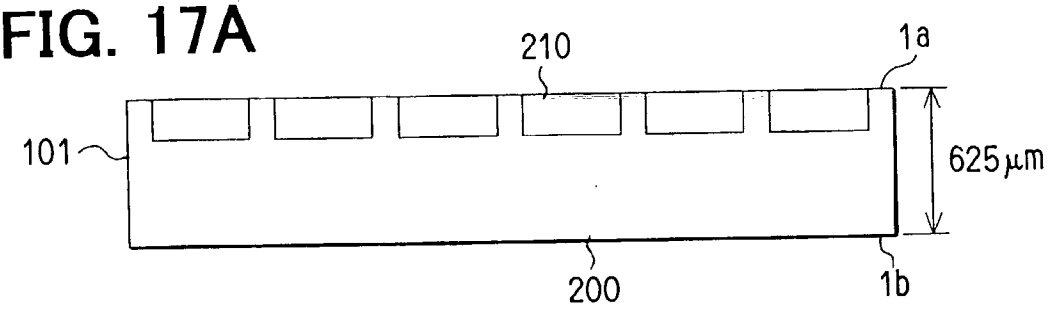


FIG. 17B

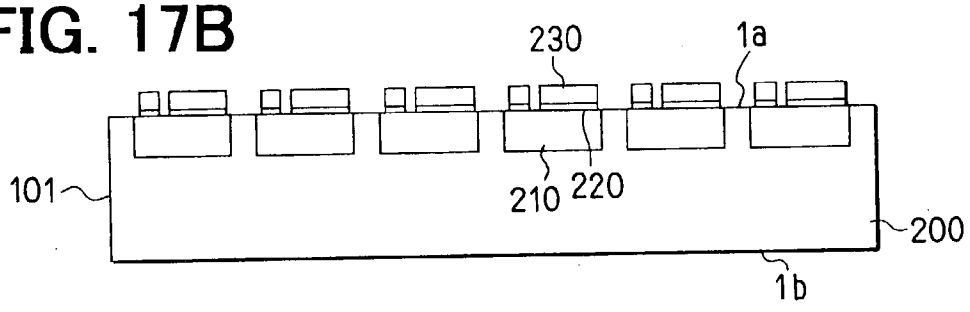


FIG. 17C

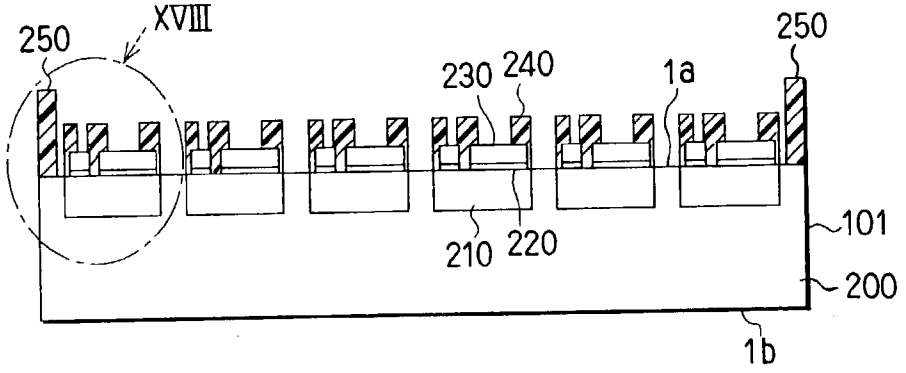


FIG. 17D

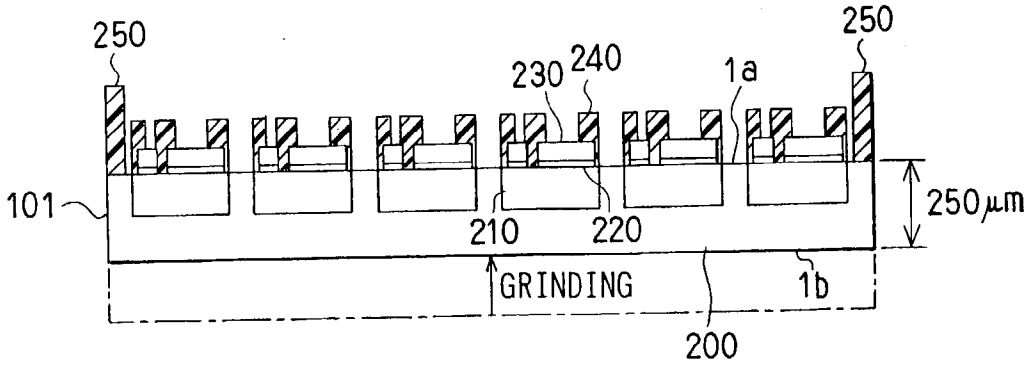


FIG. 17E

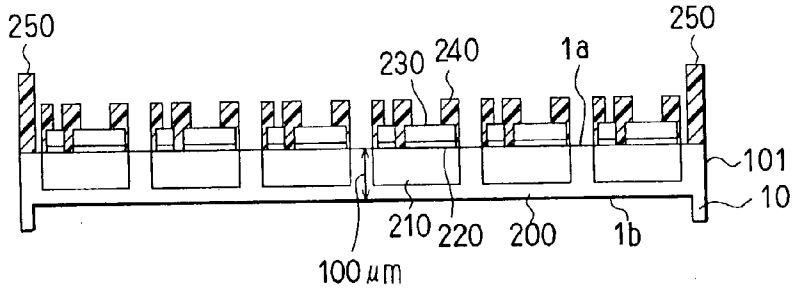


FIG. 17F

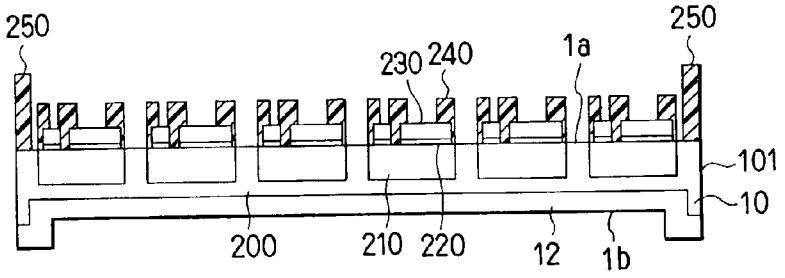


FIG. 18

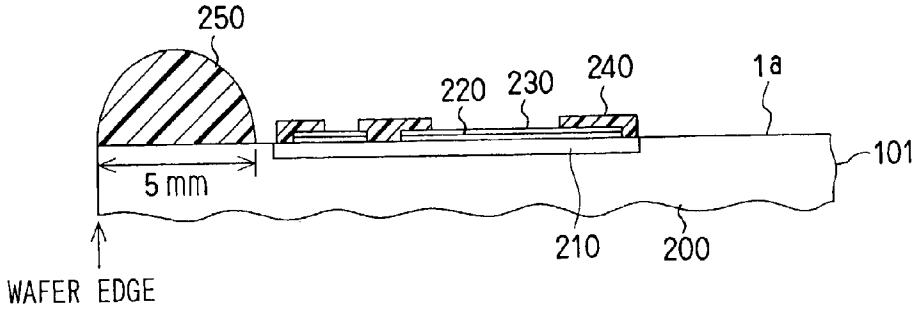


FIG. 19A

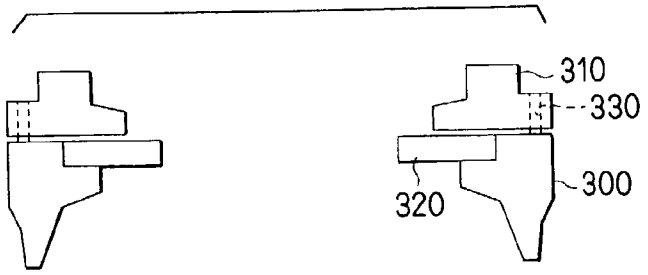


FIG. 19B

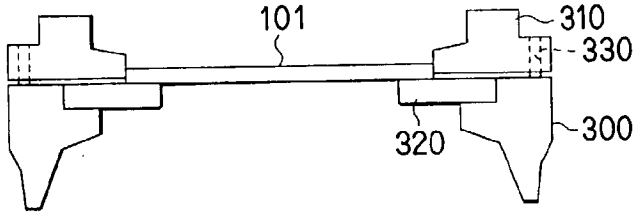


FIG. 19C

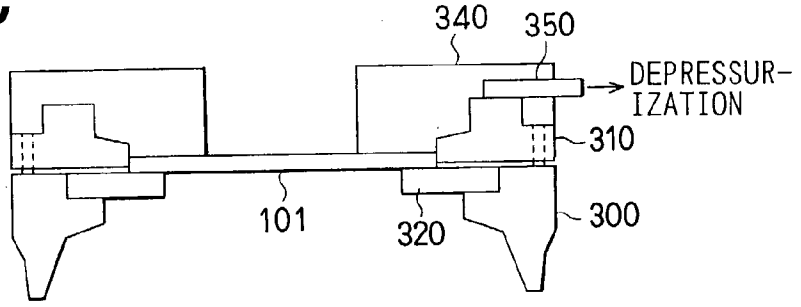


FIG. 19D

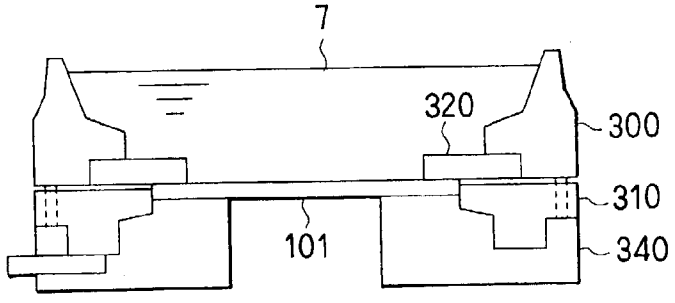


FIG. 19E

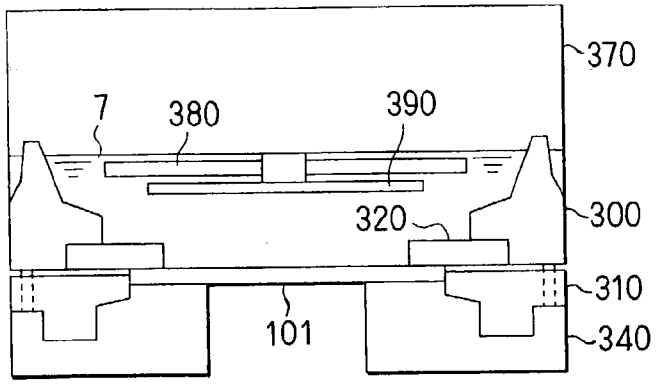


FIG. 19F

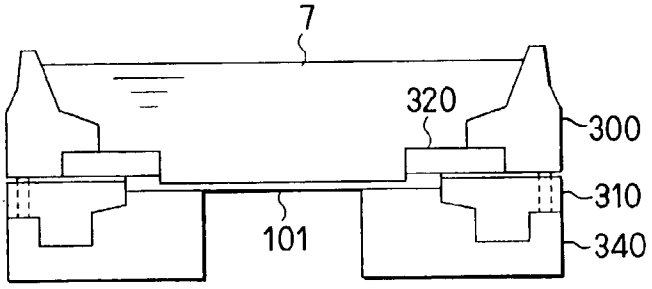


FIG. 19G

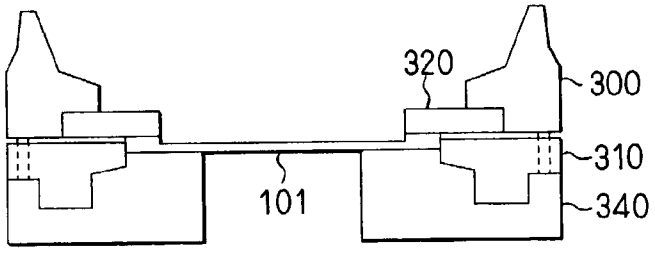


FIG. 19H

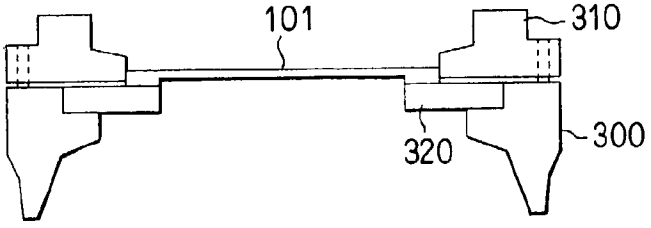


FIG. 19I

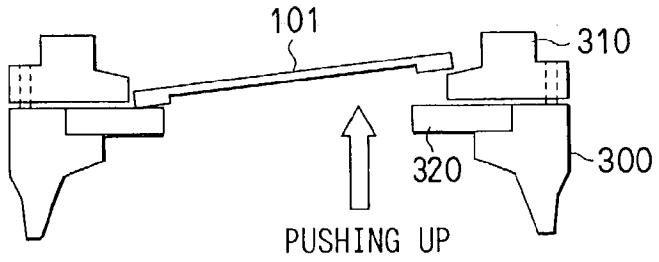


FIG. 19J

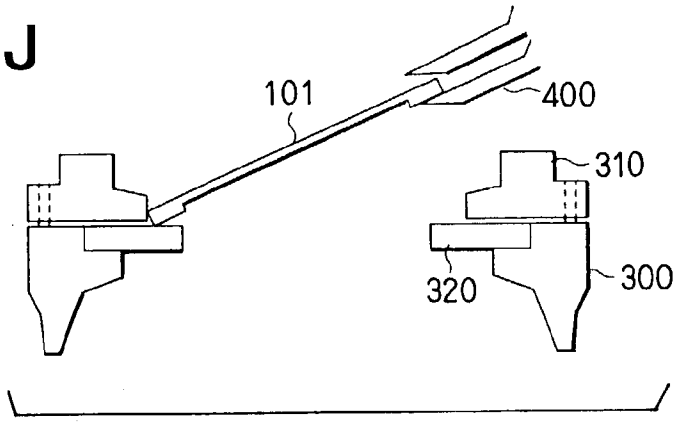


FIG. 20

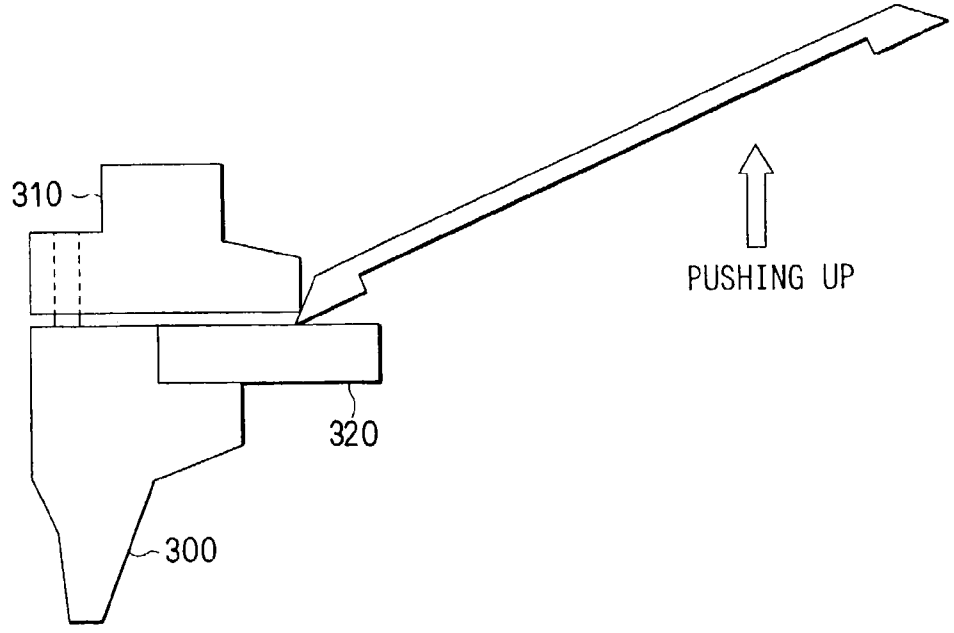


FIG. 21A

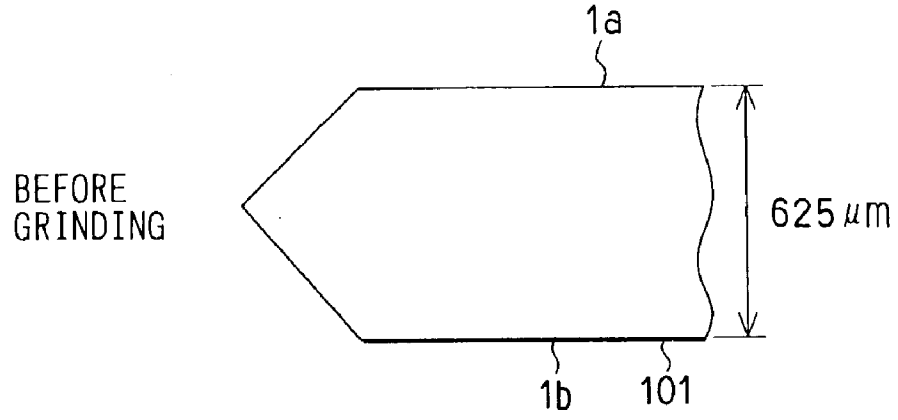


FIG. 21B

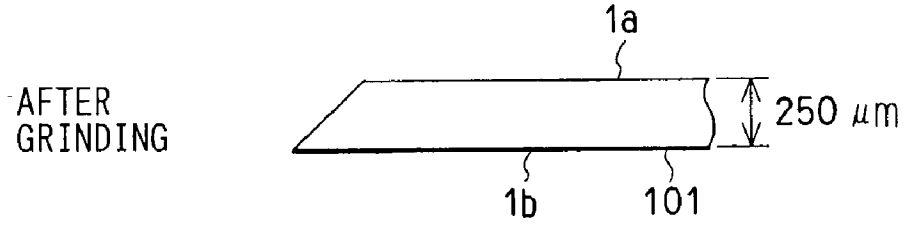


FIG. 21C

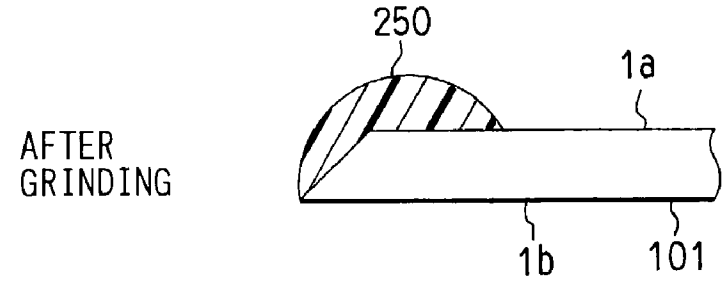


FIG. 22

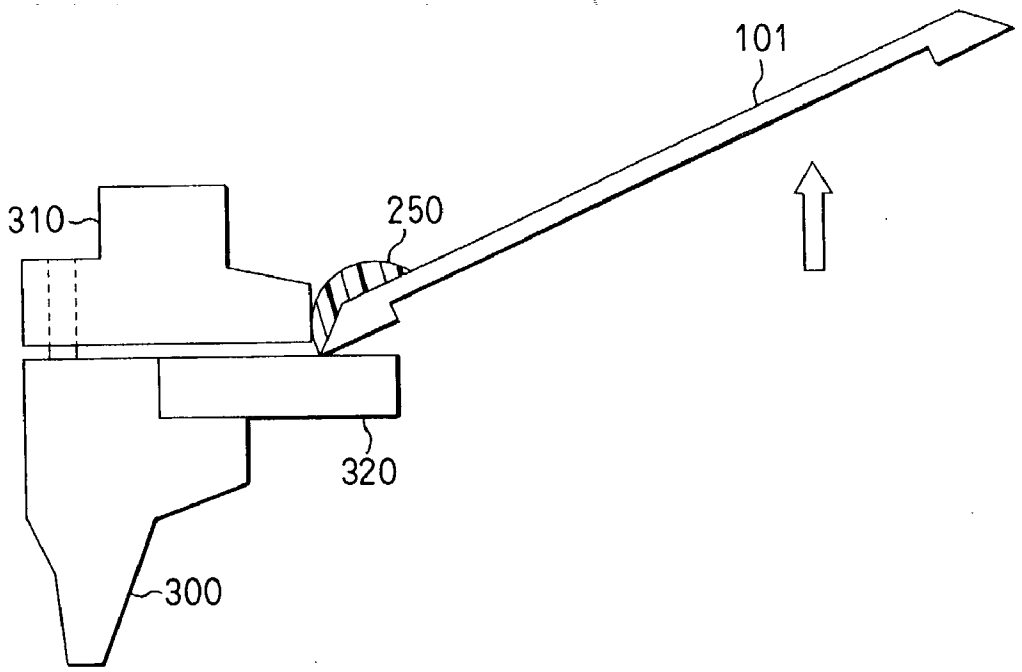


FIG. 23

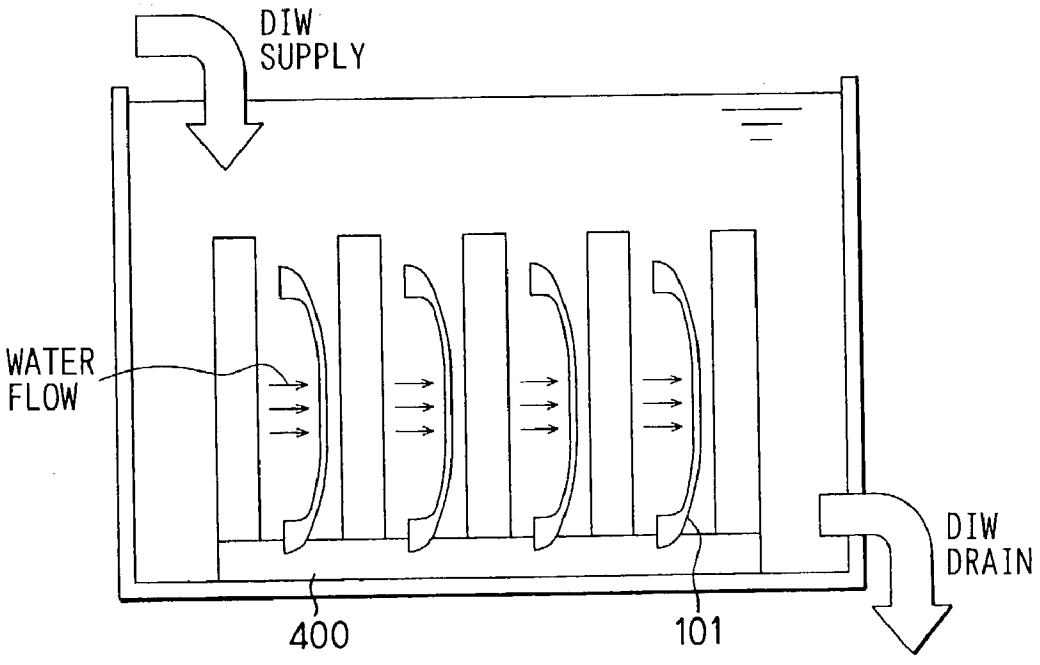


FIG. 24A

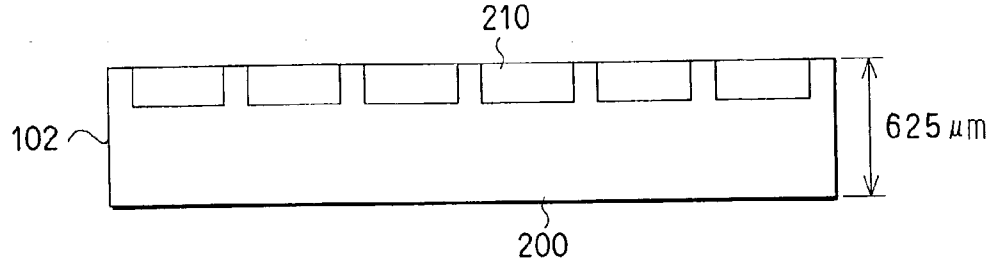


FIG. 24B

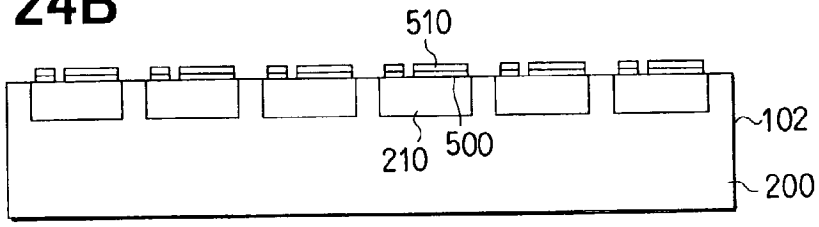


FIG. 24C

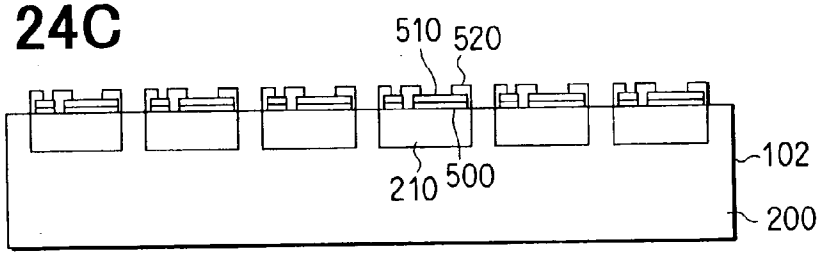


FIG. 24D

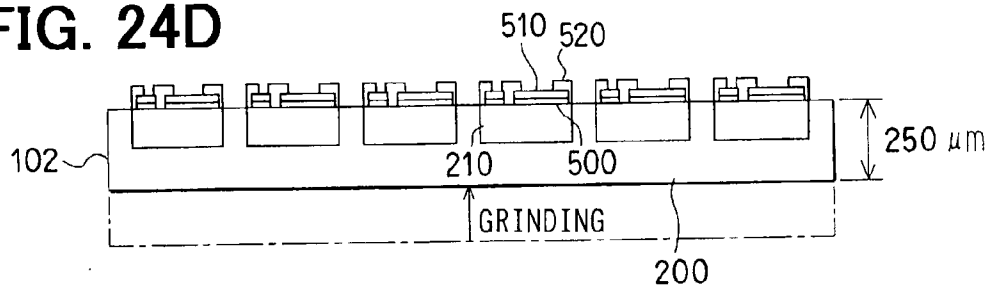


FIG. 24E

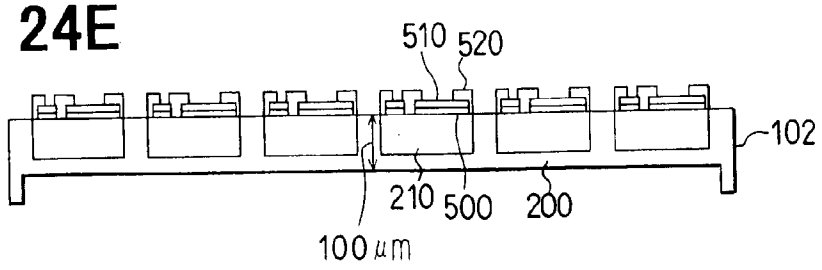


FIG. 25

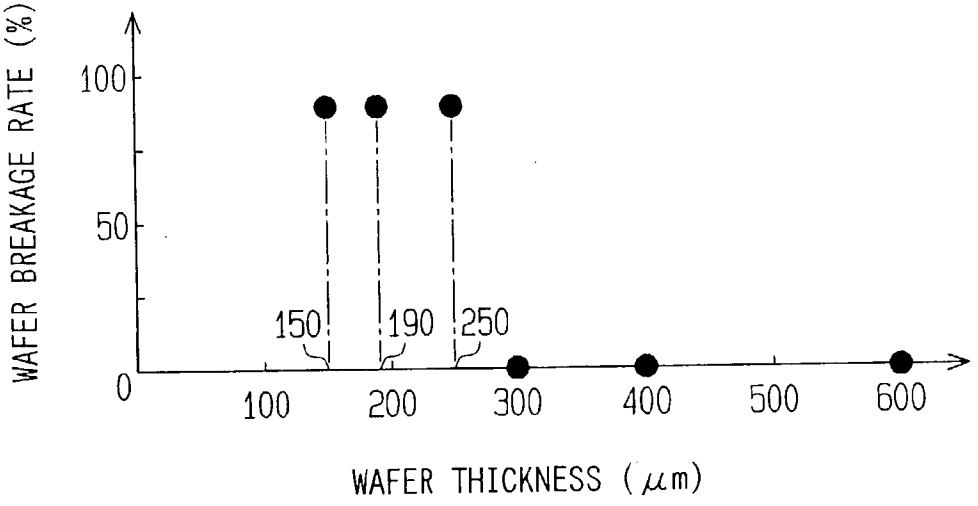

WAFER BREAKAGE RATE (%)
100
50
0
150
190
250
100
200
300
400
500
600
WAFER THICKNESS (μm)

FIG. 26

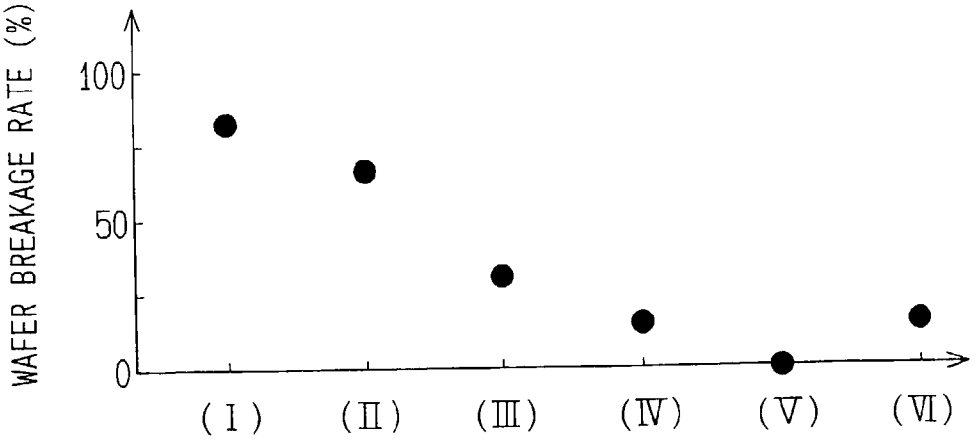

WAFER BREAKAGE RATE (%)
100
50
0
(I)
(II)
(III)
(IV)
(V)
(VI)

FIG. 27A

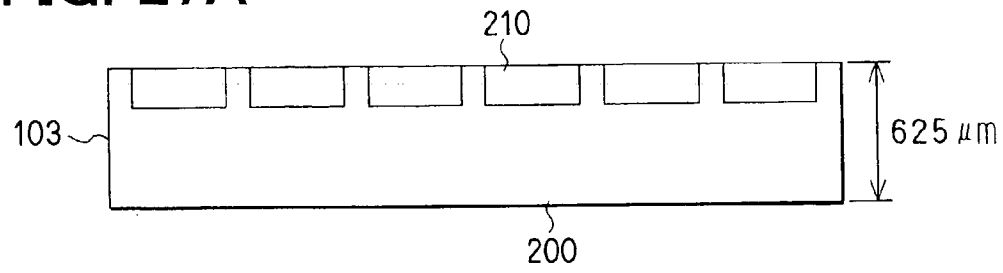


FIG. 27B

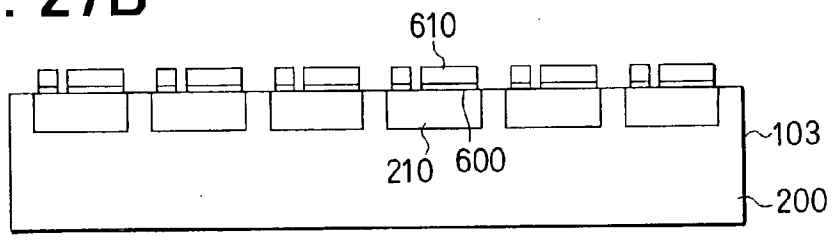


FIG. 27C

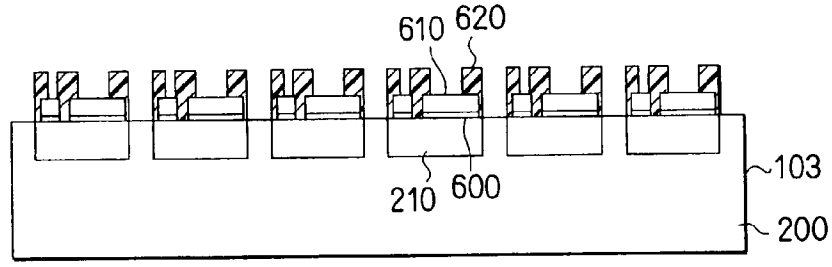


FIG. 27D

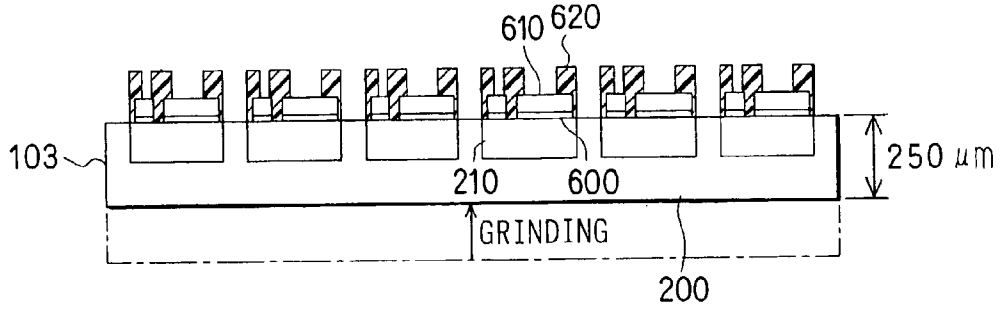


FIG. 27E

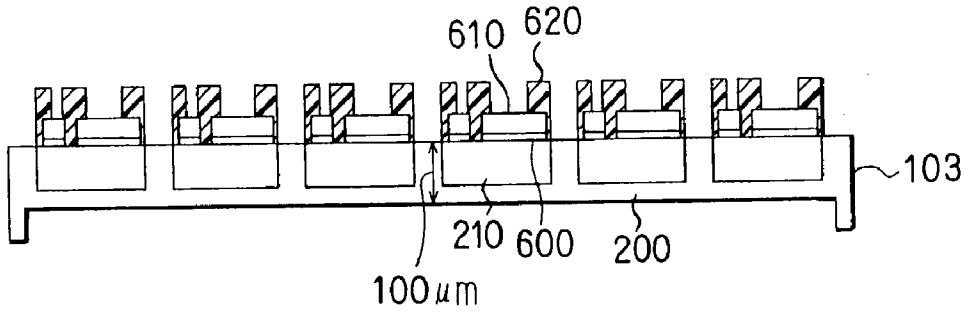
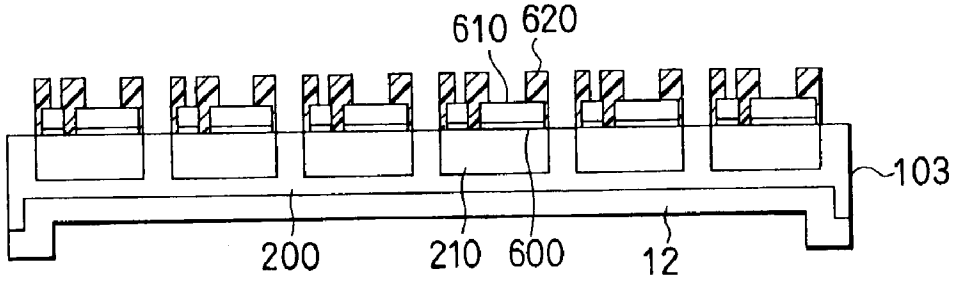


FIG. 27F



METHOD FOR MANUFACTURING SEMICONDUCTOR POWER DEVICE

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application is based on and incorporates herein by reference Japanese Patent Applications No. 2001-378725 filed on Dec. 12, 2001, No. 2002-106327 filed on Apr. 9, 2002, and No. 2002-264135 filed on Sep. 10, 2002.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to a method for manufacturing a semiconductor power device. With the method, the ON resistance of the device is improved.

[0003] A variety of methods have been proposed to reduce the ON resistance of a power device. In the methods, the resistance of the semiconductor layer included in the device is decreased. For example, JP-B-2513055, corresponding U.S. Pat. No. of which is 5,242,862, discloses a method for manufacturing a vertical semiconductor power device. The method includes the following steps. At first, a device layer, which includes MOSFETs, and a front surface electrode are formed on the front surface of a semiconductor wafer. Then, the wafer is evenly ground from back surface, which is opposite to the front surface, such that the wafer has a thickness of 200 to 450 μm. Next, a back surface electrode is formed on the back surface of the wafer. The semiconductor layer included in the power device is thinned by the grinding, so the resistance of the semiconductor layer is decreased. As a result, the ON resistance of the power device is reduced.

[0004] However, with the method according to the publication, the fragility of the wafer increases drastically if the wafer is ground to thinner than 200 μm. As a result, the yield of the power device is lowered due to the wafer breakage during the grinding or when an adhesive film that is stuck to the wafer is peeled from the wafer. Therefore, it is substantially impossible to make the wafer thinner than 200 μm by the method according to the publication. That is, it is substantially impossible to drastically reduce the ON resistance of the power device by the method according to the publication.

[0005] On the other hand, JP-A-5-121384 discloses a method, with which the above problem can be solved. In the method, a semiconductor wafer is thinned only at its central area from the back surface using a polishing machine, which includes a grindstone having a diameter smaller than that of the wafer, and a rim is formed at the periphery of the wafer after polishing. The wafer is not thinned in the periphery, so the rim has the original thickness of the wafer to reinforce the wafer. Therefore, it is possible to make the wafer thinner than 200 μm.

[0006] However, with the method disclosed in JP-A-5-121384, the wafer is damaged at its polished back surface. Accordingly, the contact resistance between the back surface and a back surface electrode, which is formed on the back surface, is relatively high. In addition, it is substantially impossible to form a beam in the central area for reinforcing the central area because the wafer is polished with the grindstone, which has a diameter smaller than that of the wafer. As a result, if a wafer having a relatively large diameter needs to be polished, the wafer may break or warp. Therefore, in that case, the method disclosed in JP-A-5-121384 is less effective.

SUMMARY OF THE INVENTION

[0007] The present invention has been made in view of the above aspect with an object to provide a method for manufacturing a semiconductor device having relatively low ON resistance while the wafer used for the manufacturing is prevented from breaking or warping even if the wafer has a relatively large diameter.

[0008] In the present invention, a semiconductor device, in which a semiconductor element layer is located on a semiconductor layer, is manufactured using the following steps. First, a semiconductor wafer that includes a semiconductor layer and a semiconductor element layer, which is located on the semiconductor layer, is formed. The wafer has a first surface, at the side of which the semiconductor element layer is located. The wafer has a second surface, which is opposite to the first surface, and at the side of which the semiconductor layer is located. Then, the wafer is ground evenly from the second surface to a predetermined thickness. Next, the wafer is etched to a predetermined thickness from the second surface while the periphery of the wafer is masked against the etchant to form a rim at the periphery.

[0009] Alternatively, a semiconductor device, in which a semiconductor element layer is located on a semiconductor layer that has a relatively low impurity concentration, is manufactured using the following steps. First, a semiconductor wafer that includes a semiconductor layer, which has a relatively low impurity concentration, and a semiconductor element layer, which is located on the semiconductor layer, is formed. The wafer has a first surface, at the side of which the semiconductor element layer is located. The wafer has a second surface, which is opposite to the first surface, and at the side of which the semiconductor layer is located. Then, the wafer is ground evenly from the second surface to a predetermined thickness. Next, the wafer is etched to a predetermined thickness from the second surface while the periphery of the wafer is masked against the etchant to form a rim at the periphery. Then, a high impurity concentration layer, which has an impurity concentration higher than the semiconductor layer, is formed at the second surface.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The above and other objects, features and advantages of the present invention will become more apparent from the following detailed description made with reference to the accompanying drawings. In the drawings:

[0011] **FIGS. 1A** to 1D are schematic cross-sectional views showing manufacturing steps of a semiconductor power device using the method according to the first embodiment of the present invention;

[0012] **FIG. 2** is a schematic cross-sectional view showing a manufacturing step of the semiconductor power device using the method according to the first embodiment;

[0013] **FIG. 3** is a schematic cross-sectional view showing a manufacturing step of the semiconductor power device using the method according to the first embodiment;

[0014] **FIG. 4** is a schematic cross-sectional view showing a manufacturing step of the semiconductor power device using the method according to the first embodiment;

[0015] **FIG. 5** is a schematic cross-sectional view showing a manufacturing step of the semiconductor power device using the method according to the first embodiment;

[0016] **FIG. 6** is a schematic cross-sectional view showing a manufacturing step of the semiconductor power device using the method according to the first embodiment;

[0017] **FIG. 7A** is a schematic plan view of a semiconductor wafer after the wafer is separated into semiconductor chips, and **FIG. 7B** is a schematic cross-sectional view of the wafer taken along the line VIIB-VIIB;

[0018] **FIG. 8** is a schematic cross-sectional view of an etching pot;

[0019] **FIG. 9** is a schematic cross-sectional view of an etching apparatus;

[0020] **FIG. 10** is a partially enlarged cross-sectional view of the etching pot;

[0021] **FIG. 11** is a partial enlarged view of a semiconductor power device according to the first embodiment;

[0022] **FIG. 12** is a graph showing the correlation between the contact resistance, which is the resistance between the back surface of a semiconductor wafer and an electrode formed on the back surface, and the thinning methods of the wafer;

[0023] **FIG. 13** is a partial enlarged view of a semiconductor power device according to the second embodiment;

[0024] **FIG. 14** is a plan view of a semiconductor wafer having beams in its central area in addition to a rim in its periphery;

[0025] **FIG. 15** is a plan view of a semiconductor wafer having grid-like beams;

[0026] **FIGS. 16A** to **16**C are partial cross-sectional views of modified versions of the semiconductor power device in **FIG. 13**;

[0027] **FIGS. 17A** to **17**F are schematic cross-sectional views showing a manufacturing process of a semiconductor power device using the method according to the third embodiment of the present invention;

[0028] **FIG. 18** is a partially enlarged view of the cross-section in the circle XVIII in **FIG. 17C**

[0029] **FIGS. 19A** to **19**J are schematic cross-sectional views showing steps in the etching of a semiconductor wafer;

[0030] **FIG. 20** is a schematic cross-sectional view showing a problem to be solved in the etching of a semiconductor wafer;

[0031] **FIGS. 21A** to **21**C are schematic cross-sectional views respectively showing the shape of an end of a semiconductor wafer before grinding, after grinding, and after a polyimide rim is formed;

[0032] **FIG. 22 a** schematic cross-sectional view showing an effect of the method according to the third embodiment in the etching of a semiconductor wafer;

[0033] **FIG. 23** is a schematic cross-sectional view showing a state that a semiconductor wafer is rinsed with deionized water after etching;

[0034] **FIGS. 24A** to **24**E are schematic cross-sectional views showing a manufacturing process of a semiconductor power device having a conventional metal electrode and a passivation film;

[0035] **FIG. 25** is a graph showing the correlation between wafer breakage rate and wafer thickness;

[0036] **FIG. 26** is a graph showing the correlation between wafer breakage rate and combination of passivation film, polyimide rim, and aluminum alloy film; and

[0037] **FIGS. 27A** to **27**F are schematic cross-sectional views showing another manufacturing process of a semiconductor power device using the method according to the third embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0038] The present invention will be described in detail with reference to various embodiments.

[0039] First Embodiment

[0040] As shown in **FIG. 1A, a** semiconductor wafer **1** includes a semiconductor layer **200**, which is n^+-type or p^+-type and has a relatively high impurity concentration, and a semiconductor element layer **2**, which is located on the semiconductor layer **200**. The semiconductor element layer **2** includes semiconductor elements. The semiconductor wafer **1** has a first surface **1***a,* or a front surface **1***a,* and a second surface **1***b,* or a back surface **1***b,* which is opposite to the front surface **1***a*. The wafer **1** has a thickness of 625 μm.

[0041] As shown in **FIG. 2**, the wafer **1** is evenly ground with a grindstone **3** from the back surface **1***b* such that the wafer **1** has a thickness of, for example, 250 μm. In the grinding, the entire back surface **1***b* is thinned to a determined thickness. After the grinding, the wafer **1** has a cross-sectional structure shown in **FIG. 1B**. Then, as shown in **FIG. 3**, an adhesive tape **13** is stuck on the back surface **1***b,* and a plurality of cutting grooves **6**, each of which has a predetermined depth from the front surface la, are formed in the element layer **2** using a cutter **5**.

[0042] Next, as shown in **FIG. 4, a** protection member **4**, or an adhesive tape **4**, is stuck on the front surface **1***a,* and the wafer **1** is placed at a predetermined position in an etching pot **8** such that the back surface **1***b* is exposed to an etchant **7** during the etching of the wafer **1** except for the periphery of the back surface **1***b,* which is masked by a gasket **9**. Then, the wafer **1** is etched from the back surface **1***b* by the etchant **7** until the thickness of the wafer **1** becomes 100 μm at the etched area. The thickness of the wafer **1** at the etched area is greater than the depth of the cutting grooves after the etching. With the etching, as shown in **FIG. 1C, a** rim **10** is formed at the periphery of the wafer **1** because the periphery is masked by the gasket **9** during the etching. At the same time, a recess **11**, which is defined by the rim **10**, is formed in the wafer **1**.

[0043] Subsequently, as shown in **FIG. 1D, a** back surface electrode **12**, or a drain electrode **12**, is formed on the entire back surface **1***b* by depositing a metal using vacuum evaporation, sputtering, CVD, and so on. Then, as shown in **FIG. 5**, the wafer **1** and the adhesive tape **4** are supported such that the front surface la faces downward, and the wafer **1** is

pressed by a break roller **14** to bend. With the bending deformation, the wafer **1** breaks along the cutting grooves **6** and separates into a plurality of semiconductor devices **15**, or semiconductor chips **15**. Finally, as shown in **FIG. 6**, each chip **15** is picked up from the wafer **1** shown in **FIG. 7** and mounted at a predetermined place.

[**0044**] The etching step schematically shown in **FIG. 4** will be described in detail. As shown in **FIG. 8**, an etching pot **8** includes a plate-shaped pot base **20** and a cylinder-shaped pot ring **21**. The wafer **1** is placed on top of the pot base **20**, and the pot ring **21** is placed on top of the wafer **1** such that the wafer **1** closes the opening of the pot ring **21**. The central area of the pot base **20** is a stage for holding the wafer **1**. An annular recess **22** is located at the periphery of the pot base **20** around the stage. A projection **23** of the pot ring **21** fits into the annular recess **22**. The annular recess **22** is used for aligning the pot ring **21**. A lower seal surface S1, which is flat and in a ring shape, is located on the pot base **20** around the annular recess **22**, as viewed in **FIG. 8**. An annular recess **24** is located in the lower seal surface S1 to function as a vacuum pocket.

[**0045**] An annular inner gasket **9** is fixed in the inner surface of the lower part of the pot ring **21**. The inner gasket **9** prevents the etchant **7** from leaking out of an etching bath formed by the pot ring **21** and the wafer **1** mounted on the pot base **20**. Furthermore, an upper sealing surface S2, which is flat and in a ring shape, is located on a flange of the lower part of the pot ring **21**, as viewed in **FIG. 8**. An annular recess **25** is located in the upper sealing surface S2 to function as a vacuum pocket. An annular outer gasket **26**, which has an X-shaped cross section as shown in **FIG. 8**, is placed between the lower sealing surface S1 and the upper sealing surface S2. By pumping air out of the annular recesses **24**, **25** using a vacuum pump, the outer gasket **26** is shrunken to fix the pot base **20** and the pot ring **21** while permitting the inner gasket **9** to seal a gap between the pot ring **21** and the wafer **1**.

[**0046**] The etching pot **8** of **FIG. 8** is set in a pot etching system, as shown in **FIG. 9**. Then, the etchant **7** is supplied into the etching pot **8**. The inner gasket **9** does not only seal the gap between the pot ring **21** and the wafer **1** against the etchant **7**, but also masks the periphery of the wafer **1** from the etchant **7**. Therefore, when the etching pot is filled with the etchant **7**, the etchant **7** does not contact the periphery of the wafer **1** on the back surface **1***b*.

[**0047**] More specifically, the etching pot **8** is mounted on to a pot stage **27**, and the upper opening of the etching pot **8** is plugged with a lid **28**. A stirrer **29** is supported by the lid **28** while being sealed with a sealing material **30**. The stirrer **29** is driven by a motor **31** to agitate the etchant **7**. A heater **32** for heating the etchant **7** is also supported by the lid **28** while being sealed with a sealing material **33**. A temperature sensor **34** for measuring the temperature of the etchant **7** is also supported by the lid **28** while being sealed with a sealing material **35**. During the etching by the pot etching system in **FIG. 9**, the etchant **7** is continuously agitated by the stirrer **29**, while the heater **32** is electrically controlled by a temperature controller **36** to keep the temperature of the etchant **7** at a predetermined temperature, which is sensed by the temperature sensor **34**.

[**0048**] Furthermore, the lid **28** includes a passage **37** for deionized water (DIW), so deionized water can be supplied into the etching pot **8** falling down along the inner wall of the pot ring **21**. The lid **28** also includes a drain opening **38** for draining out waste water by having the waste water overflow the etching pot **8**. As shown in **FIG. 9**, the pot base **20** includes a thickness sensor **39** to measure the thickness of the wafer **1** at the bottom of the recess **11**, and the progress of etching is monitored to detect the etching end point, as shown in **FIG. 10**. The thickness sensor **39** measures the thickness of the wafer **1** at the bottom of the recess **11** on the basis of the first light reflected on the front surface **1***a* and the second light reflected on the back surface **1***b*

[**0049**] When a predetermined thickness is etched off and the thickness of the wafer **1** at the bottom of the recess **11** becomes a predetermined thickness, deionized water is supplied into the etching pot **8** through the passage **37** to dilute and cool off the etchant **7** and stop the etching process. Waste water is drained out from the drain opening **38**. Then, the vacuum pump stops pumping out air from the annular recesses **24**, **25**, and the annular recesses **24**, **25** are brought back to the atmospheric pressure. Then, the lid **28** and the pot ring **21** removed. At this stage, the etched silicon wafer **1** has the cross-sectional structure shown in **FIG. 1C**.

[**0050**] In the proposed method, as described above, a wafer is thinned with a grindstone, which has a diameter smaller than that of the wafer, so the thinned area needs to be circular to provide the maximum number of chips. As a result, the dimension of the thinned area is limited by the orientation flat of the wafer. In contrast, with the etching system of **FIG. 9**, the rim **10** is formed by masking the periphery of the back surface **1***b* with the gasket **9** against the etchant **7** when the wafer **1** is etched from the back surface **1***b*. Therefore, it is possible to form the rim **10** to conform to the outline of the wafer **1**. That is, as shown in **FIG. 7A**, the rim **10** can be formed to become linear at the orientation flat of the wafer **1** and arc-like at the rest of the periphery of the wafer **1**. Thus, with the etching system of **FIG. 9**, the dimension of a wafer is more efficiently used in comparison with the proposed method.

[**0051**] Although the thickness of the wafer **1** is as thin as 100 μm at the recess **11**, the wafer **1** has the rim **10**, at which the wafer is as thick as 250 μm, at its periphery. Therefore, the wafer **1** is prevented from breaking or warping. As a result, it is possible to use a wafer with a relatively large diameter to manufacture a semiconductor power device using the etching system of **FIG. 9**. In addition, the cycle time of the grinding step shown in **FIG. 2** is generally shorter than that of the etching step shown in **FIG. 4**, so the combination of the grinding step and the etching step shortens the manufacturing process of the semiconductor chips **15** in comparison with the case that the etching step is used alone.

[**0052**] As shown in **FIG. 4**, the wafer **1** is placed at a predetermined position in the etching pot **8** with the adhesive tape **4** stuck on the front surface **1***a*. Therefore, even if the bottom of the recess **11** reaches the cutting grooves **6** and the wafer **1** breaks during the etching step, the wafer **1** is prevented from separating apart because the wafer **1** is supported by the adhesive tape **4**.

[**0053**] As shown in **FIG. 10**, the progress of etching is monitored to detect the etching end point using the thickness sensor **39**, so the wafer **1** can be etched more accurate than in the case that the etching end point is determined on the basis of the etching rate.

[0054] As shown in **FIG. 11**, each semiconductor chip **15**, which is a vertical type power device, includes a semiconductor element layer **2**. The semiconductor element layer **2** is located on a surface of a semiconductor layer **200**, which is n^+-type or p^+-type. Each semiconductor element layer **2** includes an n^--type drift layer **40**, which is formed by epitaxial growth on the surface of the semiconductor layer **200**. In a surface of the n^--type drift layer **40**, a p-type base layer **41** is located. In a surface of the p-type base layer **41**, an n^+-type source region **42** is located. Each semiconductor chip **15** has a trench **43** extends vertically from a surface of the source region **42** to the drift layer **40** through the source region **42** and the base layer **41**, as viewed in **FIG. 11**. A gate-insulating film **44** is located on the surface defining the trench **43**. A gate electrode **45** made of doped poly crystalline silicon is located on the gate-insulating film **44** in the trench **43**.

[0055] The gate electrode **45**, the base layer **41**, and the source region **42** are covered by an interlayer insulating film **46**, which is made of boron phosphorus silicate glass (BPSG). Through a contact hole **46***a* made in the interlayer insulating film **46**, a source electrode **47** is in electric contact with the base layer **41** and the source region **42**. Although not illustrated, a gate metal film, which is in electric contact with the gate electrode **45**, and a surface protecting film, which is made of polyimide resin, are located in the front surface **1***a*. The drain electrode **12** is located on the back surface **1***b*. The drain electrode **12** is formed after the step of etching in **FIG. 1C**.

[0056] The wafer **1** becomes much thicker at the rim **10** than at the bottom of the recess **11** in the etching method shown in **FIG. 4**, so the wafer **1** is prevented from warping or breaking when the wafer **1** is thinned. Therefore, using the etching method shown in **FIG. 4**, it is possible to make a wafer drastically thin while the wafer is prevented from breaking or warping at the steps after etching. Moreover, the otherwise high contact resistance between the semiconductor layer **200** and the drain electrode **12** is reduced by thinning the wafer **1** using the etching method shown in **FIG. 4**, as explained below. As a result, it is possible to provide a vertical type power device that has drastically low ON resistance.

[0057] As shown in **FIG. 12**, the contact resistance between a semiconductor layer and a drain electrode depends on the thinning method of a wafer. For the measurement of the contact resistances in **FIG. 12**, n-type wafers having a resistivity of 0.001 to 0.006 Ω·cm were used as the semiconductor layer, and titan (Ti) was formed as the drain electrode. The thinning methods used were: (I) only grinding, (II) grinding and etching with an etchant including hydrofluoric acid and nitric acid after the grinding, and (III) grinding and etching with an etchant including hydrofluoric acid, nitric acid, and sulfuric acid after the grinding.

[0058] As shown in **FIG. 12**, the method (I) that includes only grinding provides contact resistance much higher than the methods (II), (III) that include etching. When a semiconductor wafer is grinded, a damaged layer, which is made of amorphous silicon and has a thickness of hundreds of nanometers, is formed on the grinded surface. That is, the crystal lattice of the wafer is destroyed in the damaged layer, so current flow is obstructed by the damaged layer at the interface between a semiconductor layer and a drain electrode. Therefore, the contact resistance between the semiconductor layer and the drain electrode increases in the method (I) that includes only etching. On the other hand, the damaged layer is eliminated by etching in the methods (II), (III) that include etching, so the drain electrode is formed on crystal silicon without a damaged layer. Therefore, the contact resistance between the semiconductor layer and the drain electrode is reduced by combing the grinding and the etching.

[0059] Moreover, when a semiconductor wafer is ground using a grindstone having a roughness of #2000, the roughness Ra of the ground surface becomes approximately 10 nm. In contrast, when a semiconductor wafer is etched using the etchant including hydrofluoric acid, nitric acid, and sulfuric acid, the roughness Ra of the etched surface becomes approximately 150 nm. That is, the roughness Ra can be increased by combining the etching with the grinding. As the roughness Ra increases, the actual contact area between the semiconductor layer and the drain electrode is enlarged. Therefore, the adhesion between the semiconductor layer and the drain electrode is simultaneously increased by combining the etching with the grinding.

[0060] Incidentally, the pot etching system shown in **FIG. 9**, which includes the etching pot **8**, is not necessarily used for etching the wafer **1** to form the rim **10** at its periphery. Instead of the pot etching system shown in **FIG. 9**, other etching systems such as a spin etching system may be used as long as the etching systems is capable of etching the wafer **1** to form the rim **10** at its periphery.

[0061] Second Embodiment

[0062] A semiconductor chip **16** of **FIG. 13** is a vertical type power device and different from the semiconductor chip **15** of **FIG. 11** in the following aspects. The semiconductor layer **200** of **FIG. 11** has a relatively high impurity concentration. On the other hand, a semiconductor layer **201** of **FIG. 13** is n^--type and has a relatively low impurity concentration. Although not illustrated, the semiconductor layer **201** of **FIG. 13** is formed using Czochralski (CZ) method. In the back surface **1***b* of the semiconductor layer **201** of **FIG. 13, a** high impurity concentration layer **48**, or an n^+-type drift layer **48**, which has an impurity concentration higher than the semiconductor layer **201**, is located.

[0063] The semiconductor chip **16** of **FIG. 13** is formed in the same manner as the semiconductor chip **15** of **FIG. 11** except for the n^+-type drift layer **48**. At first, a semiconductor wafer **1** is prepared. The wafer **1** includes a semiconductor layer **201**, which is n^--type and formed using CZ method, and a semiconductor element layer **2**, which is located on the semiconductor layer **201**. The wafer **1** has a front surface **1***a,* at the side of which the semiconductor element layer **2** is located, and a back surface **1***b,* which is opposite to the front surface **1***a* and at the side of which the semiconductor layer **201** is located. Then, in the same manner as shown in **FIG. 2**, the wafer **1** is ground with a grindstone **3** from the back surface **1***b*. Then, in the same manner as shown in **FIG. 3**, an adhesive tape **13** is stuck on the back surface **1***b,* and a plurality of cutting grooves **6**, each of which has a predetermined depth from the front surface **1***a,* are formed in the element layer **2** using a cutter **5**.

[0064] Next, in the same manner as shown in **FIG. 4**, an adhesive tape **4** is stuck on the front surface **1***a,* and the

wafer **1** is placed at a predetermined position in an etching pot **8** such that the back surface **1***b* is exposed to an etchant **7** during the etching of the wafer **1** except for the periphery of the back surface **1***b,* which is masked by a gasket **9**. Then, the wafer **1** is etched from the back surface **1***b* by the etchant **7** to form a rim **10** at the periphery of the wafer **1** where the wafer **1** is masked during the etching. With the eching, a recess **11**, which is defined by the rim **10**, is formed in the wafer **1**.

[**0065**] Then, as shown in **FIG. 13**, an n^+-type drift layer **48**, which has a relatively high impurity concentration, is formed in the back surface **1***b*. Subsequently, a drain electrode **12** is formed on the entire back surface **1***b* by depositing a metal using vacuum evaporation, sputtering, CVD, and so on. Then, as shown in **FIG. 5**, the wafer **1** and the adhesive tape **4** located on the front surface **1***a* are supported such that the front surface **1***a* faces downward, and the wafer **1** is pressed by a break roller **14** to bend. With the bending deformation, the wafer **1** breaks along the cutting grooves **6** and separates into a plurality of semiconductor devices **16**, or semiconductor chips **16**. Finally, as shown in **FIG. 6**, each chip **16** is picked up from the adhesive tape **4** and mounted at a predetermined place.

[**0066**] In the manufacturing process of the semiconductor chip **16** of **FIG. 13, a** p-type base layer **41** is directly formed using epitaxial growth on the semiconductor layer **201**, which is n^--type and has a relatively low impurity concentration. In contrast, in the manufacturing process of the semiconductor chip **15** of **FIG. 11**, the n^--type drift layer **40** and the p-type base layer **41** are formed using epitaxial growth on the semiconductor layer **200**. Therefore, the manufacturing cost of the semiconductor chip **16** of **FIG. 13** is lower than that of the semiconductor chip **15** of **FIG. 11**. Moreover, in the semiconductor chip **16** of **FIG. 13**, the n^+-type drift layer **48**, which has a relatively high impurity concentration, is located between the semiconductor layer **201**, which has a relatively low impurity concentration, and the drain electrode **12**. Therefore, otherwise high contact resistance between the n^--type wafer **201** and the drain electrode **12** is reduced by the n^+-type drift layer **48**.

[**0067**] If the n^+-type drift layer **48** was formed on the back surface **1***b* of the wafer **1** after the grinding without the etching, a damaged layer, which is generated in the back surface **1***b* when the wafer **1** is grinded, would lower the mobility of the carriers in the n^+-type drift layer **48**. As a result, the contact resistance between the n^+-type drift layer **48** and the drain electrode **12** would become relatively high, although the n^+-type drift layer **48** reduces the otherwise high contact resistance between the wafer layer **201** and the drain electrode **12**.

[**0068**] However, the wafer **1** is thinned by etching in the same manner as in the step of **FIG. 4**. Therefore, the damaged layer in the back surface **1***b* is eliminated by the etching, and the n^+-type drift layer **48** has relatively high quality. As a result, the otherwise high contact resistance between the wafer layer **201** and the drain electrode **12** is effectively reduced by the n^+-type drift layer **48**.

[**0069**] In the etching of the back surface **1***b* before the formation of the n^+-type drift layer **48**, it is preferred that the back surface **1***b* be etched to have small surface roughness enough to be a mirror surface. The reason is that the n^+-type drift layer **48** is formed to be homogeneous in impurity concentration and the contact resistance between the n^+-type drift layer **48** and the drain electrode **12** becomes homogeneous if the impurity is implanted and diffused into the back surface **1***b* that is a mirror surface. The back surface **1***b* can be etched to become a mirror surface using an etchant that includes nitric acid, hydrofluoric acid, sulfuric acid, and phosphoric acid.

[**0070**] The above methods for manufacturing the semiconductor chips **15**, **16** of **FIGS. 11 and 13** may be modified as follows.

[**0071**] In the above methods, when each wafer **1** is etched in the etching pot **8**, each back surface **1***b* is masked by the gasket **9** except for the periphery of each back surface **1***b* such that each wafer **1** has a rim **10** and a recess **11**, as shown in **FIG. 1C**. However, each back surface **1***b* may be masked in other shapes using a gasket and a known masking material. For example, as shown in **FIG. 14**, beams **50** can be formed in each recess **11** by masking crosswise each back surface **1***b*. The thin bottom of each recess **11** is reinforced with the beams **50**, so each wafer **1** is further prevented from warping or breaking by forming the beams **50** in addition to a rim **10**. With the beams **50**, it becomes more easy to enlarge the size of each wafer **1** to improve the productivity of the semiconductor chips **15**, **16**. The beams **50** can be formed in a shape of the grid, as shown in **FIG. 15**.

[**0072**] In the etching using the pot etching system shown in **FIG. 9**, the progress of etching is monitored to detect precisely the etching end point, as shown in **FIG. 10**. However, the etching end point can be determined on the basis of the etching rate of each wafer **1** if the requirement for the thickness of the chips **15**, **16** allows.

[**0073**] In the grinding method shown in **FIG. 2**, each wafer **1** is thinned to 250 μm. However, the thickness is not limited to 250 μm, and each wafer **1** may be thinned to any thickness as long as each wafer **1** can escape warping or breaking when any force is imposed on each wafer **1** at the manufacturing steps of the chips **15**, **16** including the grinding.

[**0074**] In the etching using the pot etching system shown in **FIG. 9**, each wafer **1** is etched to have a thickness of 100 μm at the bottom of the recess **11**. However, each wafer **1** may be etched to any thickness as long as each wafer **1** can escape breaking when the wafer **1** is handled in the manufacturing steps, for example, when the wafer **1** is removed from the etching pot **8**. However, the thickness is preferably smaller than 200 μm.

[**0075**] In the manufacturing process of the semiconductor chips **15**, **16**, the-steps shown in **FIGS. 2 and 3** are interchangeable in the order. That is, each wafer **1** may be ground with the grindstone **3** from the back surface **1***b* such that the wafer **1** has a predetermined thickness after the cutting grooves **6**, each of which has a predetermined depth from the front surface **1***a,* are formed. In either order, each wafer **1** is evenly thinned by the grinding, so the wafer **1** can be readily further thinned by the etching using the pot etching system shown in **FIG. 9**.

[**0076**] In the method shown in **FIG. 5**, each wafer **1** breaks along the cutting grooves **6**, which are formed using the cutter **5** as shown in **FIG. 3**, and separates into a plurality of semiconductor chips **15**, **16** by pressing the wafer **1** using the break roller **14**. However, each wafer **1** may be separated

into a plurality of semiconductor chips **15**, **16** using the cutter **5** shown in **FIG. 3** instead of the break roller **14** shown in **FIG. 5** without forming the cutting grooves **6** shown in **FIG. 3**. In that case, each wafer **1** may be separated into a plurality of semiconductor chips **15**, **16** by cutting the wafer **1** from the front surface la using the cutter **5**.

[**0077**] The semiconductor chips **15**, **16** shown in **FIGS. 11 and 13** are n channel MOSFET. However, the methods for manufacturing the semiconductor chips **15**, **16** can be applied to a vertical bipolar transistor, a vertical IGBT, and so on.

[**0078**] In the manufacturing process of the semiconductor chip **16** of **FIG. 13**, the n^+-type drift layer **48** is formed in the back surface **1***b* of the wafer **1** to reduce the contact resistance between the semiconductor layer **201** and the drain electrode **12**. However, the layer formed to reduce the contact resistance is not limited to the n^+-type drift layer **48**. As shown in **FIG. 16A, a** p^+-type drain layer **49**, which is p^+-type and has a high impurity concentration, may be formed to be located in the back surface **1***b* of the semiconductor layer **201** instead of the n^+-type drift layer **48**.

[**0079**] Alternatively, as shown in **FIGS. 16B and 16C**, the n^+-type drift layer **48** and the p^+-type drain layer **49** may be formed in combination. In **FIG. 16**B, the n^+-type drift layer **48** and the p^+-type drain layer **49** are layered. In **FIG. 16**C, the n^+-type drift layer **48** and the p^+-type drain layer **49** are located between the semiconductor layer **201** and the drain electrode **12**.

[**0080**] In the manufacturing process of the semiconductor chip **16** of **FIG. 13, a** wafer that is manufactured using Czochralski (CZ) method is used. However, a wafer that is formed using floating zone (FZ) method may be used instead.

[**0081**] In the semiconductor chips **15**, **16**, each conductive type of the n^--type drift layers **40**, the p-type base layers **41**, the n^+-type source regions **42**, the semiconductor layers **200**, **201**, and the n^+-type drift layer **48** can be opposite.

[**0082**] In the manufacturing process of the semiconductor chip **15** of **FIG. 11**, the n^--type drift layer **40** is formed on the semiconductor layer **200**, which has a relatively high impurity concentration, by epitaxial growth. Instead, the layers **40**, **200** may be formed by diffusing n^+-type or p^+-type impurity into an n^--type wafer.

[**0083**] Third Embodiment

[**0084**] With respect to the etching method using the pot etching system shown in **FIG. 9**, JP-A-2000-124166 discloses a method for thinning a wafer to **5** to 100 μm using a pot etching system and KOH aqueous solution after preliminarily thinning the wafer to about 300 μm using a back surface grinding machine. Alternatively, JP-A-2000-91307 discloses a method for etching a silicon wafer using, for example, a 22 weight % aqueous solution of tetramethylammoniumhydroxide (TMAH).

[**0085**] In the etching method using the pot etching system shown in **FIG. 9**, the rim **10** is formed at each periphery of the wafers **1** of the first and second embodiments as shown in **FIGS. 7A and 7B** by masking the periphery with the gasket **9** during the etching. Therefore, although the thickness of each wafer **1** is as thin as 100 μm at the bottom of the recess **11**, each wafer **1** is reinforced by the rim **10**, at which each wafer **1** is as thick as 250 μm, at its periphery. Thus, the wafers **1** are prevented from breaking or warping. However, the wafers **1** are further assuredly prevented from breaking during the machining steps shown in **FIGS. 17A** to **17**F.

[**0086**] For example, a trench-gate type vertical power MOSFET **15** in **FIG. 11** is manufactured using the steps shown in **FIGS. 17A** to **17**F, as follows. As shown **FIG. 17A, a** semiconductor wafer **101**, which has a thickness of 625 μm and includes a plurality of semiconductor element regions **210** and a semiconductor layer **200**, is formed using known semiconductor manufacturing methods. The wafer **101** has a front surface **1***a* and a back surface **1***b*, which is opposite to the front surface **1***a*. Specifically, each region is formed as follows. Firstly, an n^--type drift layer **40** and a p-type base layer **41** are formed by epitaxial growth on the surface of the semiconductor layer **200**. Then, an n^+-type source region **42** is formed in a surface of the p-type base layer **41** of each region **210**.

[**0087**] A trench **43** is formed to extend vertically from a front surface of the source region **42** to the drift layer **40** through the source region **42** and the base layer **41**. Then, a gate-insulating film **44** is formed on the surface defining the trench **43**, and a gate electrode **45** made of doped poly crystalline silicon is formed on the gate-insulating film **44** in the trench **43**. An interlayer insulating film **46** is formed, and a contact hole **46***a* is formed in the interlayer insulating film **46**.

[**0088**] Then, as shown in **FIG. 17B, a** source electrode **47**, which includes a Ti/TiN film **220** as a barrier metal, which includes a titan film and a titan nitride film, and a reinforcing film **230**, or an aluminum alloy film **230**, is formed on each region **210** as follows. Firstly, a titan layer and a titan nitride layer are formed by sputtering to have a total thickness of 300 nm. Then, an aluminum alloy layer having a thickness of 5 μm is formed on the titan nitride layer. For example, an alloy including aluminum and silicon and another alloy including aluminum, silicon, and copper may be used as the aluminum alloy film **230**. Next, each Ti/TiN film **220** and each aluminum alloy film **230** are simultaneously patterned out of the titan, titan nitride, and aluminum alloy layers using photolithography and etching. Then, each Ti/TiN film **220** and each aluminum alloy film **230** are sintered at about 450° C. in a reducing atmosphere.

[**0089**] Subsequently, as shown in **FIG. 17**C, another reinforcing film **240**, or a polyimide film **240**, which also functions as a passivation film, is formed on each source electrode **47** as follows. Firstly, a polyimide layer having a thickness of 10 μm is formed by coating liquid polyimide using a spin coater. Then, the polyimide layer is patterned using photolithography and etching. Then, each polyimide film **240** is completed by curing the patterned polyimide layer at about 350° C. to fully imidize the patterned polyimide layer. As described later, the wafer **101** is reinforced by the aluminum alloy film **230** having a thickness of 5 μm and the polyimide film **240** having a thickness of 10 μm.

[**0090**] When the polyimide film **240** is formed, a stopper film **250**, or a thick polyimide rim **250**, is formed at the periphery of the wafer **101** around the regions **210** as follows. Firstly, as shown in **FIG. 18**, precured liquid polyimide is coated with a brush on the periphery in the area within 5 mm from the circumferential edge of the wafer **101**.

Then, the polyimide rim **250** is completed by curing the precured liquid polyimide at about 350° C. The polyimide rim **250** is thick enough to function as a stopper in the horizontal direction of the **FIG. 18**, as described later.

[**0091**] Then, as shown in **FIG. 17**D, the wafer **101**, the semiconductor part **200, 210** of which has a thickness of 625 μm, is ground with a grinder from the back surface **1***b* such that the semiconductor part **200, 210** has a thickness of 250 μm. Before the grinding, the wafer **101** is plastered with a thick adhesive film on the front surface la for protecting the front surface la. The adhesive film is thick enough to prevent the wafer **101** from breaking due to the unevenness caused by the polyimide rim **250**, which is located at the periphery of the wafer **101** on the front surface **1***a,* during the grinding.

[**0092**] Next, as shown in **FIG. 17**E, the wafer **101** is etched from the back surface **1***b* until the thickness of the semiconductor part **200, 210** becomes 100 μm at the etched area, or until the semiconductor part **200, 210** is etched off by 150 μm. TMAH is used as an etchant. The steps for the etching will be explained in detail. At first, as shown in **FIG. 19**A, an annular gasket **320** is placed between a cylindrical first member **300** and an annular second member **310**, and the first and second members **300, 310** are fastened together using external threads and corresponding internal threads **330**, which are located in the second member **310**, to clamp the gasket **320** between the members **300, 310**.

[**0093**] Then, as shown in **FIG. 19**B, the wafer **101** is placed on the gasket **320** such that the back surface **1***b* faces the gasket **320** at the periphery of the back surface **1***b*. Next, as shown in **FIG. 19C, a** third member **340** is attached to the second member **310** to fix the wafer **101** between the gasket **320** and the third member **340**. Then, the space between the first and second members **300, 310** is depressurized through a depressurizing passage **35** such that the first and second members **300, 310** adhere to each other and the wafer **101** and the gasket **320** become in contact without a gap that can cause etchant leakage.

[**0094**] Subsequently, as shown in **FIG. 19**D, the assembly of **FIG. 19C** is turned upside down and filled with an etchant **360**. Then, as shown in **FIG. 19**E, the assembly filled with the etchant **360** is covered with a forth member **370**. The forth member **370** includes a heater **380** and a stirrer **390**, and the etchant **360** is heated and stirred with the heater **380** and the stirrer **390** while the wafer **101** is etched. After a predetermined etching period, the forth member **370** is dismantled from the assembly of **FIG. 19**E, as shown in **FIG. 19F**. The etchant **360** is drained out, as shown in **FIG. 19G**. Then, the assembly of **FIG. 19G** is turned upside down, and the third member **340** is dismantled from the assembly of **FIG. 19**G, as shown in **FIG. 19H**.

[**0095**] Next, as shown in **FIG. 19**I, the wafer **101** is partially, slightly pushed up from the back surface **1***b*. Then, as shown in **FIG. 19**J, the wafer **101** is pinched by a pair of tweezers at its periphery, where the wafer **101** is masked by the gasket **320** and relatively thicker, and picked up from the assembly of **FIG. 19H**. However, as shown in **FIG. 20**, if the polyimide rim **250** was not formed, the edge of the wafer **101** would readily intrude the gap between the first and second members **300, 310** and the wafer **101** would readily break when the wafer **101** was picked up.

[**0096**] As shown in **FIG. 21**A, the wafer **101** originally has a beveled edge at its end, so the edge has a relatively large angle before the grinding step of **FIG. 17D**. Therefore, if the wafer **101** was etched without the grinding, the above problem would not be caused even if the polyimide rim **250** was not formed. However, in that case, the productivity decreases because the etching rate of the wafer **101** is as low as 0.8 μm/min even when a TMAH aqueous solution having a concentration of 22% is used as an etchant. Therefore, the grinding is practically inevitable from the standpoint of productivity.

[**0097**] As shown in **FIG. 21**B, the edge of the wafer **101** would become sharpened after the grinding if the polyimide rim **250** was not formed, and the edge of the wafer **101** would readily intrude the gap between the first and second members **300, 310**, as shown in **FIG. 20**. However, the polyimide rim **250** is formed at the periphery of the wafer **101** at the step of **FIG. 17**C, so the edge has a relatively large angle and the wafer **101** is relatively thick at its end after the grinding, as shown in **FIG. 21C**. Therefore, as shown in **FIG. 22**, the edge of the wafer **101** does not intrude the gap between the first and second members **300, 310** because the polyimide rim **250** functions as a stopper. Thus, the wafer **101** is prevented from breaking when the wafer **101** was picked up.

[**0098**] The wafer **101** is placed in a wafer carrier **400** after the wafer **101** is picked up as shown **FIG. 19J**, and the wafer **101** is rinsed with deionized water (DIW), as shown in **FIG. 23**. At that time, the wafer **101** is pressed and deformed by the flow of DIW. However, the wafer **101** is reinforced by the aluminum alloy film **230**, which is elastic and has a thickness of 5 μm, and the polyimide film **240**, which is elastic and has a thickness of **10** Am. Therefore, the wafer **101** is prevented from breaking when being deformed by the flow of DIW during the rinsing.

[**0099**] On the other hand, a trench-gate type vertical power MOSFET having a conventional metal electrode and a passivation film is manufactured using the manufacturing steps shown in **FIGS. 24A** to **24**E. Firstly, as shown **FIG. 24A, a** semiconductor wafer **102**, which has includes a plurality of semiconductor element regions **210** and a semiconductor layer **200**, is formed. Then, a titan layer and a titan nitride layer are formed to have a total thickness of 300 nm, and an aluminum alloy layer having a thickness of 2 μm is formed on the titan nitride layer.

[**0100**] Next, as shown in **FIG. 24**B, each Ti/TiN film **500** and each aluminum alloy film **510** are simultaneously patterned out of the titan, titan nitride, and aluminum alloy layers using photolithography and etching. Then, each Ti/TiN film **500** and each aluminum alloy film **510** are sintered at about 450° C. in a reducing atmosphere. Then, a silicon nitride layer having a thickness of 1.5 μm is formed by CVD, and a passivation film **520**, or a silicon nitride film **520**, is patterned out of the silicon nitride layer on each aluminum alloy film **510** by using photolithography and etching, as shown in **FIG. 24C**. Then, as shown in **FIGS. 24D and 24E**, the wafer **102** is ground with a grinder and eatched.

[**0101**] In comparison with the wafer **102** of **FIG. 24**E, the wafer **101** of **FIG. 17E** is reinforced by the aluminum alloy film **230**, which is thicker than the aluminum alloy film **510**, and the polyimide film **240**. Therefore, the wafer **101** of **FIG. 17E** is less fragile than the wafer **102** of **FIG. 24E**.

[**0102**] The polyimide film **240** can be formed on the scribe lines between two semiconductor element regions **210**

adjacent to each other. However, when the wafer **101** is diced, the diced chips tend to be pitted because the dicing saw blade clogs with the polyimide resin of the polyimide film **240**. Therefore, in that case, the pitting needs to be addressed.

[**0103**] After the rinsing step shown in **FIG. 23**, the back surface **1***b* of the wafer **101** is cleansed by, for example, reverse sputtering. Then, as shown in **FIG. 17F, a** titan layer, a nickel layer, and a gold layer are deposited respectively to a predetermined thickness on the back surface **1***b* in this order to form a Ti/Ni/Au layer **12**. A part of the Ti/Ni/Au layer **12** becomes a back surface electrode **12**, or a drain electrode **12** of the device in **FIG. 11**. As shown in **FIG. 17**E, the wafer **101** has a rim **10** having a thickness of 250 μm at its periphery, so the wafer **101**, the etched area of which is as thin as 100 μm, hardly warps.

[**0104**] As a result, the wafer **101** is prevented from coming out from the loading arm that carries the wafer **101** during the depositing step. Moreover, the wafer **101** is prevented from contacting another wafer **101** when the wafers **101** are loaded into a wafer carrier to be adjacent to each other. Moreover, the polyimide rim **250** does not harmfully affect when the wafer **101** is rinsed or when the Ti/Ni/Au layer **12** is formed.

[**0105**] After the deposition step shown in **FIG. 17**F, the wafer **101** is diced into individual chips **15** to complete thin power devices that are as thin as 100 μm.

[**0106**] As shown in **FIG. 25**, wafers thinner than 300 mm readily break. However, as shown in **FIG. 26**, the wafers can become less breakable using a reinforcing film or a stopper film. In **FIG. 26**, wafer breakage rates are shown for six combinations of the reinforcing film and the stopper film; (I) a silicon nitride film and an aluminum alloy film having respectively thicknesses of 1 μm and 900 nm without a polyimide rim, (II) a polyimide film and an aluminum alloy film having respectively thicknesses of 2 μm and 900 nm without a polyimide rim, (III) a polyimide film and an aluminum alloy film having respectively thicknesses of 2 μm and 5 μm without a polyimide rim, (IV) a polyimide film and an aluminum alloy film having respectively thicknesses of 10 μm and 5 μm without a polyimide rim, (V) a polyimide film and an aluminum alloy film having respectively thicknesses of 10 μm and 5 μm and a polyimide rim, and (VI) a polyimide film and an aluminum alloy film having respectively thicknesses of 10 μm and 900 nm and a polyimide rim.

[**0107**] Comparing the combination (I) with the combination (II), it is concluded that the polyimide film having a thickness of 2 μm can prevent wafers from breaking better than the silicon nitride film having a thickness of 1 μm. Comparing the combination (II) with the combination (III), it is concluded that wafers become less breakable as the aluminum alloy film becomes thicker. Comparing the combination (III) with the combination (IV), it is concluded that wafers become less breakable as the polyimide film becomes thicker. Comparing the combination (IV) with the combination (V), it is concluded that wafers become less breakable with the polyimide rim. Comparing the combination (V) with the combination (VI), it is concluded that wafers also become less breakable as the aluminum alloy film becomes thicker in combination with polyimide rim.

[**0108**] The manufacturing process shown by **FIGS. 17A** to **17**F can be modified as shown in **FIGS. 27A** to **27**F, in which any polyimide rum **250** is not formed and which respectively correspond to **FIGS. 17A** to **17**F. Firstly, as shown **FIG. 27A, a** semiconductor wafer **103**, which has includes a plurality of semiconductor element regions **210** and a semiconductor layer **200**, is formed in the same manner as described for the step of **FIG. 17A**. Then, as shown in **FIG. 27**B, Ti/TiN films **600**, which have a total thickness of 300 nm, and reinforcing films **610**, or aluminum alloy films **610**, which have a thickness of 5 μm, are formed in the same manner as described for the step of **FIG. 17B**.

[**0109**] Subsequently, as shown in **FIG. 27C, a** reinforcing film **620**, or a polyimide film **620**, which also functions as a passivation film, is formed in the same manner as described for the polyimide film **240** of **FIG. 17C**. In the manufacturing process shown by **FIGS. 27A** to **27**F, no thick polyimide rim **250** is formed at the periphery of the wafer **103** around the regions **210**. In that aspect, the manufacturing process shown by **FIGS. 27A** to **27**F is different from that shown by **FIGS. 17A** to **17**F. Then, as shown in **FIGS. 27D and 27E**, the wafer **103** is ground with a grinder and eatched in the same manner as described for the steps of **FIGS. 17D and 17E**. Finally, as shown in **FIG. 27F, a** Ti/Ni/Au layer **12** is formed in the same manner as described for the step of **FIG. 17F**.

[**0110**] The manufacturing process shown by **FIGS. 17A** to **17**F can be further modified as follows. At the step of **FIG. 17**B, the aluminum alloy film **230** having a thickness of 5 μm is formed on each region **210**. However, the aluminum alloy film **230** may have a thickness greater than 5 μm. Instead of the aluminum alloy film **230**, a film substantially made of pure aluminum may be used. At the step of **FIG. 17**C, the polyimide film **240** having a thickness of 10 μm is formed. However, the polyimide film **240** may have a thickness greater than 10 μm. In the manufacturing process shown by **FIGS. 17A** to **17**F, both aluminum alloy film **230** and the polyimide film **240** are formed. However, only one of them may be formed. In addition, the polyimide rim **250** may be formed without forming the aluminum alloy film **230** and the polyimide film **240**.

What is claimed is:

1. A method for manufacturing a semiconductor device, in which a semiconductor element layer is located on a semiconductor layer, the method comprising steps of:

forming a semiconductor wafer that includes a semiconductor layer and a semiconductor element layer, which is located on the semiconductor layer, wherein the wafer has a first surface, at the side of which the semiconductor element layer is located, wherein the wafer has a second surface, which is opposite to the first surface, and at the side of which the semiconductor layer is located;

grinding evenly the wafer from the second surface to a predetermined thickness; and

etching the wafer to a predetermined thickness from the second surface while masking a periphery of the wafer against an etchant to form a rim at the periphery.

2. The method in claim 1, wherein the wafer is etched while an area inside the periphery is partially masked to form a beam in the area.

3. The method in claim 1, wherein the roughness of the second surface after the etching is controlled on a basis of the composition of the etchant used in the etching.

4. The method in a claim 1 further comprising a step of forming an electrode on the second surface.

5. The method in claim 1, wherein the wafer is etched while the first surface is protected with a protection member.

6. The method in claim 1, wherein the wafer is etched while the thickness of the wafer is monitored to stop etching when the wafer is etched to the predetermined thickness.

7. The method in claim 1, wherein the predetermined thickness at the etching is smaller than 200 μm.

8. A method for manufacturing a semiconductor device, in which a semiconductor element layer is located on a semiconductor layer that has a relatively low impurity concentration, the method comprising steps of:

forming a semiconductor wafer that includes a semiconductor layer, which has a relatively low impurity concentration, and a semiconductor element layer, which is located on the semiconductor layer, wherein the wafer has a first surface, at the side of which the semiconductor element layer is located, wherein the wafer has a second surface, which is opposite to the first surface, and at the side of which the semiconductor layer is located;

grinding evenly the wafer from the second surface to a predetermined thickness; and

etching the wafer to a predetermined thickness from the second surface while masking a periphery of the wafer against an etchant to form a rim at the periphery; and

forming a high impurity concentration layer, which has an impurity concentration higher than the semiconductor layer, at the second surface.

9. The method in claim 8, wherein the wafer is etched while an area inside the periphery is partially masked to form a beam in the area.

10. The method in claim 8, the roughness of the second surface after the etching is controlled on a basis of the composition of the etchant used in the etching.

11. The method in claim 8 further comprising a step of forming an electrode on the second surface.

12. The method in claim 8, wherein the wafer is etched while the first surface is protected with a protection member.

13. The method in claim 8, wherein the wafer is etched while the thickness of the wafer is monitored to stop etching when the wafer is etched to the predetermined thickness.

14. The method in claim 8, wherein the predetermined thickness at the etching is smaller than 200 μm.

15. A method for machining a semiconductor wafer, the method comprising steps of:

forming a semiconductor wafer that includes a semiconductor layer and a semiconductor element region, which is located on the semiconductor layer, wherein the wafer has a first surface, at the side of which the semiconductor element region is located, wherein the wafer has a second surface, which is opposite to the first surface, and at the side of which the semiconductor layer is located;

forming a reinforcing film, which reinforces the wafer, on the first surface;

setting the wafer in an etching apparatus such that the back surface faces a gasket at a periphery on the back surface; and

etching the wafer to a predetermined thickness from the second surface while partially masking the wafer against an etchant with the gasket to form a rim.

16. A method for machining a semiconductor wafer, the method comprising steps of:

forming a semiconductor wafer that includes a semiconductor layer and a semiconductor element region, which is located on the semiconductor layer, wherein the wafer has a first surface, at the side of which the semiconductor element region is located, wherein the wafer has a second surface, which is opposite to the first surface, and at the side of which the semiconductor layer is located;

forming a stopper film at a periphery of the wafer on the first surface;

setting the wafer in an etching apparatus such that the back surface faces a gasket at a periphery of the wafer; and

etching the wafer to a predetermined thickness from the second surface while partially masking the wafer against an etchant with the gasket to form a rim.

17. A method for machining a semiconductor wafer, the method comprising steps of:

forming a semiconductor wafer that includes a semiconductor layer and a semiconductor element region, which is located on the semiconductor layer, wherein the wafer has a first surface, at the side of which the semiconductor element region is located, wherein the wafer has a second surface, which is opposite to the first surface, and at the side of which the semiconductor layer is located;

forming a reinforcing film, which reinforces the wafer, on the first surface;

forming a stopper film at a periphery of the wafer on the first surface;

setting the wafer in an etching apparatus such that the back surface faces a gasket at a periphery of the wafer; and

etching the wafer to a predetermined thickness from the second surface while partially masking the wafer against an etchant with the gasket to form a rim.

18. The method in claim 15, wherein the reinforcing film is formed using one film selected from the group consisting of a metal film and a resin film.

19. The method in claim 18, wherein the metal film is formed to have a thickness of 5μm or greater using one film selected from the group consisting of an aluminum film and an aluminum alloy film.

20. The method in claim 18, wherein the resin film is formed to have a thickness of 10 μm or greater using a polyimide film.

21. The method in claim 16, wherein the stopper film is formed by painting a polyimide with a brush.

* * * * *