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(71) Applicant: **QUALCOMM INCORPORATED** [US/US]; ATTN: International IP Administration, 5775 Morehouse Drive, San Diego, California 92121 (US).

(72) Inventors: **DONG, Xiangyu**; 5775 Morehouse Drive, San Diego, California 92121 (US). **SUH, Jungwon**; 5775 Morehouse Drive, San Diego, California 92121-1714 (US).

(74) Agent: **LENKIN, Alan M.**; Seyfarth Shaw LLP, Suite 3500, 2029 Century Park East, Los Angeles, California 90067-3021 (US).

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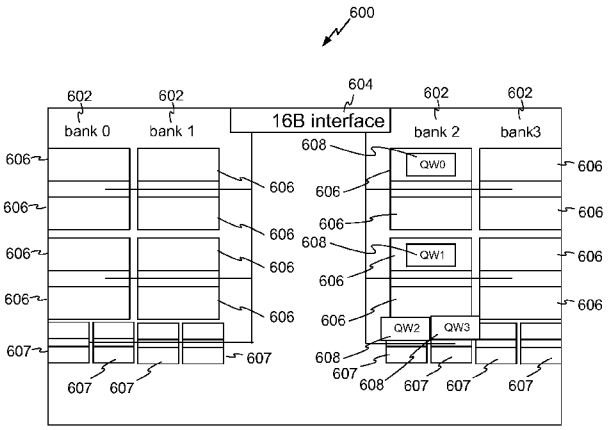

FIG. 6

(57) Abstract: A hybrid cache includes a static random access memory (SRAM) portion and a resistive random access memory portion. Cache lines of the hybrid cache are configured to include both SRAM macros and resistive random access memory macros. The hybrid cache is configured so that the SRAM macros are accessed before the resistive random memory macros in each cache access cycle. While SRAM macros are accessed, the slower resistive random access memory reach a data access ready state.

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MIXED MEMORY TYPE HYBRID CACHE

TECHNICAL FIELD

[0001] The present disclosure generally relates to memory caches. More specifically, the present disclosure relates to memory cache lines operating with different types of memory.

BACKGROUND

[0002] Unlike conventional random access memory (RAM) chip technologies, in magnetic RAM (MRAM) data is not stored as electric charge, but is instead stored by magnetic polarization of storage elements. The storage elements are formed from two ferromagnetic layers separated by a tunneling layer. One of the two ferromagnetic layers, which is referred to as the fixed layer or pinned layer, has a magnetization that is fixed in a particular direction. The other ferromagnetic magnetic layer, which is referred to as the free layer, has a magnetization direction that can be altered to represent either a "1" when the free layer magnetization is anti-parallel to the fixed layer magnetization or "0" when the free layer magnetization is parallel to the fixed layer magnetization or vice versa. One such device having a fixed layer, a tunneling layer, and a free layer is a magnetic tunnel junction (MTJ). The electrical resistance of an MTJ depends on whether the free layer magnetization and fixed layer magnetization are parallel or anti-parallel with each other. A memory device such as MRAM is built from an array of individually addressable MTJs.

[0003] To write data in a conventional MRAM, a write current, which exceeds a critical switching current, is applied through an MTJ. The write current exceeding the critical switching current is sufficient to change the magnetization direction of the free layer. When the write current flows in a first direction, the MTJ can be placed into or remain in a first state, in which its free layer magnetization direction and fixed layer magnetization direction are aligned in a parallel orientation. When the write current flows in a second direction, opposite to the first direction, the MTJ can be placed into or remain in a second state, in which its free layer magnetization and fixed layer magnetization are in an anti-parallel orientation.

[0004] To read data in a conventional MRAM, a read current flows through the MTJ via the same current path used to write data in the MTJ. If the magnetizations of the MTJ's free layer and fixed layer are oriented parallel to each other, the MTJ presents a resistance that is different than the resistance the MTJ would present if the magnetizations of the free layer and the fixed layer were in an anti-parallel orientation. In a conventional MRAM, two distinct states are defined by two different resistances of an MTJ in a bitcell of the MRAM. The two different resistances represent a logic "0" and a logic "1" value stored by the MTJ.

BRIEF SUMMARY

[0005] A hybrid cache apparatus according to an aspect of the present disclosure includes a first type of memory and a second type of memory. A first cache line of the hybrid cache apparatus includes a first memory location in the first type of memory and a second memory location in the second type of memory. The first cache line is configured for accessing the first memory location before accessing the second memory location during a cache accessing operation.

[0006] Another aspect of the present disclosure includes a method for accessing a hybrid cache apparatus. The method includes storing a first portion of cached information in a first type of memory of a first cache line, and storing a second portion of the cached information in a second type of memory of the first cache line. The method also includes accessing the first portion of the cached information before accessing the second portion of the cached information during a cache accessing operation.

[0007] A hybrid cache apparatus according to another aspect of the present disclosure includes means for storing a first portion of cached information in a static random access memory (SRAM) location of a first cache line and means for storing a second portion of the cached information in a resistive random access memory portion of the first cache line. The hybrid cache apparatus also includes means for accessing the first portion of the cached information before accessing the second portion of the cached information during a cache accessing operation.

[0008] This has outlined, rather broadly, the features and technical advantages of the present disclosure in order that the detailed description that follows may be better

understood. Additional features and advantages of the disclosure will be described below. It should be appreciated by those skilled in the art that this disclosure may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present disclosure. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the teachings of the disclosure as set forth in the appended claims. The novel features, which are believed to be characteristic of the disclosure, both as to its organization and method of operation, together with further objects and advantages, will be better understood from the following description when considered in connection with the accompanying figures. It is to be expressly understood, however, that each of the figures is provided for the purpose of illustration and description only and is not intended as a definition of the limits of the present disclosure.

DESCRIPTION OF THE DRAWINGS

[0009] For a more complete understanding of the present disclosure, reference is now made to the following description taken in conjunction with the accompanying drawings.

[0010] FIGURE 1 is a diagram of a resistive memory element.

[0011] FIGURE 2 is a diagram of a resistive memory device and circuitry for programming and reading the resistive device.

[0012] FIGURE 3 is a diagram of a memory macro.

[0013] FIGURE 4 is a diagram of a prior art SRAM cache.

[0014] FIGURE 5A is an SRAM cache pipeline timing diagram.

[0015] FIGURE 5B is an MRAM cache pipeline timing diagram.

[0016] FIGURE 6 is a diagram of a hybrid SRAM-MRAM cache according to an aspect of the present disclosure.

[0017] FIGURE 7 is a cache pipeline timing diagram for a hybrid SRAM-MRAM cache according to an aspect of the present disclosure.

[0018] FIGURE 8 is a diagram of a hybrid SRAM-MRAM cache according to an aspect of the present disclosure.

[0019] FIGURE 9 is a cache pipeline timing diagram for a hybrid SRAM-MRAM cache according to an aspect of the present disclosure.

[0020] FIGURE 10 is process flow diagram illustrating a method of accessing a hybrid SRAM-MRAM cache according to an aspect of the present disclosure.

[0021] FIGURE 11 is a block diagram showing an exemplary wireless communication system in which a configuration of the disclosure may be advantageously employed.

[0022] FIGURE 12 is a block diagram illustrating a design workstation used for circuit, layout, and logic design of a semiconductor component according to one configuration.

DETAILED DESCRIPTION

[0023] FIGURE 1 illustrates a resistive memory element 100 including a magnetic tunnel junction (MTJ) 102 coupled to an access transistor 104. A free layer 110 of the MTJ 102 is coupled to a bit line 112. The access transistor 104 is coupled between a fixed layer 106 of the MTJ 102 and a fixed potential node 122. A tunnel barrier layer 114 is coupled between the fixed layer 106 and the free layer 110. The access transistor 104 includes a gate 116 coupled to a word line 118.

[0024] Synthetic anti-ferromagnetic materials may be used to form the fixed layer 106 and the free layer 110. For example, the fixed layer 106 may comprise multiple material layers including a CoFeB, and Ru layer and a CoFe layer. The free layer 110 may be an anti-ferromagnetic material such as CoFeB, and the tunnel barrier layer 114 may be MgO, for example.

[0025] FIGURE 2 is a circuit schematic illustrating a portion of a conventional magnetic random access memory (MRAM) 200. An MRAM 200 is divided into a data circuit 260, and reference circuits 240, 210, each circuit 210, 240, 260 including multiple bitcells 212, 226 (only a single bitcell is illustrated to facilitate understanding). During read out of the bitcell of the data circuit 260, the resistance of the magnetic tunnel junction is compared to the effective resistance of two reference MTJs connected in parallel, where one is the reference parallel MTJ of the reference circuit 210 and the other is the reference anti-parallel MTJ of the circuit 240. Resistance of the bitcells is measured by applying a source voltage and determining an amount of current flowing through the bitcells. For example, in the bitcell of the parallel reference circuit 210, a

current source 220 is applied to a magnetic tunnel junction (MTJ) 212 by read select transistors 222, 224, and a word line select transistor 226. The MTJ 212 includes a fixed layer 214, tunneling layer 216, and a free layer 218. When the free layer 218 and the fixed layer 214 have magnetizations aligned substantially parallel, the resistance of the MTJ 212, and thus the bitcell 210, is low. When the free layer 218 and the fixed layer 214 have magnetizations aligned substantially anti-parallel, the resistance of the MTJ 212, and thus the bitcell 210, is high.

[0026] Bitcells of a magnetic random access memory (MRAM) may be arranged in one or more arrays including a pattern of memory elements (e.g., MTJ in case of MRAM). Spin-Transfer-Torque Magnetic Random Access Memory (STT-MRAM) is an emerging nonvolatile memory and its advantages of non-volatility, comparable speed to Dynamic Random Access Memory (DRAM), smaller chip size compared to Static Random Access Memory (SRAM), unlimited read/write endurance, and low array leakage current have opened a great opportunity to Spin-Transfer-Torque Magnetic Random Access Memory (STT-MRAM) as a universal working memory in System on Chip (SoC) design.

[0027] In resistive memory array, a reference level for read sensing is generated upon activation of a word line (WL) by assertion of a read enable signal. The generation of a reference level in resistive memories results in a longer memory access cycle. For example, in an MRAM array, after activation of the WL, five clock cycles may elapse including to accommodate a settling time for the data circuit 260 and reference circuits 240, 210 before an MRAM bitcell may reach a data out ready state. In comparison, SRAM memory cells may be accessed in three clock cycles.

[0028] FIGURE 3 illustrates a memory macro 300. The macro 300 may include a local data path (LDP) 302, a global data path (GDP) 304, a cell array 306, a decoder 308, and a global control unit 310. The LDP 302 includes one or more sense amplifiers and a programming write driver (not shown). The GDP 304 includes circuitry for input and output signal lines or pins, such as a D IN 312 and a D OUT 314.

[0029] The cell array 306 includes multiple rows corresponding to word lines, for example a WL 316 and multiple columns corresponding to bit lines, for example a bit line 318. For example, the cell array 306 may have 64 rows for word lines and 256 bits for bit lines. The cell array 306 includes numerous unit cells such as a unit cell 320, coupled to the word line 316 and the bit line 318. The memory macro 300 may be

implemented using various memory cell technologies in which each unit cell in the memory macro 300 includes a similarly constructed memory element. For example, in a resistive memory macro, each unit cell 320 includes a resistive memory element 100 as described with reference to FIGURE 1.

[0030] A cache memory may include a number of macros coupled to a cache interface. An MRAM cache includes banks of MRAM macros coupled to the cache interface. An SRAM cache includes banks of SRAM macros coupled to the cache interface. SRAM macros have an advantage of being faster than resistive memory macros such as MRAM macros. Resistive memory macros such as MRAM macros exhibit longer read latency than SRAM due to difficult bitcell sensing and longer write latency due to difficult status switching. However, SRAM macros are volatile, consume more leakage energy and are substantially larger than MRAM macros. For example, the size of an SRAM bitcell is about 200 F^2, where F is the minimum feature size of a chip. An SRAM last-level cache may consume about 50% of a modern central processing unit (CPU) area. In contrast, MRAM macros are non-volatile and are energy efficient when idle. The size of an MRAM bitcell is only about 4 F^2. Due to their small size, MRAM macros are suitable for larger level 2 and level 3 (L2/L3) on-chip cache integration.

[0031] An example of an SRAM cache architecture is described with reference to FIGURE 4. The SRAM cache 400 includes four banks 402 coupled to a cache interface 404. Each bank 402 includes a number of SRAM macros 406. In this example, the cache interface 404 is 16 bytes wide and thus is able to access one quad word (QW) 408 of memory at a time, in which each QW 408 is 16 bytes of memory in an SRAM macro 406. During a cache access, a fixed amount of data is written to or read from the cache. The memory associated with the fixed amount of data for a cache line is referred to herein as a cache line. A 64 byte cache line includes four QWs 408 in a bank 402, in which each of the QWs 408 is in a respective SRAM macro 406. A 64 byte cache access is divided into four QW accesses, in which each QW accesses reads to or writes from one of the SRAM macros 406 on the cache line.

[0032] Timing of an SRAM cache line access is described with reference to an SRAM cache line access diagram 500 in FIGURE 5A. In this example, an SRAM macro read access or write access uses three clock cycles including an enable cycle and two array access cycles. Thus, cycle 1 - cycle 3 elapse before each of the SRAM

macros can reach a data out ready state. Another cycle is used to clock each QW to or from the data bus so the four QWs (QW0 - QW3) of the SRAM cache line reach the data bus in cycle 5 - cycle 8.

[0033] The slower operation of an MRAM cache line access is described with reference to an MRAM cache line access diagram 550 in FIGURE 5B. In this example, an MRAM macro read access or write access uses five clock cycles including an enable cycle and four array access cycles. Thus, cycle 1 - cycle 5 elapse before each of the MRAM macros can reach a data out ready state. Another clock cycle is used to clock each QW onto the data, so the four QWs (QW0 - QW3) of the MRAM cache line reach the data bus in cycle 7 - cycle 10.

[0034] According to aspects of the present disclosure, MRAM macros may be used for storing non-critical QWs in which it is tolerable to allow an access delay of two or more clock cycles. The use of larger, less energy efficient SRAM macros may be reserved for situations in which such a delay is not tolerable. Referring to FIGURES 5A and 5B, according to aspects of the present disclosure, SRAM macros may be configured on a cache line to provide QWs in cycle 5 and cycle 6 of a memory access and MRAM macros may be configured to provide QWs in cycle 7 and cycle 8 of the memory access.

[0035] Further the first QW of a cache line often includes the most critical data of a memory access and the remaining QWs may include less critical information. In such configurations it is desirable to provide fast access to the first QW of a cache line but slower access to the remaining QWs of a cache line may be tolerable. According to aspects of the present disclosure, the first QW of a cache line may be stored in an SRAM macro and one or more of the remaining QWs may be stored in an MRAM macro. According to another aspect of the present disclosure, the first QW of a cache line may be configured for storing critical words of cached information.

[0036] A hybrid SRAM-MRAM cache line including both SRAM macros and MRAM macros, according to an aspect of the present disclosure, is described with reference to FIGURE 6. The hybrid SRAM-MRAM cache 600 includes four banks 602 coupled to a cache interface 604. Each bank 602 includes a number of SRAM macros 606 and a number of MRAM macros 607 coupled to the cache interface 604. In this example, the cache interface 604 is 16 bytes wide and thus is able to access one 16 byte

quad word (QW) 608 of memory at a time. A 64 byte cache line includes two QWs 608 in SRAM macros 606 of a bank 602, and two QWs 608 in MRAM macros 607 of the bank. A 64 byte cache access is divided into four QW accesses in which the first two QW accesses read to or write from the SRAM macros 606 on the cache line and the second two QW accesses read to or write from the MRAM macros 607 on the cache line.

[0037] Timing of a hybrid SRAM-MRAM cache line access in the implementation shown in FIGURE 6 is described with reference to the cache line access diagram 700 in FIGURE 7. In this implementation, each SRAM macro read access or write access uses three clock cycles including an enable cycle and two array access cycles. Each MRAM macro read access or write access uses five clock cycles including an enable cycle and four array access cycles. An SRAM macro read access or write access is used to access the first two QWs (QW0 and QW1) of a cache line. Clock cycle 1 - cycle 3 elapse before the SRAM macros can reach a data out ready state. A next clock cycle (cycle 4) is used to clock the first QW of the cache line (QW0) to or from the data bus. The following clock cycle (cycle 5) is then used to clock the second QW of the cache line (QW1) to or from the data bus. An MRAM macro read access or write access is used to access the newt two QWs (QW2 and QW3) of the cache line. The MRAM macros reach a data out ready state in clock cycle 6. Clock cycles 6 and 7 are used to clock the third QW (QW2) of the cache line and the fourth QW (QW3) of the cache line to or from the data bus.

[0038] In the implementation of a hybrid SRAM-MRAM cache shown in FIGURE 6, the number of SRAM macros and MRAM macros in a cache line are chosen so that the cache line access pipeline is matched to the difference between the SRAM macro access time of three clock cycles and the MRAM macro access time of five clock cycles. In another implementation, according to an aspect of the present disclosure the cache line access pipeline may not be perfectly matched to the difference between the SRAM macro access time and the MRAM macro access time. Accesses to more than one cache line may be interleaved in order to accommodate additional clock cycles that may elapse before MRAM macros are in a data access ready state. An implementation of a pair of interleaved hybrid SRAM-MRAM cache lines, according to an aspect of the present disclosure, is described with reference to FIGURE 8.

[0039] A hybrid SRAM-MRAM cache line including both SRAM macros and MRAM macros according to an aspect of the present disclosure is described with reference to FIGURE 8. The hybrid SRAM-MRAM cache 800 includes four banks 801 - 804 coupled to a cache interface 806. Each bank 801 - 804 includes a number of SRAM macros 808 and a number of MRAM macros 809 coupled to the cache interface 806. In this example, the cache interface 806 is 16 bytes wide and thus is able to access one 16 byte quad word (QW) 810 of memory at a time. A first 64 byte cache line includes two QWs 810 in SRAM macros 808 of a first bank 803, and two QWs 810 in MRAM macros 809 of the first bank 803. A second 64 bit cache line includes two QWs 810 in SRAM macros 808 of a second bank 804 and two QWs 810 in MRAM macros 809 of the second bank 804.

[0040] A first 64 byte cache access is divided into four QW accesses, in which the first two QWs (QW0 and QW1) are read to or written from the SRAM macros 808 on the first cache line and the second two QWs (QW2 and QW3) are read to or written from the MRAM macros 809 on the first cache line. A second 64 byte cache access is divided into four QW accesses, in which the first two QWs (QW4 and QW5) are read to or written from the SRAM macros 808 on the second cache line and the second two QWs (QW6 and QW7) are read to or written from the MRAM macros 809 on the second cache line.

[0041] Timing of a hybrid SRAM-MRAM cache line access in the implementation shown in FIGURE 8 is described with reference to the cache line access diagram 900 in FIGURE 9. In this implementation, each SRAM macro read access or write access uses three clock cycles including an enable cycle and two array access cycles. Each MRAM macro read access or write access uses seven clock cycles including an enable cycle and six array access cycles. A first SRAM macro read access or write access is used to access the first two QWs (QW0 and QW1) of the first cache line. Clock cycles 1 - cycle 3 elapse before the SRAM macros can reach a data out ready state. A next clock cycle (cycle 4) is used to clock the first QW of the first cache line (QW0) to or from the data bus. The following clock cycle (cycle 5) is then used to clock the second QW of the first cache line (QW1) to or from the data bus.

[0042] In this implementation, because the MRAM macro access takes seven clock cycles, they do not reach a data access ready state until clock cycle 8. To avoid idle cycles on the cache interface 806, a second cache line access begins while waiting for

the MRAM macros on the first cache line to reach a data out ready state. Clock cycle (cycle 6) is used to clock the first QW of the second cache line (QW4) to or from the data bus. The following clock cycle (cycle 7) is then used to clock the second QW of the second cache line (QW5) to or from the data bus.

[0043] An MRAM macro read access or write access is used to access the next two QWs (QW2 and QW3) of the first cache line. The MRAM macros on the first cache line reach a data out ready state in clock cycle 8. Clock cycles 8 and 9 are used to clock the third QW (QW2) of the first cache line and the fourth QW (QW3) of the first cache line to or from the data bus. The MRAM macros on the second cache line reach a data out ready state in clock cycle 10. Clock cycles 10 and 11 are used to clock the third QW (QW6) of the second cache line and the fourth QW (QW7) of the second cache line to or from the data bus.

[0044] FIGURE 10 is a process flow diagram illustrating a method of accessing a cache memory according to an aspect of the present disclosure. The method 1000 includes, storing a first portion of cached information in a static random access memory (SRAM) location of a cache line at block 1002, and storing a second portion of the cached information in a resistive random access memory location of the cache line at block 1004. The method also includes accessing the first portion of the information before accessing the second portion of the information during a cache accessing operation, at block 1006.

[0045] A hybrid SRAM-MRAM cache according to another aspect of the present disclosure includes means for storing a first portion of cached information in an SRAM location of a cache line and means for storing a second portion of the cached information in a resistive memory location of the cache line. The cache also has means for accessing the first portion of the information before accessing the second portion. The means storing the first portion of cached information may include the SRAM macros 606 as shown in FIGURE 6, for example. The means for storing the second portion of the cached information may include the MRAM macros 607 as shown in FIGURE 6, for example. The means for accessing may include the cache interface 604, the SRAM macros 606 and the MRAM macros 608 as shown in FIGURE 6, for example.

[0046] In another configuration, the aforementioned means may be any module or any apparatus configured to perform the functions recited by the aforementioned means. Although specific means have been set forth, it will be appreciated by those skilled in the art that not all of the disclosed means are required to practice the disclosed configurations. Moreover, certain well known means have not been described, to maintain focus on the disclosure.

[0047] FIGURE 11 is a block diagram showing an exemplary wireless communication system 1100 in which an aspect of the disclosure may be advantageously employed. For purposes of illustration, FIGURE 11 shows three remote units 1120, 1130, and 1150 and two base stations 1140. It will be recognized that wireless communication systems may have many more remote units and base stations. Remote units 1120, 1130, and 1150 include IC devices 1125A, 1125C and 1125B that include the disclosed hybrid cache apparatus. It will be recognized that other devices may also include the disclosed hybrid cache apparatus, such as the base stations, switching devices, and network equipment. FIGURE 11 shows forward link signals 1180 from the base station 1140 to the remote units 1120, 1130, and 1150 and reverse link signals 1190 from the remote units 1120, 1130, and 1150 to base stations 1140.

[0048] In FIGURE 11, remote unit 1120 is shown as a mobile telephone, remote unit 1130 is shown as a portable computer, and remote unit 1150 is shown as a fixed location remote unit in a wireless local loop system. For example, the remote units may be mobile phones, hand-held personal communication systems (PCS) units, portable data units such as personal data assistants, GPS enabled devices, navigation devices, set top boxes, music players, video players, entertainment units, fixed location data units such as meter reading equipment, or other devices that store or retrieve data or computer instructions, or combinations thereof. Although FIGURE 11 illustrates remote units according to the teachings of the disclosure, the disclosure is not limited to these exemplary illustrated units. Aspects of the disclosure may be suitably employed in many devices which include the disclosed hybrid cache apparatus.

[0049] FIGURE 12 is a block diagram illustrating a design workstation used for circuit, layout, and logic design of a semiconductor component, such as the hybrid cache apparatus disclosed above. A design workstation 1200 includes a hard disk 1201 containing operating system software, support files, and design software such as Cadence or OrCAD. The design workstation 1200 also includes a display 1202 to

facilitate design of a circuit design 1210 or a semiconductor component 1212 such as a hybrid cache apparatus. A storage medium 1204 is provided for tangibly storing the circuit design 1210 or the semiconductor component 1212. The circuit design 1210 or the semiconductor component 1212 may be stored on the storage medium 1204 in a file format such as GDSII or GERBER. The storage medium 1204 may be a CD-ROM, DVD, hard disk, flash memory, or other appropriate device. Furthermore, the design workstation 1200 includes a drive apparatus 1203 for accepting input from or writing output to the storage medium 1204.

[0050] Data recorded on the storage medium 1204 may specify logic circuit configurations, pattern data for photolithography masks, or mask pattern data for serial write tools such as electron beam lithography. The data may further include logic verification data such as timing diagrams or net circuits associated with logic simulations. Providing data on the storage medium 1204 facilitates the design of the circuit design 1210 or the semiconductor component 1212 by decreasing the number of processes for designing semiconductor wafers.

[0051] For a firmware and/or software implementation, the methodologies may be implemented with modules (e.g., procedures, functions, and so on) that perform the functions described herein. A machine-readable medium tangibly embodying instructions may be used in implementing the methodologies described herein. For example, software codes may be stored in a memory and executed by a processor unit. Memory may be implemented within the processor unit or external to the processor unit. As used herein the term "memory" refers to types of long term, short term, volatile, nonvolatile, or other memory and is not to be limited to a particular type of memory or number of memories, or type of media upon which memory is stored.

[0052] If implemented in firmware and/or software, the functions may be stored as one or more instructions or code on a computer-readable medium. Examples include computer-readable media encoded with a data structure and computer-readable media encoded with a computer program. Computer-readable media includes physical computer storage media. A storage medium may be an available medium that can be accessed by a computer. By way of example, and not limitation, such computer-readable media can include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or other medium that can be used to store desired program code in the form of instructions or data structures

and that can be accessed by a computer; disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk and blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above should also be included within the scope of computer-readable media.

[0053] In addition to storage on computer readable medium, instructions and/or data may be provided as signals on transmission media included in a communication apparatus. For example, a communication apparatus may include a transceiver having signals indicative of instructions and data. The instructions and data are configured to cause one or more processors to implement the functions outlined in the claims.

[0054] Although the present disclosure and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the technology of the disclosure as defined by the appended claims. For example, although SRAM and MRAM were described as types of memories, other memory types are also contemplated, such as DRAM, PCRAM, etc. Moreover, the scope of the present application is not intended to be limited to the particular configurations of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed that perform substantially the same function or achieve substantially the same result as the corresponding configurations described herein may be utilized according to the present disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

CLAIMS

What is claimed is:

1. A hybrid cache apparatus, comprising:

a first type of memory;

a second type of memory; and

a first cache line including a first memory location in the first type of memory and a second memory location in the second type of memory , the first cache line configured for accessing the first memory location before accessing the second memory location during a cache accessing operation.

2. The hybrid cache apparatus of claim 1, in which the first memory location comprises a first word location of the first cache line.

3. The hybrid cache apparatus of claim 1, configured for storing critical words of cached information in the first memory location.

4. The hybrid cache apparatus of claim 1, in which the second type of memory comprises a resistive memory.

5. The hybrid cache apparatus of claim 1, in which the first type of memory comprises a static random access memory (SRAM), and the second type of memory comprises a magnetic random access memory (MRAM).

6. The hybrid cache apparatus of claim 1, further comprising:

a first memory bank including the first type of memory and the second type of memory; and

a second memory bank including the first type of memory and the second type of memory.

7. The hybrid cache apparatus of claim 1, further comprising:

a second cache line including a third memory location in the first type of memory and a fourth memory location in the second type of memory, the second cache

line configured for accessing the third memory location before accessing the second memory location during the cache accessing operation.

8. The hybrid cache apparatus of claim 1, integrated in a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and/or a fixed location data unit.

9. A method for accessing a hybrid cache apparatus, comprising:

storing a first portion of cached information in a first type of memory of a first cache line;

storing a second portion of the cached information in a second type of memory of the first cache line; and

accessing the first portion of the cached information before accessing the second portion of the cached information during a cache accessing operation.

10. The method of claim 9, in which the second type of memory comprises a resistive memory.

11. The method of claim 9, in which the first type of memory comprises a static random access memory (SRAM), and the second type of memory comprises a magnetic random access memory (MRAM).

12. The method of claim 11, further comprising storing critical words of the cached information in the SRAM of the first cache line.

13. The method of claim 9, in which accessing the first portion occurs before the second type of memory reaches a ready state.

14. The method of claim 9, further comprising:

storing a third portion of cached information in the first type of memory of a second cache line;

storing a fourth portion of the cached information in the second type of memory of the second cache line; and

accessing the third portion of the cached information before accessing the second portion of the cached information during the cache accessing operation.

15. The method of claim 9, further comprising integrating the hybrid cache apparatus into a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and/or a fixed location data unit.

16. A hybrid cache apparatus, comprising:

means for storing a first portion of cached information in a static random access memory (SRAM) location of a first cache line;

means for storing a second portion of the cached information in a resistive random access memory portion of the first cache line; and

means for accessing the first portion of the cached information before accessing the second portion of the cached information during a cache accessing operation.

17. The hybrid cache apparatus of claim 16, further comprising:

means for storing critical words of the cached information in the SRAM location of the first cache line.

18. The hybrid cache apparatus of claim 16, further comprising:

a first memory bank including the means for storing the first portion and means for storing the second portion; and

a second memory bank including the means for storing the first portion and means for storing the second portion.

19. The hybrid cache apparatus of claim 16, further comprising:

means for storing a third portion of cached information in the static random access memory (SRAM) location of a second cache line;

means for storing a fourth portion of the cached information in a resistive random access memory portion of the second cache line; and

means for accessing the third portion of the cached information before accessing the second portion of the cached information during the cache accessing operation.

20. The hybrid cache apparatus of claim 16, integrated in a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and/or a fixed location data unit.

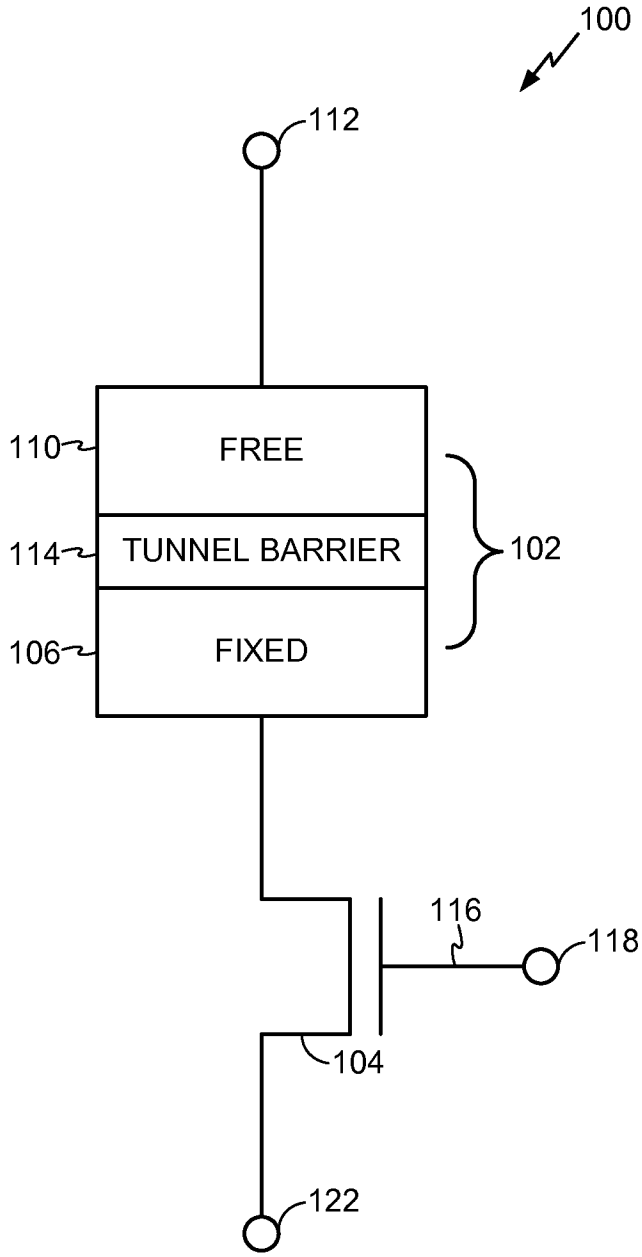


FIG. 1
PRIOR ART

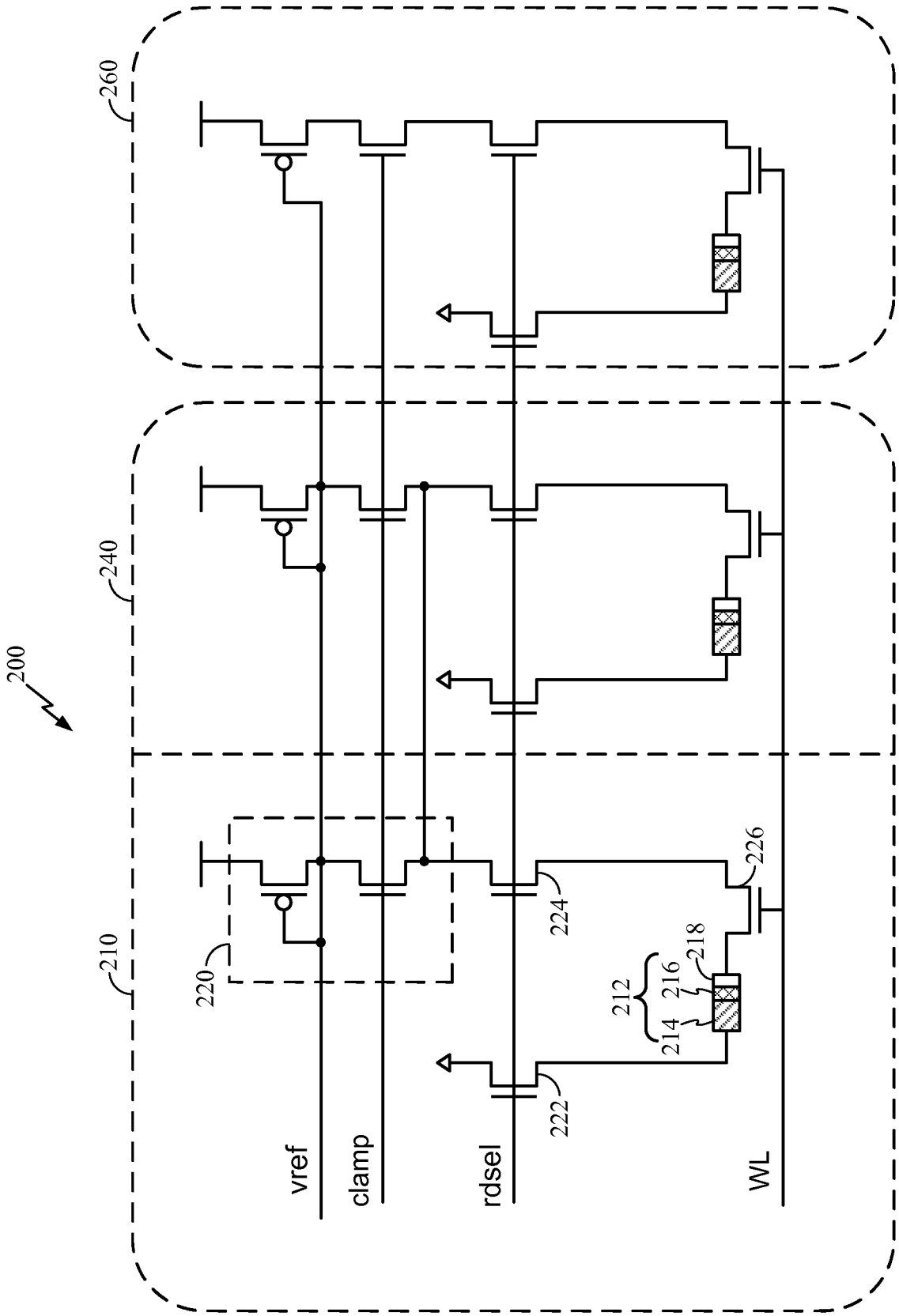

200
210
220
240
260
212
214
216
218
222
224
226
vref
clamp
rdsel
WL

FIG. 2

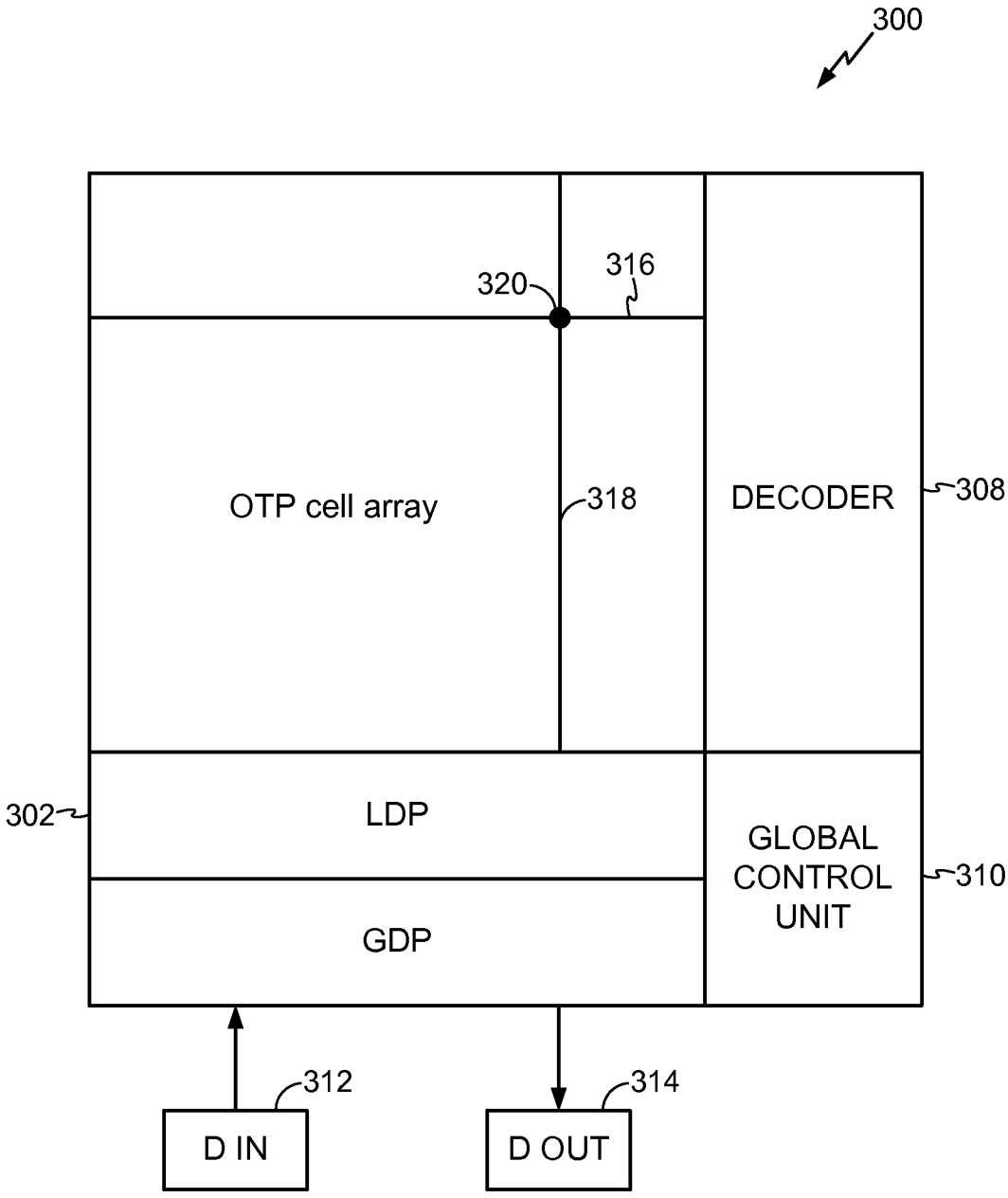
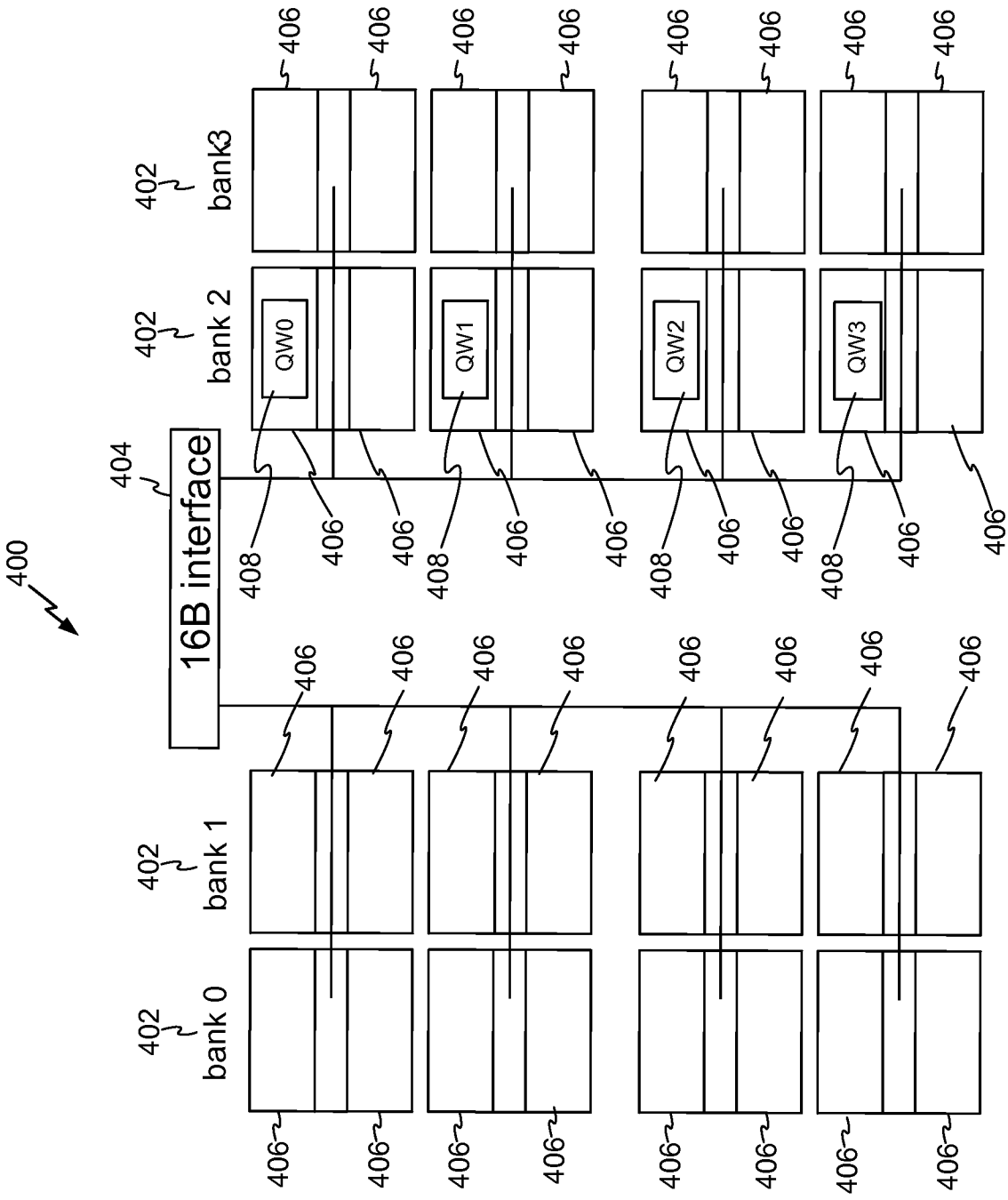


FIG. 3
PRIOR ART



PRIOR ART
FIG. 4

500

	Cycle 1	Cycle 2	Cycle 3	Cycle 4	Cycle 5	Cycle 6	Cycle 7	Cycle 8	Cycle 9
Block QW0	Enable	Array access	Array access	Data Out Ready					
Block QW1	Enable	Array access	Array access	Data Out Ready					
Block QW2	Enable	Array access	Array access	Data Out Ready					
Block QW3	Enable	Array access	Array access	Data Out Ready					
Bus	-	-	-	-	QW0	QW1	QW2	QW3	

FIG. 5A

550

	Cycle 1	Cycle 2	Cycle 3	Cycle 4	Cycle 5	Cycle 6	Cycle 7	Cycle 8	Cycle 9	Cycle 10
Block QW0	Enable	Array access	Array access	Array access	Array access	Data Out Ready				
Block QW1	Enable	Array access	Array access	Array access	Array access	Data Out Ready				
Block QW2	Enable	Array access	Array access	Array access	Array access	Data Out Ready				
Block QW3	Enable	Array access	Array access	Array access	Array access	Data Out Ready				
Bus	-	-	-	-			QW0	QW1	QW2	QW3

FIG. 5B

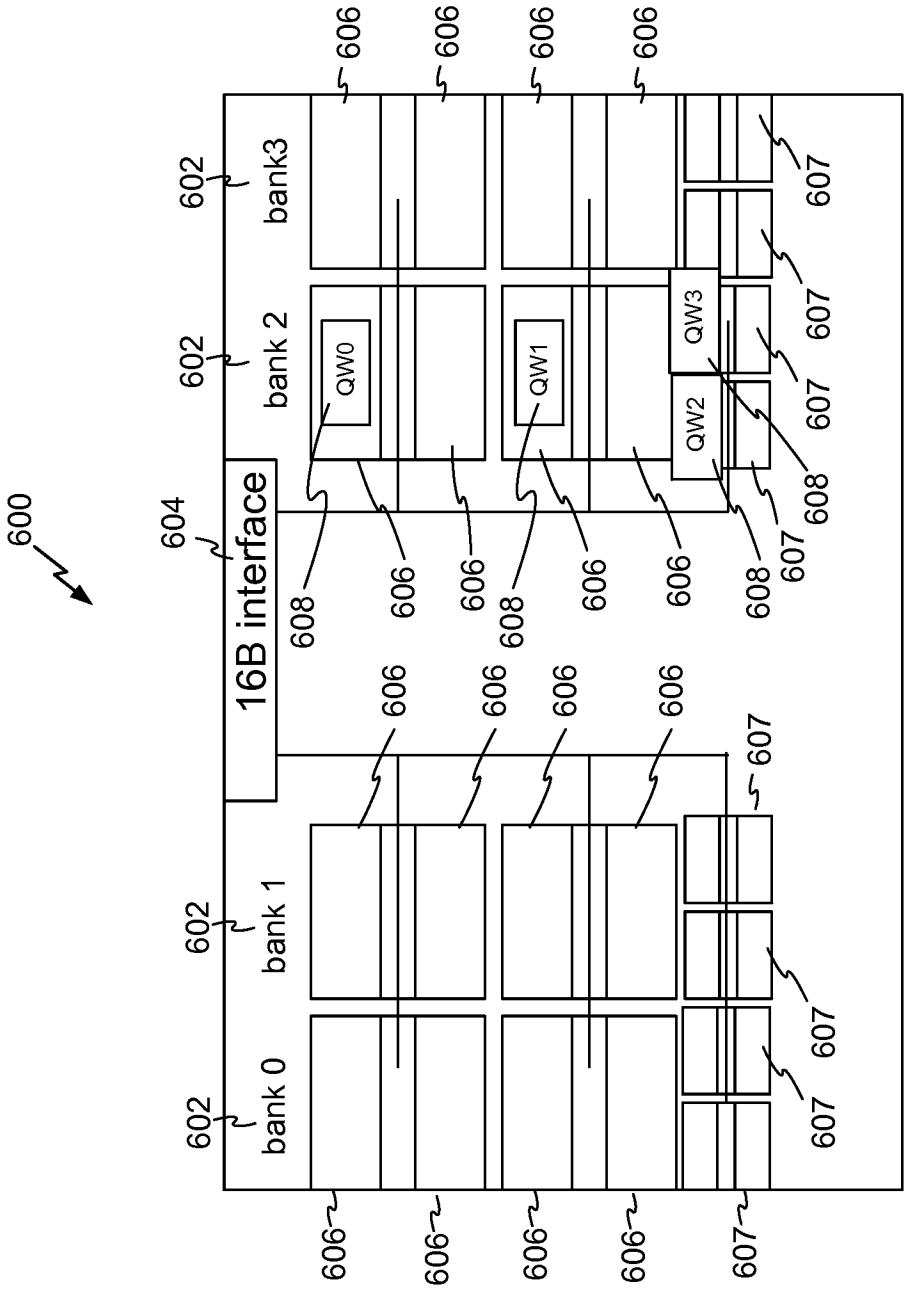

600
604
16B interface
602
bank3
bank 2
bank 1
bank 0
QW0
QW1
QW2
QW3
606
607
608

FIG. 6

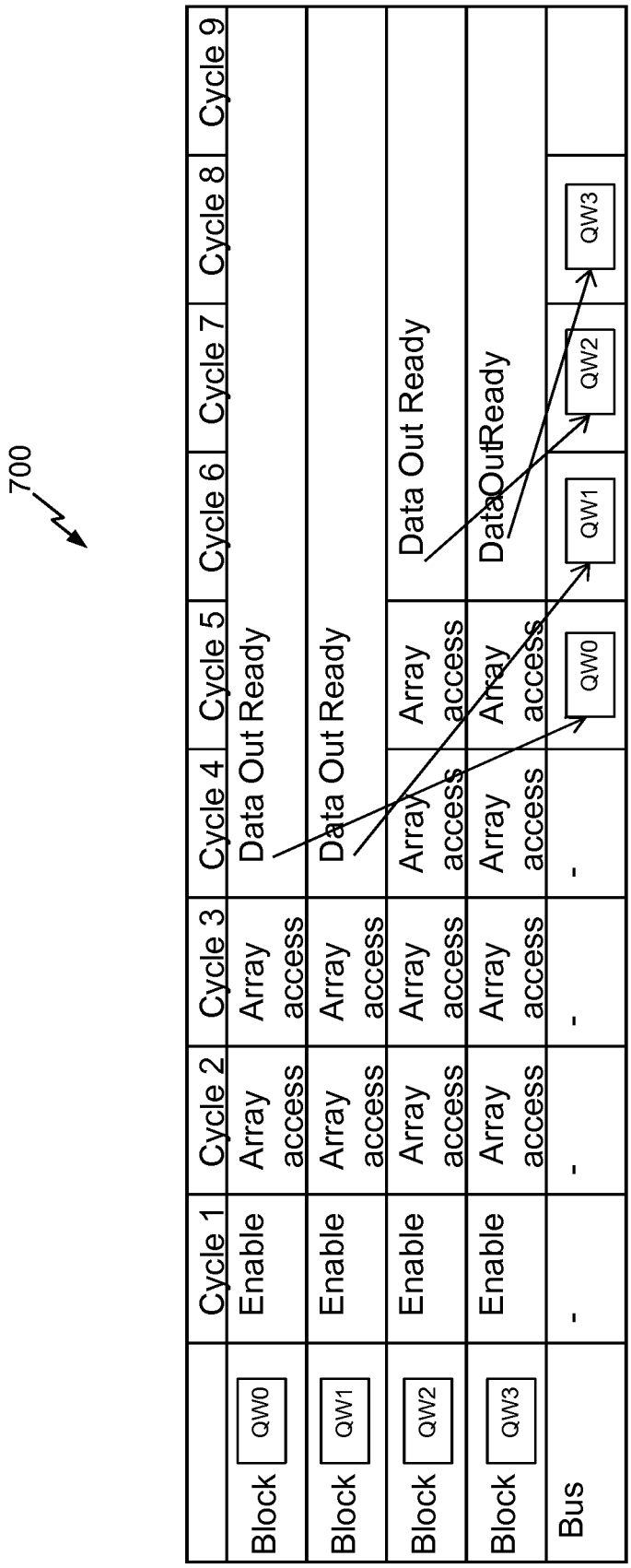

700
Cycle 1
Cycle 2
Cycle 3
Cycle 4
Cycle 5
Cycle 6
Cycle 7
Cycle 8
Cycle 9
Block QW0
Block QW1
Block QW2
Block QW3
Bus
Enable
Array access
Data Out Ready
QW0
QW1
QW2
QW3
-

FIG. 7

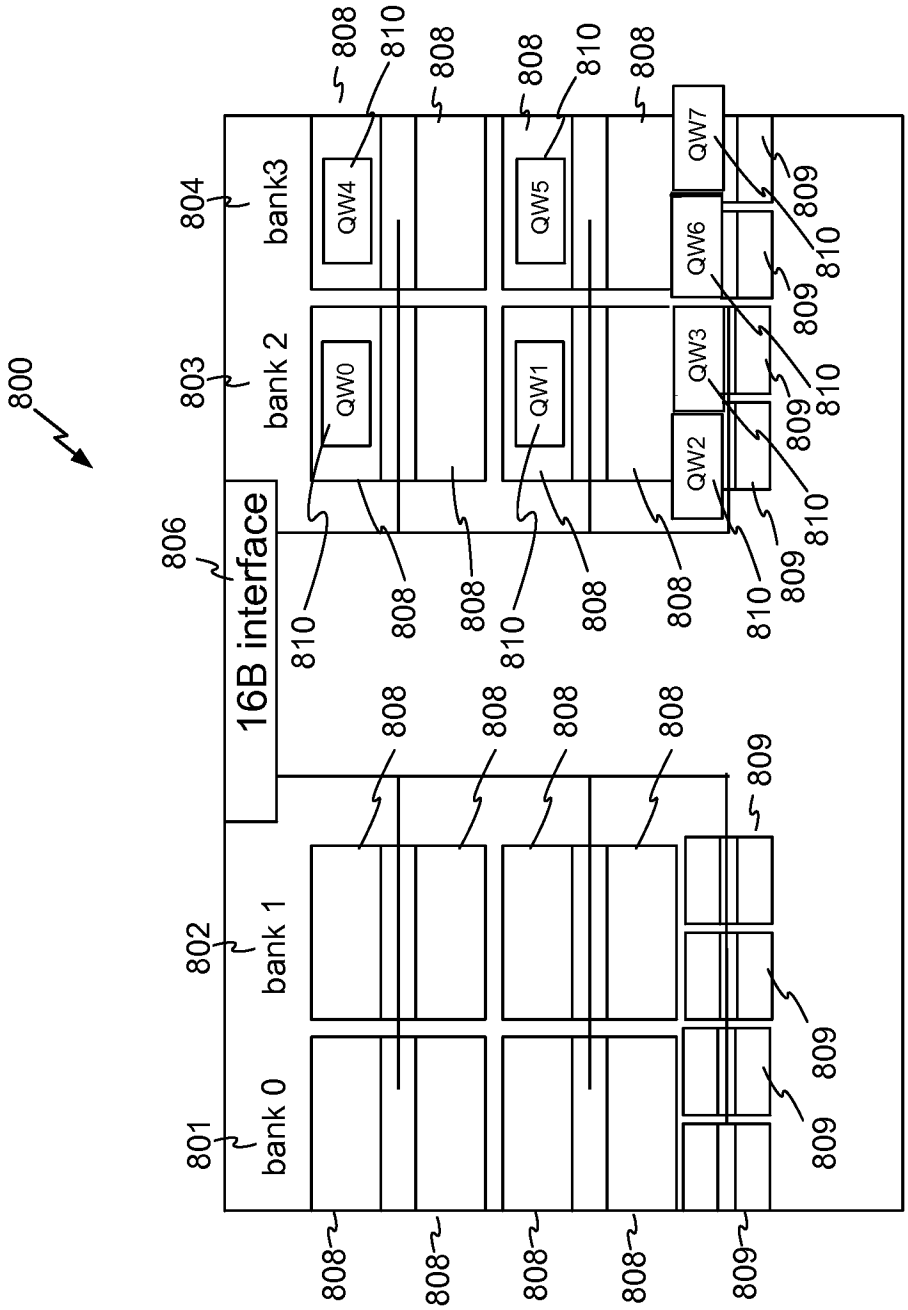

800
801
bank 0
802
bank 1
803
bank 2
804
bank3
806
16B interface
QW0
QW1
QW2
QW3
QW4
QW5
QW6
QW7
808
809
810

FIG. 8

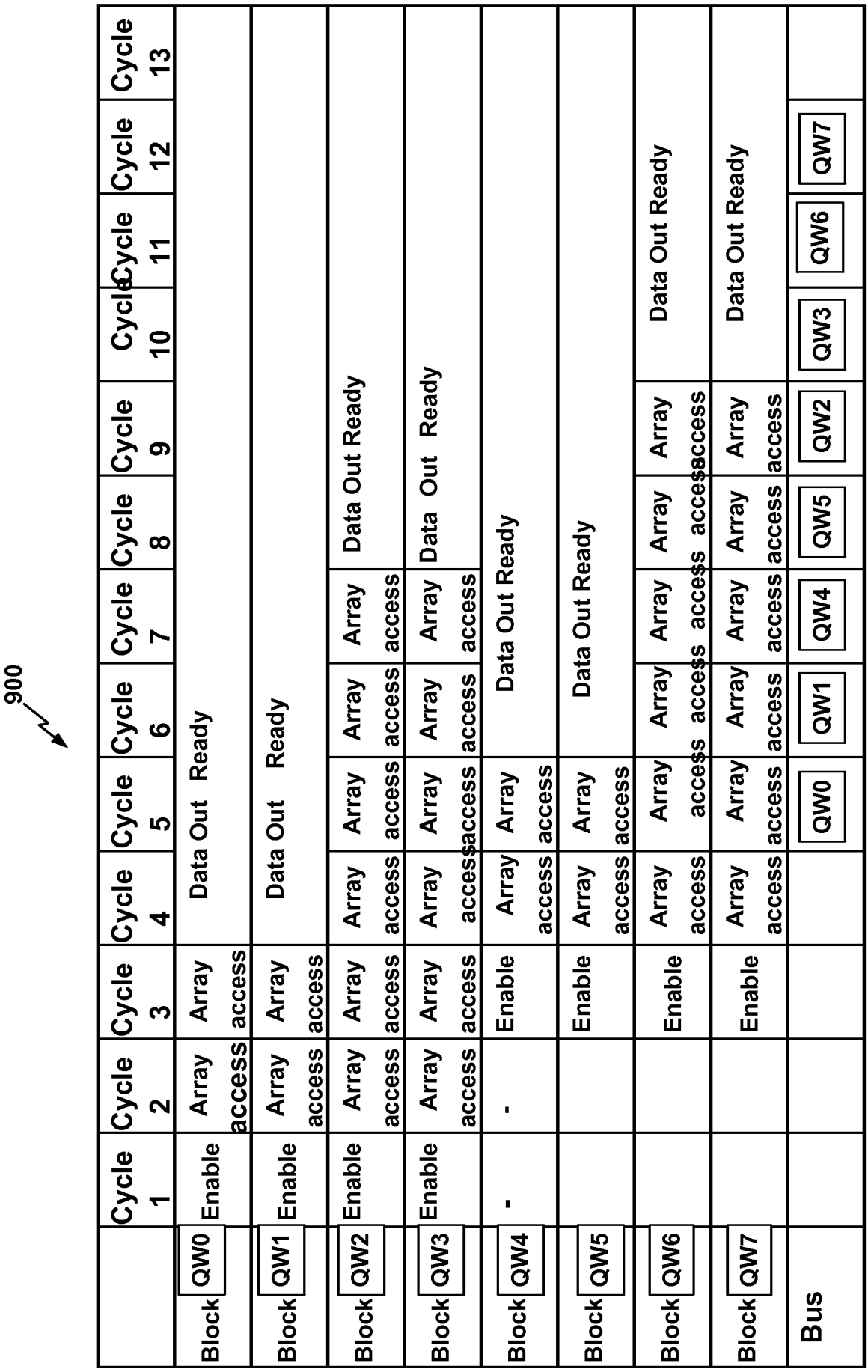

900
Cycle 1
Cycle 2
Cycle 3
Cycle 4
Cycle 5
Cycle 6
Cycle 7
Cycle 8
Cycle 9
Cycle 10
Cycle 11
Cycle 12
Cycle 13
Block QW0
Enable
Array access
Data Out Ready
Block QW1
Enable
Array access
Data Out Ready
Block QW2
Enable
Array access
Data Out Ready
Block QW3
Enable
Array access
Data Out Ready
Block QW4
-
Enable
Array access
Data Out Ready
Block QW5
Enable
Array access
Data Out Ready
Block QW6
Enable
Array access
Data Out Ready
Block QW7
Enable
Array access
Data Out Ready
Bus
QW0
QW1
QW4
QW5
QW2
QW3
QW6
QW7

FIG. 9

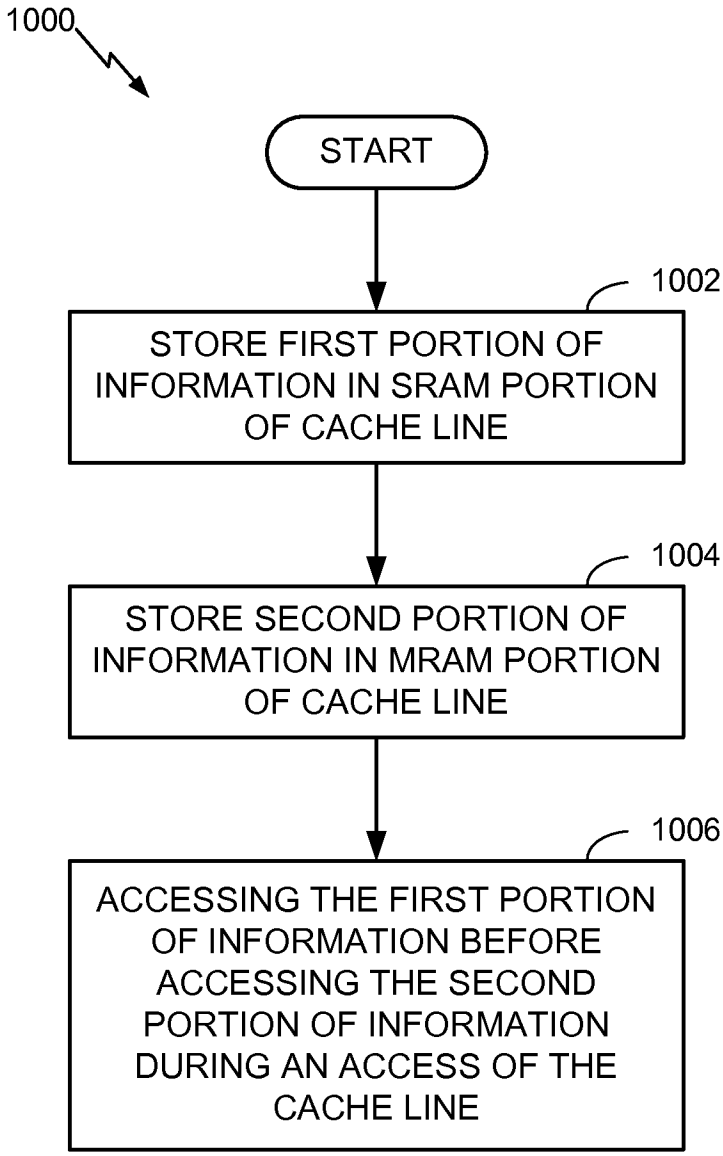

1000
START
1002
STORE FIRST PORTION OF INFORMATION IN SRAM PORTION OF CACHE LINE
1004
STORE SECOND PORTION OF INFORMATION IN MRAM PORTION OF CACHE LINE
1006
ACCESSING THE FIRST PORTION OF INFORMATION BEFORE ACCESSING THE SECOND PORTION OF INFORMATION DURING AN ACCESS OF THE CACHE LINE

FIG. 10

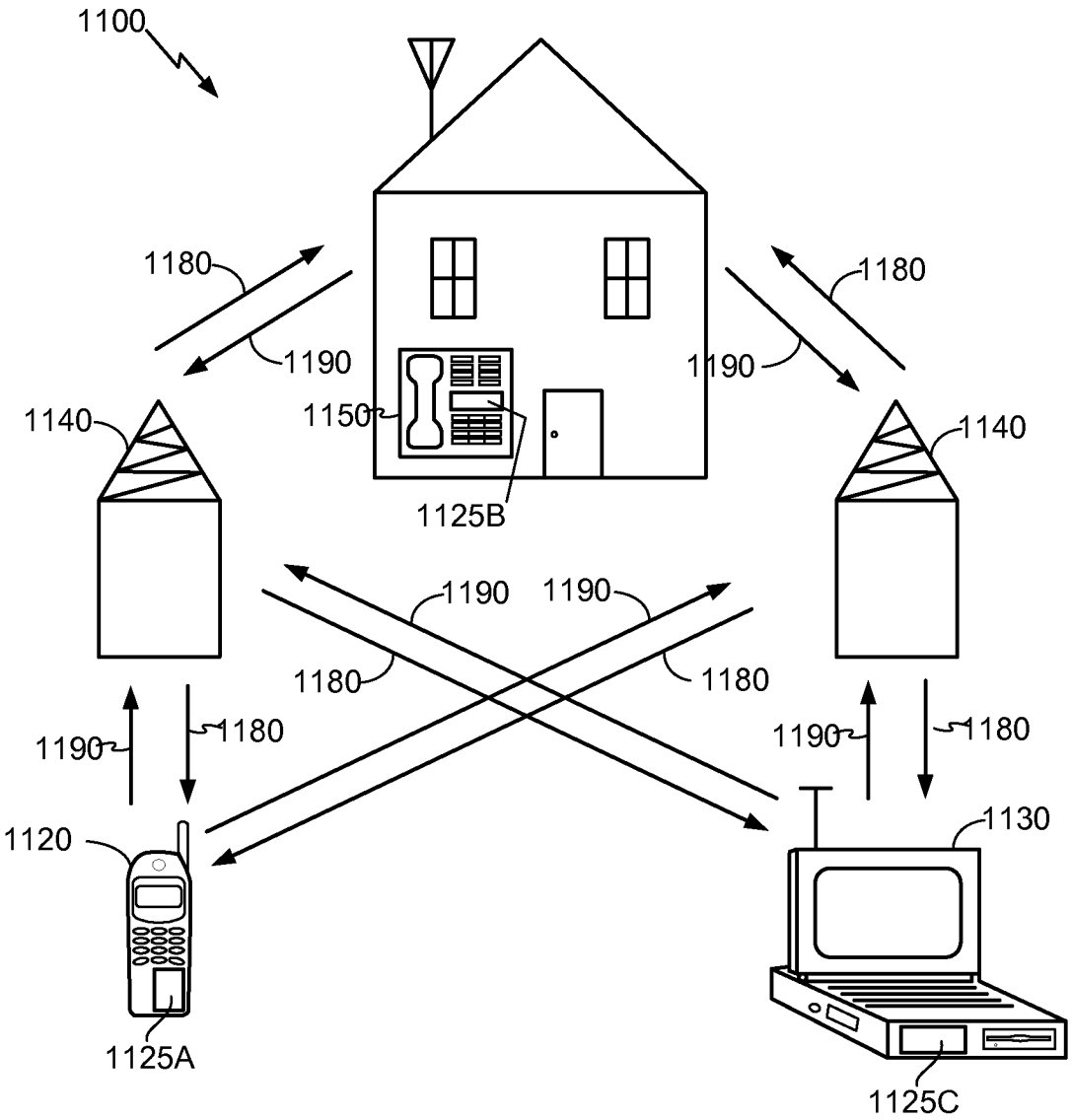

1100
1180
1190
1180
1190
1140
1150
1125B
1140
1190
1190
1180
1180
1190
1180
1190
1180
1120
1130
1125A
1125C

FIG. 11

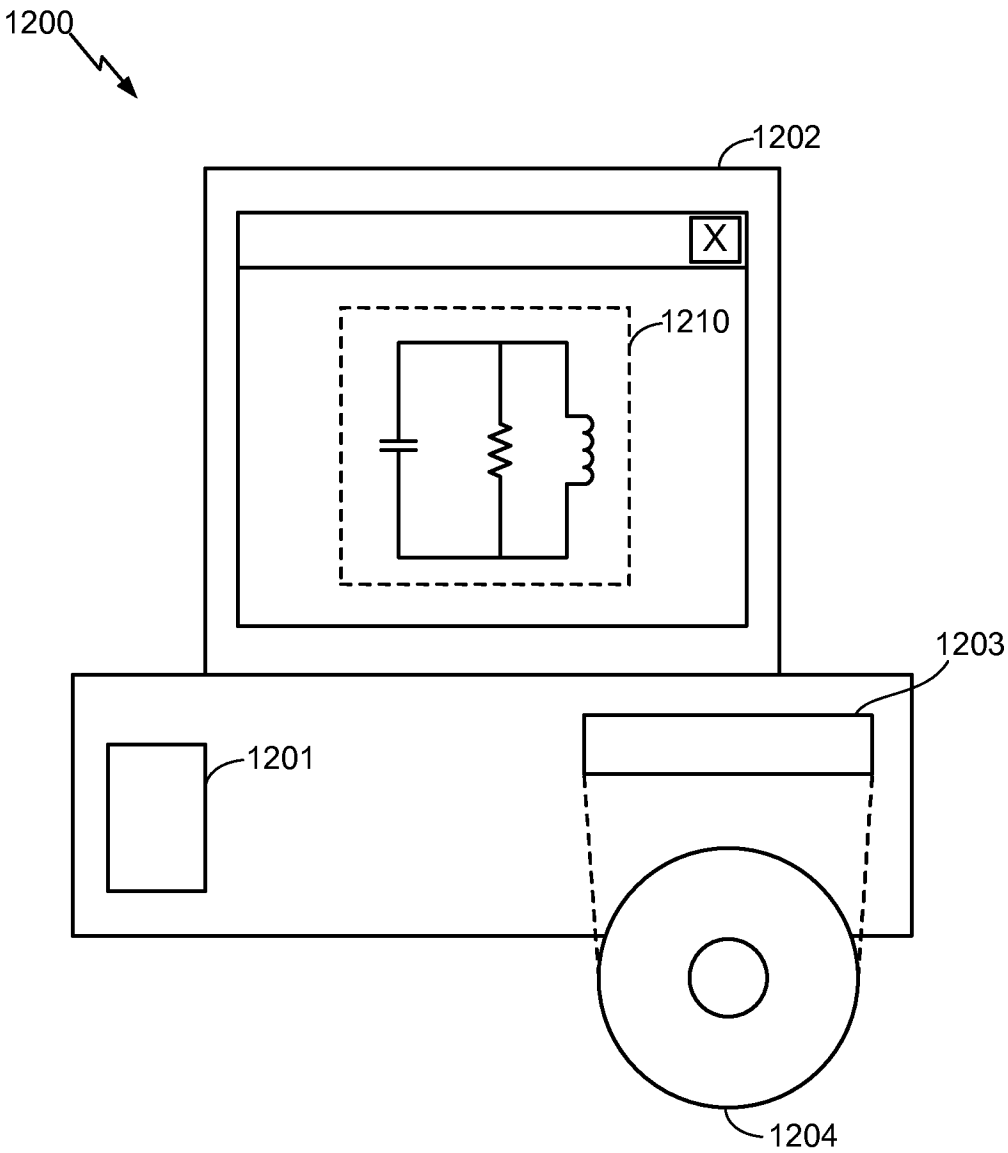


FIG. 12

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/025971

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F12/08
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2008/126716 A1 (DANIELS SCOTT L [US]) 29 May 2008 (2008-05-29) paragraph [0025] - paragraph [0038]; figures 1-5 paragraph [0042] - paragraph [0064] -----	1-3,6-9, 14,15 4,5, 10-13, 16-20
X	US 6 292 426 B1 (IKEDA HITOSHI [JP] ET AL) 18 September 2001 (2001-09-18) column 4, line 14 - column 7, line 31; figures 1-6 column 8, line 40 - column 10, line 61 ----- -/--	1,9,14, 15

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 July 2014	29/07/2014

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Toader, Elena Lidia

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/025971

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	VINAY SARIPALLI ET AL: "Exploiting Heterogeneity for Energy Efficiency in Chip Multiprocessors", IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS, IEEE, PISCATAWAY, NJ, USA, vol. 1, no. 2, 1 June 2011 (2011-06-01), pages 109-119, XP011381025, ISSN: 2156-3357, DOI: 10.1109/JETCAS.2011.2158343 Chapter B.Hybrid SRAM-MRAM Architecture; page 6 - page 8	4,5, 10-13, 16-20
A	HYUNJUN JANG ET AL: "A Hybrid Buffer Design with STT-MRAM for On-Chip Interconnects", 2012 IEEE/ACM SIXTH INTERNATIONAL SYMPOSIUM ON NETWORKS-ON-CHIP, 1 May 2012 (2012-05-01), pages 193-200, XP055129306, DOI: 10.1109/NOCS.2012.30 ISBN: 978-0-76-954677-3 Chapter B.An On-Chip Router Architecture with Hybrid Buffer Design; page 196 - page 197	4,5, 10-13, 16-20
A	GUANGYU SUN ET AL: "A novel architecture of the 3D stacked MRAM L2 cache for CMPs", HIGH PERFORMANCE COMPUTER ARCHITECTURE, 2009. HPCA 2009. IEEE 15TH INTERNATIONAL SYMPOSIUM ON, IEEE, PISCATAWAY, NJ, USA, 14 February 2009 (2009-02-14), pages 239-249, XP031435382, ISBN: 978-1-4244-2932-5 Chapter 5.2 SRAM-MRAM Hybrid L2 Cache; page 246 - page 247	4,5, 10-13, 16-20

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2014/025971

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