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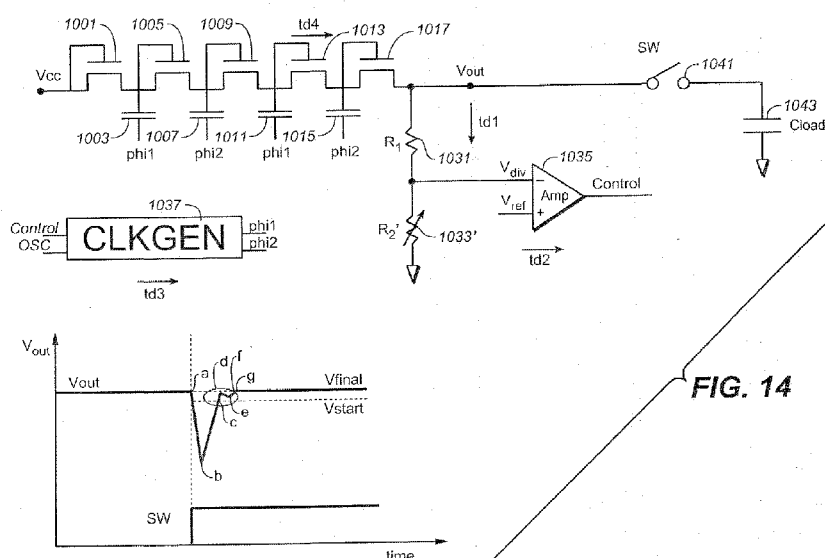


FIG. 14

(57) Abstract: A charge pump system for supplying an output voltage to a load is described. The charge pump system includes a charge pump connected to receive an input voltage generate from it the output voltage. The system also includes regulation circuitry connected to receive the output voltage and a reference voltage, where the regulation circuitry is connected to the charge pump to regulate the output voltage based upon the values of the reference voltage and the output voltage. During ramp up or a recovery operation the output voltage is initially regulated according to a first level and subsequently regulated to a second level higher than the first level, the second level corresponding to a desired regulated output voltage.

TECHNIQUES TO REDUCE CHARGE PUMP OVERSHOOT

FIELD OF THE INVENTION

[0001] This invention pertains generally to the field of charge pumps and more particularly to the reduction of overshoot during ramp-up or the recovery mode charge pumps.

BACKGROUND

[0002] Charge pumps use a switching process to provide a DC output voltage larger than its DC input voltage. In general, a charge pump will have a capacitor coupled to switches between an input and an output. During one clock half cycle, the charging half cycle, the capacitor couples in parallel to the input so as to charge up to the input voltage. During a second clock half cycle, the transfer half cycle, the charged capacitor couples in series with the input voltage so as to provide an output voltage twice the level of the input voltage. This process is illustrated in Figures 1a and 1b. In Figure 1a, the capacitor 5 is arranged in parallel with the input voltage V_{IN} to illustrate the charging half cycle. In Figure 1b, the charged capacitor 5 is arranged in series with the input voltage to illustrate the transfer half cycle. As seen in Figure 1b, the positive terminal of the charged capacitor 5 will thus be $2 * V_{IN}$ with respect to ground.

[0003] Charge pumps are used in many contexts. For example, they are used as peripheral circuits on EEPROM, flash EEPROM and other non-volatile memories to generate many of the needed operating voltages, such as programming or erase voltages, from a lower power supply voltage. A number of charge pump designs, such as conventional Dickson-type pumps, are known in the art. But given the common reliance upon charge pumps, there is an on going need for improvements in pump design, particularly with respect to trying to reduce the amount of layout area and the current consumption requirements of pumps.

[0004] Figure 2 is a top-level block diagram of a typical charge pump arrangement. The designs described here differ from the prior art in details of how the pump section 201. As shown in Figure 2, the pump 201 has as inputs a clock

signal and a voltage V_{reg} and provides an output V_{out} . The high (V_{dd}) and low (ground) connections are not explicitly shown. The voltage V_{reg} is provided by the regulator 203, which has as inputs a reference voltage V_{ref} from an external voltage source and the output voltage V_{out} . The regulator block 203 regulates the value of V_{reg} such that the desired value of V_{out} can be obtained. The pump section 201 will typically have cross-coupled elements, such as described below for the exemplary embodiments. (A charge pump is typically taken to refer to both the pump portion 201 and the regulator 203, when a regulator is included, although in some usages “charge pump” refers to just the pump section 201.)

[0005] Figure 3 illustrates schematically a charge pump typical of the prior art. The charge pump receives an input at a voltage V_{in} and provides an output at a higher voltage V_{out} by boosting the input voltage progressively in a series of voltage multiplier stages. The voltage output is supplied to a load, for example the word line of an EPROM memory circuit. Figure 3 also shows a feedback signal from the load to the charge pump, but without explicitly showing the regulator block. Most charge pump arrangements will typically have two such branches of one or more stage that alternately provide V_{out} as the clock signals alternate.

[0006] Figure 4 schematically illustrates a voltage multiplier stage as commonly implemented in the prior art. The stage pumps charge in response to a clock signal shown as “CLK.” When the clock signal is at a low portion of the clock cycle (e.g. 0V) the driver circuit output is LOW. This means that the lower terminal of capacitor C is at 0 volts. An input supplies a voltage V_{n-1} through the diode D (typically a diode connected transistor) and provides approximately V_{n-1} to the upper terminal of C (ignoring the voltage drop across the diode, D). This will deposit a charge Q on the capacitor, where $Q = CV_{n-1}$. When the clock signal transitions to a high state the output of the driver circuit is high, for example V_{CLK} and so the lower terminal of C is at V_{CLK} . This will force the upper terminal of C to be $(V_{n-1} + \Delta V_{CLK})$ since charge, Q, is conserved and C is constant. Thus the output voltage of the voltage multiplier stage is: $V_n = V_{n-1} + \Delta V_{CLK}$. The driver will drive one side of the capacitor to V_{clk} , however because of parasitic capacitance the other side will be increased by ΔV_{CLK} , a voltage less than V_{CLK} .

[0007] Figure 5 illustrates the regulated output voltage of a typical charge pump of the prior art while maintaining a voltage, for example the programming voltage of a flash memory V_{pp} . When the output voltage falls below a margin of V_{pp} , the pump is turned on by the regulator. The pump delivers a high current to the load and drives the voltage higher than V_{pp} . The pump then switches off in response to a feedback signal from the load. The voltage on the load then drops due to leakage current until it reaches a predetermined voltage, lower than V_{pp} by a fixed amount. Then the charge pump switches on again. This cycle produces the ripples in voltage shown. If these ripples (shown by ΔV) are large they may cause problems; for the V_{pp} example, this can be manifested by problems such as by programming a floating gate to the wrong voltage level, or by causing a greater variation in program levels.

[0008] The recovery mode of a charge pump is when, after the application of a load, the output of the pump is ramped-up to the voltage level at which the output is to be regulated. This requires a large current to charge the load to the required voltage as rapidly as possible. After the output voltage ramps up to the regulation level, the output will typically overshoot the desired regulation level, placing stress on the circuit elements.

SUMMARY OF THE INVENTION

[0009] According to a first set of aspects, a charge pump system for supplying an output voltage to a load is presented. The system includes a charge pump connected to receive an input voltage generate from it the output voltage. The system also includes regulation circuitry connected to receive the output voltage and a reference voltage, where the regulation circuitry is connected to the charge pump to regulate the output voltage based upon the values of the reference voltage and the output voltage. During ramp up or a recovery operation the output voltage is initially regulated according to a first level and subsequently regulated to a second level, where the second level is higher (or of greater amplitude) than the first level and corresponds to a desired regulated output voltage.

[0010] Other aspects present a method of operating a charge pump system to provide an output voltage at an output. A load is applied the output and, in response, the

charge pump is operated during ramp up or in a recovery phase, that includes regulating the output voltage according to a first level and subsequently regulating the output voltage according to a second level of greater amplitude than the first level. The output regulated according to the second level is then subsequently supplied to the load.

[0011] Various aspects, advantages, features and embodiments of the present invention are included in the following description of exemplary examples thereof, which description should be taken in conjunction with the accompanying drawings. All patents, patent applications, articles, other publications, documents and things referenced herein are hereby incorporated herein by this reference in their entirety for all purposes. To the extent of any inconsistency or conflict in the definition or use of terms between any of the incorporated publications, documents or things and the present application, those of the present application shall prevail.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The various aspects and features of the present invention may be better understood by examining the following figures, in which:

Figure 1a is a simplified circuit diagram of the charging half cycle in a generic charge pump.

Figure 1b is a simplified circuit diagram of the transfer half cycle in a generic charge pump.

Figure 2 is a top-level block diagram for a regulated charge pump.

Figure 3 illustrates a charge pump of the prior art.

Figure 4 illustrates a voltage multiplier stage of the prior art.

Figure 5 illustrates the voltage output of a typical charge pump of the prior art.

Figure 6 illustrates the voltage output of a pump in the recovery and regulation modes.

Figure 7 is a box diagram of a charge pump system having three pumps.

Figure 8 shows the cumulative charge pumped by the arrangement of Figure 7 when enabled.

Figure 9 illustrates some of the various signals involved when the pump system of Figure 7 is in regulation.

Figure 10 is a box diagram for an exemplary embodiment of a multiple charge pump system with delay enable.

Figure 11 shows the cumulative charge pumped by the arrangement of Figure 10 when enabled.

Figure 12 illustrates some of the various signals involved when the pump system of Figure 10 is in regulation.

Figure 13 is a schematic illustration of a typical charge pump system and the phenomenon of overshoot during recovery.

Figure 14 is a schematic illustration of an exemplary embodiment and its behavior during a 2-phase recovery process.

Figure 15 shows the overshoot behavior during recovery in an actual charge pump system.

Figures 16 and 17 show two examples of a two phase recovery.

DETAILED DESCRIPTION

[0013] To be adaptable to multiple purposes (loads and voltages), one relatively large charge pump is divided up into several smaller charge pumps connected in parallel to provide their individual outputs together as a combined output. To reduce the amount of ripple at the output during regulation, the multiple pumps are not all immediately enabled, but some are delayed and only enabled if the initial output is insufficient to drive the load at the regulation level.

[0014] More information on prior art charge pumps, such as Dickson type pumps, and charge pumps generally, can be found, for example, in “Charge Pump Circuit Design” by Pan and Samaddar, McGraw-Hill, 2006, or “Charge Pumps: An Overview”, Pylarinos and Rogers, Department of Electrical and Computer Engineering University of Toronto, available on the webpage “www.eecg.toronto.edu/~kphang/ece1371/chargepumps.pdf”. Further information on various other charge pump aspects and designs can be found in US Pat. Nos. 5,436,587; 6,370,075; 6,556,465; 6,760,262; 6,922,096; 7,030,683; 7,554,311; 7,368,979; and 7,135,910; US Patent Publication numbers 2009-0153230-A1; 2009-0153232-A1; and 2009-0058506-A1; and applications Nos. 11/295,906 filed on December 6, 2005; 11/303,387 filed on December 16, 2005; 11/845,939, filed

August 28, 2007; 12/144,808 filed on June 24, 2008; 12/135,948 filed June 9, 2008; 12/146,243 filed June 25, 2008; 12/337,050 filed December 17, 2008; 12/506,998 filed on July 21, 2009; and 12/570,646 filed on September 30, 2009. In particular, US patent number 6,734,718 presents complementary ripple reduction techniques.

[0015] Charge pumps often operate in two modes, ramp-up or recovery mode and regulation mode. Figure 6 illustrates the voltage on the load in these two modes of operation. Mode 1 is the ramp-up or recovery mode during which the load is brought to a predetermined voltage. (The Mode 2 region is similar to Figure 5.) This requires a large current to charge the load to the required voltage as rapidly as possible. The figure shows an example of charging up a load (e.g. a wordline) from V_{cc} to V_{pp} in a time t_0 . Mode 2 is the regulation mode during which the voltage is held as closely as possible to the required voltage, V_{pp} . That is, ΔV in Figure 6 is made as small as possible. (This requires a smaller current because a large current deposits a large quantum of charge each time the pump is turned on.

[0016] Figure 7 is a box diagram of a charge pump system having three pumps, Pump A 601, Pump B 603, and Pump C 605 each receiving the clock signal PMPCLK and that are connected in parallel to drive the, in this example, capacitive load Cload 611. The output level is also fed back to the regulation element 621, which generates a flag telling the pump control circuit 623 to provide the clock enable signal CLKEN to the pumps when these are to be turned on. The use of three pumps allows the output to be adapted to the load.

[0017] In this example, the three pumps are connected in parallel and enabled by the same CLKEN signal to deliver charge to the output. Since they are controlled simultaneously by the signal CLKEN, when this signal is asserted all three will drive the load, which can lead to a potential overshoot and resultant high ripple level. The resultant waveform in such open regulation is shown in Figure 8, which shows the cumulative charge sent to the node marked Vout on Figure 7. In regulation mode starting when the pumps are enabled (CLKEN asserted), in each cycle (indicated by the vertical dotted line) the amount of charge bracketed at right is supplied to the output node. The horizontal dotted line show the amount each pump contributes in the first cycle, which in this example are taken to be equal.

[0018] Figure 9 illustrates an example of some of the various signals involved in regulation and corresponding Vout value. The specific waveforms shown are Vout 811, PMPCLK 813, FLAG 815, and CLKEN 817. For the Vout waveform 811, the lower line shows the voltage which will trigger the pumps coming back on and the upper line is where the pump will be disabled, as the voltage has passed the desired level. The waveforms begin with the Vout voltage on the load decreasing as shown in 801, decreasing until it reaches the lower level. This will cause the regulation element 621 to assert FLAG 815, with the pump control 623 in turn asserting CLKEN 814. Here, these are all shown to coincide with a rising edge of the PMPCLK single 813. Once the pumps are enabled, the supply charge to the output node. As shown in Figure 8 at 803, during regulation, within one clock edge, they may be capable of delivering more than required charge to keep in regulation. As the single cycle causes the upper Vreg value to be exceeded, the pump is disabled, the level are Vout drops off and the process is repeated. Consequently, a high degree of ripple can result.

[0019] Figure 10 presents an exemplary embodiment to illustrate some of the aspects presented here. As shown there, with the exception of elements 633 and 635, equivalents elements are arranged in the same way. The exemplary embodiment again shows three charge pumps (#A 601, #B 603, #C 605), but more generally the concept can be applied to any multiple number of pumps, whether 2, 3, or more. The charge pumps themselves can be of any of the various designs, such as those presented in the various references noted above, and not all of the pumps in the system need be of the same design. Here they are taken to of the same type, to have the same output, and to have same PMPCLK signal received in phase, but more generally any of these could be different.

[0020] To reduce the amount of ripple with respect to Figure 7, a delay logic is enabled during regulation. This is implemented by the delay elements 633 and 635. As shown in Figure 10, Pump #A 601 is controlled by the original CLKEN signal; Pump #B 603 is controlled by some delay time from CLKEN signal due to delay element 633; and Pump #C 605 is controlled through 635 by some longer delay time than B (illustrated schematically by the larger size of 635) from CLKEN signal. Depending on the embodiment and configuration, the amount of relative delay between the various delayed stages (here two, #B and #C) can be taken the same or

different and can be preset, user configurable, or even dynamically adaptable. For the example here, 633 will have a delay of two cycles and 635 will have a delay of two cycles.

[0021] The idea is that in order to raise the output voltage from the level which will trip the regulation into enabling the charge up to the desired regulated voltage, the use of all three pumps may be too much, as has been described with respect to Figures 7-9. Instead, the embodiment of Figure 10 initially only invokes one of the pumps, reducing the potential for overshoot; should this not be enough, a second pump will start, followed, if needed, by the third. This provides a more incremental approach to the desired level during the regulation mode.

[0022] Figure 11 shows an example of the cumulative charge pumped to the output node under this arrangement during open regulation at 901. The waveform from Figure 8 is also superimposed at 903 for comparison. In the first two clock pulses (separated by the vertical lines) after the pump the enable signal is asserted, only pump #A 601 is enable, supplying the quantity of charge indicated by the horizontal lines. If this is not sufficient to bring the output up to the regulation level, pump #B 603 is enabled, with pump #C605 following in the next cycle. Thus, if needed, all three pumps will eventually be enabled to drive the load.

[0023] In term of regulation, this is as shown in Figure 12. The waveforms 913, 915, and 917 are much the same as their counterparts in Figure 9; however, the CLKEN is now only supplied to Pump #A 601. During the first two clock pulse, only the one pump is enabled and the other two are off the exemplary embodiment. Consequently, the CLKEN2 919 and CLKEN 3 921 are not asserted. As shown at top in 911, since these two cycles are enough to bring the output voltage 923 up to the regulation value in the example, the other pair of pumps will not be needed for the load being driven. This example shows that something like a third of the original ripple (superimposed at 803) is reduced.

Reduction of Overshoot During Recovery and Ramp-Up

[0024] As discussed above, during the ramp-up or recovery phase the output of the charge pump typically overshoots the desired level of regulation for the output voltage. After a large capacitive load is connected to the output, the voltage level at

the pump's output drops and recovery begins, with the output ramping up until the desired regulation level is reached, as shown above with respect to Figure 6. Due to the finite delay in the feedback path, by the time the regulation circuitry registers that the desired regulation level has been reached, the current output level will have been over corrected. For the elements being supplied by the charge pump, this can result in reliability concerns and breakdown in components as they are overstressed. There are various techniques to deal with such overshoot (speeding up the feedback path, controlling clock frequency, power input, etc.), these techniques are typically at odds with other design constraints.

[0025] It should be noted that whereas the previous section was concerned with ripple during regulation, this section is concerned with the sort of overshoot that can occur during ramp-up or the recover mode. When the circuit is in the regulation phase, there will some (typically fairly small) swing in the output level. Due to the finite delay in the feedback path, there is a lag in detection of the output level and a resultant over-correction. This leads to the sort of ripple or regulation noise discussed above, but the amount of over-correct is typically not significant in a well regulated system. However, where the output voltage differs significantly from the desired target level, such as occurs when the pump is initially connected to drive a load, the op-amp or comparator of the regulation circuitry is tempted to over-correct the error of the output voltage and dump excess power into the system. Again due to the finite delay in the system's feedback, this leads to overshoot in the regulation process, an overshoot that is generally larger than that found in the ripple or regulation noise when the pump is in the regulation phase.

[0026] Overshoot phenomena can be illustrated further with respect to Figure 13, the top part of which shows a schematic illustration of a charge pump system and the bottom part of which shows the response when a load is applied. The upper left portion of Figure 13 shows a charge pump, here a 4-stage Dickson-type pump receiving an input voltage V_{cc} and generating from it the output voltage V_{out} . The diode connected transistors 1001, 1005, 1009, 1013, 1017 are arranged in series with one of the capacitors 1003, 1007, 1011, 1015 having its top plate connected between a corresponding pair of the diodes and the bottom plates of the capacitors alternately receiving one of a pair of clock signals $\phi 1$ and $\phi 2$. The output of the pump can

then be connected by the switch SW 1041 to drive a load, here represented by the load capacitor Cload 1043. Vout is also supplied to the regulation circuitry.

[0027] The regulation circuitry is here represented by Amp 1035, where a first input is fed a reference voltage value Vref (from a bandgap circuit, for example) and a second input is fed with a value derived from Vout. Here the second input is taken from a node between the resistive elements R_1 1031 and R_2 1033 connected in series between Vout and ground. (More generally, the voltage divider for this feedback path can also be capacitive or other combinations of elements.) Based on the value at this node relative to Vref, the circuitry generates a control signal Control, which is then used to regulate the output. In this example, this is done by supplying Control to the clock generating circuit CLKGEN 1037. CLKGEN 1037 also receives as an input an oscillator or clock signal OSC and, based on these inputs, generates the clock signals phi1 and phi2 used to drive the charge pump. Based on Control, CLKGEN 1037 could, for example, vary the amplitude or frequency of phi1 and phi2.

[0028] The regulation is based the current level of Vout, but when the level of Vout changes the result of the regulation will lag due to the finite delays through regulation path, clock generation, supply voltage regulation, and so on. For example, as shown in Figure 13 when Vout changes there will be a delay td1 from the output node to the input of Amp 1035, a delay td2 as Control is generated and propagated to the clock generation circuit, a delay td3 through CLKGEN 1037, and then a delay of td4 as the newly regulated clock signal propagate the output through the pump itself to the output node. This can lead to an overcorrection of the regulation and significant deviation from desired regulated voltage level, as illustrated in the plot of Vout versus time.

[0029] Prior to driving the load, the switch SW 1041 is open (the corresponding control signal SW is low) and Vout is initially being held at the regulation level. At a time t_a , the control signal SW is asserted, the corresponding switch SW 1041 closed, and the output of the pump applied to the load. Correspondingly, Vout drops as the load is driven and there will also be a delay as this drop propagates through the delays td1, td2, td3, and td4 until Vout begins to ramp up at t_b . The recovery phase continues until, at t_c , Vout obtains the desired regulation level of Vfinal. However, by the time Vfinal is reached and this information and the corresponding recovery to

regulation change is propagated through the system, V_{out} has continued ramping up until t_d , overshooting V_{final} . At this point, V_{out} then drops back down until the system goes into regulation mode at t_e . (Once in regulation there will also be ripple as discussed above and developed further in US patent application number 12/146,243 filed June 25, 2008, but this will be overlooked for the purposes of this section.) This voltage overshoot can lead to damage in circuit elements being supplied by the pump as the Electrical Design Rule (EDR) is violated, stressing the load and possibly causing gate/junction breakdown.

[0030] The techniques presented here treat this overshoot problem through use of a two-stage recovery process. If, when the load is connected, the voltage drops to a level significantly lower than the desired target level (V_{final}), the pump is regulated based on an initial, lower target regulation level V_{start} , $V_{start} = V_{final} - \Delta V$. (For example, if V_{final} is 4V, ΔV could be 200mV---the value of ΔV is usually based on the specific circuit design, the amount of overshoot will vary from design to design.) Once the output voltage hits V_{start} , the system changes the target regulation to V_{final} . In the initial part of the recovery phase based on the V_{start} , as any overshoot is relative to this lower level, it will be lower; and as the difference between V_{start} and V_{final} is relatively small, the overshoot during the incremental additional ramp-up after raising the regulation level to V_{final} will produce a smaller deviation in the second recovery phase as well. Consequently, the over-correction due to the voltage difference from final target level during recovery is minimized. If, on the other hand, the drop in V_{out} is relatively small, this will typically not lead to significant overshoot and the initial phase need not be invoked.

[0031] Relative to other approaches, this two-stage ramp-up or recovery can also lead to a reduction of the delay through the regulation path. When regulating a voltage supply, the specification typically specifies that the output level can vary by a certain amount, say $\pm 10\%$. One way for dealing with such overshoot is to detect how close the voltage is to the final regulation level and then slow down the pump clock to reduce the output power of charge pump. Doing so causes an extra delay. Under the two-phase arrangement given here, the output is given a margin to allow overshoot in the first phase, so that there is no need to slow the system down while still allowing it to fall into the desired range (i.e., $\pm 10\%$). Subsequently, the regulation level is

changed to the second regulation level, and all known techniques to reduce output noise can then be applied. In this way, during the first phase the system can operate at full speed and still end up in the desired range while still avoiding the design rule (EDR) concerns.

[0032] Figure 14 illustrates an exemplary embodiment for implementing such a 2-stage recovery process. The upper part of Figure 14 again shows a charge pump as in Figure 13 with the corresponding elements similarly numbered and the lower part shows behavior at the output as a function of time. Relative to Figure 13, R'_2 1033' is now a variable resistance that, in this example, has 2 discrete values, allowing the input of the amp (or, more generally, comparator) 1035 connected to the node above R'_2 1033' to be set at two different values relative to the level on V_{out} . The higher value of R'_2 1033' corresponds to V_{final} of the desired, final regulation level used in the second phase of recovery and would have the same value as for R_2 1033 in Figure 13. The lower value of R'_2 1033' corresponds to the initial phase of recovery based on V_{start} . When the pumps system goes into recovery mode, the regulation circuitry starts with R'_2 1033' at the lower value corresponding to the V_{start} and, aside from the lower target value for V_{out} , the recovery process larger proceeds in the usual way. Once the output has recovered to the initial V_{start} level, the R'_2 1033' switches to the higher value corresponding to actual desired target level of V_{final} for the second recovery phase. As before, in other embodiments the resistances R_a and R'_2 can be replaced or used in conjunction with capacitive or other elements.

[0033] The level of V_{out} versus time for this two stage recovery is shown at bottom left in Figure 14. As in the corresponding part of Figure 13, prior to driving the load, the switch SW 1041 is open (the corresponding control signal SW is low) and V_{out} is initially at the (final) regulation level corresponding to V_{final} . At a time $t'a$, the control signal SW is asserted, the corresponding switch SW 1041 closed, and the output of the pump applied to the load. Correspondingly, V_{out} drops as the load is driven and there will also be a delay as this drop propagates through the delays $td1$, $td2$, $td3$, and $td4$ until V_{out} begins to ramp up at $t'b$. The first phase of the recovery is based on V_{start} using the lower value of R'_2 . The first recovery phase continues until, at $t'c$, V_{out} reaches V_{start} . As before, by the time V_{start} is reached and this information and the corresponding regulation change is propagated through the

system, V_{out} has continued ramping up until $t'd$, overshooting V_{start} . At this point, V_{out} then drops back down until $t'e$. Although there is again overshoot, the overshoot at $t'd$ is relative to V_{start} , rather than an overshoot relative to V_{final} , so that peak level at V_{out} is lowered.

[0034] Once the information that V_{out} has reached V_{start} at $t'c$, the regulation level switches to V_{final} for the second phase of recovery. There can be a finite delay between switching from the first regulation level to the second regulation level, with (in the embodiment of Figure 14) the value of R'_2 1033' being changed to correspond to V_{final} . (As the overshoot is a characteristic of the finite delay in the feedback path, and the over-correction is due to large output deviation from target value, the system may also switch right after hitting V_{start} , since between V_{start} and V_{final} , the voltage difference is smaller compared with initial voltage difference. If the design is done properly, the output should not be over-corrected, and should have much less noise.) Within this period, V_{out} drops back down from the first phase's overshoot before it begins to ramp back up in the second recovery phase at $t'e$. The system then recovers to V_{final} . There may again be some overshoot in this second phase, but this is relatively small since no significant over-correction is happening in the second regulation phase. In the embodiment of Figure 14, where the regulation level is set by varying the value of R'_2 1033', the value of this resistance is set and changed by the regulation circuitry based on a detection from the comparator AMP 1035. For other implementations, the output of comparator can similarly be used to perform this switching.

[0035] Although the preceding discussion, as well as that which follows, is based on a charge pump for generating a positive output voltage, the same techniques can readily be applied to for pump systems that generate negative regulated voltages. Such systems are known and are regulated much as discussed above, but with, roughly speaking, the various levels involved inverted with respect to ground. For example, in the case of the negative charge pump, the behavior shown by V_{out} in the lower part of Figure 13 would again be exhibited, but in this case the values would be negative and what is being shown would be the magnitude of V_{vout} , $|V_{vout}| = -V_{vout}$. In particular, the same overshoot phenomena would be exhibited as shown, except the output would now go too negative. Consequently, the negative pump situation can be

addressed again as described with respect to the lower part of Figure 14 using a two-phase or –stage regulation during recovery or ramp-up (or, perhaps, “ramp-down” in this case). The first stage of recovery would use a first regulation level less negative (or lesser amplitude) than that of the second stage, which would use the regulation of the desired final level of regulation.

[0036] Figures 15-17 illustrate the actual behavior of a pump system for one stage and two stage recovery. Figure 15 is a one phase recovery process and the desired V_{out} level is 4.2V, although electric design rule (EDR) is approved for 4.3V in some corners. As the trace shows, after the load is connected, V_{out} drops down and recovery begins. Before settling to the regulation level of 4.2V, the overshoot occurs, having a maximum value of 4.55 V, exceeding 4.2V for 0.62us and 4.3V for 0.47us. This exceeds the EDR and can place significant stress on the load.

[0037] Figure 16 illustrates a two phase recovery. V_{final} is again 4.2V and V_{start} is taken as 4.0V. The top portion of Figure 16 schematically illustrates the two phases: once V_{out} drops below $L1=V_{start}$, the regulation switches to regulation based on this initial level and recovery begins. Once the level $L1$ is reached, after some delay, the regulation is switched to V_{final} for the final, relatively small, phase of recovery. An actual trace of this behavior is shown in the lower portion of Figure 16, where the bottom trace shows signal controlling when the lower level of regulation $L1=V_{start}$ is being used. In this example, $V_{start}=4.0V$. The top trace is V_{out} . Once the load is connected, V_{out} drops below 4.0V, the $L1$ control signal is asserted, and recovery based on the a 4.0V regulation level is used. The output ramps up and after the output initial reaches 4.0V, after a delay to let the overshoot drop back, the $L1$ control signal is de-asserted and the regulation is then based on $V_{final}=4.2V$. The amount of delay can be preset or trimable. In this example, the maximum V_{out} is reduced to 4.39V (as opposed to 4.55V in Figure 15) and 4.3V is exceeded for 0.21us (compared to 0.47us in Figure 15). The full recovery time for both phases is 1.91us.

[0038] Figure 17 corresponds to the lower portion of Figure 16, but with $V_{start}=3.9V$. In this case the maximum value of V_{out} is 4.33V and V_{out} exceeds 4.3V for 0.09us. The full recovery time for both phases is 1.91us. In all these cases, the system will then operate in regulation mode based on V_{final} .

[0039] The discussion here was based on a Dickson-type pump, using a two stage recovery, and where the regulation is effected through the clock circuitry, but the techniques are more generally applicable. For example, they can be applied to other pump types (such as voltage doublers) and other methods of regulation (such as varying clock frequency, clock amplitudes, input voltages, number stages, and so on), such as those described in the various references cited above. Similarly, instead of using of two discreet regulation levels, more levels can used or even a continuously varied regulation level. The differing regulation levels can also be implemented in a number of ways: in Figure 14, the value of R'_2 1033 is varied, but alternately the value of R_1 1031 or V_{ref} could be varied, for example.

[0040] Although the invention has been described with reference to particular embodiments, the description is only an example of the invention's application and should not be taken as a limitation. Consequently, various adaptations and combinations of features of the embodiments disclosed are within the scope of the invention as encompassed by the following claims.

IT IS CLAIMED:

1. A charge pump system for supplying an output voltage to a load, comprising:

a charge pump connected to receive an input voltage generate therefrom the output voltage;

regulation circuitry connected to receive the output voltage and a reference voltage, the regulation circuitry connected to the charge pump to regulate the output voltage based upon the values of the reference voltage and the output voltage,

wherein during a recovery operation, the output voltage is initially regulated according to a first level and subsequently regulated to a second level of greater amplitude than the first level, the second level corresponding to a desired regulated output voltage.

2. The charge pump system of claim 1, wherein the regulation circuitry generates a control signal based upon the values of the reference voltage and the output voltage, the charge pump system further comprising:

a clock generation circuit connected to receive the control signal and an oscillator signal and generate therefrom a clock signal dependent upon the control signal, wherein the charge pump is connected to receive the clock signal and generates the output voltage based on the clock signal.

3. The charge pump system of claim 2, wherein the frequency of the clock signal is dependent upon the control signal.

4. The charge pump system of claim 2, wherein the amplitude of the clock signal is dependent upon the control signal.

5. The charge pump system of claim 1, wherein the regulation circuitry includes:

first and second elements connected in series between the output voltage and ground;

a comparator having a first input connected to receive the reference voltage, having a second input connected to a node between the first and second elements, and

generating as output a control signal having a value based upon the first and second inputs, wherein the charge pump is regulated based upon the value of the control signal.

6. The charge pump system of claim 5, wherein one or more of the first and second elements are resistances.

7. The charge pump system of claim 6, wherein the value of one of the elements has a first value when regulating according to the first level and a second value when regulating according to the second level.

8. The charge pump system of claim 5, wherein one or more of the first and second elements are capacitances.

9. The charge pump system of claim 1, wherein the charge pump has a Dickson-type pump structure.

10. The charge pump system of claim 1, where the first and second levels are positive voltage levels, the second level being higher than the first level.

11. The charge pump system of claim 10, wherein the regulation circuitry regulates the charge pump according to the first level in response to the output voltage dropping below the first level and regulates the charge pump according to the second level in response to the output voltage rising above the first level.

12. The charge pump system of claim 11, wherein, subsequent to the output voltage rising above the first level, the regulation circuitry continues to regulate the charge pump according to the first level for a delay period before regulating the charge pump according to the second level.

13. The charge pump system of claim 1, where the first and second levels are negative voltage levels, the second level being more negative than the first level.

14. A method of operating a charge pump system to provide an output voltage at an output, comprising:

applying a load to the output;

in response, operating the charge pump in a recovery phase, including:

regulating the output voltage according to a first level; and

subsequently regulating the output voltage according to a second level, the second level being of a greater amplitude than the first level; and

subsequently supplying the load with the output regulated according to the second level.

15. The method of claim 14, where the first and second levels are negative voltage levels, the second level being more negative than the first level.

16. The method of claim 14, where the first and second levels are positive voltage levels, the second level being higher than the first level.

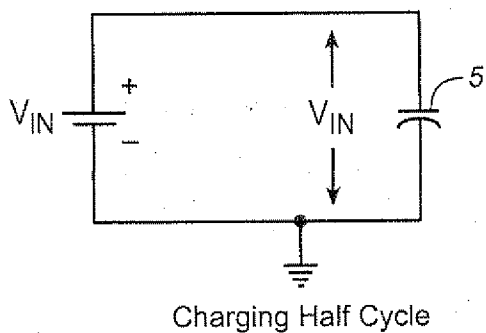
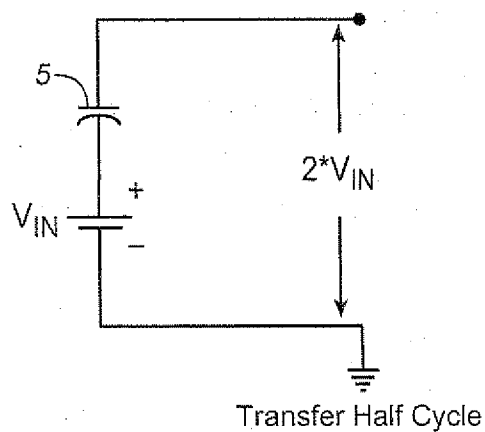
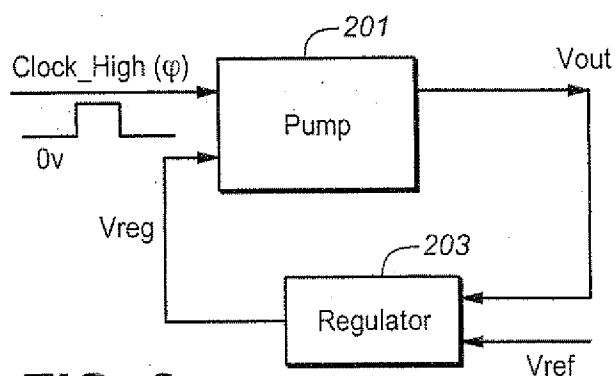
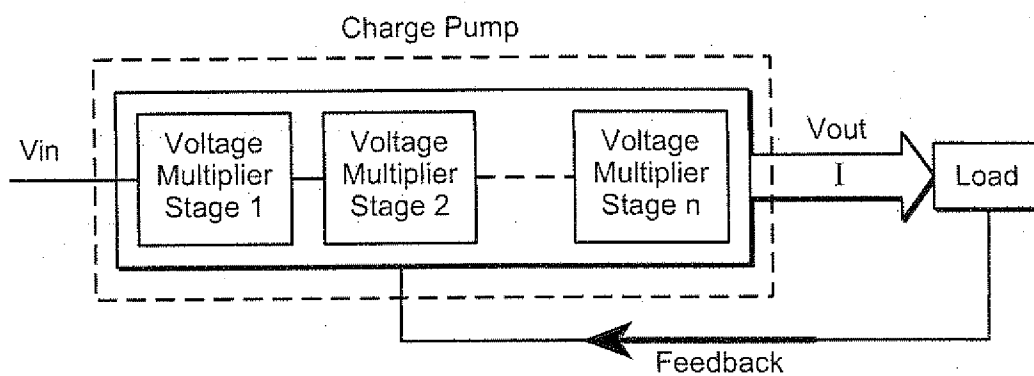
17. The method of claim 14, wherein the charge pump operates in the recovery phase in response to the amplitude of output voltage dropping below the amplitude of first level.

18. The method of claim 14, the recovery phase further comprising:

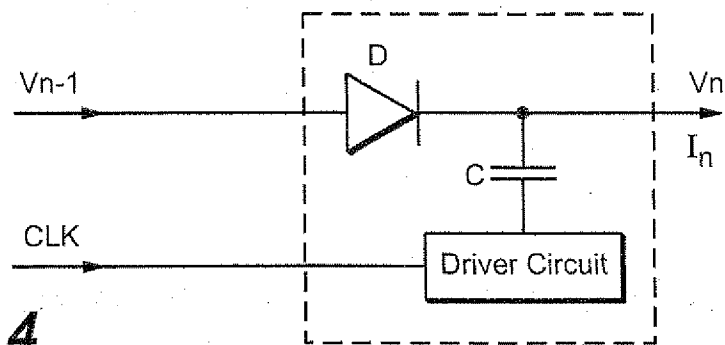
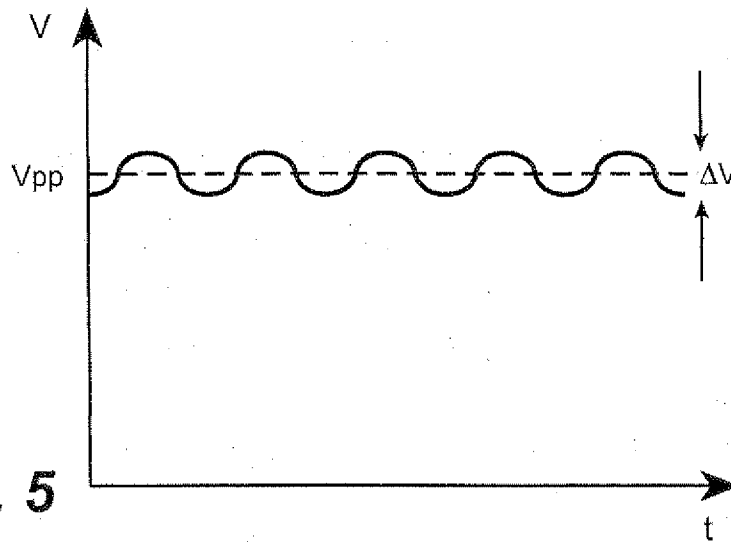
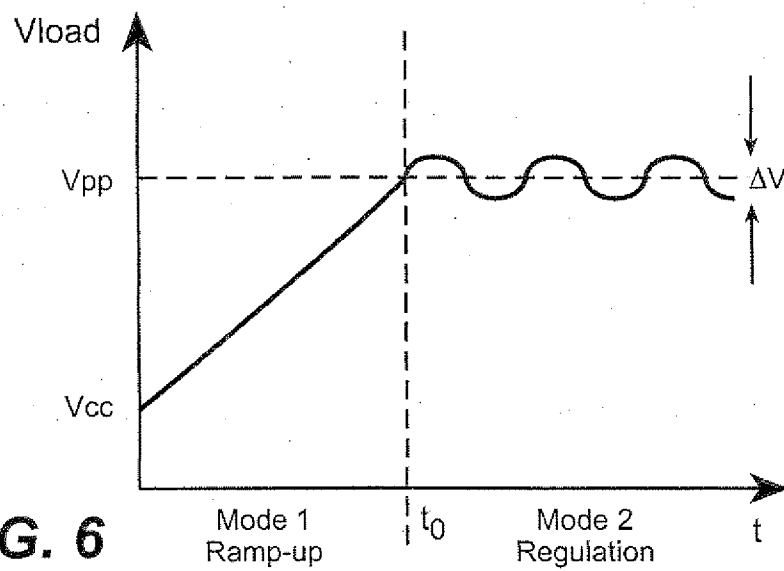
while regulating the output voltage according to the first level, detecting that the output voltage has reached the first level, wherein the output voltage is regulated according to the second level in response to detecting that the amplitude of the output voltage has reached the first level.

19. The method of claim 18, wherein, subsequent to detecting that the amplitude of the output voltage has reached the first level, the output voltage is regulated according to a first level for a delay before regulating the output voltage according to the second level.

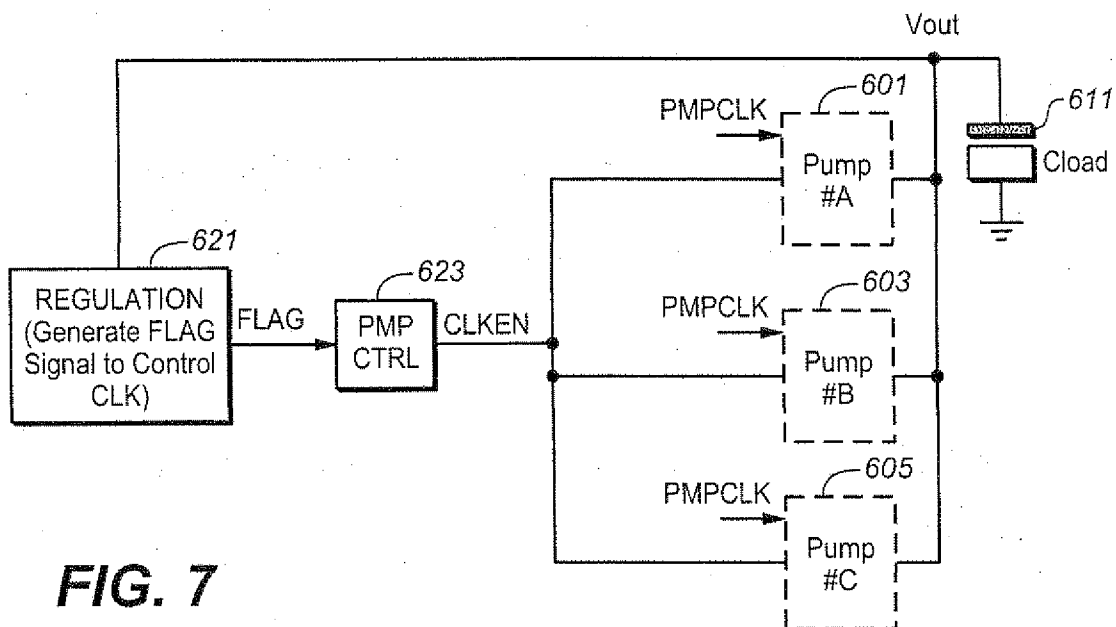
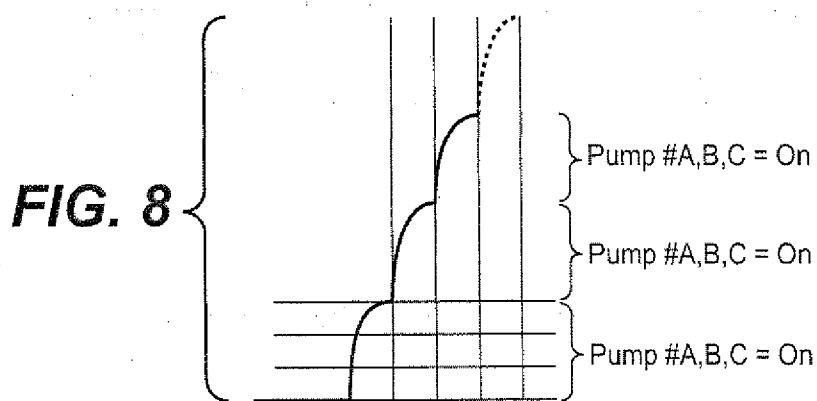
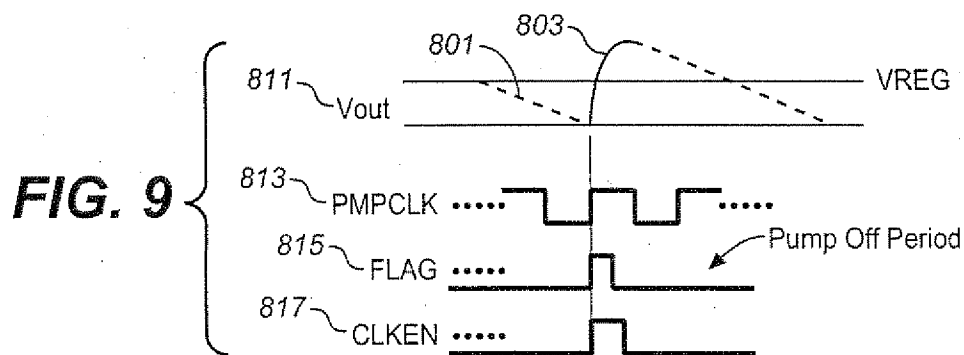
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**FIG. 1A****FIG. 1B****FIG. 2****FIG. 3**

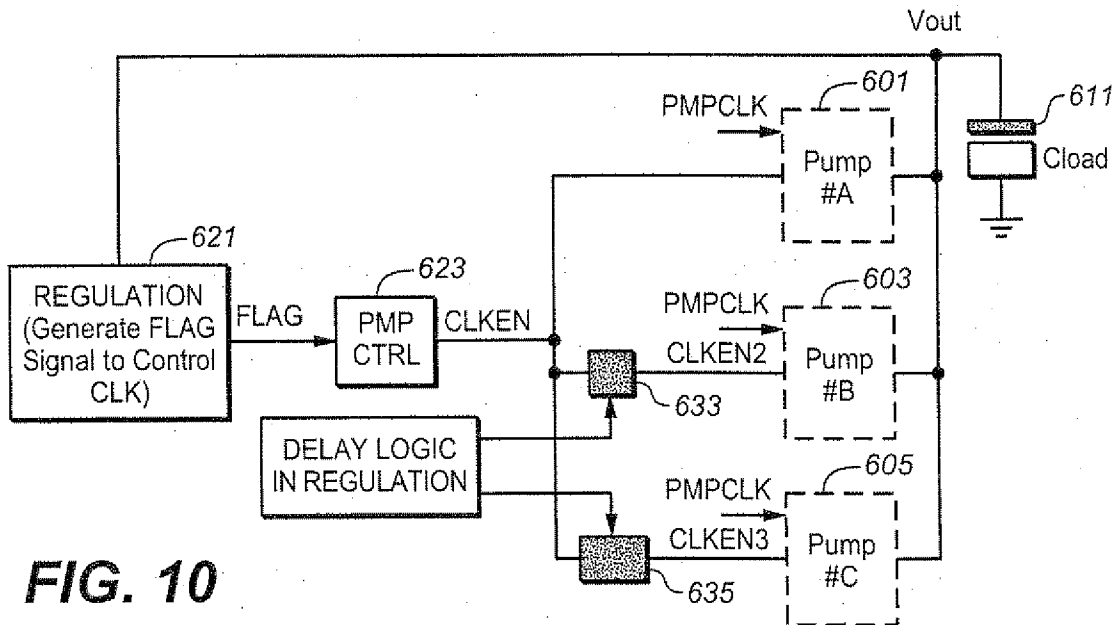
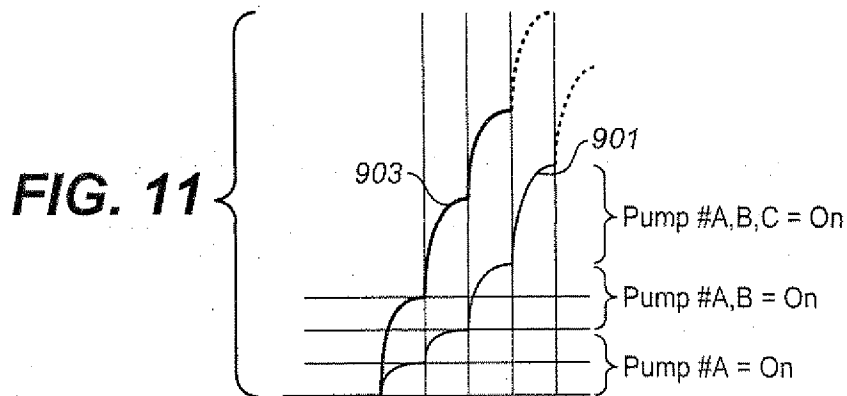
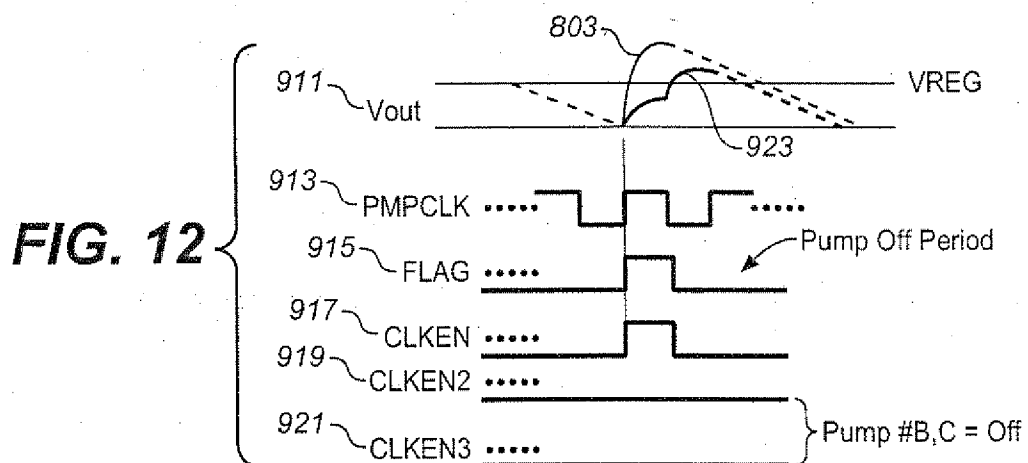
2 / 9

**FIG. 4****FIG. 5****FIG. 6**

3 / 9

**FIG. 7****FIG. 8****FIG. 9**

4 / 9

**FIG. 10****FIG. 11****FIG. 12**

5 / 9

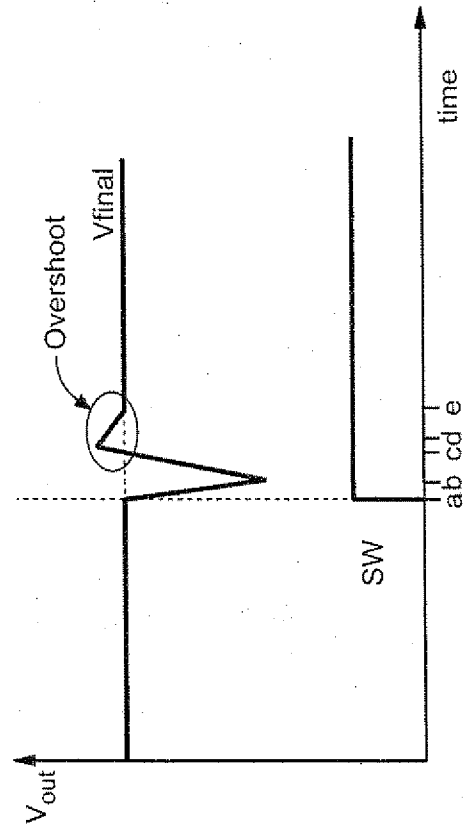
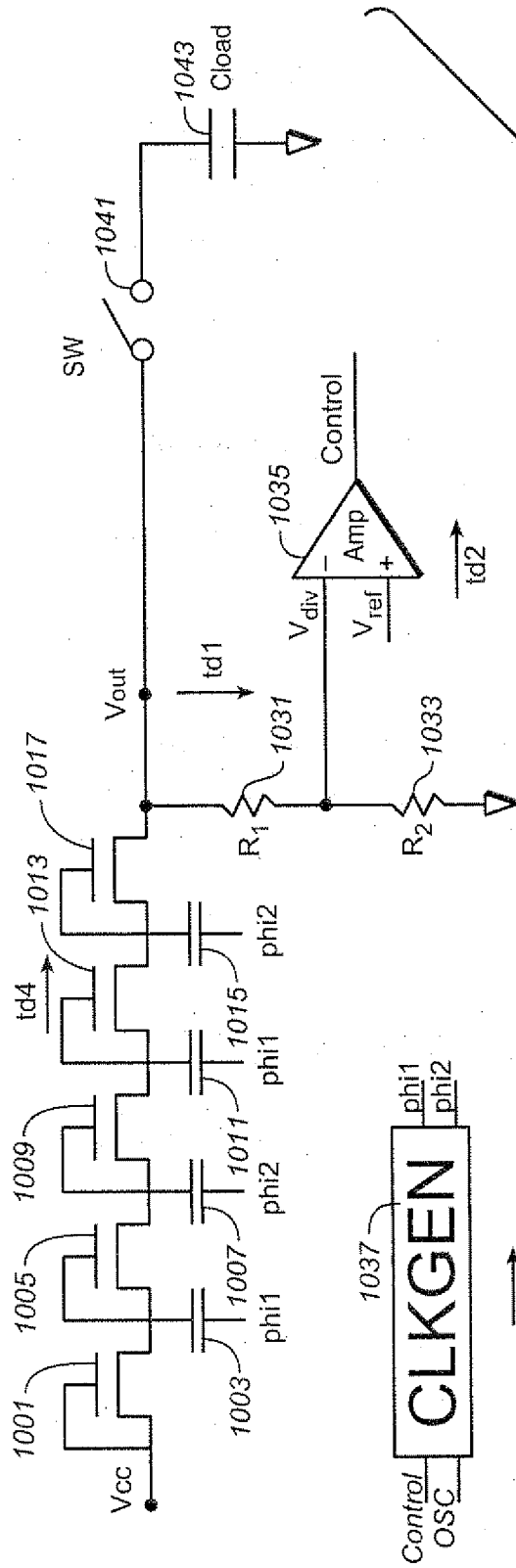


FIG. 13

6 / 9

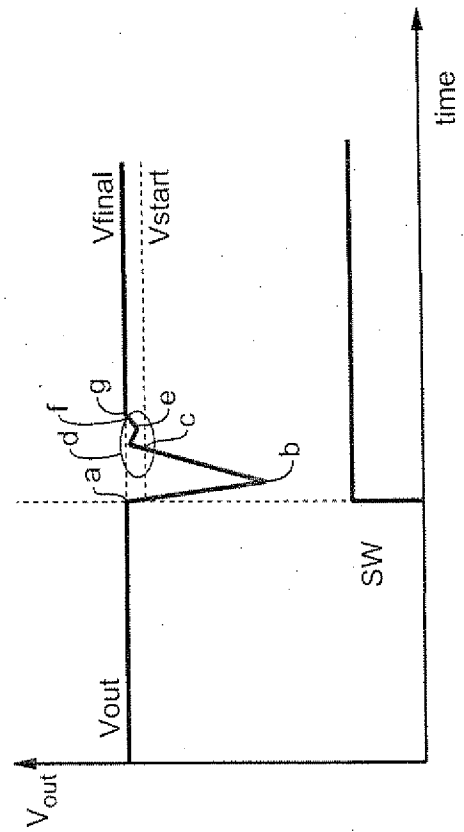
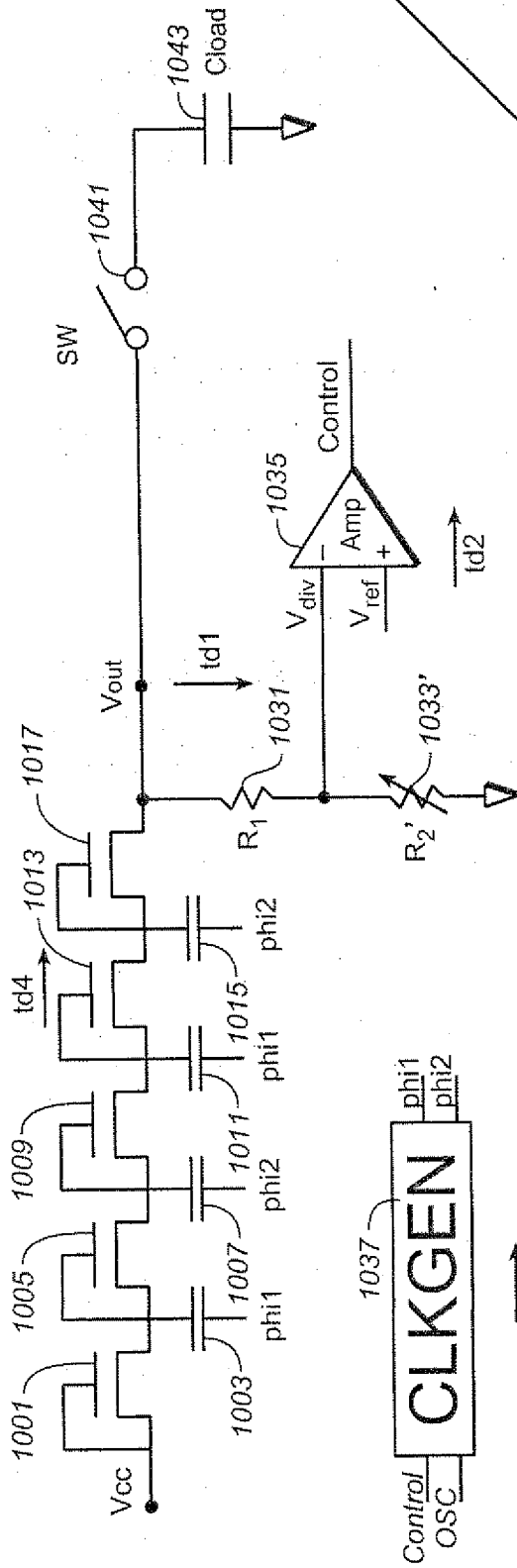


FIG. 14

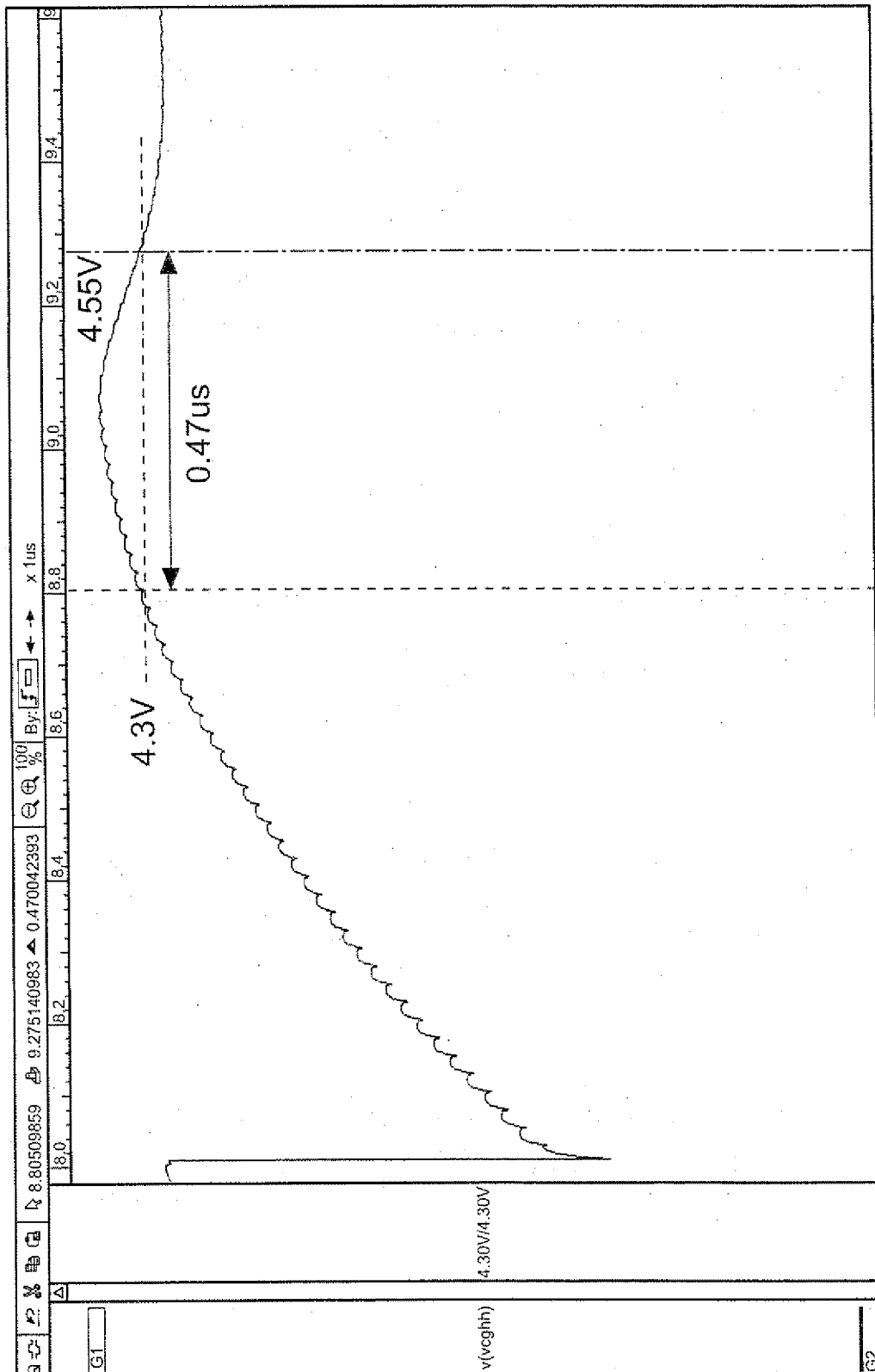
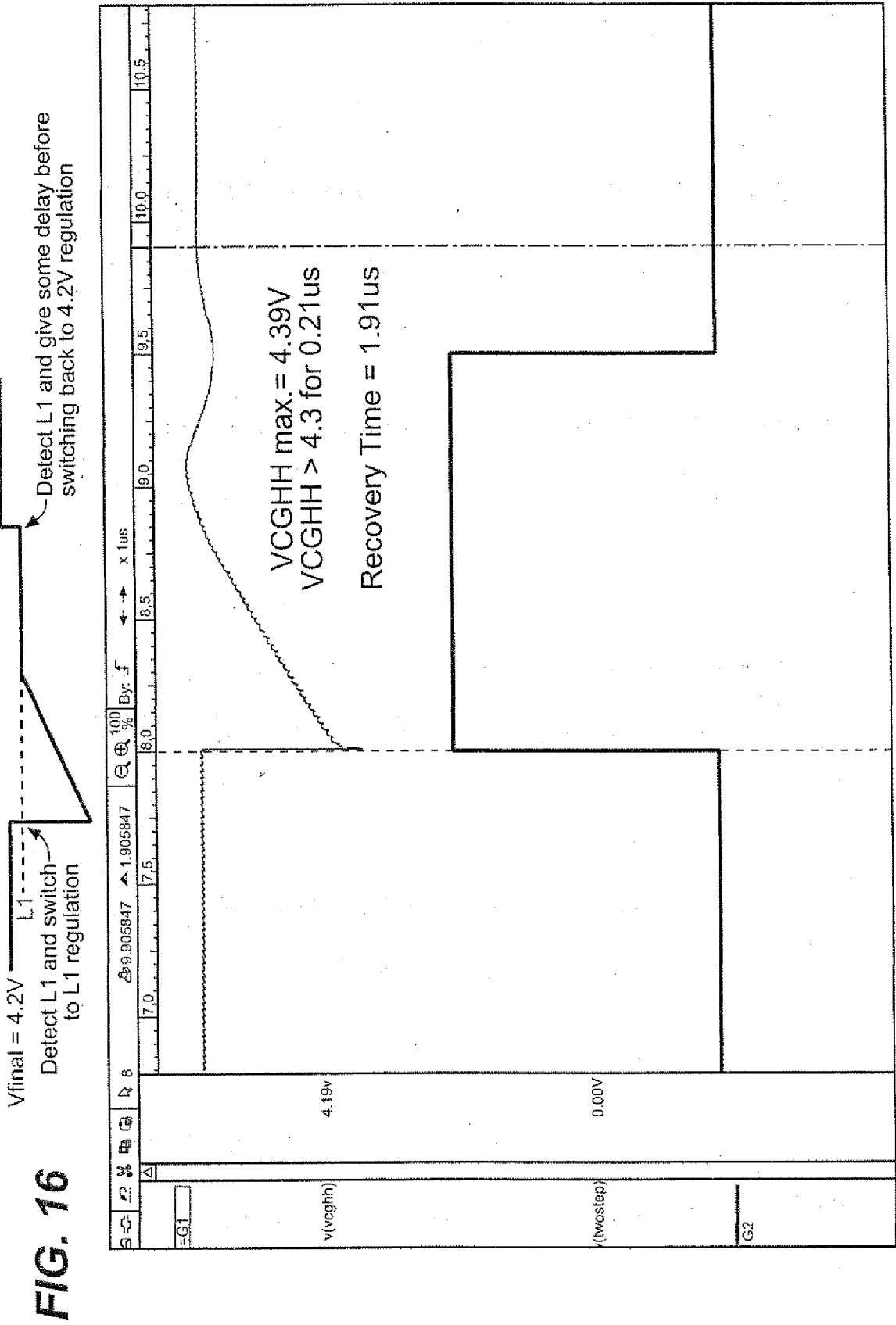


FIG. 15



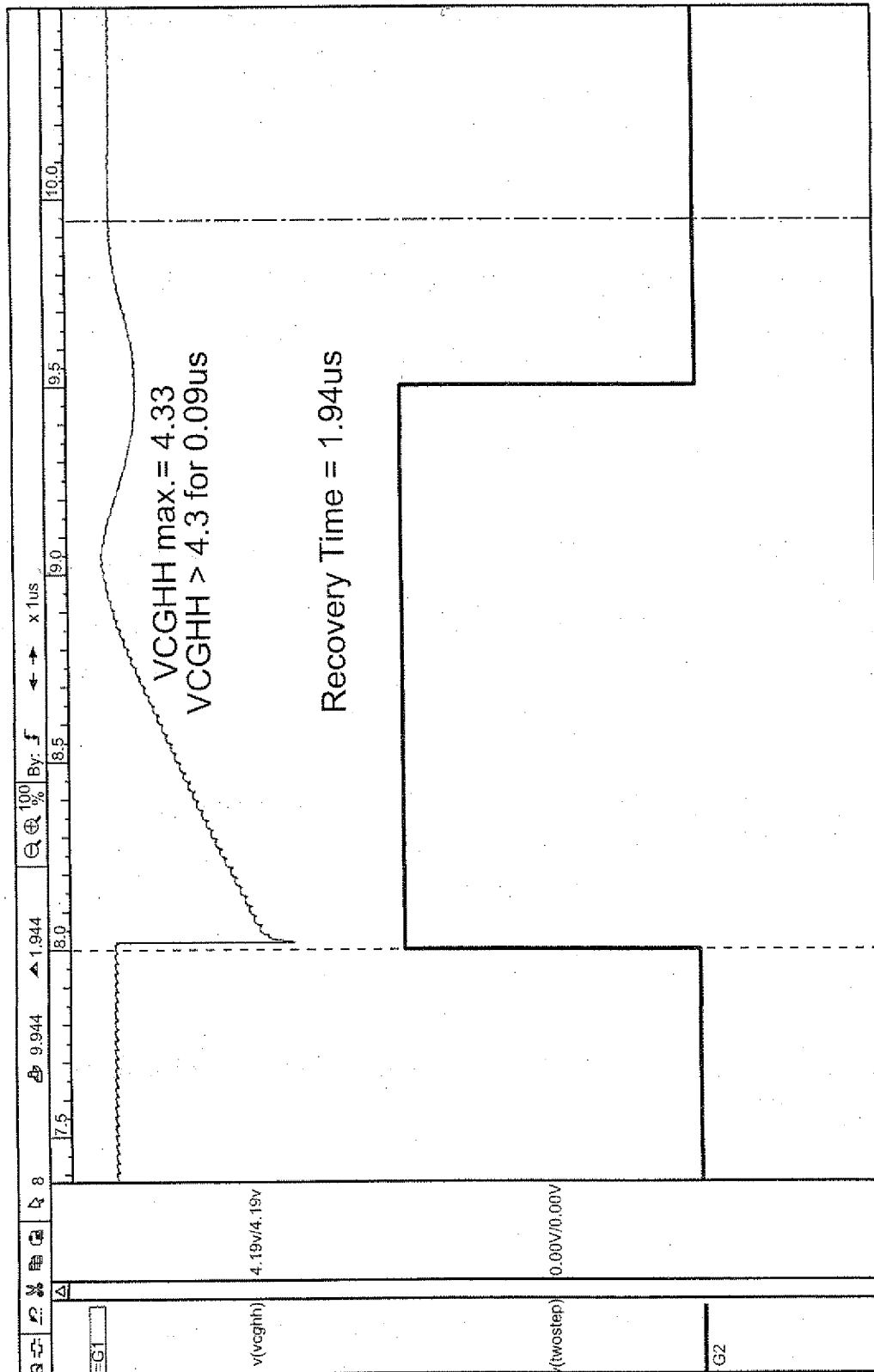


FIG. 17

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/060195

A. CLASSIFICATION OF SUBJECT MATTER INV. G11C5/14 G11C16/30 H02M3/07 H03K19/00 ADD.		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) G11C H02M H03K		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practical, search terms used) EPO-Internal, IBM-TDB, WPI Data		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DE 10 2007 026290 A1 (SAMSUNG ELECTRONICS CO LTD [KR]) 3 July 2008 (2008-07-03) paragraph [0027] - paragraph [0043]; figures 3,4	1-19
A	----- US 2009/033306 A1 (TANZAWA TORU [JP]) 5 February 2009 (2009-02-05) paragraph [0038] - paragraph [0045]; figures 5,6	1-19
A	----- US 2008/218134 A1 (KAWAKAMI YOSHIHITO [JP] ET AL) 11 September 2008 (2008-09-11) paragraph [0033] - paragraph [0052]; figures 3-5 -----	1-19
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents : "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art. "&" document member of the same patent family		
Date of the actual completion of the international search 6 April 2011		Date of mailing of the international search report 15/04/2011
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016		Authorized officer Lindquist, Jim

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

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