

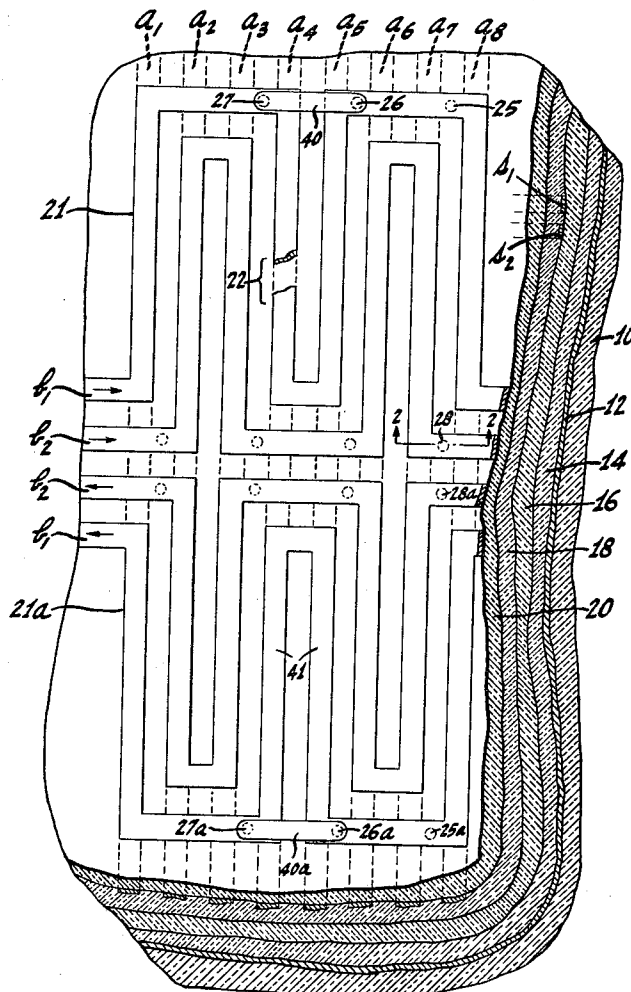
[72] Inventor **Robert A. Gange**
Belle Mead, N.J.
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 [73] Assignee **RCA Corporation**

[56] **References Cited**
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Primary Examiner—Terrell W. Fears
Attorney—H. Christoffersen

[54] **REPAIR OF THIN-FILM STRUCTURE SUCH AS CRYOELECTRIC MEMORY**
 10 Claims, 2 Drawing Figs.

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 340/174
 [51] Int. Cl..... G11c 11/44
 [50] Field of Search..... 340/174
 (TF), 173.1; 29/575, 401, 402, 472.1

ABSTRACT: Insulated riser conductors extend from the substrate to the outermost leads (those which are exposed) of a cryoelectric memory. A break in one of these leads may be repaired by soldering or otherwise connecting a wire or other conductor between two riser conductors.



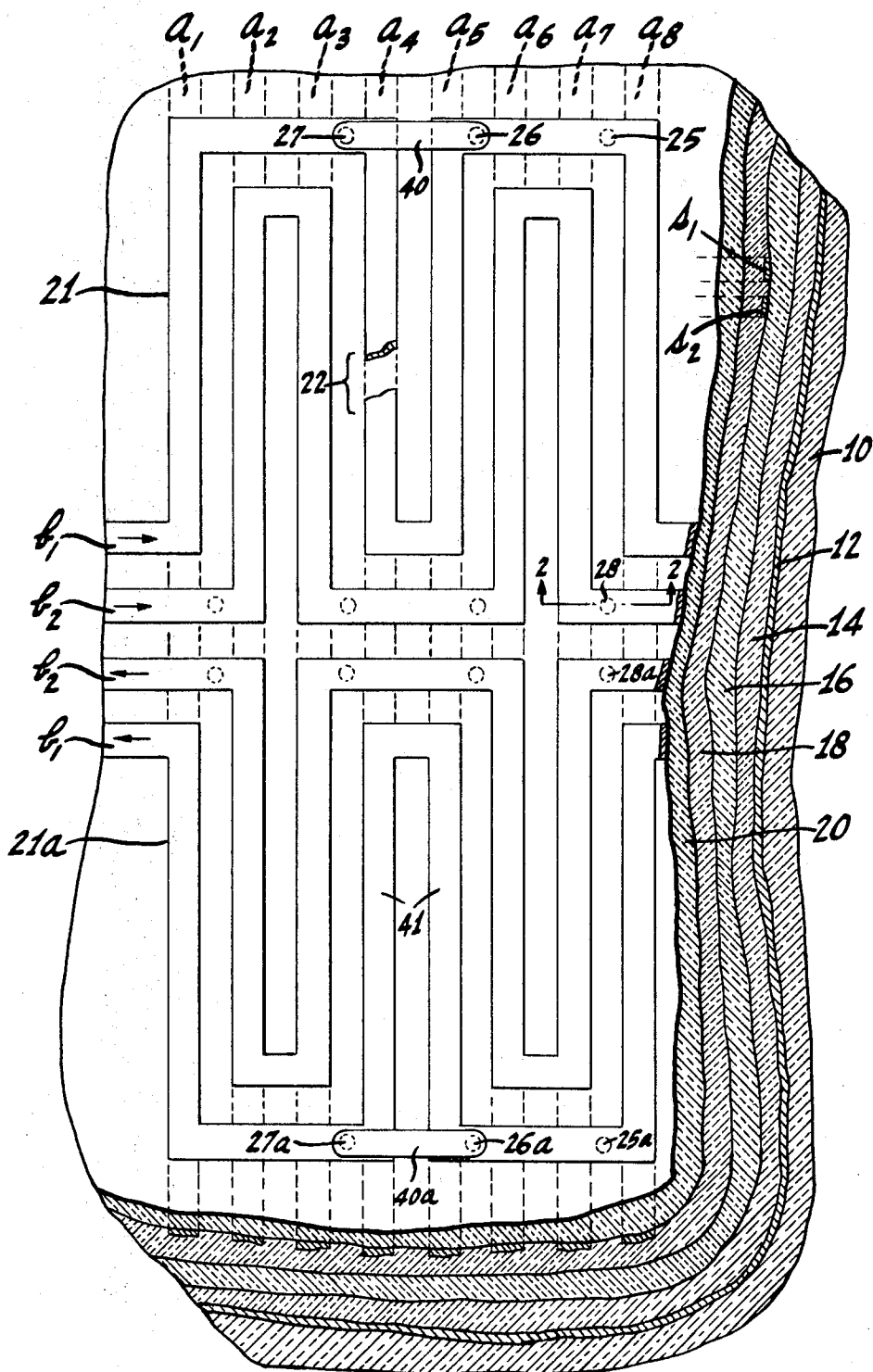


Fig. 1.

INVENTOR
ROBERT A. GANGE

BY *Samuel A. Gange*
ATTORNEY

REPAIR OF THIN-FILM STRUCTURE SUCH AS CRYOELECTRIC MEMORY

In the manufacture of cryoelectric memories such as are described by the present inventor in the article, "Taking Cryoelectric Memories Out of Cold Storage," *ELECTRONICS*, Apr. 17, 1967, page 111, the statistical possibility of defects increases as the number of storage locations per plane increases. One source of such defects is opened in the very last layer of the memory, that is, opens in the *b* drive lines (such lines are shown, for example, on page 117 of the article).

While the *b* drive lines are visible and it is possible with the aid of a microscope or magnifying glass visually to detect where the open or break occurs, it has been found not to be possible to repair this damage. The reason is that the *b* line is quite fragile, of the order of only 1 micron (10^{-6} meters) thick and any effort to solder or otherwise secure a wire to the *b* line results only in further damage to the *b* line. And, even if it were possible to repair the *b* line, the mechanical stresses which would result when the memory temperature was changed as, for example, when the memory was cooled from room temperature to several degrees Kelvin, would cause the *b* line to separate from the insulation and become damaged again.

An object of the present invention is to provide a simple but effective way of making repairs in open lines of a thin-film structure such as a cryoelectric memory plane.

Another object of the invention is to provide a balanced drive line arrangement for a memory, which arrangement can be repaired without adversely affecting the balance of the lines and without introducing noise.

BRIEF SUMMARY OF THE INVENTION

In the thin-film structure of the invention, spaced riser conductors extend from the substrate to a lead of the outermost layer of the structure. A break in this lead may be repaired by securing a wire or other conductor between two of the riser conductors.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a perspective showing of a portion of a cryoelectric memory plane which includes the structure in accordance with the present invention which permits both easy repair of the *b* lines and practical array operation; and

FIG. 2 is a section taken along line 2-2 of FIG. 1.

DETAILED DESCRIPTION

The memory plane shown in part in FIGS. 1 and 2 includes a substrate 10 formed of an insulating material such as glass and a thin layer of metal 12 such as chromium covered by gold. A ground plane 14 which may be formed of lead is over the layer 12. The layer 12 forms a chemical bond to the substrate and the lead ground plane adheres tightly to the gold interface between the lead and the chromium.

The ground plane 14 is covered by a layer of insulation 16 and the sense lines, only two of which s_1 and s_2 are shown, lie on the layer of insulation 16. The sense lines are formed with loops such as shown in the article above but which are not shown in the present FIGS.

The sense lines are covered by a layer of insulation 18 and the *a* drive lines, eight of which $a_1, a_2, \dots, a_8$ are shown, are located on the layer of insulation 18. Another layer of insulation 20 covers the *a* drive lines and the final layer comprises specially patterned *b* drive lines, two of which are shown at b_1 and b_2 . Each *b* line consists of two portions, one the mirror image of the other. For example, the line b_1 has one meandering portion 21 which is the mirror image of the other portion 21a of the same line b_1 . Each line such as b_1 is spaced from the next adjacent line b_2 at the point of entry by a distance comparable to the line width—about 2 mils in one practical design.

This arrangement permits either line b_1 or line b_2 to be driven in a balanced fashion and the riser column repair structure 26, 26a, 27, 27a, etc. shown in FIGS. 1, 2 and discussed shortly does not adversely affect this balance. In the absence of the riser columns, the two *b* current waves of opposite polarity (the arrows indicate the directions of *b* current flow) move periodically away from and toward each other as the *b* signal propagates. The image current return path initially forms at the point of entry of the *b* current and is of the order of five line widths in length at its greatest length. Continuity of the image current thereafter is maintained through displacement current flow through the insulators 16, 18, 20.

Thus the magnetic field energy is at each point confined to the volume of space between the *b* conductor and the ground plane 14. The image current return path is at the point at which the source current (the *b* drive current) enters the plane and therefore contributes a negligible amount to the total magnetic field energy. The electric field components of the signal propagate in a manner such that equal amounts of charge are simultaneously injected into and removed from the ground plane 14 along the *b* source current wave fronts. Noise which otherwise would be introduced into the sense or digit lines through the sense or digit-line-to-ground plane capacitance is thus avoided since the ground plane remains at system ground potential throughout the signal propagation. As the riser columns are also arranged in symmetrical fashion (25a opposite 25, 26a opposite 26 and so on) they do not adversely affect the balance of the system and introduce no noise.

The sense lines may be formed of a superconductor material such as tin. The *a* and *b* drive lines may be formed of a superconductor material such as lead. They and the other memory layers may be manufactured by known vapor deposition and chemical etching techniques. The manner of operation of the memory, which is not of direct concern in the present application, is described in the article and elsewhere in the literature.

In the manufacture of the memory such as shown in the FIGS. it sometimes occurs that there are breaks in the *b* line such as shown, for example, at 22. In the past, it has been found not possible to repair such a break. The reason is that the *b* line is of very small cross section and is quite fragile. Any effort to bridge the break by connecting across it an extremely fine wire results only in further damage to the *b* line as already discussed.

In the memory structure according to the present invention, the *b* lines are symmetrically positioned as already described and riser columns are strategically located in symmetrical fashion at various points along the *b* lines. The latter are illustrated in FIG. 1 by dashed circles such as 25, 25a, 26, 26a, 27, 27a, 28 and so on. Each riser column is secured to the substrate 10 and is insulated from all conductors in the memory except the *b* line.

A detailed showing of riser column 28 appears in FIG. 2. It is fabricated in the following manner. First, a layer of chromium is deposited onto a heated glass substrate 10 as, for example, by vacuum deposition. The heat forms a chromium oxide bond between the chromium and the glass; a thin layer of gold is then deposited onto and adheres to the chromium. A photoresist pattern may be laid down onto the gold chrome layer 12 and developed and a portion of the layer not exposed may be washed away. The chromium-gold layers are selectively etched, the hardened photoresist removed or stripped, and the result is a region such as shown at 30 which may be from one to five mils or larger in area surrounded by a conductor free area.

After the pattern above is obtained, the surface of the gold chromium layer 12 may be cleaned as, for example, by bombarding with ions and then the ground plane 14 may be laid down. A photo-etch technique similar to the above may be employed to provide the small region 32 of lead which is spaced from the remainder of the ground plane. Next the layer 16 of insulation may be deposited. The insulation not only covers the ground plane 14 but also passes into the opening 34

so as to fill the space between the regions 30, 32 and the remaining portion of layers 12 and 14. Although in filling this space, a contour forms along the top boundary of the insulator, a straight line is used in FIG. 2 for reasons of clarity.

One of a number of techniques may be employed to keep the top surface of the lead (Pb) region 32 free of insulation 16. For example, the insulator may be deposited through a stencil mask in a manner such that the region 32 is shielded from the insulator. Another technique is to not remove or strip the hardened photoresist layer prior to depositing the insulator which previously protected region 32 from etching. Instead, the insulator is deposited over the area including region 32. A "window" may then be formed by stripping the hardened photoresist and with it, the small region of insulator which lies above it.

A tin layer is next deposited, and the sense lines are patterned with photo-etch techniques similar to those described above. During the deposition of the tin layer, contact is made between the exposed upper surface of the lead region 32 and the tin layer. Subsequent to photo-lithographic patterning, a tin region 36 adheres to the lead region 32. The sequence of events is repeated; insulator 18 is deposited in a manner similar to insulator 16, and the lead region 38 is deposited on the tin 36 at the same time that the *a* lines are laid down. The final portion of the riser 28 consists of the lead (Pb) of the *b* line, *b*₁.

As should be clear from FIG. 2, the riser, while of relatively small cross section, is a rugged structure that connects from the *b* line to the solid support provided by the glass substrate 10. Should a break be present in the *b* line such as shown at 22 in FIG. 1, a repair can be effected by connecting a conductor such as shown at 40 between two adjacent risers such as shown at 26 and 27. Although the conductor shown is a metal strip about 2 mils wide, other forms of connection are possible, e.g., a 2 mil (or larger) gold wire can be welded between the riser columns, or soldered using small land soldering techniques. Other methods of repair include the use of infrared soldering techniques and the use of etched conductors on mylar or kapton as the repair connections.

In order to maintain the symmetry of the memory and its relatively noise-free performance, any time a repair is made between two risers, a corresponding wire or other conductor is connected to the pair of symmetrically located risers. This is illustrated in FIG. 1 by the connection 40a between risers 26a and 27a. Note that this second connection is made even though there is no open or other defect in the length of line 41 between these risers.

While the riser columns illustrated are shown to occur throughout the memory, other constructions are possible. For example, the riser columns may be located only at the outer edges of the memory. This makes their construction somewhat more convenient. It makes it possible, for example, to prevent insulation from being deposited onto the columns during their fabrication by employing tabs at the edges of the masks through which the insulation is deposited. These tabs mask the ends of the riser columns. Although this approach permits each insulator layer to be deposited in one rather than two steps, a disadvantage is that when a repair is made, twice as many memory locations are lost than in the approach illustrated in FIG. 1. Note that in FIG. 1, all memory locations lying between risers 27 and 26 are bypassed by the conductor 40 and are not employed for the storage of information. The same is true for the memory locations between risers 26a and 26b.

While the invention has been described in terms of a cryoelectric memory, it is to be understood that this is merely illustrative as the repair techniques are applicable to other

thin-film structures whether cryoelectric or not.

I claim:

1. In a thin-film structure having an insulating substrate, conductors and insulation on the substrate and a final layer spaced from the substrate which includes a thin-film conductor, the improvement comprising:
 - a plurality of spaced, conductive riser columns extending between the substrate and said thin-film conductor of said final layer, said columns being insulated from all conductors of the thin-film structure except said thin-film conductor of said final layer.
2. In the thin-film structure as set forth in claim 1, said final layer thin-film conductor having an open therein between two of said riser columns; and
 - further including means for repairing said open comprising a conductor conductively connected between said riser columns.
3. In a cryoelectric memory plane having an insulating substrate, a conductive ground plane on the substrate and alternate layers of insulation and conductors over the ground plane and a final layer spaced from the ground plane which includes a thin-film conductor, the improvement comprising:
 - said ground plane formed with spaced openings therein; and
 - a plurality of spaced, conductive riser columns extending through said openings in said ground plane between the substrate and said thin-film conductor of said final layer, said columns being insulated from all conductors of the thin-film structure except said thin-film conductor of said final layer.
4. In a cryoelectric memory plane as set forth in claim 3, said thin-film conductor of said final layer being formed with a break therein and further including means which repair said break comprising a conductor secured between lead to riser columns, one on each side of said break.
5. In a cryoelectric memory which includes an insulator substrate, a ground plane on the substrate, and drive lines insulated from and lying over the ground plane, an improved drive line layout comprising: a plurality of drive lines lying on an insulating layer, each such drive line entering and leaving the region of the insulating layer over the ground plane at relatively closely spaced points, each such drive line comprising two portions, one the mirror image of the other, one for carrying current onto the ground plane and each drive line portion taking a meandering path which alternately approaches and becomes further spaced from the mirror image portion of the same line.
6. In a cryoelectric memory as set forth in claim 5, said drive line portions lying side-by-side and being substantially equidistant from one another throughout their length.
7. In a cryoelectric memory as set forth in claim 6, each drive line portion being spaced from the next adjacent drive line portion by a distance comparable to the width of the drive line.
8. In a cryoelectric memory as set forth in claim 5, further including a plurality of spaced conductive riser columns extending through openings in said ground plane between the substrate and the two portions of each drive line, said columns being insulated from all conductors of said memory except for said drive line portions, the spaced conductors for each drive line portion being symmetric with the spaced conductors for the mirror image portion of said drive line.
9. In a cryoelectric memory as set forth in claim 5, said drive lines being arranged in pairs.
10. In a cryoelectric memory as set forth in claim 8, at least some of said riser columns being located at the portions of one of said drive lines which are spaced furthest apart from one another.

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,576,551 Dated April 27, 1971

Inventor(s) Robert A. Gange

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 4, line 43, after "and" insert ---the other for
carrying current off the ground
plane, and---

Signed and sealed this 7th day of September 1971.

(SEAL)
Attest:

EDWARD M. FLETCHER, JR.
Attesting Officer

ROBERT GOTTSCHALK
Acting Commissioner of Pat