May 14, 1963 S. RUHMAN ETAL 3,090,035

DIGITAL COMPUTING SYSTEMS

Filed Oct. 25, 1954 2 Sheets-Sheet 1

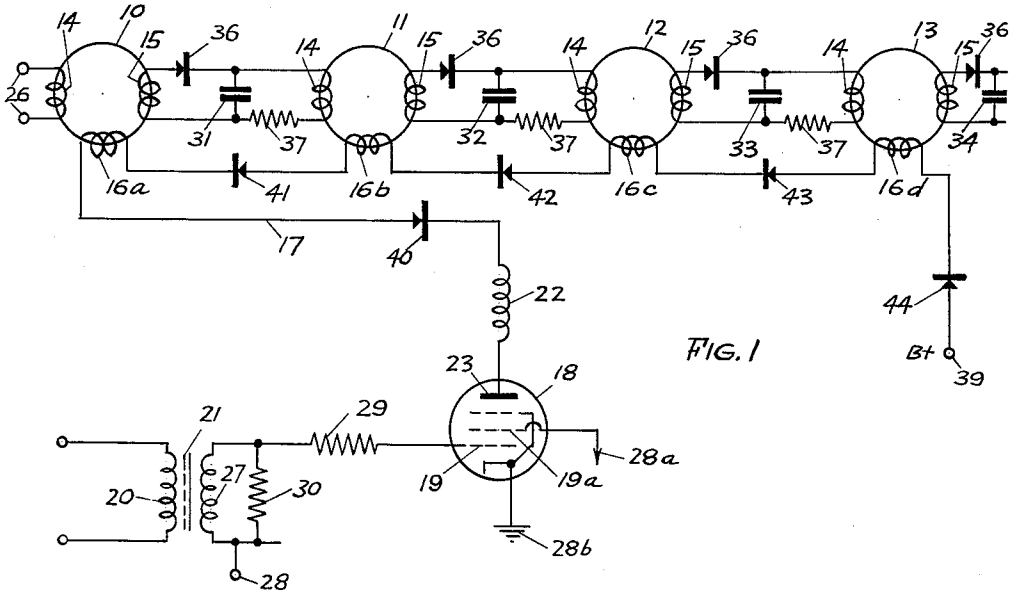


FIG. 1

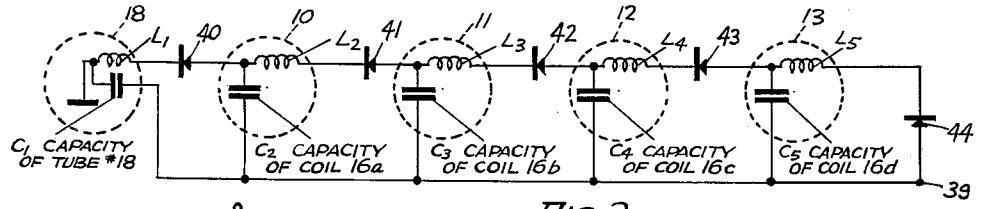


FIG. 2

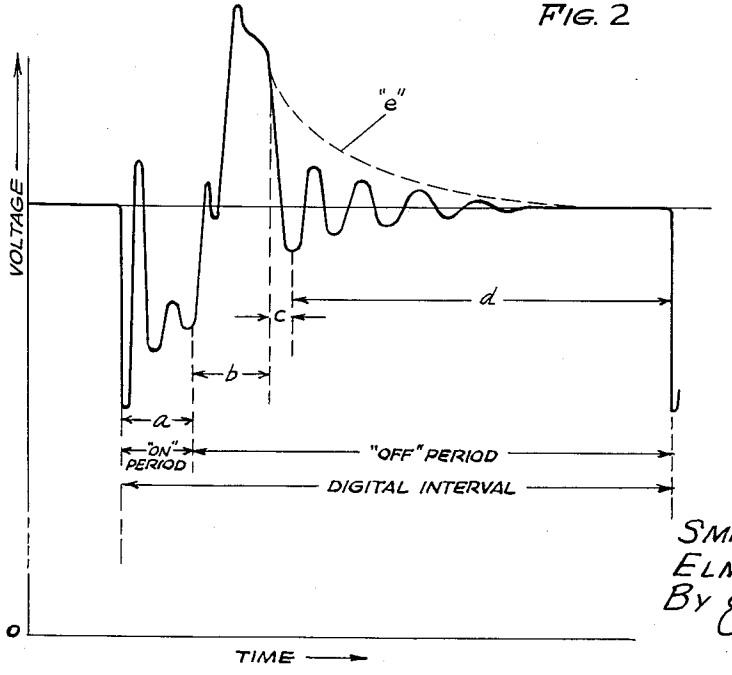


FIG. 3

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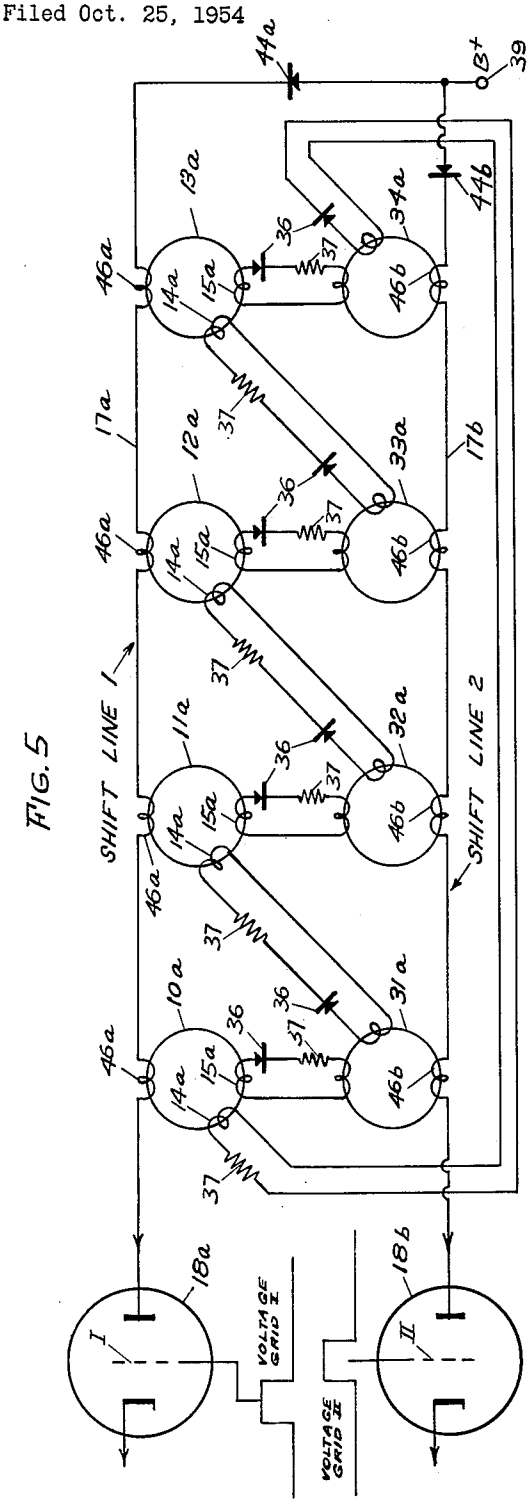


FIG. 5

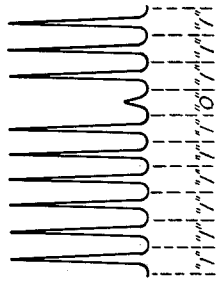


FIG. 4b

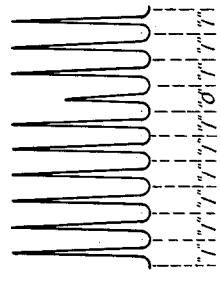


FIG. 4a

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DIGITAL COMPUTING SYSTEMS

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This invention relates to computing systems, and particularly to computing or counting in binary code by progressively shifting digital information-representing currents along a series of magnetically controlled circuits.

The invention provides means for preventing, or nullifying the effect of, undesirable oscillations and reverse current flow tendencies inherent in binary computing systems utilizing magnetic cores of a composition providing a rectangular or near rectangular hysteresis curve characteristic serially linked by digit-transferring windings and also by actuating windings upon which digit-shifting currents are impressed intermittently, such devices being commonly called "shift registers."

Because of the intermittent nature of the energization of the magnetic cores, and the fact that the duration of "read-in" and "read-out" pulses, particularly in high speed registers, is an extremely small fraction of a millisecond, the transformation of an individual magnetic core from a condition of saturation in one direction to a condition of saturation in the opposite direction is correspondingly rapid. This rapidity of energy transfer creates a problem in the matter of ridding the current-carrying actuation circuit or circuits of residual charge each time current flow is cut off by pulse cessation. Each cut-off operation gives rise to a tendency toward residual energy flow in both directions throughout the various interlinked subcircuits, particularly during the "off" periods between entry of successive flux-driving, or shift, pulses into the actuating windings of the successive cores. These residual currents are particularly troublesome in the shift-producing, or actuating, circuit or circuits because in such locations they have the potentiality of reversing the digital representations previously stored or registered in individual cores along the multi-stage computing line constituting the shift register. The more dense the pattern being stored and registered, the higher the frequency of cycling, or the more numerous the computing stages entering into a single registering line, the greater becomes this tendency toward reversal of the magnetic condition characterizing individual cores. In fact, with registers incorporating cores of low coercive force materials, even moderate conditions as to density, number of stages, or cycling speed may be sufficient to cause a build-up of residual current discharge during "off" periods of the register to a value high enough to cause read-in of "1" values (flux saturation in a predetermined direction) into cores which had just previously lost their "1" flux state, and for this reason, from the standpoint of maintaining the accuracy of the computation, should remain in the "0" flux state. The present invention provides a method and means to nullify the error-producing propensities of such residual energy, the method herein proposed being to interpose a barrier to the flow of such residual energy in such a direction as to interfere with the correctness of digital representations incorporated into the cores by the normal functioning of the core flux-directing (shift) circuit.

Other objects and characteristics of the invention will become apparent upon reference to the following description of the embodiments of the invention illustrated in the accompanying drawings wherein:

FIG. 1 is a diagrammatic view of a system embodying the invention;

FIG. 2 is an equivalent circuit diagram illustrating electrical factors inherent in the system;

FIGS. 3, 4*a* and 4*b* are graphs showing examples of voltage patterns at different points in the system with and without inclusion of the present invention; and

FIG. 5 shows a second embodiment of the invention.

Referring first to FIG. 1, the magnetic cores **10**, **11**, **12**, and **13** have input windings **14**, output windings **15**, and actuation ("shift") windings **16** (*a*, *b*, *c*, and *d*, respectively), the latter being serially connected in the plate circuit **17** of a driver tube **18** whose grid **19** receives signal voltage pulses at a rate (for example, 100 kc. per second) determined by the rate of pulse input to the primary winding **20** of a transformer **21** whose secondary circuit **27** is connected to a source **28** of negative potential for cut-off bias of grid **19**, the said secondary circut **27** also including a current-limiting resistor **29** in series relation to the secondary winding of the transformer and an oscillation absorbing resistor **30** in shunt relation to the secondary winding of the transformer. An inductance unit **22** may be inserted between plate **23** of the tube **18** and the shift winding **16***a* of the core **10**, and a source of positive potential (for example, 200 volts) is provided at the opposite terminal **39** of the circuit **17**. A second source **28***a* of positive potential (for example, **150** volts) supplies screen grid **19***a*, while the suppressor grid and cathode of tube **18** are connected to ground potential as shown at **28***b*.

Pulses representing the information to be registered in the computor are applied to the terminals **26** of the first input winding **14** in code pattern. For example, if the information is in binary digital code, there may be a pulse applied for each digital interval wherein a binary "1" is to be registered, while a pulse will be omitted during each digital interval wherein a binary "0" is to be registered, successive digital intervals being measured by the repetition rate of the actuating ("shift") pulses applied to shift windings **16** (*a* to *d*) under the control of transformer **21** and driver tube **18** during the "on" period of *a* length, as represented in FIG. 3, which is a graph of voltage development across the plate-cathode circuit of driver tube **18**, during the successive stages of each digital interval, stage *a* being marked by a sharp voltage drop from the "B+" level toward the zero point as the tube **18** begins to conduct, then a momentary rise as the tube tends to "flicker," then a more or less steady lower level for the remainder of the shift pulse period *a*. When excitation of grid **19** ceases and the tube **18** stops conducting, there is a sudden rise of voltage as energy applied to circuit **17** is converted into storage charges tending to satisfy the distributed capacitance and inductance values C_1 to C_5 and L_1 to L_5, shown in FIG. 2 and more fully explained hereinafter. This capacitance charging occurs during portion *b* (FIG. 3) of the cycle, and is followed by rapid discharge of the capacitance energy during stage *c*, and by a ringing tendency during stage *d*, the latter being due largely to inductance leakage from the cores **10** to **13**.

The presence of a pulse of positive polarity in winding **14** of the first magnetic core **10** will cause said core to become saturated in what may be regarded as the positive direction of flux flow; hence the next succeeding shift pulse applied to shift winding **16***a* of core **10** (assuming the polarity of all such shift pulses to be such as to produce a condition of negatively directed saturation in the core **10**) will shift the magnetization of the core **10** to its opposite saturation state, whereupon there will be generated in the output winding **15** of core **10** a high amplitude pulse whose charge will be delivered to the first of a series of storage condensers **31**, **32**, **33**, and **34**. The charge thus delivered to condenser **31** will then begin to flow toward the input winding **14** of the next suc-

ceeding core **11**, but the major portion of the charge will remain in the condenser **31** for the duration of the contemporaneous period of shift pulse application (measured in microseconds) the shift pulse occupying, however, only the minor portion *a* of the complete digital interval, as above noted. As the "loaded" condensers **31** to **34**, that is, those condensers holding current charges representative of "1" values, discharge current into the input windings **14** of the adjacent cores to accomplish the "read-in" function above described, the rate of such discharge is abruptly stepped up at the moment of conclusion of shift pulse application. Because of such sudden rise in the current discharge rate of these "1" carrying condensers there is a rapid magnetic flux reversal in those cores receiving these "1" read-in current surges. Such rapid flux reversal will cause current generation not only in the input windings **14** of such cores (to fulfill the "1" registering function) but will also operate to charge the distributed capacitance values inherent in the shift windings **16** of the same cores, as above noted. These capacitance values (indicated at C_2 to C_5 in the equivalent circuit shown in FIG. 2), as well as the capacitance value (C_1 of FIG. 2) inherent in tube **18**, will be absorbed by the line **17** during the continuation of the "read-in" process above referred to. When this "read-in" process (which occupies the *b* portion of the cycle, as shown in FIG. 3) is substantially completed, there will be a relatively rapid discharge by the capacitance units C_1 to C_5 of the current just previously absorbed therein as above described. This rapid current discharge from the capacitance units C_1 to C_5 will coincide with the *c* period (FIG. 3) of sharp voltage drop in line **17** from the maximum voltage point which occurred at the height of the above-described "read-in" process. This capacitance current discharge will be supplemented by concurrent inductance leakage as represented by the inductance values L_1 to L_5 (FIG. 2) inherent in the constituent components of line **17** as indicated.

These discharging currents flowing in stages *c* and *d* (FIG. 3) of the "off" period of the shift pulse will be flowing in a direction opposite to the direction taken by the shift pulse current when the latter is "on." This can be explained as follows:

There is a pre-established relationship between each shift coil **16** (*a* to *d*) and its associated magnetic core such that normal current passing through the shift coil will be in the direction to read a "0" value into the associated core; hence any "0" value-establishing flux change in the core will necessarily induce a correspondingly directed current charge into the shift coil. In other words, capacitance charging of a shift coil and normal feeding of shift pulses to such shift coil will occur in one and the same direction and, conversely, capacitance discharging from a shift coil will tend to occur in the opposite direction. This latter direction, that is, the direction of flow of the capacitance discharging current, is opposite to the "working" or effective direction of flow established by the "B+" potential for the actuating circuit **17**; and as this discharge current is subjected to its greatest reverse voltage motivation during the *c* (FIG. 3) portion of the "off" period, when pulse energy application to the shift windings **16** is undesirable, it interferes with normal functioning of the register. In fact, with high frequency of pulse application or with high density in the informational pattern being transmitted, as above noted, these discharge currents may actually cause "1" values to be registered spuriously, thus introducing erroneous computations.

It has been found that the above-described difficulty can be corrected by interposing, at one or more selected locations along the line of the shift circuit **17**, current flow-interrupting means capable of preventing any effective application of reverse actuating voltage to the individual shift windings **16** for the duration of the "off" periods during which tube **18** is not conducting. As illustrated in FIGS. 1 and 2, such preventive means takes the form of uni-directional impedance elements, such as the crystal diodes **40** to **44**, inclusive, illustrated as located in the several sections into which line **17** may be regarded as being divided by the successive shift windings **16**, these diodes being so poled as to permit free passage of current from the source **39** of positive potential during any period when tube **18** is conducting, while on the other hand operating to open-circuit, and thus de-energize, all shift windings **16** (*a* to *d*) during every period when tube **18** is not conducting. The use of such diodes in these several sections of line **17** operates to convert the sharp voltage drop at *c* (FIG. 3) into a much more gradual and attenuated recession (as indicated by the dash-line alternate curve section "*e*" in FIG. 3) by providing almost complete elimination of current flow in the "off" periods of driver **18**. Substantial correction of the reverse current effects may be obtained by use of the single diode **44**, adjacent terminal **39**; hence the other diodes **40**, **41**, **42**, and **43** may be omitted except where extreme sensitivity characterizes the installation and thus calls for maximum protection at all key points.

FIGS. *4a* and *4b* are voltage patterns of the "read-in" voltage across any one of the condensers **31** to **34** as it develops from cycle to cycle during circulation of a binary pattern of digital values along the successive stages of a register, such as that illustrated in FIG. 1, except that the particular register that would be employed to obtain the voltage patterns illustrated in FIGS. *4a* and *4b* would be a seven-stage register. The digital pattern applied to the register, as shown, is a pattern of six "1" values followed by a single "0" value. FIG. *4a* shows the "0" voltage reading as building up to a value approaching that of the "1" readings, hence coming objectionably close to the point where it might cause a spurious "1" value to be entered in the register. This is a condition frequently occurring in the absence of the protecting diodes **41** to **44** provided by the present invention. FIG. *4b*, on the other hand, shows how the diodes **41** to **44** (or even the single diode **44**) holds the "0" voltage development to a safe low value relative to the much higher "1" values, it being possible to maintain a ratio of at least 5-to-1 between the "1" and "0" voltage readings by the inclusion of the diode control factor.

FIG. 5 shows the invention applied to a magnetic core register having dual shift lines with sequential application of shift pulses thereto. In this FIG. 5 arrangement the magnetic cores **10***a*, **11***a*, **12***a* and **13***a* correspond to the cores **10**, **11**, **12**, and **13**, respectively, of FIG. 1, and the cores **31***a*, **32***a*, **33***a*, and **34***a* correspond (functionally) to the condensers **31**, **32**, **33**, and **34**, respectively, of FIG. 1. Also input, output, and shift windings **14***a*, **15***a*, and **46***a* (or **46***b* as the case may be) correspond to windings **14**, **15**, and **16**, respectively, of FIG. 1.

With this FIG. 5 arrangement, one cycle of operation consists of, first, applying a shift pulse to the principal cores **10***a*, **11***a*, **12***a* and **13***a*, and secondly, to the auxiliary cores **31***a*, **32***a*, **33***a*, and **34***a*. If a "1" value is stored in core **10***a*, the application of a shift pulse thereto (by way of shift line **17***a* and windings **46***a*) will cause transfer of the "1" value to auxiliary core **31***a*. Then, as a shift pulse is applied to line **17***b* and windings **46***b*, the "1" value will move along from core **31***a* to principal core **11***a*, to complete the digit-transferring cycle. These lines **17***a* and **17***b* will be subject to the same reverse current flow tendencies as line **17** of FIG. 1, due to the alternating conditions of conduction and non-conduction through driving tubes **18***a* and **18***b*, respectively, and the effect thereof in producing alternate charging and discharging of the distributed capacitance of lines **17***a* and **17***b* in a manner corresponding to the action occurring in line **17** of FIG. 1, as above explained. The prevention of such reverse flow can be accomplished in

analogous fashion, namely, by inserting diodes 44*a* and 44*b* in the lines 17*a* and 17*b*, respectively, as indicated in FIG. 5, thereby preventing current flow toward source 39 during the "off" periods of tubes 18*a* and 18*b*, respectively.

The diodes 36 and resistors 37 of FIGS. 1 and 5 function as current direction and oscillation controls, respectively, and in serving these purposes they behave as more fully described in copending patent application No. 395,692, filed December 2, 1953, and assigned to the assignee of the subject invention, their counterparts being the diodes 15 and resistors 34 of said copending application.

Alternatively, diodes 41 to 44 of FIG. 1 (or diodes 44*a* and 44*b* of FIG. 5) may be replaced by electronic switching means interrelated with tube 18 (or with tubes 18*a* and 18*b* as the case may be) in such manner as to establish an open circuit in line 17 (or lines 17*a* and 17*b*) for the duration of each "off" period of tube 18 (or tubes 18*a* and 18*b*). Again, the desired result may be achieved by adding a controlled path for draining off to ground or to other suitable potential levels, all undesirable current flowing in line 17 (or lines 17*a* and 17*b*) during such "off" periods.

Many other modifications will be apparent to persons skilled in the art, and it is accordingly desired that this invention be not limited to the particular details of the embodiments illustrated herein, except to the extent defined by the appended claims.

What is claimed is:

1. In a magnetic control system comprising a plurality of magnetic cores and windings interlinking said cores for the transfer of electrical current along conductors interconnecting said windings, means including an actuating circuit including an actuating winding interlinking each of said cores for generating currents in those windings associated with magnetic cores possessing a predetermined direction and magnitude of flux content, means including an electronic device having alternate "on" and "off" periods for controlling generation of such currents periodically, means inherent in the capacitance aspects of said system for establishing a tendency toward current flow in said actuating circuit during "off" periods in a direction opposite to the direction of flow prevailing during said "on" periods, and a rectifier incorporated into said actuating circuit adjacent to each actuating winding to nullify said tendency due to said capacitance.

2. In a magnetic control system comprising a plurality of magnetic cores and a corresponding plurality of coils wound about said cores, shift-producing means including additional windings on each of said cores for controlling generation of current in said first-named coils, said means having inherent therein capacitance to cause unwanted current flow in said last-named windings between the intervals of controlled current generation in said first-named coils, and a rectifier having direct electrical connection with each of said last-named winding for nullifying said unwanted current flow between said intervals.

3. A single core-per-bit magnetic control system comprising a plurality of magnetic cores, input and output circuits interlinking said cores, a third circuit including an actuating winding on each of said cores controlling the operation of said input and output circuits, means for energizing said third circuit at predetermined time intervals, means for producing delayed current flow in said input circuits and thereby inducing voltage into said third circuit, and a plurality of rectifiers forming a part of said third circuit for preventing flow of reverse current in each actuating winding in said third circuit when voltage is induced therein during operation of said delayed current flow-producing means.

4. A magnetic control system comprising a plurality of magnetic cores, input and output circuits interlinking said cores, a single third series-connected core circuit comprising a separate actuating winding on each magnetic core controlling the operation of said input and output circuits, means for supplying current in one direction to said third circuit at predetermined time intervals, means for producing delayed current flow in said input circuits and thereby inducing voltage into said third circuit in a direction opposite to the voltage gradient prevailing in said third circuit during said predetermined time intervals, and a rectifier connected in series with each actuating winding rendering said oppositely directed voltage ineffective to produce current flow.

5. A magnetic control system comprising a magnetic core having input and output windings applied thereto, an actuating circuit including series-connected actuating windings controlling the operation of said input and output windings, means for supplying current in one direction to said actuating circuit at predetermined time intervals, temporary storage means for producing delayed current flow in said input winding and thereby inducing unwanted residual voltage into said actuating circuit during time periods alternating with said predetermined time intervals, and a rectifier connected in series with each actuating winding permitting current flow only in one direction for rendering said residual induced voltage ineffective.

6. In a magnetic control system, a magnetic core having an input winding, means including an actuating circuit having an actuating winding on each core and a current storage circuit for producing delayed current flow in said input winding, a source of energy for said actuating circuit, means for cutting off said source of energy during the period of delayed current flow in said input winding, and a rectifier connected in series with each of said actuating windings for rendering ineffective any voltage induced into said actuating circuit, by way of said magnetic core, during said cut-off period.

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