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3,587,055

SHEET 1 OF 9

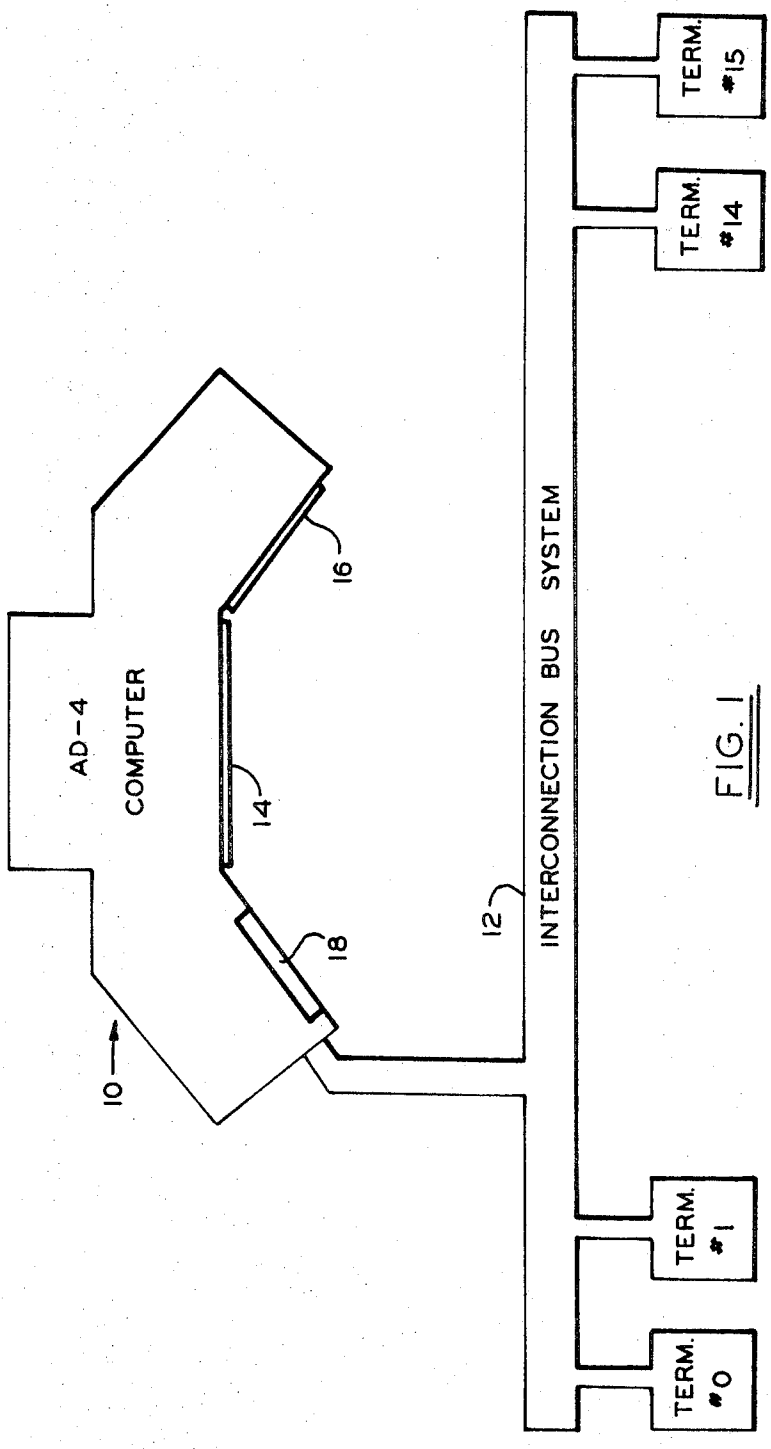



FIG. 1

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# United States Patent

[11] 3,587,055


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[73] Assignee **Reliance Electric Company**


[54] **PLURAL OPERATOR-STATION TIME-SHARED ANALOG COMPUTER APPARATUS**
**23 Claims, 9 Drawing Figs.**


[52] **U.S. Cl.** ..... **340/172.5,** 235/150.5, 235/184
[51] **Int. Cl.** ..... **G06f 3/02,** G06g 7/06
[50] **Field of Search** ..... 235/157, 150.5, 183, 184; 340/172.5



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*Attorney*—Richard G. Stephens



ABSTRACT: A plurality of users situated at a plurality of remote terminal units are enabled to utilize a general-purpose analog computer in a time-sharing arrangement allowing each user to obtain solutions of his own versions of one or several basic problems which are simultaneously patched on the analog computer. An addressing system services the remote terminal units sequentially, and the analog computer runs one or more problem solutions when a given terminal unit is being serviced using coefficient data and problem configuration data established by the user at the given terminal unit. Both analog and digital arrangements for transmitting coefficient data from each terminal unit to the analog computer are illustrated.

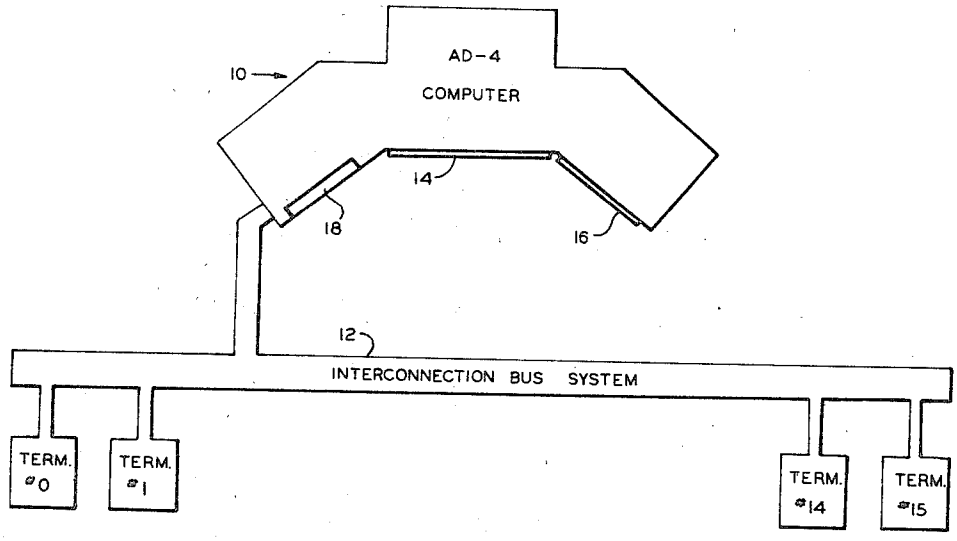
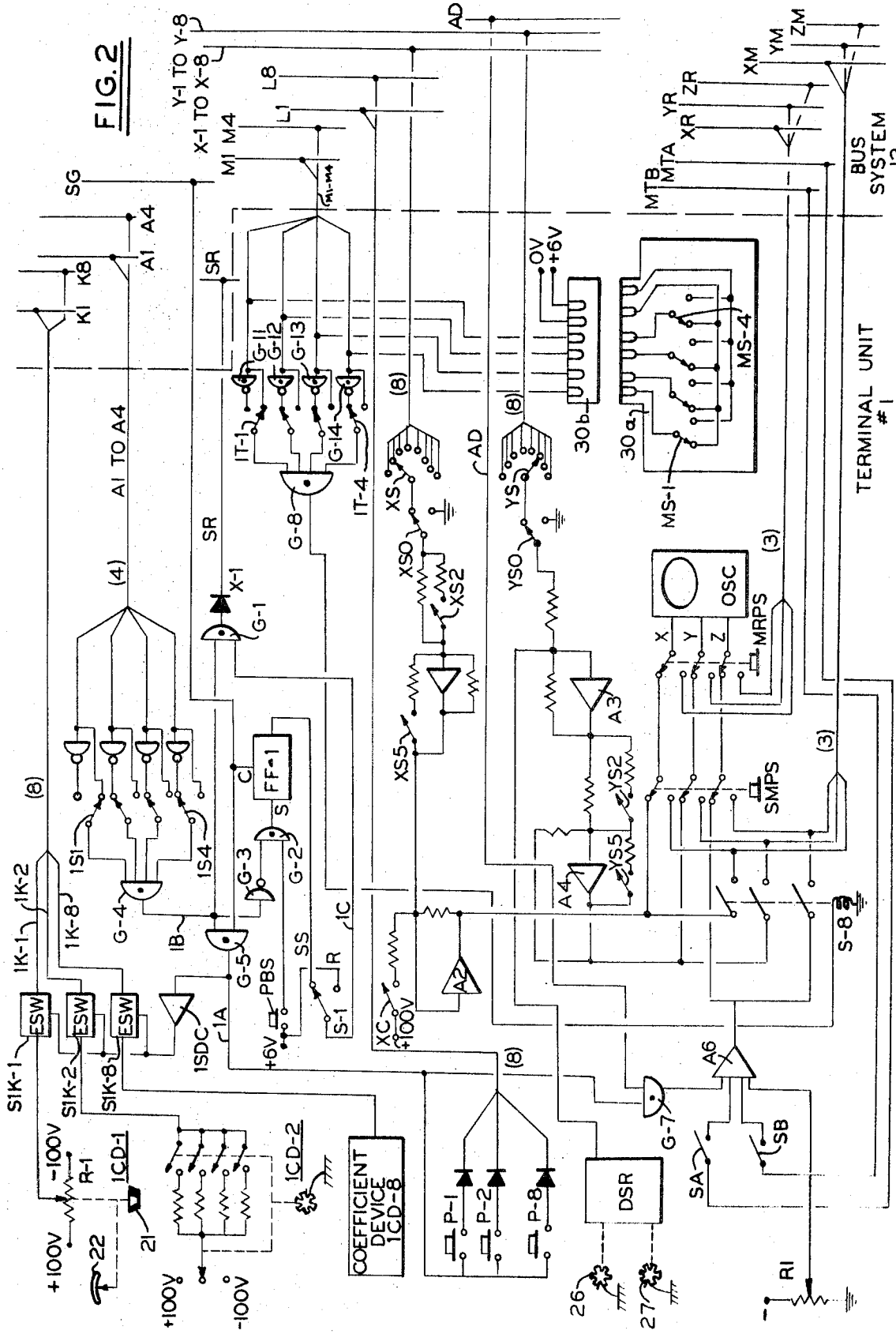



FIG. 2


Y-1 TO Y-8
X-1 TO X-8
AD
L8
L1
M1 M4
SG
A1 A4
K1 K8
SR
A1 TO A4
(4)
(8)
G-11
G-12
G-13
G-14
IT-1
IT-4
G-8
X-1
G-1
XS
XSO
XS2
XS5
YS
YSO
YS2
YS5
A3
A4
A2
A6
OV
+6V
30b
30a
MS-4
MS-1
OSC
MRPS
SMPS
X
Y
Z
(3)
BUS SYSTEM 12
TERMINAL UNIT #1
MTB
MTA
XR
YR
ZR
XM
YM
ZM
S-8
1K-1
1K-2
1K-8
ESW
S1K-1
S1K-2
S1K-8
1S1
1S4
G-4
G-3
G-2
G-5
FF-1
C
S
R
1B
1C
1A
1SDC
PBS
SS
S-1
+6V
XC
+100V
-100V
R-1
1CD-1
1CD-2
21
22
COEFFICIENT DEVICE 1CD-8
P-1
P-2
P-8
DSR
G-7
SA
SB
RI
26
27

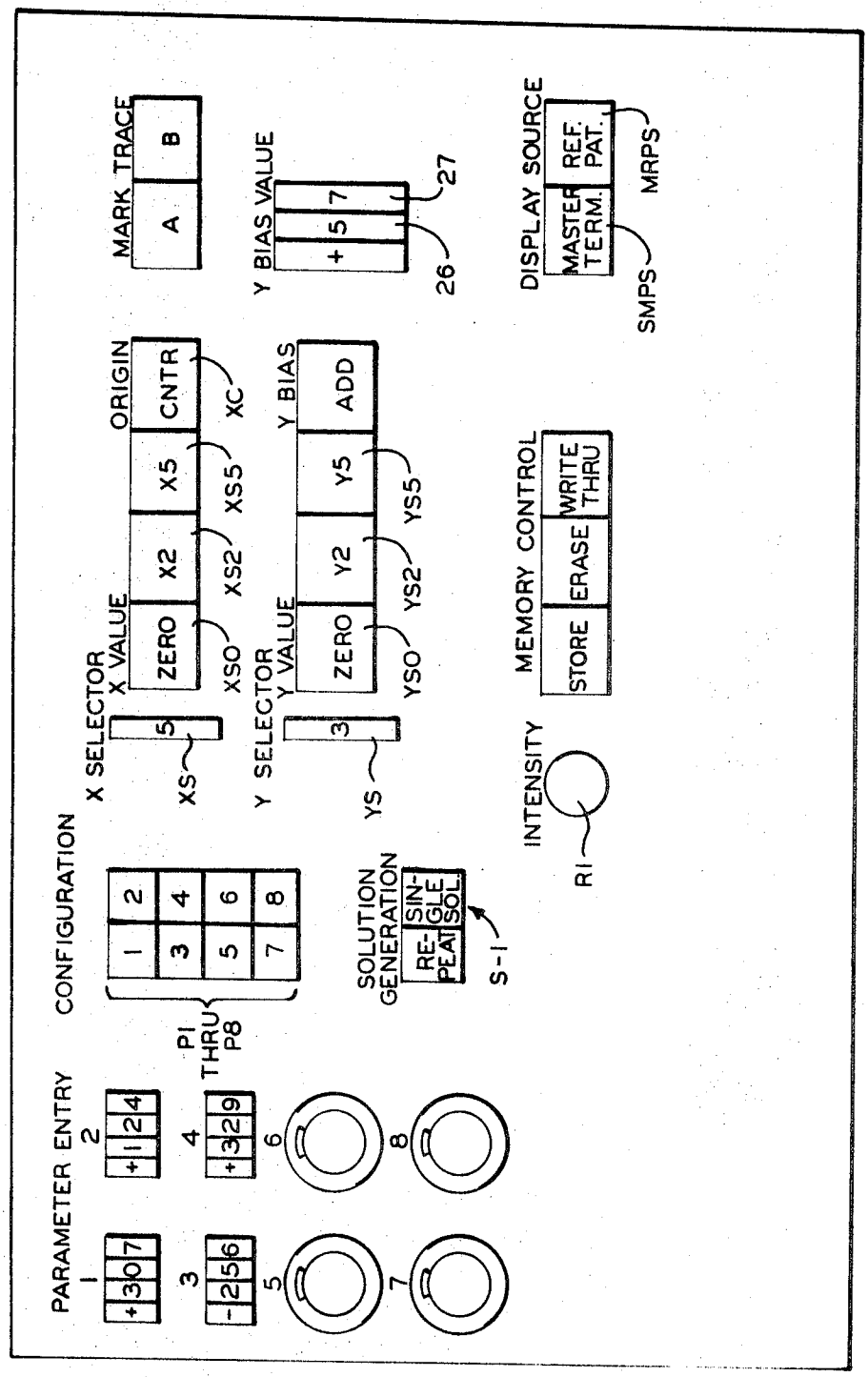

PARAMETER ENTRY
1
+307
2
+1124
3
-2556
4
+3299
5
6
7
8
CONFIGURATION
P1 THRU P8
1
2
3
4
5
6
7
8
SOLUTION GENERATION
RE-PEAT
SIN-GLE SOL
S-1
X SELECTOR
5
XS
X VALUE
ZERO
X2
X5
ORIGIN
CNTR
XSO
XS2
XS5
XC
Y SELECTOR
3
YS
Y VALUE
ZERO
Y2
Y5
Y BIAS
ADD
YSO
YS2
YS5
INTENSITY
RI
MEMORY CONTROL
STORE
ERASE
WRITE THRU
MARK TRACE
A
B
Y BIAS VALUE
+57
26
27
DISPLAY SOURCE
MASTER TERM.
REF. PAT.
SMPS
MRPS

FIG. 2a

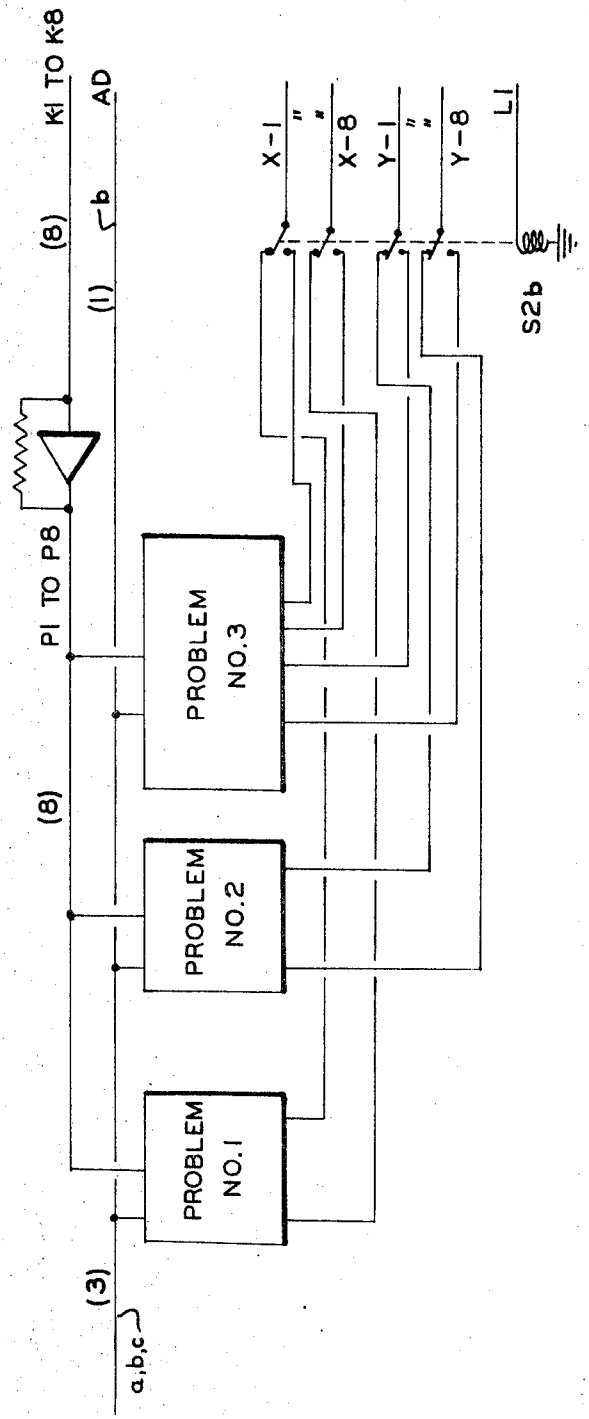
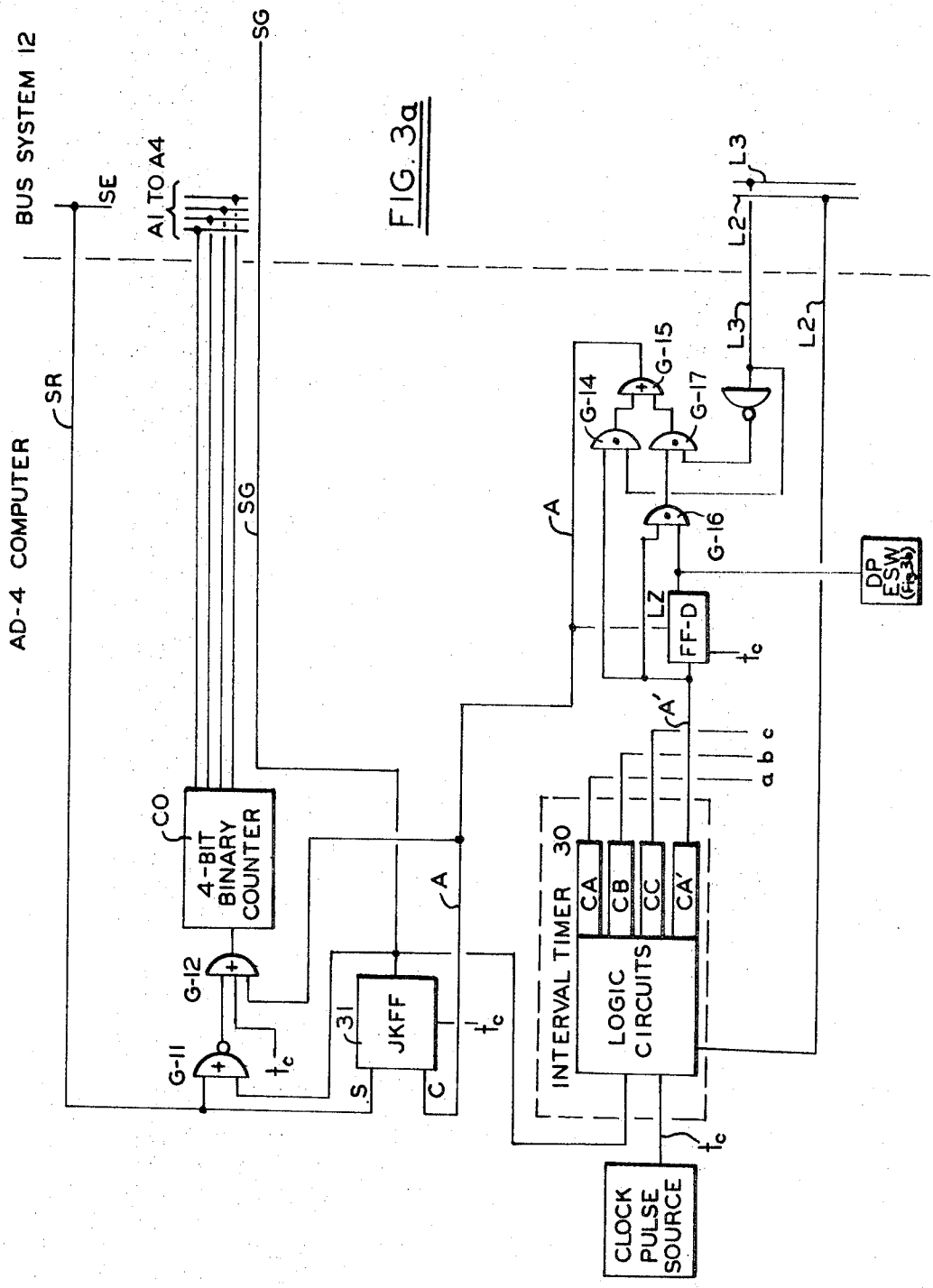

K1 TO K8
AD
(8)
b
(1)
X-1
X-8
Y-1
Y-8
L1
S2b
P1 TO P8
PROBLEM NO.3
PROBLEM NO.2
PROBLEM NO.1
(8)
(3)
a,b,c

FIG. 2b

FIG. 3a


BUS SYSTEM 12
AD-4 COMPUTER
SR
SE
A1 TO A4
SG
SG
L3
L2
L3
L2
G-14
G-15
G-17
G-16
A
LZ
FF-D
$t_c$
DP
ESW
(Fig. 3b)
A'
a b c
CO
4-BIT
BINARY
COUNTER
G-12
G-11
$t_c$
31
JKFF
S
C
A
$t_c$
INTERVAL TIMER 30
CA
CB
CC
CA'
LOGIC
CIRCUITS
$t_c$
CLOCK
PULSE
SOURCE

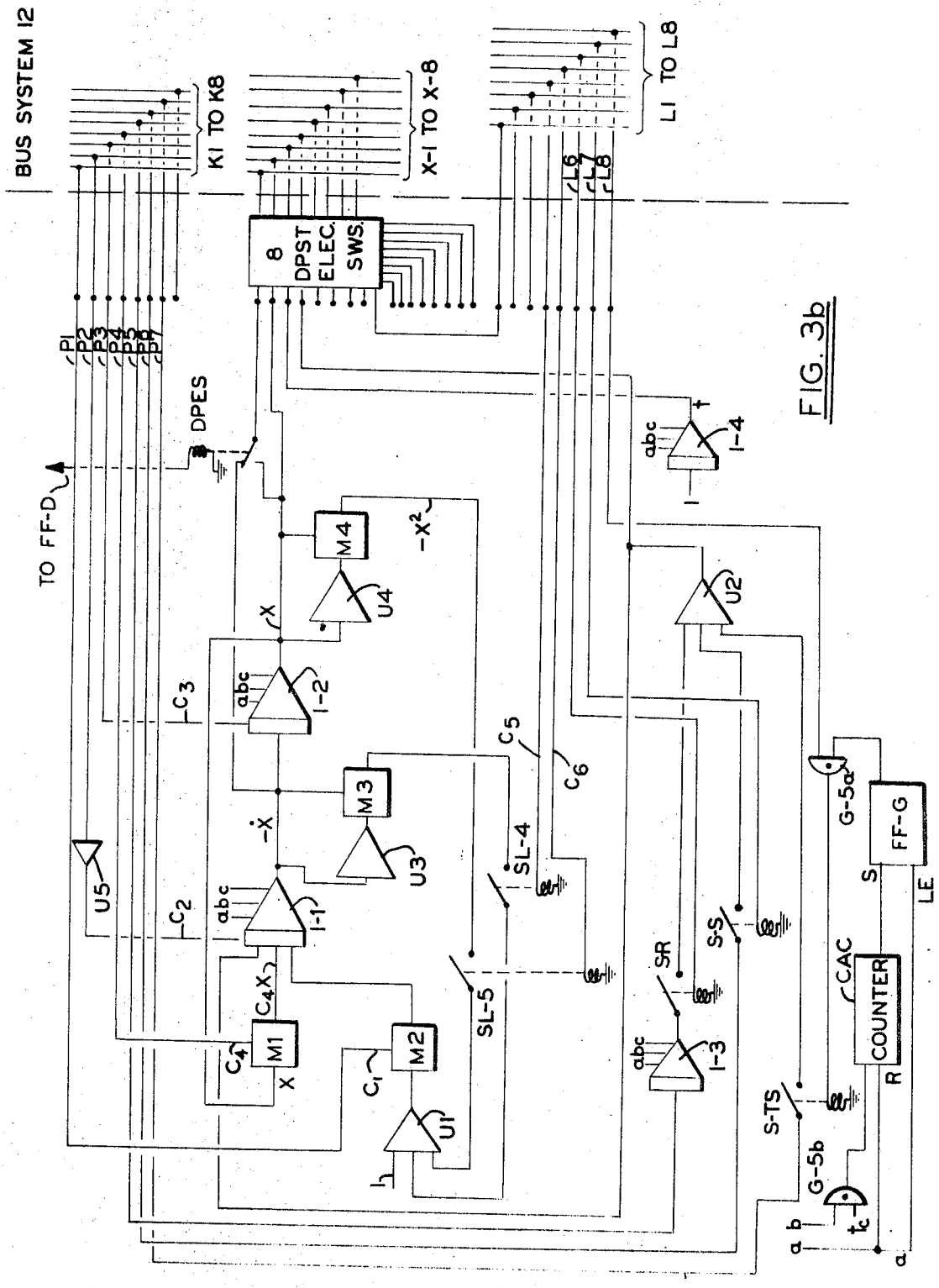

BUS SYSTEM 12
K1 TO K8
X-1 TO X-8
L1 TO L8
8 DPST ELEC. SWS.
P1
P2
P3
P4
P5
P6
P7
DPES
TO FF-D
M4
U4
-X²
X
I-2
C3
M3
U3
-Ẋ
I-1
C2
U5
C4X
M1
C4
X
M2
C1
U1
SL-5
SL-4
C5
C6
I-4
U2
SR
S-S
I-3
S-TS
G-5a
FF-G
S
LE
CAC
COUNTER
R
G-5b
a b
a

FIG. 3b

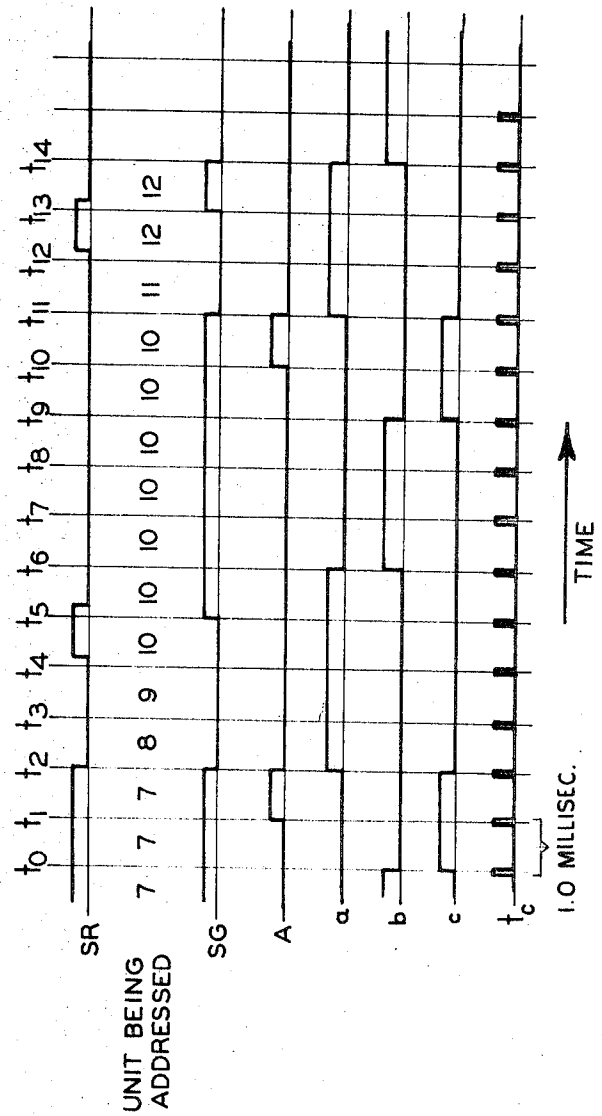

SR
SG
A
a
b
c
$t_c$
UNIT BEING ADDRESSED
7 7 7 8 9 10 10 10 10 10 10 10 11 12 12
$t_0$ $t_1$ $t_2$ $t_3$ $t_4$ $t_5$ $t_6$ $t_7$ $t_8$ $t_9$ $t_{10}$ $t_{11}$ $t_{12}$ $t_{13}$ $t_{14}$
1.0 MILLISEC.
TIME

FIG. 4

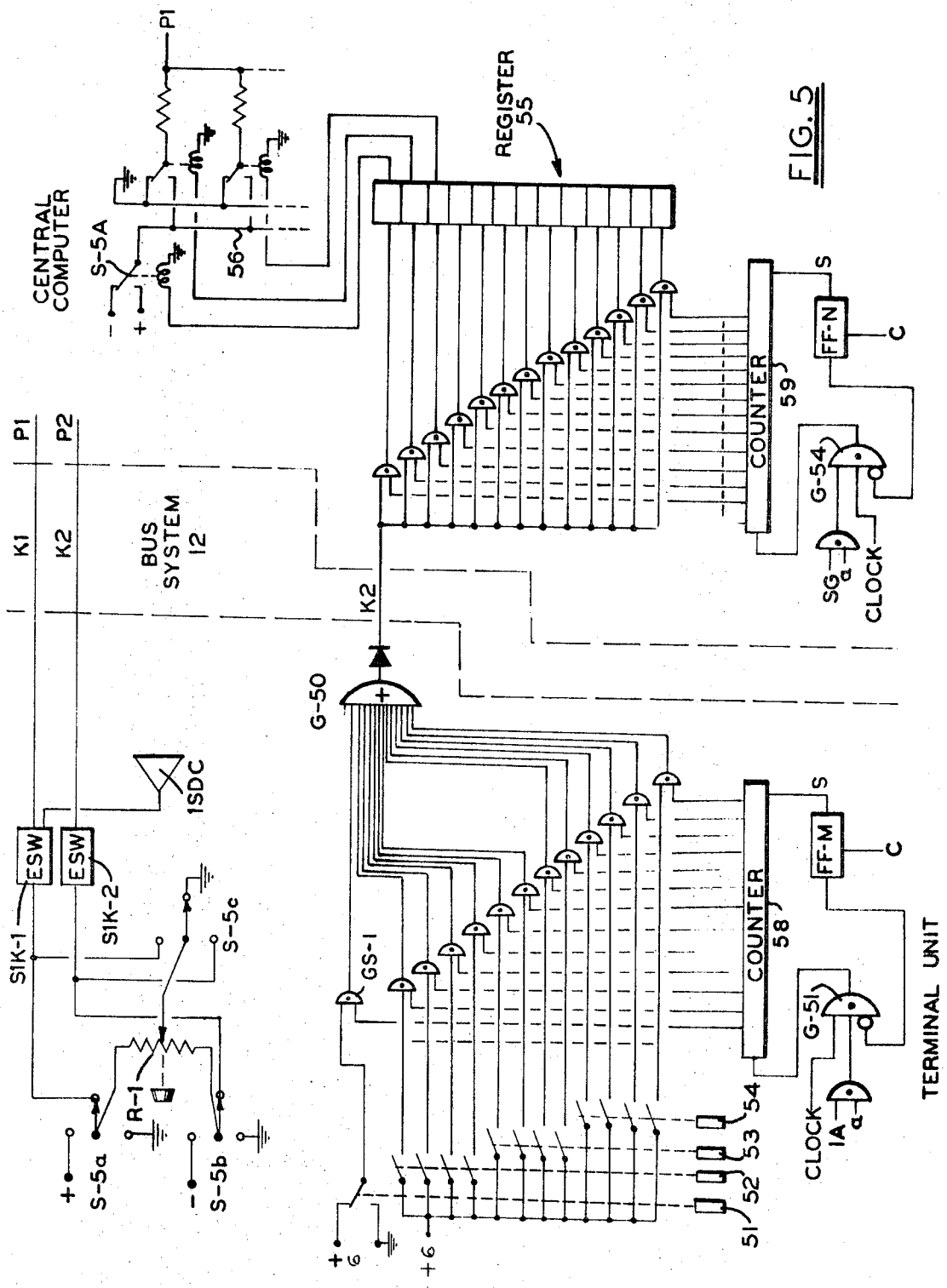

CENTRAL COMPUTER
P1
S-5A
56
REGISTER 55
COUNTER 59
FF-N
S
C
G-54
SG
CLOCK
P1
P2
K1
K2
BUS SYSTEM 12
K2
G-50
1SDC
ESW
ESW
S1K-1
S1K-2
S-5c
R-1
S-5a
S-5b
GS-1
COUNTER 58
FF-M
S
C
G-51
CLOCK
IA
51
52
53
54
TERMINAL UNIT

FIG. 5

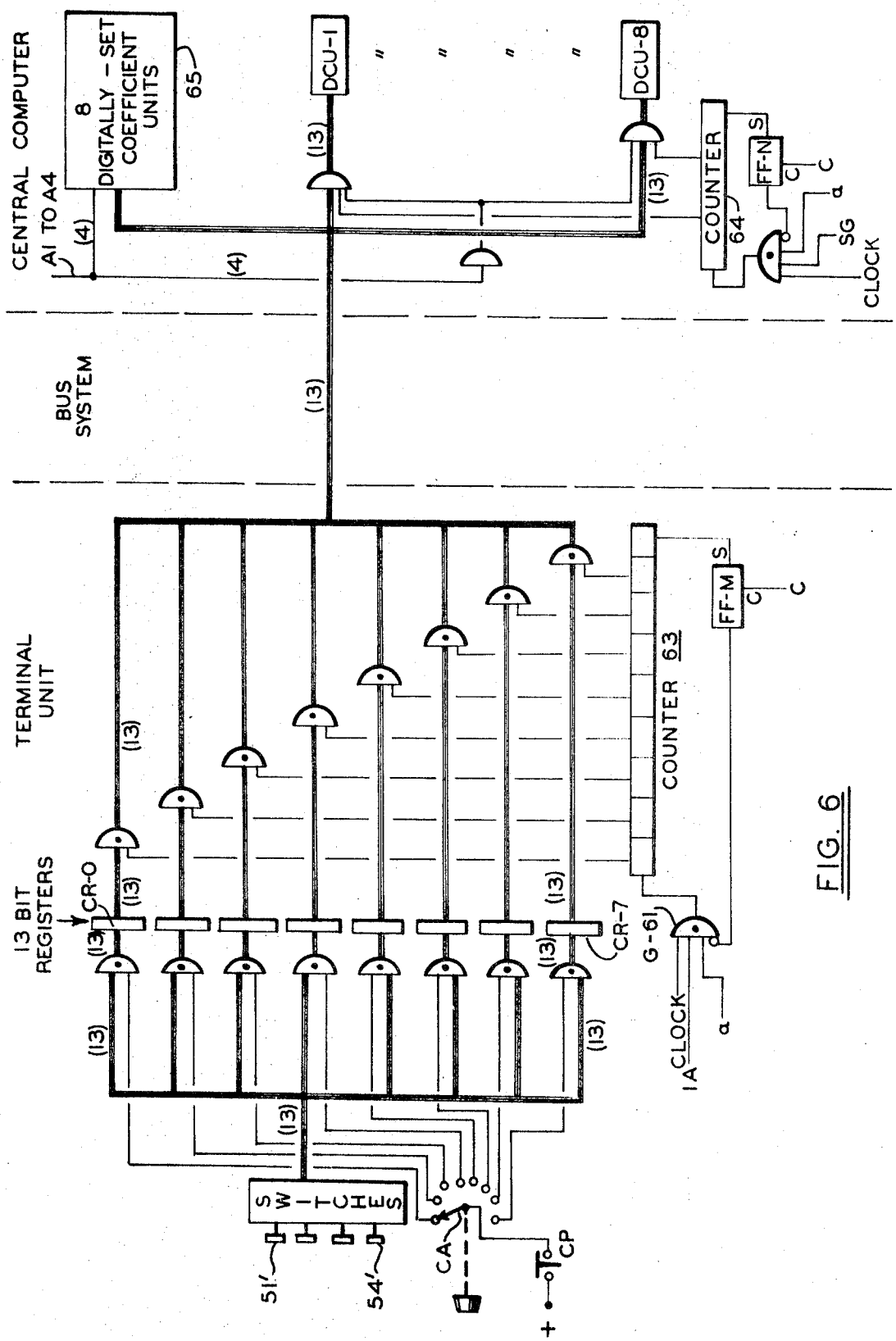

CENTRAL COMPUTER
AI TO A4
(4)
8
DIGITALLY - SET
COEFFICIENT
UNITS
65
DCU-1
DCU-8
(13)
(4)
COUNTER
64
FF-N
S
C
SG
CLOCK
BUS
SYSTEM
TERMINAL
UNIT
13 BIT
REGISTERS
CR-0
CR-7
COUNTER 63
FF-M
G-61
CLOCK
SWITCHES
51'
54'
CA
CP

FIG. 6

# PLURAL OPERATOR-STATION TIME-SHARED ANALOG COMPUTER APPARATUS

The purpose of this invention is to increase the utility of general-purpose analog computers by allowing a plurality of users to solve a plurality of problems simultaneously. Because of the complexity of various systems which one may wish to simulate or complexity of various problems one may wish to solve, it has become common to build large general-purpose computers laving as many as several hundred operation amplifiers. Each problem to be solved or system to be simulated is ordinarily programmed by insertion of patchcords and patchplugs into a removable patchboard.

In most scientific laboratories equipped with large general-purpose analog computers there is a wide variety in the complexity between various problems and systems. Most problems to be solved require the use of some number less than the total complement of amplifiers and other computing elements, and some problems require the use of only a small fraction of the total complement of computing elements. Where a plurality of problems of different sizes need solution, it is common in such laboratories to program each different problem on a different patchboard, and to solve the problems successively by inserting the different pathboards successively into the computer. If a number of the different problems are "small," i.e. require use of only a small fraction of the total complement of computing elements, it will be apparent that a considerable amount of computer time will be wasted. Also, shutting down the computer a number of times to substitute successive patchboards will be seen to be wasteful of computer time. A primary object of the present invention is to provide a computer system incorporating a large or medium-size general-purpose analog computer in which a plurality of problems may be solved substantially simultaneously.

In scientific computation laboratories different problem solutions and system simulations frequently are desired by different individuals who have no concern with the problems of other individuals. It is another object of the invention to provide a computer system of the type described in which a plurality of different users may simultaneously have their respective problems solved on the computer without interfering with each other, with each individual operator receiving output data, such as on a display device, at a respective computer terminal.

It is known in the digital computer art to "time-share" a large general-purpose digital computer between a number of different users, with each user provided with terminal equipment to insert his problem into the computer and to receive output problem solution data from the computer. In such digital systems the central processor usually solves the problems presented to it from the various terminal units in the order in which the problems are presented, although a priority scheduling routine often is superimposed. While such systems are adequate for very many problems which can be solved on a digital computer, the basic concept of such systems is not readily applicable to very many problems which are best solved by analog computation, including, for example, many problems for which oscilloscope output displays are desired. The marked speed advantage of analog computers over digital computers makes time-sharing of an analog computer between a plurality of terminals especially desirable. However, certain basic differences between analog and digital computation have prevented any straightforward application of digital time-sharing techniques to analog computation where a plurality of remote terminal units must be provided. A conventional digital computer is inherently a time-sharing device which performs a number of operations successively, using various of its components, such as its accumulator, for example, over and over again for many of the successive calculations. An analog computer, on the other hand, usually provides a separate computing element for each operation to be performed, and operates all of the computing elements simultaneously. Due to their bivalued nature, the accuracy of



digital signals is much less affected by transmission over lines to and from remote terminals than that of analog signals. Furthermore, analog computers frequently involve many feedback amplifier circuits incorporating electrical devices, such as potentiometers, into which desired input data is set, and it is difficult to extend some such circuits over lengthy lines which interconnect a computer and a remote terminal unit, as the capacitance and inductance of such lines may cause amplifier instability. Furthermore, the analog computer requirement that most or all mathematical operations proceed simultaneously prevents the use of program branching, for example, which greatly facilitates time sharing of a stored program digital computer. Also, analog computer solutions in general must be provided with much greater speed than the solutions of many digital computer problems which are ordinarily time shared.

In a number of engineering mathematics and science courses taught in universities it is highly desirable that a large group of users, such as students, be given the opportunity to simulate various physical systems and to run solutions of various problems on an analog computer. If, as is most often the case, the principal purpose of such instruction is to provide such students with an insight into a particular physical system, such as a servomechanism or a chemical plant process, rather than to provide experience in computer patchboard setup on a particular model of computer, the delays and extra instructor time required to set up and adjust a series of problems on an analog computer become doubly wasteful. Computer time often has been sufficiently costly, and patchboard setup time sufficiently lengthy, that some engineering courses have not attempted to allow individual students to run problems, but have instead merely incorporated demonstrations by an instructor, with a group of students merely watching. Such a system of instruction fails to afford each student the extra insight or understanding of a system which can be readily obtained if a student is given "hands on" control, and allowed to adjust system parameters himself and simultaneously watch the effects of such adjustments on successive solutions. In accordance with one central concept of the present invention, economical apparatus is provided so that a group of students in an engineering course or the like, are all enabled to run solutions simultaneously on different (or the same, if desired) versions of the same basic problem or physical system. For example, a group of students in an automatic control course can all simultaneously operate the computer to simulate a basic servomechanism, with each student enabled to insert a unique set of system parameters and system coefficients into the computer and enabled to view the variation of a number of system parameters as a servomechanism provided with such a unique set of coefficients is simulated. Each student is enabled to work independently of other students, and hence enabled to progress at his own rate, and each student is enabled to make his own adjustments to a large complex system being simulated. Thus it is a primary object of the present invention to provide a computer installation in which a plurality of operators situated at a plurality of remote terminal units may be enabled to utilize an analog computer substantially simultaneously, so that each operator may obtain solutions of a basic problem utilizing coefficients and related data respecting his own version of the basic problem.

It is another object of the invention to provide a computer installation of the type described in which different versions of one or more analog computer problems simultaneously presented to a central analog computer from a plurality of remote terminal units are solved rapidly in succession and repeatedly by the analog computer and problem solutions are appropriately routed to the various terminal units.

It is a very important object of the present invention to provide a computer installation of the type described which is readily applicable to contemporary general-purpose analog computers, and which makes use of many of the computing elements already provided in such computers, and which requires a minimum of additional apparatus, so that provision

of such a computer installation becomes economically attractive.

Other objects of the invention will in part be obvious and will, in part, appear hereinafter.

The invention accordingly comprises the features of construction, combination of elements, and arrangement of parts, which will be exemplified in the constructions hereinafter set forth, and the scope of the invention will be indicated in the claims.

For a fuller understanding of the nature and objects of the invention reference should be had to the following detailed description taken in connection with the accompanying drawings, in which:

FIG. 1 is a block diagram of a computer system according to the invention incorporating a large general-purpose analog computer and a plurality of remote terminal units, each of which may be controlled by a separate student or a separate group of students.

FIG. 2 is a schematic diagram illustrating the apparatus included in each remote terminal unit of FIG. 1, and showing the connection of such apparatus to an interconnection bus system which interconnects each remote terminal unit and the central computer.

FIG. 2*a* shows the face or control panel of one of the remote terminal units.

FIG. 2*b* illustrates in block diagram form how the parameter and coefficient signals on a bus system which interconnects each terminal unit and the central computer may be connected from the bus system to a plurality of problems set up on the central computer.

FIGS. 3*a* and 3*b* illustrate a typical arrangement which may be used at the central computer and the connections of the central computer to the interconnection bus system.

FIG. 4 is a timing diagram useful in illustrating the operation of the apparatus of FIG. 3*a* to enable the computer to successively service the remote terminal units.

FIG. 5 is an electrical schematic diagram illustrating several modifications which may be made to the apparatus of FIGS. 2, 3*a* and 3*b*.

FIG. 6 is a schematic diagram illustrating further modifications may be made to the apparatus of FIGS. 2, 3*a* and 3*b*.

In FIG. 1 a large general purpose analog computer **10** is shown interconnected by an interconnection bus system **12** to a plurality of remote terminal units. The arrangement of FIG. 1 will be described with the assumption that sixteen remote terminal units are connected to bus system **12**, through only the first two and the last two of the terminal units are shown in FIG. 1. In a typical installation the computer **10** and all of the terminal units will be situated in a large room, or in several adjacent rooms, with each terminal unit located atop a separate desk or table or the like. The total length of each conductor in the cabling in bus system **12** between the terminal units and computer **10** may be of the order of several hundred feet, for example. Each terminal unit includes a plurality of controls operable by a student, and a display unit, such as an oscilloscope upon which problem solutions are displayed.

The computer **10** is assumed to be a Model AD–4 computer, a large general-purpose electronic analog computer sold by Applied Dynamics, Inc., of Ann Arbor, Michigan. Such a computer includes a large complement of operational amplifiers, servo set potentiometers, digitally set coefficient units (DCU's), computing capacitors, comparators and various other analog computing elements, all of which may be interconnected to solve a particular problem by appropriately interconnecting them by insertion of patchcords and plugs into analog patchboard **14**. The AD–4 computer also includes a collection of logic elements, such as electronic counters, flip-flops, gates and the like, which may be interconnected to each other, and to analog circuits of a problem by appropriately inserting patchcords and patchplugs into logic patchboard **16**. Patchboards **14** and **16** are removable, and ordinarily a plurality of such patchboards are furnished with a computer so that future problems may be set up on other sets of patchboards while solutions are being run on the problem set up on one set of patchboards. In usual use of the AD–4 computer for analog problems a single operator controls the computer to solve only one problem at a time, using control switches and the like located at a control panel **18**, and observing the results of problem solutions on an output device, such as an oscilloscope or pen recorder (not shown). While the invention will be described in connection with a model AD–4 computer, the invention is readily applicable to a wide variety of other models of general-purpose analog computer, of course. Various lines of bus system **12** terminate at one or more detachable connectors adjacent the AD–4 computer, and lines from mating connectors extend to various patchholes on the analog or logic patchboards. If desired, the various bus lines may be connected permanently to various signal, power and ground terminals at the AD–4 computer.

FIG. 2 illustrates schematically the equipment located at one of the sixteen terminal units, assumed to be terminal unit **01**, and FIG. 2*a* shows the face of the terminal unit. Each terminal is provided with a plurality (assumed to be eight) of coefficient-adjusting devices. In FIG. 2 one of the coefficient devices **1CD–1** is shown for sake of illustration as comprising a precision potentiometer R–1 having its winding excited by reference voltages routed over the bus system form the AD–4 computer) and its wiper arm arranged to be adjusted by control knob **21**, with the setting of the potentiometer indicated by a pointer relative to a scale **22**. Closure of electronic switch **S1K–1** will be seen to apply a voltage commensurate with the potentiometer setting via line **1K–1**, and via line **K1** of the interconnection bus **12**, to the AD–4 computer. A second coefficient-adjusting device **1CD–2** is shown for sake of illustration as comprising a plurality of switches which are selectively closed at different positions of a detented thumb wheel to selectively connect currents to electronic switch **S1K–2**. In actual practice such a device preferably comprises four thumb wheels, with three of the thumb wheels each connected to selectively close four switches to set in one decimal digit of a three decimal digit coefficient, and with the fourth thumb wheel connected to control a switch to determine coefficient sign or polarity. A terminal unit may include all voltage-deriving coefficient devices, or all current-deriving coefficient devices, or any desired mix between the two types. Though inconsistent with FIG. 2, the control panel in FIG. 2*a* assumes for convenience of illustration that the first four coefficient-entry devices are thumb wheel-set switches and that the last four are precision potentiometers, the controls for eight coefficient devices being shown at the left in FIG. 2*b* under the label "Parameter Entry." The last of the eight coefficient devices is shown in FIG. 2 in block form at **1CD–8**. The output lines of all eight coefficient devices are connected through respective electronic switches to coefficient lines **K–1** to **K–8** of the interconnection bus system **12**, and all of the eight switches are driven together by switch driver **1SDC**, so that eight coefficient signals are applied via bus lines **K1** to **K8** to the AD–4 computer when a logic 1 signal appears on line **1A** of terminal **01**. The eight coefficient devices in each of the other **15** terminal units are similarly connected through electronic switches to bus lines **K1** to **K8**. In order that only one terminal unit controls the bus lines **K1** to **K8** at a given time, it is manifestly necessary that the switch driver **1SDC** be energized in only one terminal unit at a time. For certain applications adjustable parameters may be entered into a problem at the computer from a terminal unit in several other ways, as explained below in connection with FIG. 5, including connection of a potentiometer or digital coefficient device to ground, for example, rather than to a reference voltage, so that the terminal presents a resistance, rather than a voltage or current to the computer, or by utilizing two or three of the **K1** to **K8** lines to connect a potentiometer winding and slider to the computer, or by transmitting digital data over various of the **K1** to **K8** lines to set DCU's located in the central computer.

The terminal unit also includes eight configuration-select latching pushbuttons **P1** through **P8**, only three of which are

shown in FIG. 2. Each pushbutton is connected to line 1A, and hence when line 1A is raised in terminal 01, logic signals are applied to logic lines L–1 through L–8 of the bus system 12 in a pattern dependent upon the selective depression of the eight configuration select pushbuttons. Line 1A is raised in only one terminal unit at a time. A diode is shown connected in series with each configuration pushbutton to isolate the pushbutton switches of a given terminal from logic lines L–1 through L–8 when line 1A of the given terminal unit is low.

The terminal also includes a SPDT selector switch S–1 settable to either a "repeat" position or a "single solution" position. When put in a "repeat" position, a logic 1 signal is applied continuously on line 1C to AND gate G–1, so that a logic 1 signal will be applied via diode X–1 to the "service request" line SR of bus system 12 each time line 1B of terminal 01 is raised, and as soon as line 1B is raised. Line 1B will be periodically raised by signals sent over address lines A1 to A4 from the AD–4 computer, as will be explained below. When switch S–2 is put in the "single solution" position, gate G–1 will be enabled to raise the "service request" line only after flip-flop FF–1 has been set. Flip-flop FF–1 is set by depression of momentary pushbutton PBS, which applies a logic signal through AND gate G–2, which also receives an input from logic inverter G–3, preventing momentary pushbutton PBS from setting flip-flop FF–1 during instants when the the terminal unit is being addressed by the AD–4 computer.

The AD–4 computer, as will be shown below, includes a 4-stage binary counter which repeatedly counts through 16 count conditions, applying 16 successive binary numbers to address lines A1 to A4 of the bus system. Each terminal unit includes four switches IS1 to IS4 which may be selectively set so that a given terminal will respond to a respective one of the 16 unit addresses. The connections of switches IS1 to IS4 may be permanently wired in many installations, and no such switches are shown on the control panel in FIG. 2*a*. When an address of 0001 appears on the four address lines, AND gate G–4 in terminal unit 01 will be seen to be enabled, thereby raising line 1B. Thus the addressing of the terminal unit 01 will result in "service request" line SR being raised if line 1C is simultaneously raised, whether continuously from positioning of switch S–1 to its "repeat" position or temporarily from a previous depression of pushbutton PBS to set flip-flop FF–1. Shortly after it receives a service request signal on line SR of bus system 12, the AD–4 computer provides a "service granted" signal on line SG of bus system 12, resetting flip-flop FF–1, and also enabling AND gate G– 5 to raise line 1A. Raising of line 1A connects the signals from the coefficient devices to lines K–1 to K–8, and connects logic signals from the configuration select pushbuttons (P–1 to P–8) to lines L–1 to L–8 of the bus system as explained above. After one problem solution has been run, (or sometimes several problem solutions as will be explained below) the address counter in the AD–4 computer will be stepped to a succeeding address, thereby disabling gates G–4 and G–5 in the terminal which has been controlling the problem and receiving the solution, and thereby disconnecting its coefficient and logic signals from bus lines K1 to K8 and L1 to L8.

The interconnection bus system 12 is shown in FIG. 2 as including sixteen analog lines X–1 to X–8 and Y1 to Y8, all of which are preferably shielded coax lines, and which are used to route output signals from the computer to the terminal units. By the positioning of two 8-pole selector switches XS and YS the operator at a terminal unit is enabled to select one of eight variables from one of lines X1 to X8 to control the X drive of his display oscilloscope OSC, and one of eight variables from one of lines Y1 to Y8 to control the Y drive. Though shown as 8-pole selector switches in FIG. 2, switches XS and YS preferably each comprise a 16-pole selector switch connected to all 16 of lines X1 to X8 and Y1 to Y8, so that the display may be driven by two X or two Y signals, as well as by one X and one Y signal, for a reason which will be made clear below in connection with FIG. 2*b*. By the positioning of switch XSO the X drive to the scope may be made zero, by closure of switch XS2 the X drive may be multiplied by a factor of 2, and by opening switch XS5 the X drive may be multiplied by a factor of 5. By closure of switch XC a constant potential is applied to amplifier A2 to move the origin of the X drive from the left side to the center of the oscilloscope screen. By positioning of switch YSO the Y drive may be made zero, by closure of switch YS2 the Y drive may be multiplied by a factor of 2, and by opening switch YS5 the Y drive may be multiplied by a factor of 5. Also summed together to bias the selected waveform upwardly or downwardly on the scope is an adjustable bias current applied to amplifier A3 from a manually set digital resistance device DSR which is adjusted by detented thumb wheels 26 and 27 and operates in a manner similar to coefficient device CD–2. By adjustment of the thumb wheels 26 and 27 the operator may adjust the trace upwardly and downwardly by measured amounts, and hence measure the heights of various ordinates of interest in the scope display. Amplifier A6 receives an input from an intensity control potentiometer RI and an input from AND gate G–7. Gate G–7 receives an input from line 1A and an input from line AD of bus system 12. Line AD is energized by the AD–4 computer either at the beginning of a problem solution or at a selected time during a problem solution, as will be explained below. In the absence of an output signal from gate G–7, the input to amplifier A6 blanks the oscilloscope. When the terminal unit has been addressed, however, and has sent a service request signal to the AD–4 computer, and has received a service granted signal from the AD–4 computer, and has received an "Activate Display" signal on line AD, the enabling of gate G–7 unblanks the oscilloscope, so that the problem solution is traced on the oscilloscope. Thus it will be seen that although output signals during a given problem run are routed on some or all of bus lines X1 to X8 and Y1 to Y8 to all of the terminal units, only the addressed terminal unit which is controlling the problem for that problem run will ordinarily present the solution on it oscilloscope. (By means of a special master terminal control arrangements, a solution controlled by one terminal unit may be made available to all of the other terminal units, as will be discussed presently.)

The selected X drive and Y drive inputs and a Z axis or intensity input from amplifier A6 are connected to the conventional X, Y and Z input terminals of the oscilloscope via a selector switch system which allows the oscilloscope to receive not only the problem solution associated with the coefficient values and problem configuration set in by that terminal unit, but also a reference pattern, or a master terminal pattern from a different one of the terminal units. With multipole double-throw switches SMPS and MRPS set in the positions shown, the oscilloscope at a given terminal will display the trace selected by selector switches XS and YS, and that trace will represent a problem solution using the coefficients and configuration controlled by the given terminal. If switch MRPS is translated to its opposite position, the scope instead will display a reference pattern, such as a grid, for example, defined by sweep signals applied to lines XR, YR, ZR of bus system 12 by the AD–4 computer. Two further lines MTA and MTB lead from the AD–4 computer over bus system 12 to each terminal unit, to carry time-varying waveforms which may be used at each unit to mark the traces presented on the oscilloscope of the unit. Closure of switch SA applies Z-axis modulation to the oscilloscope so as to divide a trace into a series of dots, for example, while closure of switch SB may divide a trace into a series of dashes, for example, while closure of both switches will mark the trace with a third pattern of dashes formed by dots, and opening of both switches will make the trace continuous or unmarked.

If switch MRPS is in its position shown but switch SMPS is translated to its opposite position, the oscilloscope will instead display the trace or pattern defined by the signals on lines XM, YM and ZM of bus system 12. Means are provided so that the amplifier A2, A4 and A6 output signals from any one of the terminal units may be applied to interconnection bus lines

XM, YM and ZM, but only one such terminal unit can control the bus lines at a given time, of course. A three-pole relay switch S–8 is shown provided to connect the terminal **01** pattern from amplifiers A2, A4 and A6 to lines XM, *m* and ZM when terminal **01** pattern from amplifiers A2, A4 and A6 to lines XM, YM and ZM when terminal **01** is to provide the master pattern. In order to control which terminal unit is acting as the master trace generator, bus system **12** includes four lines M1 to M4 which are selectively energized by insertion of a plug connector at one terminal unit. The plug connector is shown in FIG. **2** as comprising a set of four switches MS–1 to MS–4. Engagement of the female portion **30***a* of the connector with male portion **30***b* will be seen to apply a 4-bit address to bus lines M1 to M4. The signal on lines M1—M4 is decoded at each terminal unit, and if the decoded signal corresponds to the number of the unit, an output signal from gate G–8 of the unit energizes relay S–8 of the unit to connect the X, Y and Z outputs from the unit to the master terminal bus lines XM, YM and ZM. When the master terminal address on lines M1 to M4 corresponds to the terminal number determined by the positions of switches IT–1 to IT–4, outputs from gates of the group G–11 through G–14 provide an input to enable AND gate G–8 and energize relay S–8. The provision of master address lines M1 to M4 and provision of a decoding circuit (such as G–11 through G–14, switches IT–1 and IT–4 and G–8) at each terminal unit allows an instructor located at any one of the terminal units to monitor the solutions being obtained at any one of the other terminal units to monitor the solutions being obtained at any one of the other terminal units, and to make the solutions being obtained by such other one of the terminal units available on bus lines XM, YM, ZM for viewing by all of the students, by selectively operating switches MS–1 to MS–4 so that they correspond to the identification of the other terminal unit, as determined by the positions of switches IT–1 to IT–4 in the other unit. In simplified versions of the invention where remote selection of the master terminal unit is not deemed necessary, address lines M1 to M4 may be eliminated, and the decoding circuit (G–11 to G–14, switches IT–1 to IT–4 and gate G–8) may be eliminated at each terminal, and switch S–8 either may be changed from relay to a latching double-throw switch, preferably key-operated, or energization of relay S–8 may be arranged to occur at a given terminal whenever the instructor's plug **30***a* is plugged in at that terminal, by additional contacts (not shown) on plug **30***a*.

FIG. **2***b* illustrates the connection of bus system **12** to the AD–4 computer in clock diagram form, and a number of sets of lines are shown as single lines accompanied by a numeral in parenthesis to indicate the number in the set. FIG. *b* assumes that three separate basic types of problems are patched on the AD–4 analog patchboard, and that problems Nos. 1 and 2 are "smaller" problems than No. **3**, i.e. that fewer numbers of computing elements are required to solve problems Nos. 1 and 2. All three problems are arranged to run simultaneously on the AD–4 computer, and the computer is controlled in successive "initial condition," "compute" and "hold" modes by three control signals *a*, *b* and *c*, derived by the computer interval timer in a manner described below in connection with FIG.**3***a*. The *b* or "operate" signal is also applied to bus line AD to activate the display at each terminal as described above in connection with FIG. **2**.

The eight coefficient lines of bus system **12** are each connected, through an individual amplifier, if desired, to each of the problems, in a manner which is dictated by the nature of each problem, and one example of which is shown in FIG. **3***b*. A number of terminals from each problem are connected via individual electronic switches (shown as a simple relay S2*b* in FIG. **2***b*) to the **16** signal lines X1 to X8 and Y1 to Y8 of bus system **12** to provide solution outputs to the terminals. Since problem No. **3** is assumed to be a large problem than Nos. **1** and **2**, switches are provided to connect as many as **16** output signals from problem No. **3**, but only half as many from problems Nos. **1** and **2**. If a student at a given terminal wishes to work on problem No. **3**, he depresses his latching configuration pushbutton P1 so that logic line L1 is raised when he is granted service, thereby connecting as many as **16** outputs from problem No. **3** to his terminal. If he wishes instead to work on problem No. **1** or No. **2**, he unlatches his pushbutton P1, so that eight outputs each from problems Nos. **1** and **2** are connected to the **16** signal lines, and the student observes whichever of those outputs he is interested in by adjustment of his XS and YS selector switches (FIG. **2**).

It will be seen that the eight coefficient signals selected by a given terminal are shown arranged to be connected to all three problems when that terminal is granted service, even though the coefficients ordinarily will bear a sensible relationship to only one of the problems, and may cause a number of amplifiers to become overloaded in the other two problems. If desired, one or more logic lines may be utilized to prevent operation of unselected problems. In FIG **2***b* a pair of switches (not shown) controlled by the L1 logic signal may be used to prevent application of the *b* or "operate" signal to problems Nos. **1** and **2**. A further logic line may be used along with the L1 signal to control a further switch (not shown) to determine whether the "operate" signal is applied to problem No. **1** or problem No. **2**.

In FIG. **3***a* an exemplary manner in which a plurality of logic elements and other circuits of the AD–4 computer may be interconnected and connected to various bus lines of bus system **12** is shown. A 4-bit binary counter CO is periodically advanced in a manner to be described, so that its four output lines provide a 4-bit address on lines A1 to A4 to successively address the **16** terminal units, and JK flip-flop **31** raises line SG to indicate that service has been granted when the terminal unit being addressed has requested service by raising bus line SR. The system is shown using synchronous logic which is clocked at a 1.0 kilohertz rate by 300 nanosecond clock pulses shown at $t_c$ in FIG. **4** and shown as inputs to the various logic elements in FIG. **3***a*. The output transitions of the logic elements at the trailing edges of the clock pulses, shown at times $t_0$ through $t_{14}$ in FIG. **4**, depend upon the inputs which existed to the logic elements at the beginning of the clock pulses. The AD–4 computer, like most general-purpose computers, includes an interval timer **30** which repeatedly cycles through three successive states for timed intervals which may individually be adjusted by thumb wheels (not shown). During each of the three states of interval timer **30**, a respective one of its output lines *a*, *b* and *c* is raised. In most applications, the three states *a*, *b* and *c* of the interval timer correspond to the periods during which the integrators in a problem are in their "initial condition" or "reset," "operate" or "compute," and "hold" modes, respectively. The interval timer in the AD–4 computer also provides an end signal A a predetermined time before the end of the "hold" period, as shown in the timing diagram of FIG. **4**. The interval timer in the AD–4 computer basically comprises some logic circuits and a plurality of counters responsive to pulses from a clock pulse source. When the interval timer is enabled by a logic **1** on its input line, pulses are applied to advance a first counter CA through a predetermined number of counts, and while counter CA is counting output line *a* is raised. The timing diagram in FIG. **4** assumes that the frequency of the oscillator and the number of stages in counter CA are selected so that a complete counting cycle of counter CA takes one millisecond, so that line *a* is raised to provide a 1.0 millisecond "reset" or "initial condition" period. At the end of the CA counting cycle, counter CA halts and counter CB counts, raising line *b* as long as counter CB is counting, and a complete counting cycle of counter CB is assumed to take 3 milliseconds, so that line *b* is raised to provide a 3.0 millisecond "compute" period. At the end of the CB counting cycle, counter CC begins counting and counter CB halts, and line *c* is raised as long as counter CC continues to count, for a period assumed to be 2.0 milliseconds, so that line *c* is raised to provide a 2.0 millisecond "hold" period. During a terminal portion (shown as 1.0 millisecond) of the "hold" period, counter CA′ counts, and line A′ is raised. At the end of the " hold" period counters CC and CA′ halt and counter

CA begins again through a similar initial condition period, and the interval timer cycles successively through its three periods. If the timer input line becomes low during any phase of the interval timer cycle, the counter within the interval timer which is then counting is caused to halt, at whatever count it has reached, and whatever timer output line (or lines) were high remain high until the timer is enabled again and the counter can finish its cycle. In general, the raising of the A′ line of the interval timer during the terminal portion of the "hold" period operates to cause counter CO to be advanced at the end of the "hold" period so that a succeeding terminal unit will be addressed. However, while interval timer **30** raises line A′ during the last half of each "hold" period, gating circuits may be provided as shown to allow certain A′ signals to be ignored, or not applied to advance counter CO, with the result that the computer will grant service again to the same terminal throughout a succeeding set of "IC," "operate" and "hold" periods, and during the succeeding "operate" period the terminal granted service can receive and display a different solution. If the student at the terminal granted service has depressed configuration control button P–3 so that logic line L–3 is energized at the computer, each A′ signal will be seen to be applied via AND gate G–14 and OR gate G–15 to raise line A (eventually to advance counter CO, as will be explained). On the other hand, if logic line L–3 is low, gate G–14 is disabled, and an A′ signal raises line A (G–16 and G–17 and OR gate G–15″) only if flip-flop FF–D is set. The occurrence of an A signal preparatory to advancement of counter CO to a new address applies an input to the "load to zero" input line of flip-flop FF–D, so that that flip-flop is cleared. With logic line L–3 low and flip-flop FF–D cleared, the end of the first A′ signal occurring after the terminal has been addressed will cause FF–D to be set, and then the second A′ signal will be applied via gates G–16, G–17, G–15 to raise line A, so that two problem solutions will be obtained by that terminal before the succeeding terminal is addressed. It will be apparent that by minor changes in the logic circuits between lines A′ and A, counter CO may be made to advance only after three or more "hold" periods have occurred, if desired. The output of flip-flop FF–D is applied to control a double-pole electronic switch circuit DPES, to connect different problem solution signals to one of the signal lines X1 during the two successive solution times accorded to the terminal. The connections of switch DPES to the signal lines are shown in FIG. 3*b*. Thus by control of logic line L–3 by means of his P–3 pushbutton, a student at a terminal may obtain two successive problem runs each time his unit is granted service, with the first problem run providing a display of one problem variable such as X, and with the second problem run providing a display of another problem variable such as its time derivative $\dot{X}$, so that both X and $\dot{X}$ appear as traces on the scope at the terminal unit.

Assume that terminal unit **07** is requesting service in its "repeat" mode (i.e. switch S–1, see FIG. 2, in terminal unit **07** is in its "repeat" position), so that it continuously energizes bus line SR, and that terminal unit **07** is being serviced. Such conditions are assumed to exist prior to time $t_0$ in FIG. 4. During such time counter CO will be in its binary 0111 or decimal "7" state and addressing unit **07** over address lines A1 to A4. Assume that pushbutton P–3 in terminal **07** has been depressed, so that line L–3 is high, and terminal unit **07** is requesting only one problem solution for each time it is granted service. The A signal provided by timer **30** during the last portion of the hold or *c* period causes the counter to advance to its 1000 or "8" state at time $t_2$ (FIG. 4), the end of the hold period. The A signal from timer **30** is connected to the counter CO input line through OR gate G–12, and also connected to the clear input line of JK flip-flop 31. Occurrence of the A signal also clears JK flip-flop **31** at the end of the *c* period, even though the SR input to its set input line is then also high, since a JK type flip-flop switches to an opposite state when clocked if both its set and clear input lines are high. With flip-flop **31** cleared and line SG low, interval timer **30** is not enabled, and it remains in its *a* or reset state until a service request sets flip-flop **31**.

Assuming that terminal unit **08** is not requesting service, the SR line at the computer will fall shortly after time $t_2$ when terminal **08** is addressed, and both lines SR and SG will thereafter be low when counter CO is in its "8" state, thereby providing a logic 1 output from NOR gate G–11, so that a pulse will be applied through NOR gate G–11 and OR gate G–12 at time $t_3$ to increment counter CO to the "9" state. Assuming that terminal **09** is not requesting service, the next clock pulse at time $t_4$ then will pass through gates G–11 and G–12 to advance counter CO to its "10" state. Terminal **010** is assumed to be requesting service, so that advancement of the counter to the "10" state to address terminal **010** raises line SR, with some delay as the address propagates out to terminal **010** and the Sr signal from terminal **010** propagates back to the computer. With line SR high prior to time $t_5$, JK flip-flop **31** will be seen to become set at time $t_5$. The setting of flip-flop **31** prevents further output pulses from G–12 by disabling NOR gate G–11, and hence counter CO then will remain in its "10" state while terminal unit "10" is serviced. The setting of flip-flop **31** also enables interval timer **30**, which then progresses through its *a* state and through its *b* and *c* states. FIG. **4** assumes that terminal unit **010** was requesting "single solution" service. The setting of flip-flop **31** at time $t_5$ propagates out to clear flip-flop FF–1 in terminal **010**, shortly thereafter lowering line SR at the computer, as shown in FIG. 4. A JK type flip-flop does not change its output at the clock time if both its set and clear inputs are low, and hence JK flip-flop **31** does not respond to the lowering of SR, which occurs shortly after time $t_5$, and interval timer **30** remains enabled, raising its *b* line at time $t_6$ to provide a 3 millisecond "compute" or "operate" period, raising its *c* line at time $t_9$ to provide a 2 millisecond "hold" period, and also providing the A signal during the last portion of the "hold" period. FIG. 4 assumes that terminal unit **011** is not requesting service but that terminal **012** is requesting service in its repeat mode. The A signal from interval timer **30** clears flip-flop **31** at time $t_{11}$ and applies a logic 1 signal to OR gate G–12, so that a clock pulse advances counter CO to its "11" state at time $t_{11}$, and a further clock pulse advances the counter to its "12" state at time **12**. After the "12" address propagates out to terminal **12** the SR signal propagates back to the computer, raising line SR at the computer, thereby disabling gate G–11 to hold the counter in its **12** state, and setting flip-flop **31** to run interval timer **30** and provides solution period for terminal **012** in the same manner as described above for terminal **07**. Utilizing the synchronous logic system shown, with the logic elements clocked at a 1 kilohertz rate, it will be seen that transmission delays between the computer and the terminal units may approach as much as 1 millisecond without affecting system operation.

Logic line L2 is shown connected to interval timer **30**. Depression of pushbutton PB–2 at a terminal unit raises logic line L2 when that unit is granted device, and whether or not logic line L2 is raised determines the rate at which the counters within the interval timer are advanced. A high L2 signal may cause pulses to be supplied at a 1.0 **kilohertz rate, for example, which allows solutions to be traced conveniently on an oscilloscope, while a low L2 signal may provide a clock frequency of one hertz, for example, which is convenient for recording solutions with a pen recorder. The clock inputs to the logic elements are synchronized, of course, and preferably derived from the same pulse generator as is used to cycle the interval timer counters. It should be emphasized that the details of the control logic shown patched at the AD–4 logic patchboard in FIG.** 3*a* are exemplary only. Various other logic lines (of the group L1 to L8) may be used, and further similar logic lines (not shown) provided to be controlled similarly by further pushbuttons, to provide varied operation, so as to run the interval timer at a variety of different rates, for example, or to cause the system to skip the servicing of terminal units presenting certain problem configurations to the computer, for example. When a terminal requests a long solution period by raising its L2 line, its address may be stored, and then line SR at the computer may be forced down during a number of successive occur-

rences of that address, so that service requests by that terminal are ignored for a desired time, so that that terminal unit cannot "hog" too much computer time. While FIGS. 3*a*, 3*b* and 4 illustrate the use of an interval timer arrangement which provides three modes "Reset," "Compute" and "Hold," a number of applications of the invention may desirably include timing arrangements having different numbers of modes. Many problems may be solved utilizing only the "Reset" and "Compute" modes, for example, and in such applications no *c* signal period need be provided in the interval timer sequence, and the A signal shown in FIG. 4 may be arranged to occur during the last portion of the "Compuet" or "Operate" mode.

FIG. 3*b* illustrates a typical problem of three basic problems which may be patched simultaneously on the computer with the operator at each terminal unit enabled to enter coefficient and configuration data respecting his own version of any one of the three basic problems, and to receive solutions therefor.

The problem shown patched in FIG. 3*b* is that of a basic second-order system application to a variety of physical systems, and the equation which the system is connected to solve may be written as follows: $\ddot{X}=C_1(1-C_5\dot{X}^2-C_6X^2)+C_4X+f(t)$ wherein X, $\dot{X}$, and $\ddot{X}$ may represent position, velocity and acceleration of a body, for example, $C_1$, $C_4$, $C_5$ and $C_6$ are coefficients relating those variables, and $f(t)$ is a function of time. The interconnection of the computing elements to solve the exemplary equation is straightforward and will be readily understood by those skilled in the art. Integrators I–1 to I–4 are conventional integrators, and each is connected to be mode-controlled by lines *a*, *b* and *c* from the interval timer 30 (FIG. 3*a*). U1 and U2 are conventional summing amplifiers and U3 to U5 are conventional inverting amplifiers. The initial conditions of integrators I–1 and I–2 are determined by coefficients $C_2$ and $C_3$ which are connected to the integrators over bus lines K–2 and K–3 and patch cords P2 and P3 at the computer. One notable difference between the system as shown patched in FIG. 3*b* and the usual manner in which such an equation would ordinarily be patched on the computer if no remote terminal units were provided is the use of an electronic multiplier wherever an amplifier output must be multiplied by a coefficient which is to be adjustable or selectable at the terminal units. Such multiplication can be done in ordinary computation at the computer using a resistance (potentiometer) excited by the amplifier output and adjusted in accordance with the desired coefficient. However, the coefficient lines leading from each terminal unit to the central computer, such as lines 1K–1 to 1K–8 (in FIG. 2), preferably transmit either voltages or currents to represent the coefficients rather than presenting adjustable resistances or conductances to the central computer in order to represent coefficients, particularly where the problem would require such an adjustable resistance to be located in a feedback loop, since the length of the lines between the terminal units and the central computer sometimes make it difficult to avoid instability. In the modified system shown in FIG. 5 a digitally set DCU located in the central computer is set by pulses transmitted from a terminal unit, and by using such a technique various electronic multipliers, such as M1 and M2 in FIG. 3*b*, may be replaced by such DCU's. In FIG. 3*b* coefficient $C_1$ is determined by the voltage applied to electronic multiplier M2 by a potentiometer in a terminal unit (such as potentiometer R–1 in FIG. 2), with the voltage connected M2 via line 1K–1 in FIG. 2, and via bus line K1 to line P1 at the central computer patchboard, and thence by a patchcord to multiplier M2. In FIG. 2 coefficient device 1CD–2 for generating coefficient C2 is shown as comprising a current-generating device which applies a current via line 1K–2 and bus line K2 to line P2 at the central computer, and amplifier U5 is shown connected to convert that current to a voltage which determines the initial condition of integrator I–1. The third coefficient device of FIG. 2 is assumed to be a voltage type which supplies the initial condition C3 of integrator I–2 via lines 1K–3, K3 and P3, and the fourth coefficient device is assumed to apply a voltage via lines 1K–4, K4 and P4 to multiplier M1 to insert coefficient $C_4$ into the problem. Two coefficients ($C_5$ and $C_6$) are shown not made continuously adjustable but instead controlled to be either 1 or 0 by logic lines L4 and L5, which are controlled at each terminal unit by operation of latching pushbuttons P–4 and P–5. Thus by pushbutton control a terminal operator may selectively insert and remove various equation terms, and receive problem solutions which portray system operation either with or without the physical relationships which the various terms represent. The fifth coefficient device in terminal 01 is assumed to apply a selected magnitude current via lines 1K–5, K–5 and P5 to integrator I–3, to determine the slope of a ramp when a solution using a ramp forcing function is desired. The output from integrator I–3 is connected to switch S–R. The sixth coefficient device in terminal 01 is assumed to apply a selected voltage via lines 1K–6, K6 AND P6 to switch S–S at the computer to determine the size of an initial step function to be applied to the problem, and the seventh coefficient device to apply a selected voltage via lines IK–7, K7 and P7 to switch S–TS at the computer, to determine the size of a delayed step function to be applied to the problem. Switches S–R, S–S and S–TS are all connected to apply inputs to summing amplifier U2, the output of which constitutes the forcing function $f(t)$ for the problem.

Whether the forcing function is a ramp, an initial step, a step occurring after a timed interval, or some combination of the three, is shown determined by operation of configuration control pushbuttons P–6, P–7 and P–8 at the terminal unit. A logic 1 on line L6 closes switch S–R so that a ramp is applied to U–2 at the beginning of the "operate" period as integrator I–3 begins to integrate, and a logic 1 on line L7 closes switch S–S so that a step voltage is applied to U2 throughout the problem solution. A logic 1 on line L8 applies one input to AND gate G–5*a*. The *a* signal from the interval timer resets counter CAC to a zero count and clears flip-flop FF–G during the reset period, and then clock pulses advance counter CAC during the "operate" period as timer signal *b* enables AND gate G–5*b*. When counter CAC reaches a predetermined count, it sets flip-flop FF–G and enables AND gate G–5*a* closing switch S–TS, thereby applying a step voltage to amplifier U2 at a predetermined time during the "operate" period. It will be apparent that a variety of different forcing functions, such as sine waves, square waves, etc., may be generated instead at the computer and selectively applied to the problem under control of the configuration pushbuttons located at the terminal units.

Signal lines X–1 to X–8 of bus system 12 connect to 8 patchholes of the AD–4 computer, and four selected outputs from the problem (X, $\dot{X}$, $f(t)$ and $t$) are shown connected to lines X–1 to X–4. Four further problem variables could be patched to lines X–5 to X–8, of course, if desired. Double-pole electronic switch DPES is shown connected to both the X and $\dot{X}$ outputs, so that those two quantities may be traced one immediately after the other when the terminal is requesting a double solution, as described above in connection with logic line L3 and FIG. 3*a*. If desired, a plurality of further switches (not shown) similar to DPES controlled by the output of flip-flop FF–D may be utilized to change one or more coefficients or configuration signals between the two successive solutions, so that the coefficient signal received on bus line K4 provides the $C_4$ coefficient during the first solution and the coefficient signal received on bus line K8 provides the $C_4$ coefficient during the second solution, for example.

FIG. 5 illustrates several modifications which may be made at the terminal units in order to present coefficient data from the terminal units to the computer in different manners. The first coefficient device is again illustrated as comprising a potentiometer R–1, but three 3-pole selector switches S–5*a*, S–5*b* and S–5*c* are provided at the terminal unit so that the potentiometer not only may be excited by plus and minus reference voltages, but instead connected between switch S1K–1 and ground, or instead connected between switch S1K–2 and ground, to provide a desired resistance to ground on line P1 or P2 at the computer when the terminal is granted

service, and further it will be seen that a selected resistance may be connected between switches S1K–1 and SIK–2, to provide a selected resistance between lines P1 and P2 at the computer.

The lower portion of FIG. 5 illustrates an arrangement for transmitting coefficient data from each terminal unit to the computer in digital form, and while data representing a given coefficient may be transmitted in parallel form, a serial form is preferred for the apparatus shown in FIG. 5 in order to reduce the number of wires required in bus system 12. Four thumb wheels 51—54 are used to select the sign and three decimal digits of a coefficient. The switch operated by sign thumb wheel 51 applies a logic 1 signal to AND gate GS–1 if the sign of the coefficient is positive, and a logic 0 if the sign is negative. Thumb wheel 52 controls four switches to apply logic signals to four AND gates in accordance with a binary-coded representation of the most significant decimal digit of the coefficient, and thumb wheels 53 and 54 similarly each control four switches to apply logic signals to four AND gates in accordance with the binary code of a lesser decimal digit of the coefficient. Thus logic signals indicating the sign and three decimal digits of the coefficient are connected to 13 AND gates as shown. The output signals from the AND gates are all applied to OR gate G–50. A ring counter 58 having 14 stages is shown connected to enable the AND gates successively to apply the thumb wheel-derived signals successively to OR gate G–50, and over bus line K2 to the central computer. In the system shown in FIG. 5, unlike that of FIG. 2, the "initial condition" and "hold" signals *a* and *c* are routed over two further lines of bus system 12 between the central computer and each terminal unit. During each "hold" period, the *c* input from the interval timer clears flip-flop FF–M, removing the inhibit input from AND gate G–51. When the terminal is addressed and receives service, so that its line 1A is raised, as explained above in connection with FIG. 2, gate G–51 is enabled, so that clock pulses, at approximately a 20 kilohertz rate or higher are applied to advance ring counter 58, which previously has been stopped at its "14" count. As counter 58 advances to its "1" count, its "2" count, and to successive counts, successive ones of the 13 AND gates are enabled, thereby providing a 13-digit serial pulse train on coefficient line K2 to indicate the coefficient sign and magnitude. When counter 58 reaches its "14" count, flip-flop FF–M is set, thereby disabling AND gate G–51 and stopping counter 58.

Back at the computer, flip-flop FF–N will be cleared by the preceding "hold" or *c* signal from the interval timer, so that upon occurrence of the service granted signal and the start of the "reset" period AND gate G–54 will be enabled, and clock pulses will be applied at the same 20 kilohertz rate to counter 59. As counter 59 is advanced to its "1" count and succeeding counts, the sign bit and data bits of the serial pulse train are routed by means of the 13 AND gates shown to successive stages of a 13-bit register 55. When counter 59 reaches its last count, it sets flip-flop FF–N and disables gate G–54.

The first stage of register 55 controls reed switch S–5*s* to determine the polarity of the voltage applied to line 56 in accordance with the transmitted sign bit. Each of the other stages of register 55 control a respective magnetic reed switch to determine whether or not the reference voltage on line 56 is applied to line P1 through a respective weighting resistor, the connections for only two of the other stages being shown in FIG. 5. The sizes of the weighting resistors are selected in accordance with the BCD code shown, and hence the total current applied to line P1 represents the value of the coefficient selected by thumb wheels 51—54. It will be apparent that the counter 58 output lines may connect at each terminal unit to similar sets of 13 AND gates to simultaneously transmit pulse trains representing the other coefficients to the central computer, and that counter 59 at the central computer can simultaneously drive further sets of 13 AND gates to store such pulse trains in respective registers and generate further coefficient currents. Thus each time a terminal is granted service, its coefficient data is transmitted to the central computer, at the start of the "initial condition" mode, and successive terminal units change the coefficient data as they are successively granted service. The digital transmission scheme shown in FIG. 5 may be used to transmit logic signals instead of or in addition to magnitude signals. For example, if eight of the 13 AND gates strobed by counter 58 were connected to receive the outputs of pushbuttons P–1 to P–8 of FIG. 2, it will be apparent that register 55 at the computer would receive the eight logic signals, and eight of the stages of the register could be connected to control the operation of the central computer in the same way in which logic lines L1 to L8 are shown connected, and thus only one logic line then need extend between the terminal units and the central computer to carry all eight configuration pushbutton signals.

While the digital data transmission system of FIG. 5 contemplates serial transmission from a terminal unit to the central computer of the bits representing a given coefficient, with eight gating systems of the type shown provided and the eight pulse trains representing the eight coefficients being transmitted simultaneously, a modified arrangement illustrated in FIG. 6 contemplates instead that 13 bits representing a given coefficient all be transmitted in parallel over 13 wires, with the eight different coefficient values being transmitted in succession over the same set of 13 wires.

A single set of four thumb wheel switches 51′ to 54′ similar to those shown at 51—54 in FIG. 5 are used to energize 13 lines in accordance with the sign and magnitude of a desired coefficient, and the 13 lines are applied to eight AND gate circuits. Addressing means shown as a simple 8-pole selector switch allows the operator to select which of eight coefficients he wishes to set, and upon depression of momentary pushbutton switch CP one of the AND gate circuits is enabled, thereby filling the selected one of eight 13-bit coefficient registers CR–0 through CR–7. The contents of each register are applied to a respective AND gate which also receives an input from a respective stage of a nine-state ring counter 63. When a given terminal unit is addressed and granted service, so that its line 1A is high, the beginning of the "reset" or "*a*" period will enable AND gate G–61, thereby causing counter 63 to successively read out the contents of the eight 13-bit registers onto a 13-wire bus which extends between each terminal and the central computer. At the central computer the address of the terminal being serviced, which address is carried in lines A1 to A4, is used to direct the incoming data to a particular group of digitally used coefficient units of DCU's, a separate group of eight DCU's being provided in the computer for each terminal unit. In FIG. 6 only the first and last DCU's for one terminal are shown at DCU–1 and DCU–8, and another group of eight DCU's related to a different terminal is intended to be indicated by a simple block at 65. Counter 64 operates in a manner similar to counter 59 of FIG. 5, to route the eight successive 13 parallel-bit coefficient data words to set the eight addressed DCU's.

It should be noted that coefficient registers such as CR–0 to CR–7 relating to a given terminal may be filled in a number of ways different from that shown, such as from a digital computer connected to receive input data from typewriters located at the terminal units. Also, it will be apparent that the gating arrangement shown in FIG. 6 may be used to transmit words which comprise configuration logic bits instead of, or in addition to, coefficient data words.

While the arrangement illustrated in FIGS. 2 and 3*b* contemplates transmission of solution data all in analog from to the terminals, it is within the scope of the invention for one or more of the solution variables to be converted to digital form by the analog-to-digital converter contained within the AD–4 computer, and for the bus system to include wires to distribute such digital data, preferably in parallel multibit words, to the terminals, to operate an incremental plotter, for example, or printer, or digital recording device, at a terminal.

It will thus be seen that the objects set forth above, among those made apparent from the preceding description, are efficiently attained, and since certain changes may be made in the

above constructions without departing from the scope of the invention, it is intended that all matter contained in the above description or shown in the accompanying drawings shall be interpreted as illustrative and not in a limiting sense.

The embodiments of the invention in which I claim an exclusive property or privilege are defined as follows:

1. An analog computer installation comprising, in combination: a central analog computer having a plurality of computing elements interconnected to solve a problem; a plurality of remote terminal units each having a plurality of controls adjustable by a respective operator and a display device observable by said respective operator; and an interconnection bus system including a number of lines extending between said central computer and each of said remote terminal units, said computer including address means for applying address signals over said interconnection bus system to address each of said terminal units in succession, the plurality of controls in each of said terminal units being adjustable to provide a respective first plurality of further signals, each of said terminal units including transmitting means responsive to receipt of a respective address signal identifying the terminal unit for transmitting said first plurality of further signals from said terminal unit to said computer over a first plurality of said lines of said bus system, said computer including control means responsive to various of said further signals of said first plurality for causing said computer to operate to solve said problem utilizing data represented by various of said further signals of said first plurality and to simultaneously provide a plurality of output signals, said output signals being connected over said interconnection bus system to said display device of said terminal unit.

2. A computer installation according to claim 1 in which said control means includes timing means for cycling a group of said computing elements through a sequence of operating modes in order to solve said problem, and in which one of said further signals from the terminal unit addressed at a given time is operative either to halt said timing means and advance said address means to provide a successive address signal or to advance said timing means through said sequence of operating modes, depending upon the character of said one of said further signals.

3. An installation according to claim 1 in which said transmitting means in each of said terminal units includes adjustable switch circuit means responsive upon receipt of said respective address signal to provide a first logic signal on a further line of said interconnection bus system in which said computer includes means responsive to said first logic signal for applying a second logic signal over said interconnection bus system, and in which the transmitting means of each of said terminal units is operative to connect a set of said further signals of said first plurality to a set of said lines of said first plurality upon simultaneous receipt of its respective address signal and said second logic signal.

4. A computer installation according to claim 1 in which the plurality of controls at each terminal unit includes switch means adjustable to provide a respective multibit digital signal representing the sign and magnitude of a numerical coefficient, and in which each of said transmitting means is operative in response to receipt of its respective address signal for applying said multibit digital signal over said interconnected bus system as one of said further signals of said first plurality.

5. A computer installation according to claim 1 in which said computing elements include an electronic analog integrator controllable between plural operating modes, and said computer includes timing means for repetitively cycling said electronic integrator between said modes, said timing means being operable to control said address means to increment said address signals at the completion of a given one of said modes.

6. A computer installation according to claim 1 in which said computer includes timing means for repetitively cycling said computer through a sequence of operating modes, in which the transmitting means of each of said remote terminal units includes switch circuit means for providing a logic signal on one of said lines of said first plurality, and in which said logic signal is connected to interrupt or enable the cycling of said timing means.

7. A computer installation according to claim 1 in which the transmitting means in each of said remote terminal units comprises a plurality of adjustable electrical devices connected through respective switches to a group of said lines of said first plurality, and in which each of said terminal units includes means responsive to receipt of its respective address signal for closing said switches.

8. A computer installation according to claim 1 in which said computing elements of said analog computer are interconnected in a plurality of groups to solve a plurality of respective problems, and in which said various of said further signals are connected to each of said groups of computing elements and output signals are connected over said bus system from each of said groups of computing elements, each of said terminal units including means for selectively connecting various of said output signals to its respective display device.

9. A computer installation according to claim 1 in which said output signals are connected to a second plurality of lines of said bus system, in which said bus system includes a third plurality of lines extending to each of said remote terminal units, each of said remote terminal units includes first switching means for connecting the output signals received by the respective unit on said second plurality of lines to said third plurality of lines, and each of said remote terminal units includes second switching means for connecting signals on said third plurality of lines to its respective display device in lieu of said output signals on said second plurality of lines.

10. A computer installation according to claim 1 in which the plurality of controls at each terminal unit includes at least one adjustable resistance device and in which each of said transmitting means is operative in response to receipt of its respective address signal for applying an electrical signal commensurate in magnitude with the adjustment of said resistance device over one of said lines of said first plurality to constitute one of said further signals of said first plurality.

11. A computer installation according to claim 1 in which the plurality of controls at each terminal unit includes at least one adjustable switch and in which said each of transmitting means is operative in response to receipt of its respective address signal for applying an electrical logic signal having a character dependent upon the adjustment of said switch over one of said lines of said first plurality to constitute one of said further signals of said first plurality.

12. A computer installation according to claim 1 in which the transmitting means in each of said terminal units includes adjustable switch circuit means responsive upon receipt by its respective transmitting means of its respective address signal to provide a first logic signal on a further line of said interconnection bus system, in which said computer includes means responsive to said first logic signal for applying a second logic signal over said interconnection bus system, and in which the transmitting means of each of said terminal units is operative upon simultaneous receipt of its respective address signal and said second logic signal to apply a sequence of said further signals of said first plurality over said first plurality of lines of said bus system.

13. A computer installation according to claim 2 in which said timing means is operative to provide an incrementing signal upon used of one of said operating modes to advance said address means to provide a successive address signal.

14. A computer installation according to claim 4 in which said central computer includes register means connected to receive and store said multibit digital signal and switching means responsive to the stored contents of said register means for controlling the magnitude of a current connected to one of said computing elements.

15. A computer installation according to claim 4 in which said central computer includes register means connected to receive and store said multibit digital signal and switching

means responsive to the stored contents of said register means for establishing a selected interconnection between said plurality of computing elements.

16. An installation according to claim 6 in which said computer means includes means responsive to said logic signal for applying a second logic signal over said interconnection bus system to the then-addressed terminal unit, said timing means is operable to apply a third logic signal over said interconnection bus system upon occurrence of a selected one of said operating modes, and in which each terminal unit includes a gating circuit responsive to said second and third logic signals for activating the display device in the then-addressed terminal unit.

17. An installation according to claim 6 in which the transmitting means of each of said terminal units includes second switch circuit means for controlling a second logic signal on a second one of said lines of said first plurality, and in which said second logic signal is connected to control the speed of said timing means to vary the time durations of said operating modes.

18. An installation according to claim 6 in which said computer includes means responsive to receipt of said logic signal for applying a further signal over said interconnection bus system to reset said switch circuit means to alter the character of said logic signal.

19. A computer installation according to claim 8 in which at least one of said further signals of said first plurality is operative to prevent the operation of one of said groups of computing elements to solve its respective problem.

20. A computer installation according to claim 9 in which said bus system includes a fourth plurality of lines extending to each of said remote terminal units, one of said terminal units includes means for applying a continuous address signal to said fourth plurality of lines, and each of said terminal units includes means responsive to said continuous address signal for controlling said first switching means.

21. A computer installation according to claim 12 in which said transmitting means in each of said terminal units includes adjustable means for storing a plurality of bit patterns, and sampling means operative upon simultaneous receipt of the respective address of a given terminal unit and said second logic signal for transmitting successive bits of each of said bit patterns sequentially over said first plurality of lines to said central computer, said central computer including a plurality of register means connected to receive and store said bit patterns.

22. A computer installation according to claim 12 in which said transmitting means in each of said terminal units includes adjustable means for storing a plurality of bit patterns, and sampling means operative upon simultaneous receipt of the respective address of a given terminal unit and said second logic signal for transmitting each of said bit patterns in succession over said first plurality of lines to said central computer, said central computer including a plurality of register means connected to receive and store said bit patterns.

23. A computer installation according to claim 13 in which one of said further signals is operative to prevent the application of said incrementing signal to advance said address means, and thereby cause said timing means to cycle through said sequence of operating modes a plurality of times before said address means is advanced to a successive address.