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- (81) **Designated States** (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
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(54) **Title:** SEMICONDUCTOR CHIP MOUNTING

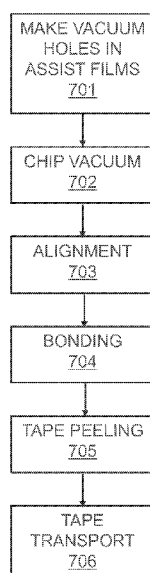


FIG. 7

(57) **Abstract:** A semiconductor chip having conductive bumps on its main surface is held by its back via an elastic film using a suction tool having a plurality of suction holes, the semiconductor chip is positioned against a substrate provided with connection wires corresponding to the conductive bumps, and the semiconductor chip is mounted onto the substrate in such a manner that the conductive bumps connect to the connection wires, and uniform pressure is applied from the oversized bonding tool suction to the semiconductor chip via the film while the semiconductor chip is being pressed against the substrate by oversized bonding tool to keep constant pressure in order to bond the conductive bumps with the connection wires. The film assisted bonding tool has a film cooling system to assist in making vacuum holes and a through-hole tool movable relative to the bonding head to create a plurality of holes in the assist film with a plurality of needles.



**Declarations under Rule 4.17:**

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

- *with international search report (Art. 21(3))*

SEMICONDUCTOR CHIP MOUNTING

[0001] Embodiments of the invention are directed, in general, to semiconductor chip packaging and, more specifically, mounting a thin semiconductor chip onto a substrate.

BACKGROUND

[0002] A method for mounting a semiconductor chip onto a substrate referred to as flip-chip mounting has been widely adopted. In the case of flip-chip mounting, a body provided with several conductive bumps, that is, bumps usually made of gold, serving as connecting terminals is placed face down onto the surface (referred to as main surface, hereinafter) where circuits are formed on a semiconductor chip, that is, with the main surface facing the substrate, in order to bond the conductive bumps directly to the wires on the substrate.

[0003] A semiconductor chip is held by suction using a vacuum suction tool and placed over the area where the bumps are to be mounted onto the wires formed on the substrate. When bonding the gold bumps onto the wires, a fixed amount of pressure is applied to the semiconductor chip using a suction tool, and the substrate is heated at the same time.

[0004] In order to apply pressure via the suction tool to the semiconductor chip, it is important to bring the suction tool and the semiconductor chip into close contact by means of vacuum suction. However, a minute gap may be created between the suction surface of the suction tool and the back of the semiconductor chip placed against the suction surface, resulting in a drop in suction power. This drop in suction power not only reduces the pressure applied to the bumps but also creates another problem.

[0005] That is, when the suction power of the suction tool drops, the semiconductor chip can no longer follow the pressure applied to the tool, resulting in the problem that tip of the suction tool ends up abrading the surface of the semiconductor chip due to friction. Some of the scraped-off fine silicon particles stick to the back of the semiconductor chip, land on the substrate, and may even be incorporated into a device eventually.

[0006] The particles stuck to the semiconductor chip have potential for causing serious problems depending on the ultimate use of the semiconductor chip. For example, a preamplifier bare chip to be mounted on an actuator in a hard disk device may be mentioned. The scraped-off particles (they are 0.1-5 μm or so in size) stuck to the semiconductor chip come loose inside the device due to vibrations caused by revolution of the magnetic disk and ultimately fall onto the disk. Because the magnetic head floats at a distance of 50 μm or less from the disk surface, the scraped-off particles on the disk seriously affect the function of the hard disk drive.

[0007] As a result, with either elastic film, not only was the same bonding strength as that of the conventional example secured, but also the creation of particles due to abrading of the semiconductor chip was avoided entirely.

[0008] However, elastic film is effective to prevent mechanical damage on silicon chip by ultrasonic vibration but heat transfer is low when bonding tool is heated up to accelerate bump bonding.

[0009] Additional background is described in US 6,269,999.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 is an oblique view showing an example of prior art bonding tool.

[0011] FIG. 2 shows a possible thermocouple position problem with prior art between the die edge and die center.

[0012] FIG. 3 is two graphs showing a temperature GAP cause by the prior art bonding tool.

[0013] FIG. 4 shows lack of constant pressure when the semiconductor is thin.

[0014] FIG. 5 is a diagram showing an oversized bonding tool overlapping semiconductor chip.

[0015] FIG. 6 is a profile view of new tool and comparison with prior art tool.

[0016] FIG. 7 is a flowchart illustrative of the steps in the process of thin semiconductor chip mounting in accordance with an embodiment of the invention.

[0017] FIG. 8 shows a film cooling system to make vacuum hole by air spray in accordance with an embodiment of the invention.

[0018] FIGS. 9A-9C shows tension control during vacuum and bonding.

[0019] FIGS. 10A and 10B show a prior art single vacuum hole.

[0020] FIGS. 11A and 11B show bonding tool vacuum hole designs.

[0021] FIG. 12 shows the alignment between the semiconductor chip and the substrate.

[0022] FIG. 13 shows bonding stage design in accordance with embodiment of the invention to reduce temperature GAP.

[0023] FIG. 14 shows heat tool attachment and heat shield in accordance with embodiment of the invention to reduce temperature.

[0024] FIG. 15 shows tape peeling in accordance with embodiment of the invention.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0025] FIG. 1 shows a prior art suction tool. The suction tool is one of the constituents of a device, such as a flip-chip tape assisted bonding device 10, used to mount a semiconductor chip onto a substrate. The bonding tool 11 has a suction nozzle 12 whose tip constitutes a suction surface for the semiconductor chip. The semiconductor chip is held onto the suction surface by means of vacuum suction achieved by the suction power obtained through a single suction hole at the tip of the suction nozzle. In the prior art, an ultrasonic horn for supplying ultrasonic vibrations is connected halfway up the suction nozzle 12. The ultrasonic horn supplies lateral vibrations of a specific frequency to the suction nozzle 12 for a prescribed period of time. The tip of the suction nozzle 12 and ultimately the semiconductor chip held there by means of vacuum suction are vibrated microscopically in the lateral direction by the vibrations. The semiconductor chip is bonded to the substrate by the vibrations, pressure, and heat.

[0026] Elastic film 30 is configured as a long tape-like shape and is taken up on a winding reel from a feeding reel. The elastic film is positioned between the suction surface of the suction nozzle 12 and the semiconductor chip when the ultrasonic vibrations are applied to the semiconductor chip via the bonding tool 11. The intervention by the elastic film prevents the semiconductor chip from coming into direct contact with the suction nozzle, so that the back of the semiconductor chip will not be abraded by the suction surface. The suction nozzle 12 is moved to the position where a through-hole tool is provided while the film 30 is carried along in front of the suction nozzle. The through-hole tool contains a needle pin with a sharp tip whereby a hole is created in the film 30 at the position corresponding to the suction hole on the suction nozzle 12. A semiconductor chip 32 held by suction by the suction nozzle 12 is carried onto a substrate 33 fixed onto a mount 34.

[0027] In the elastic film feeder device, the tape-like film is mounted onto the device in such a manner that it is positioned in front of the suction surface 11a of the suction nozzle. Every time the step of mounting a semiconductor chip onto the substrate begins, the feeder device drives the reel in such a manner that a new surface of the film is supplied to the front of the suction surface. Although the present invention is not restricted by any specific configuration of the feeder device, it is preferred that the feeder be fixed to the suction tool.

[0028] The elastic film which must be capable of efficiently apply pressure to the thin semiconductor chip. The strength to stand up to pressure and thermal tolerance are needed. The thickness of the elastic film, which the inventor has confirmed through experiments to meet these requirements, falls into a range of 10-50 μm . Furthermore, the distance the suction nozzle travels 0.5-1.5 μm or so. In addition, fluoro-resin (elasticity: approximately 1.7 MPa) and straight chain type polyimide resin (elasticity: approximately 6370 MPa) were found to be suitable as the material of the film.

[0029] A problem with the prior art bonding tool is a temperature gap. FIG. 2 shows a possible thermocouple position problem between the die edge 210 and die center 220. FIG. 3 are two graphs showing a temperature gap cause by the prior art bonding tool. The temperature profile comparison between the two graphs confirms that there is temperature gap between die center and die corner by using a larger attachment to bonding tool compared with the prior art attachment. 10mm attachment is used for the comparison.

[0030] Another problem with the prior art bonding tool is uneven pressure applied to the semiconductor chip. This causes a breakage problem for thin semiconductor chips. FIG. 4 shows lack of constant pressure when the semiconductor is thin. Bonding tool 11 applies pressure 410. During flipchip bonding, peripheral bump contact pressure is lost due to thin die. Prior art bonding tool 11 is too small. Chip edge to bump edge is around 200 μm in the example. Loss of pressure due to thin chip is show at points 420. Many bump count is high pressure by reaction force, especially after non-conductive paste NCP hardening 430. Low density bond finger is not much reaction force compare with high density bond finger 440. Table 1 shows size difference between a typical chip and prior art chip vacuum attachment size.

[0031]

TABLE I

	X (mm)	Y (mm)
Chip	5.92	5.05
Chip Vacuum Attachment	5.466	4.601
Difference	0.454	0.449

[0032] FIG. 5 is a diagram showing an oversized bonding tool 520 overlapping semiconductor chip. Prior art bonding tool is not enough size to do flat bonding. 10mm x 10mm bonding tool used as example compared with current bonding tool. In the prior art, the bonding tool 11 was sized for the semiconductor chip 32. Embodiments of the invention use a bonding tool sized larger than the semiconductor chip 32. The oversized bonding tool keeps constant pressure, reduces the temperature gap and provides for a universal bonding tool, which will not need to be changed for different chip sizes.

[0033] FIG. 6 is a profile view of new bonding tool 610 and comparison with prior art tool. The bonding tool 610 is oversized. The bonding tool 610 may be constructed as part of a new machine or as an attachment to preexisting machine.

[0034] FIG. 7 is a flowchart illustrative of steps in the thin semiconductor chip mounting method 700 in accordance with an embodiment of the invention. In Step 701, a plurality of vacuum holes are made into the assist film 810. Assist film is of similar properties as elastic film of the prior art. Not only elastic film, but metal film could also be used to improve heat transfer from bonding tool 610 to silicon die. Metal film is for example, aluminum, copper or steel. Thickness of the metal foil should have enough peel strength for rewind motion. Elastic film including metal particles is another option to have both features of elasticity and good thermal conductivity.

[0035] In the next step 702, a vacuum is provide to handle chip. The bonding tool 610 is moved to the position to which a semiconductor chip 632 is supplied. The suction is activated in order to hold the semiconductor chip 632 by means of vacuum suction. Although the assist film 810 is positioned between the bonding tool 610 couple to suction and the semiconductor chip 632, the suction power of the bonding tool 610 couple to suction is transmitted to the semiconductor chip 332 through the holes created in the assist film 810 in the previous step. As a result, not can only the semiconductor chip 632 be held by suction, but also the suction surface can be prevented from coming into direct contact with the semiconductor chip 632. A single hole was used in the prior art tool, however, the single hole is not possible with thin semiconductor chips due to breakage problem. Therefore, new

hole patterns are provided to provide increase vacuum power in a more distributed fashion, details in FIGS. 11a and 10b.

[0036] In the preferred embodiment, a film cooling system on a through-hole tool 820 makes the vacuum holes as is shown in FIG. 8 by air spray 823. The air spray 823 is for the cooling of the assist film. Bonding tool 610 movable coupled to a suction nozzle such as 12 or the through-hole tool 820 is moved relative to the other in order to create a plurality of holes in the assist film 810 with one or more needle(s) 825. In such a case, it is desirable to bring the assist film 810 into contact with the suction surface in order to prevent the position of the film from shifting relative to the suction surface after the holes are created, and to apply a fixed level of tension to the assist film 810. Bonding tool 610 may coupled to a single suction nozzle such as that of prior art 12 or suction source may be channeled through a manifold to several holes in bonding tool 610 matched to through-hole tool 820. The final part of a bonding tool that holds the semiconductor chip via suction through the suction holes may be referred to as a bonding head.

[0037] An imaging unit 830 is used in alignment as is disclosed below and to recognize/identify semiconductor chip and substrate. An example imaging unit is a charged-coupled device CCD camera.

[0038] An alternative embodiment comprises: 1) rolling out/sending the film to the bonding tool 610, 2) moving the through hole tool 820 under the bonding tool 610, 3) downing the bonding tool 610 toward the through hole tool 820 with the air spray 823, 4) moving the bonding tool 610 to the original position, and 5) moving the through hole tool 810 to the original position.

[0039] In the next step 702, the bonding tool 610 with suction is moved to the position to which a semiconductor chip 632 is supplied. The suction tool is activated in order to hold the semiconductor chip 632 by means of vacuum suction. Although the assist film 810 is positioned between the bonding tool 610 and the semiconductor chip 632, the suction power of the suction tool is transmitted to the semiconductor chip 632 through the holes created in the film 810. As a result, not can only the semiconductor chip 632 be held by suction, but also the suction surface can be prevented from coming into direct contact with the semiconductor chip 632.

[0040] In order to increase vacuum power and distribute the vacuum power to avoid stress points of thin semiconductor chip and miss alignment, a novel vacuum hole design is

provided. A single hole was used in the prior art tool, however, the single hole is not possible with thin semiconductor chips due to breakage problem. FIGS. 9A-9C shows tension control during vacuum and bonding.

[0041] FIGS. 10A and 10B show the prior art single hole for vacuum suction. This single hole design does not provide enough suction and results in a stress point which may break a thin semiconductor chip.

[0042] FIGS. 11A and 11B show the new bonding tool vacuum hole designs. The novel designs result in more suction and distributed suction power to control suction at different positions on the chip. The bonding tool 610 include multiple holes and manifold to distribute suction power. The distribution of the suction may also be in places in machine apart from the bonding tool 610 with multiple nozzles coupled to multiple holes in bonding tool 610. FIG. 11a shows an X pattern design in assist film 810. FIG. 11b shows an assortment of vacuum hole patterns as examples. Other patterns are deemed to be in the spirit and scope of the embodiments of the invention.

[0043] Alignment is provided in step 703. Bonding is provided in step 704. FIG. 9 shows tension control of film for miss alignment. Torque control system is shown for assist film 810 shrinkage tension during temperature GAP between alignment time for miss alignment and contact temperature.

[0044] The semiconductor chip 632 held by suction by the suction nozzle is carried onto a substrate 633, where it is to be mounted and positioned there. That is, gold bumps 632a on the semiconductor chip 632 are aligned with wires 633a on the substrate 633. The bonding tool 610 with semiconductor chip 632 held by suction is lowered to bring them into contact. At this time, the bonding tool 610 applies a prescribed amount of pressure in order to press the semiconductor chip 632 against the substrate 633. The substrate 633 is heated to a prescribed temperature. The substrate 633 may also be sealed into the package together with the semiconductor chip. Torque control system is used on assist film 810 to control tension and shrinkage during temperature GAP between alignment time for miss alignment.

[0045] FIG. 12 shows the alignment between the semiconductor chip 632 and the substrate 633. The alignment is assisted by use of the imaging unit 830. The imaging unit is positioned between the chip 632 and the substrate 633.

[0046] New material in addition to the design may reduce temperature GAP if used as a mount. PhotoveelTM ceramic material is a high performance machinable ceramic with

high strength and low thermal expansion. This material and the like materials may be used to create a heat shield. Alumina is used in the prior art and has a thermal conductivity of 30 W/mK. The thermal conductivity of Photoveel™ material is 1.7 W/mK.

[0047] FIG. 13 shows bonding stage design in accordance with embodiment of the invention to reduce temperature GAP.

[0048] FIG. 14 shows heat tool 1410 and attachment 1420 used in the prior art. The temperature in prior art may reach 116 degrees C. A heat shield 1430 in accordance with embodiment of the invention may be used to reduce temperature cause by radiation heating. In the example, the temperature with heat shield 1430 may be only 86 degrees C.

[0049] Tape peeling is provided in step 705. FIG. 15 shows tape peeling in accordance with embodiment of the invention. Assist film remover 1510 peels assist film from the semiconductor chip.

[0050] Tape transport is provided in step 706. Assist film 810 in FIG 8 is taken up by a reel as a feeder device is driven, and a new film surface is supplied to the front of the bonding tool 610 coupled to suction.

[0051] Those skilled in the art to which the invention relates will appreciated that modifications may be made to the described embodiments, and also that many other embodiments are possible, within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. A method for mounting a semiconductor chip, the method comprising:
providing a bonding tool sized larger than the semiconductor chip, the bonding tool coupled to a vacuum source;
providing an unused area elastic assist film from a spool of assist film;
creating a plurality of suction holes in a section of the elastic assist film;
holding the semiconductor chip by a second surface via suction through the plurality of suction holes in the elastic assist film;
positioning the semiconductor chip against a substrate provided with connection wires corresponding to the conductive bumps;
applying pressure from the oversized bonding tool to the semiconductor chip via the elastic assist film while the semiconductor chip is being pressed against the substrate in order to bond the conductive bumps with the connection wires.
2. The method according to claim 1, wherein the film is shaped like a long tape, and an unused area of the film is fed into the space between the bonding tool and the back of the semiconductor chip every time a new semiconductor chip is mounted.
3. The method according to claim 1, wherein the plurality of suction holes on the film are shaped by the oversized suction bonding tool.
4. The method according to claim 1, wherein the plurality of suction holes on the film are shaped by a plurality of shaped needles in the oversized suction bonding tool.
5. The method according to claim 1, wherein the plurality of suction holes form a pattern.
6. The method according to claim 5, wherein the pattern is a square pattern.
7. The method according to claim 5, wherein the pattern is a star pattern.

8. The method according to claim 5, wherein the pattern is a cross pattern.
9. The method according to claim 5, wherein the pattern is an X pattern.
10. A method for peeling a semiconductor chip from a film from a film assisted bonding tool, the method comprising moving a plurality of lift up sliders from a first plurality of areas and towards a second area of the semiconductor chip.
11. The method according to claim 10, wherein the second area is a center of the semiconductor chip.
12. The method according to claim 10, wherein the first plurality of areas are the corners of the semiconductor chip.
13. The method according to claim 1, wherein the film is shaped like a long tape, and an unused area of the film is fed into the space between the bonding tool and the back of the semiconductor chip every time a new semiconductor chip is mounted.
14. A film assisted bonding tool mechanism for bonding a semiconductor chip to a substrate, comprising:
 - a bonding head sized larger than the semiconductor chip, the bonding tool coupled to a vacuum source;
 - a film cooling system to assist in making vacuum holes in a section of assist film by a spray; and
 - a through-hole tool movable relative to the bonding head to create a plurality of holes in the assist film with a plurality of needles.
15. A film assisted bonding tool mechanism of claim 14 further comprising a part to provide tension.

16. A film assisted bonding tool mechanism of claim 14 further comprising a part to peel the film from the semiconductor chip.

17. A film assisted bonding tool mechanism of claim 16, wherein the part to peel the film from the semiconductor chip comprising a plurality of sliders.

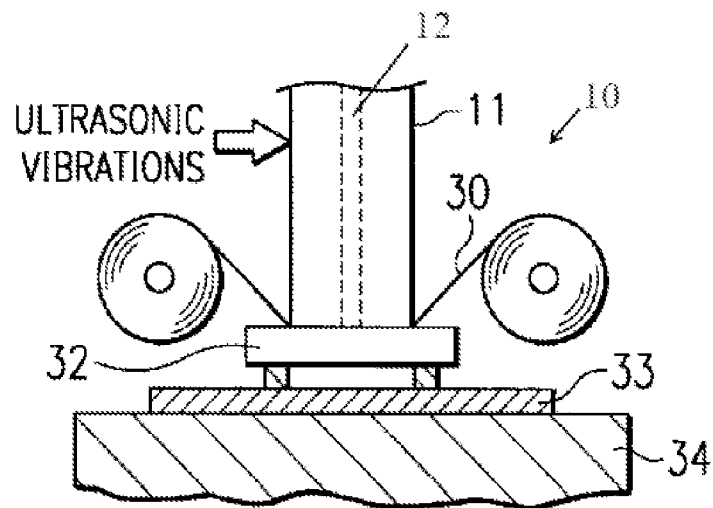


FIG. 1
PRIOR ART

Thermocouple position 200

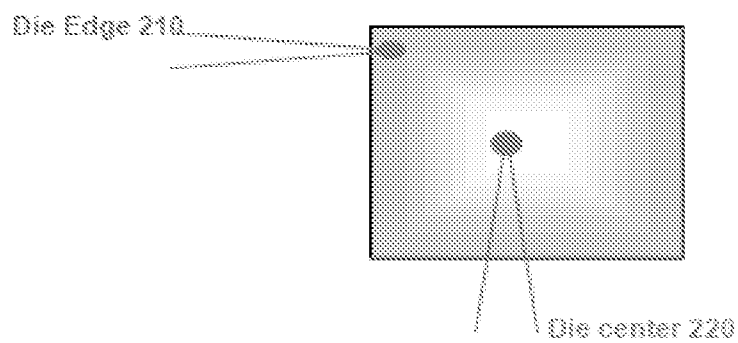


FIG. 2

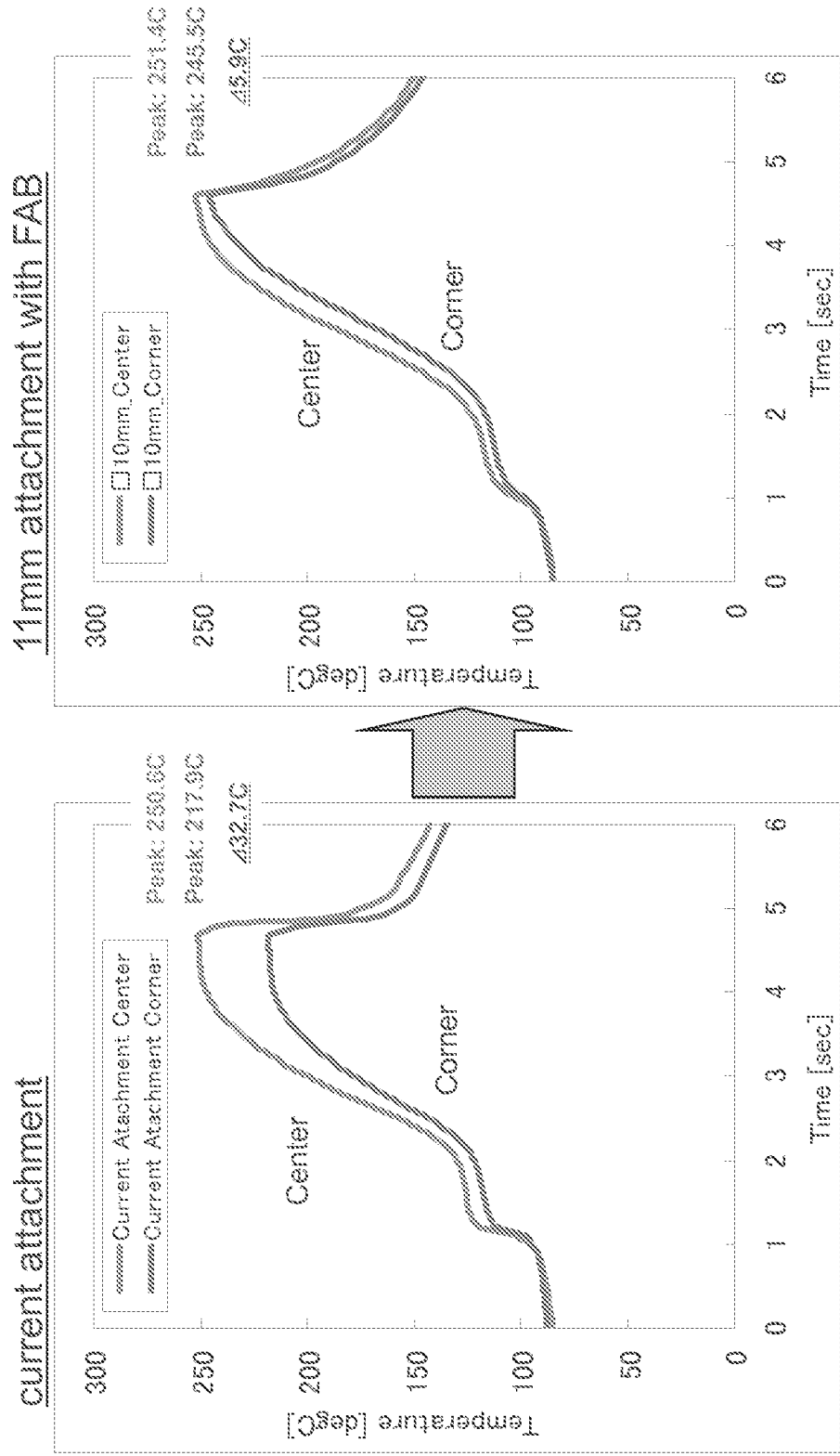


FIG. 3

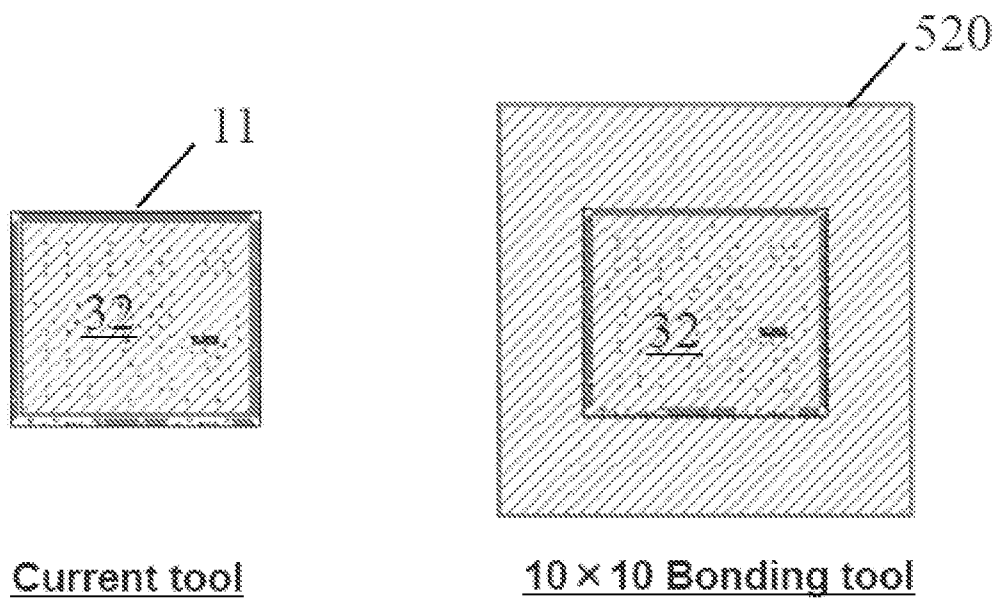
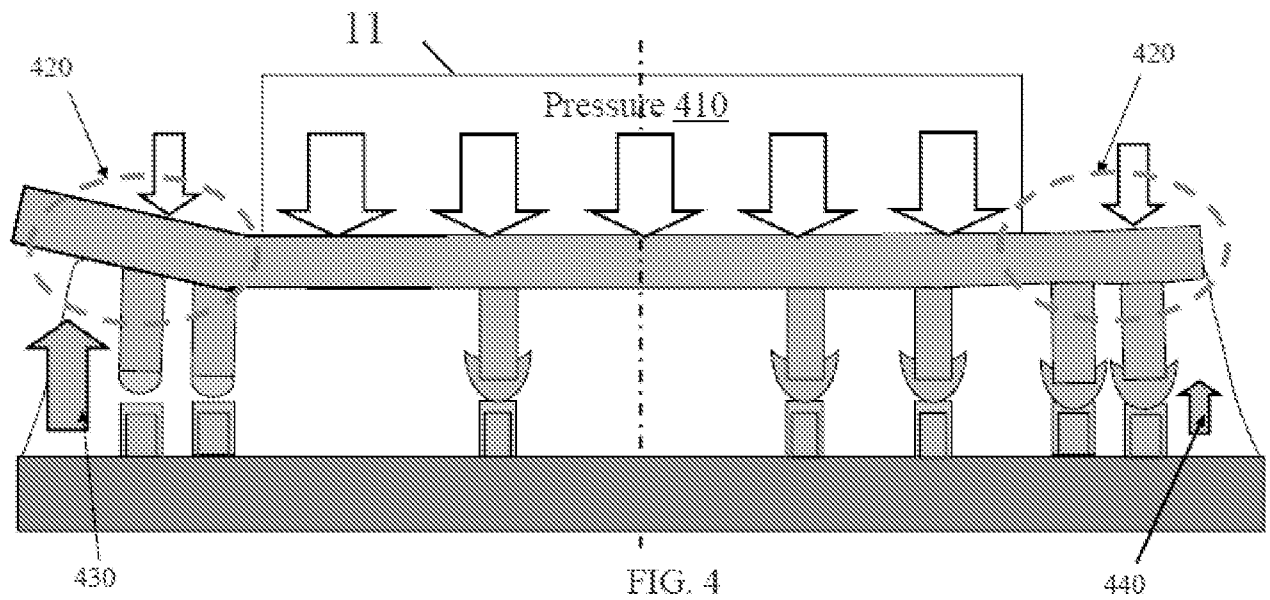


FIG. 5

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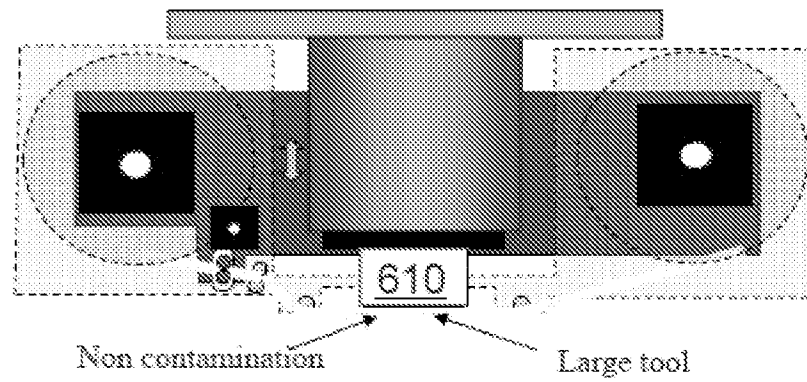


FIG. 6

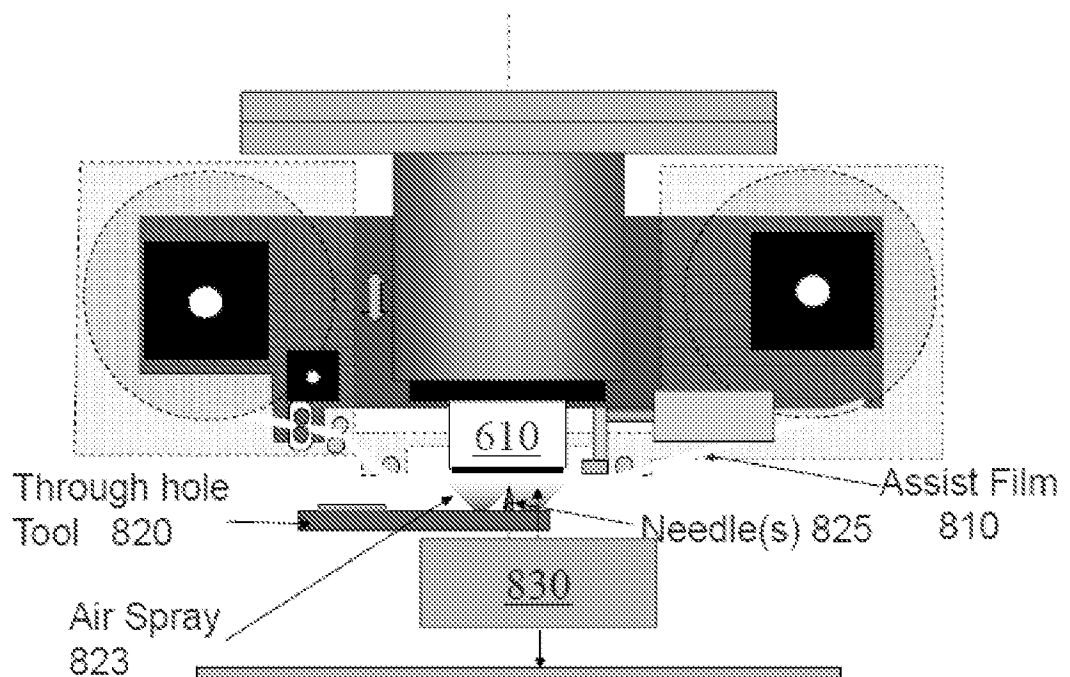


FIG. 8

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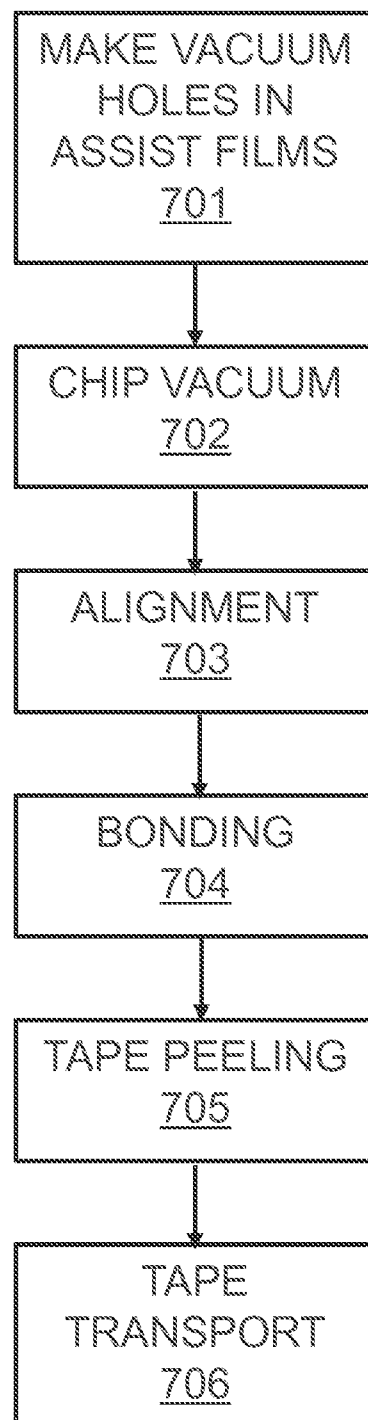


FIG. 7

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FIG. 9A

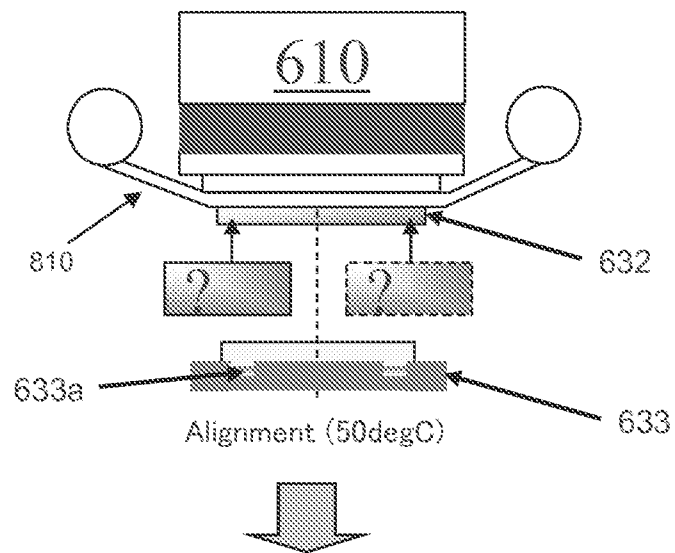


FIG. 9B

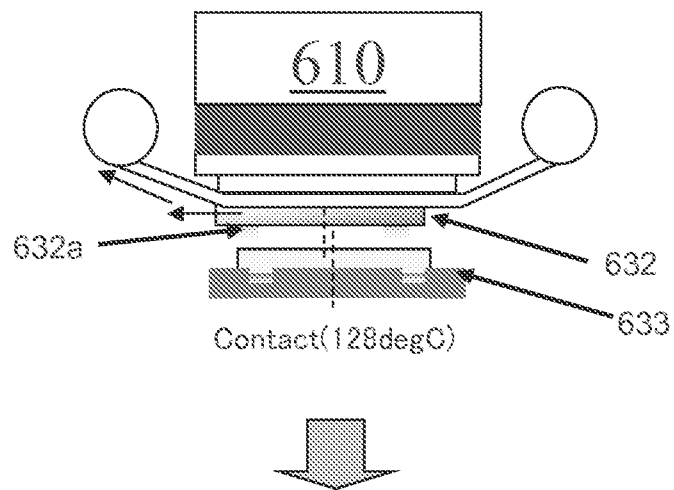
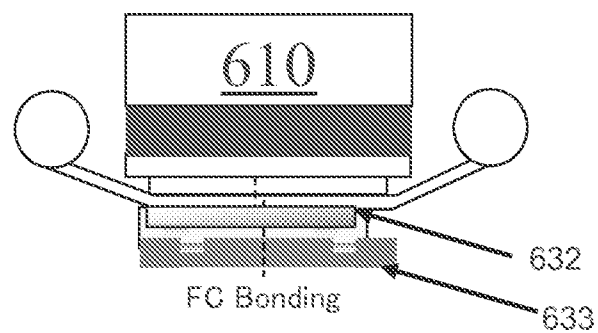


FIG. 9C



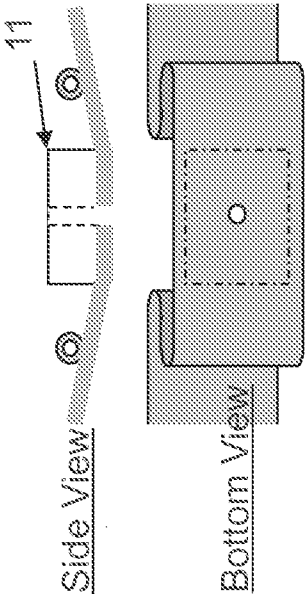


FIG. 10a
PRIOR ART

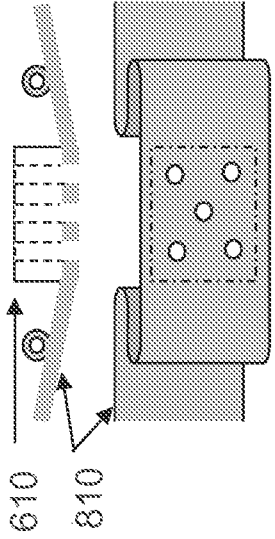


FIG. 11a

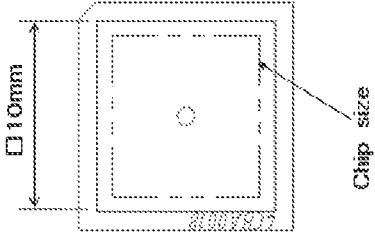


FIG. 10b
PRIOR ART

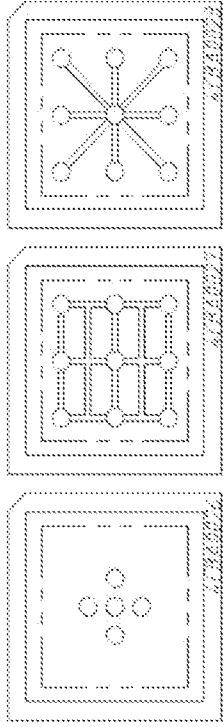


FIG. 11b

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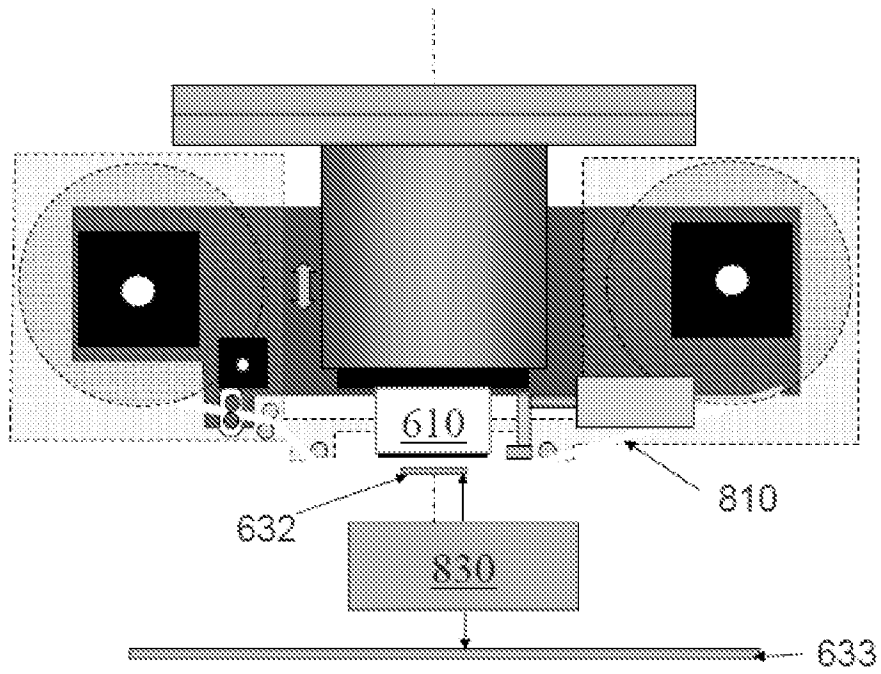


FIG. 12

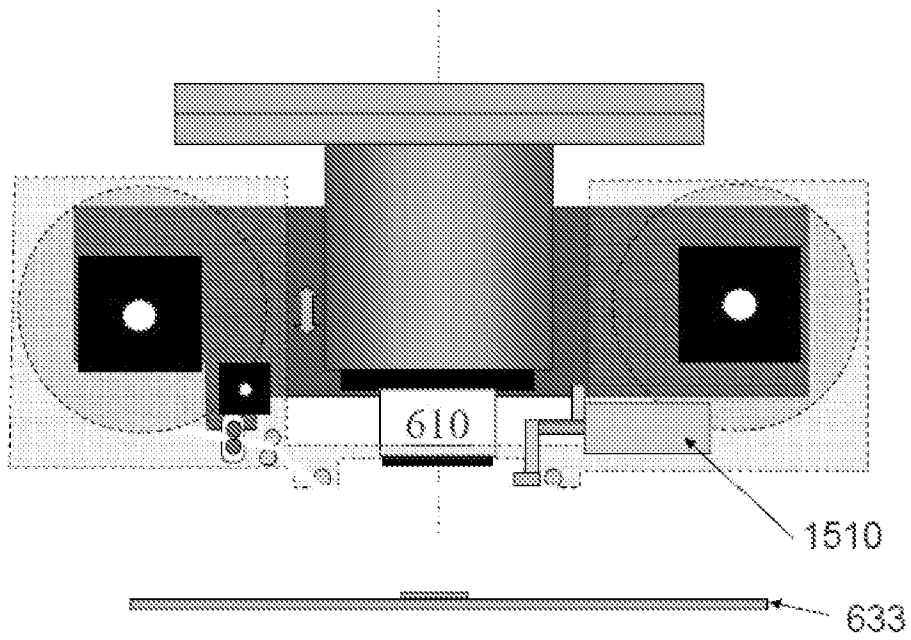
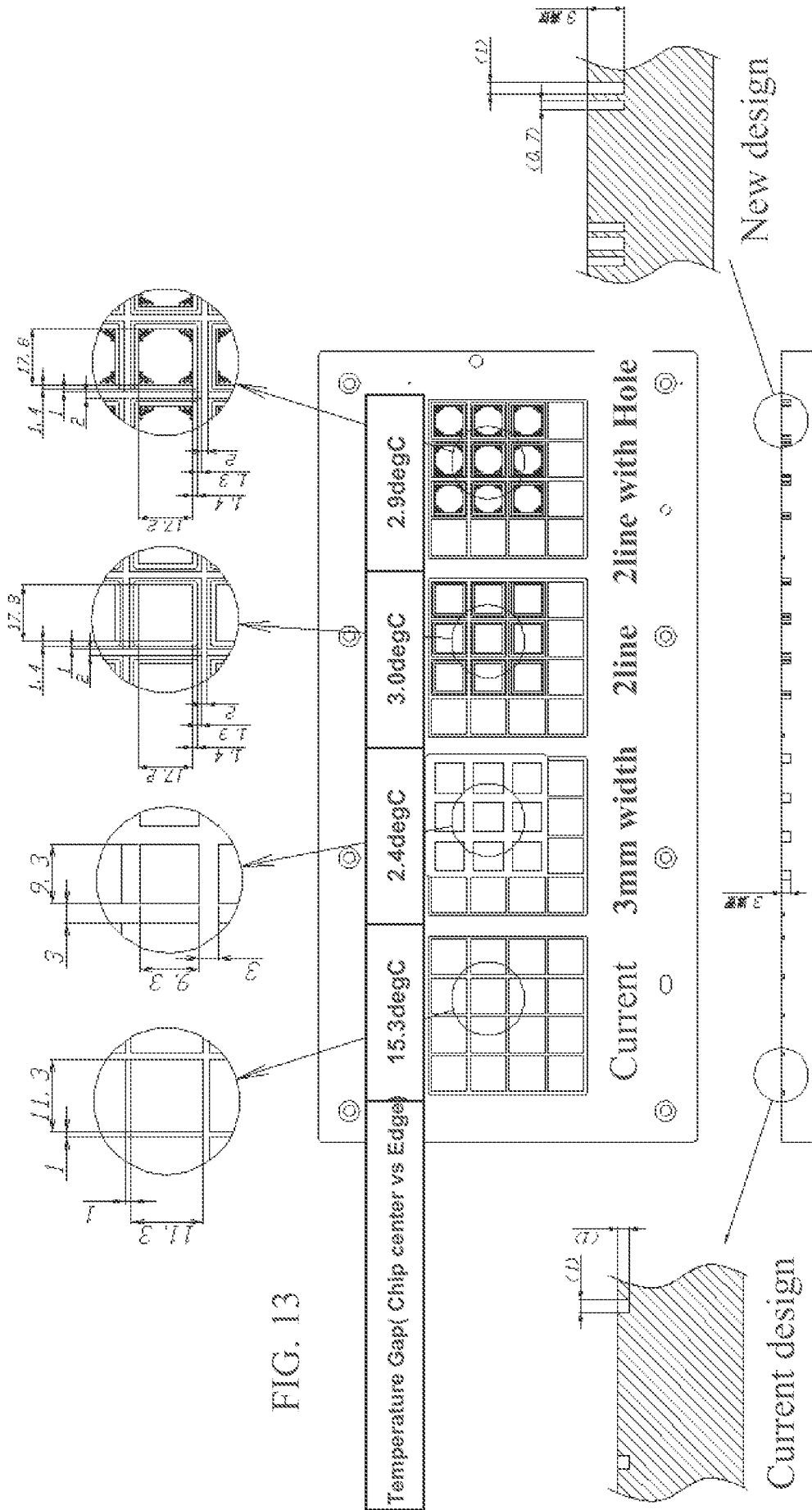


FIG. 15

New Bonding stage design to reduce temp GAP



Bonding Stage design is effective to reduce temperature GAP on the substrate.

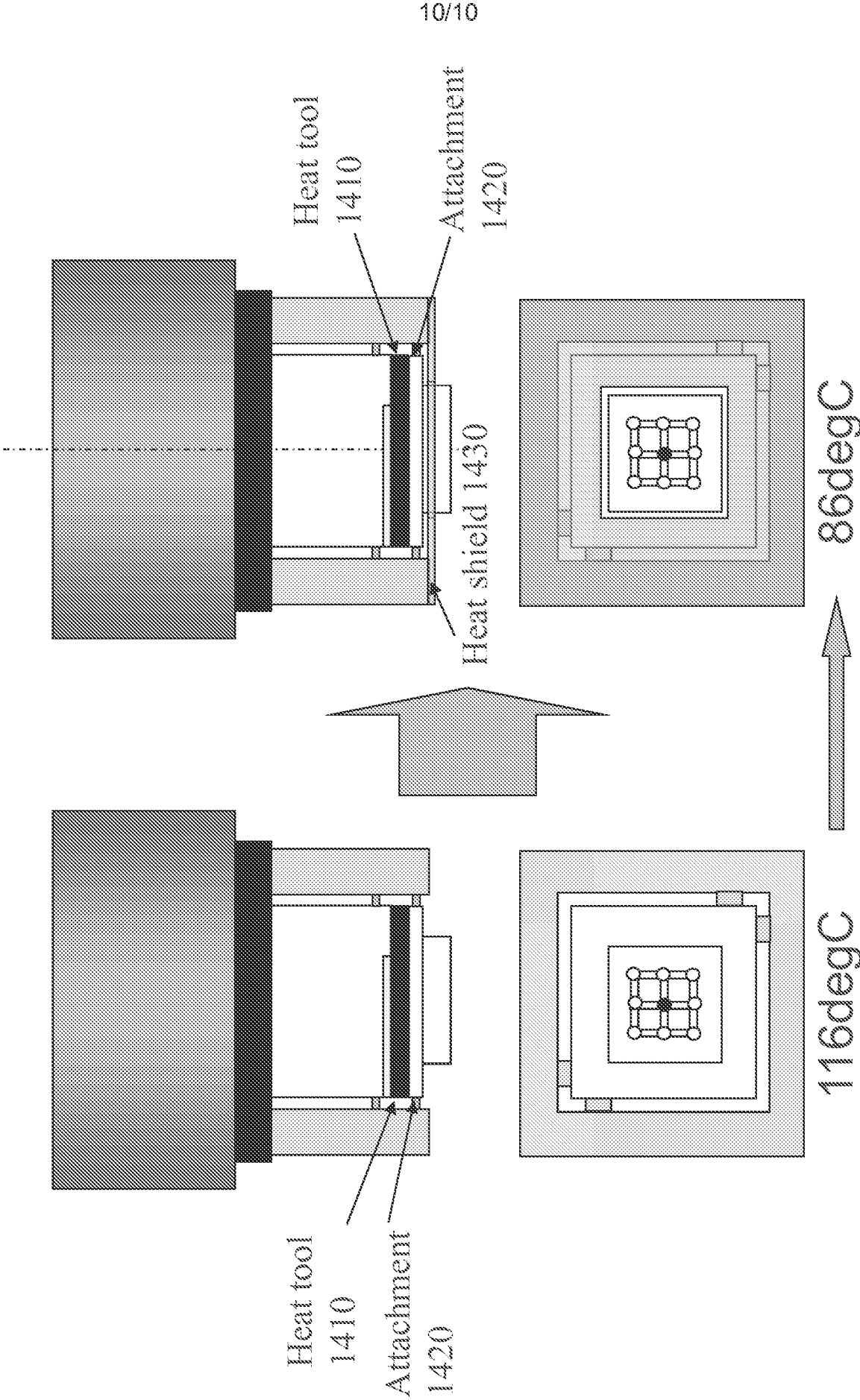


FIG. 14

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/059773**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/60(2006.01)i, H05K 3/32(2006.01)i, H01L 23/12(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/60; B23K 1/06; H01L 21/607; H01L 21/56; B32B 37/02; B23K 5/20; B32B 37/14; H05K 3/32; H01L 23/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: semiconductor, chip, bonding, substrate, suction, hole, oversize and elastic

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012-0043005 A1 (TAKATOYO YAMAKAMI et al.) 23 February 2012 See paragraphs [0031]-[0059], claims 1-10 and figures 1A-6C. (Note: This international search report has been established on the assumption that claim 13 is dependent on claim 10.)	10-13
Y		1-9, 14-17
Y	US 6269999 B1 (TOMOHIRO OKAZAKI et al.) 07 August 2001 See column 2, line 15 - column 4, line 63 and figures 3A-4F.	1-9
Y	JP 2011-135108 A (FUJITSU SEMICONDUCTOR LTD.) 07 July 2011 See paragraphs [0037]-[0058], claims 1-4 and figures 1-6.	14-17
A	JP 2003-258037 A (NIPPON AVIONICS CO., LTD.) 12 September 2003 See paragraphs [0013]-[0028], claims 1-7 and figures 1-3.	1-17
A	KR 10-0603709 B1 (AMKOR TECHNOLOGY KOREA INC.) 20 July 2006 See abstract, claims 1-2 and figures 1-3c.	1-17



Further documents are listed in the continuation of Box C.



See patent family annex.

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

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