[Continued on next page]

(54) Title: ALGORITHM ENGINE FOR ULTRA LOW-POWER PROCESSING OF SENSOR DATA

FIG. 2
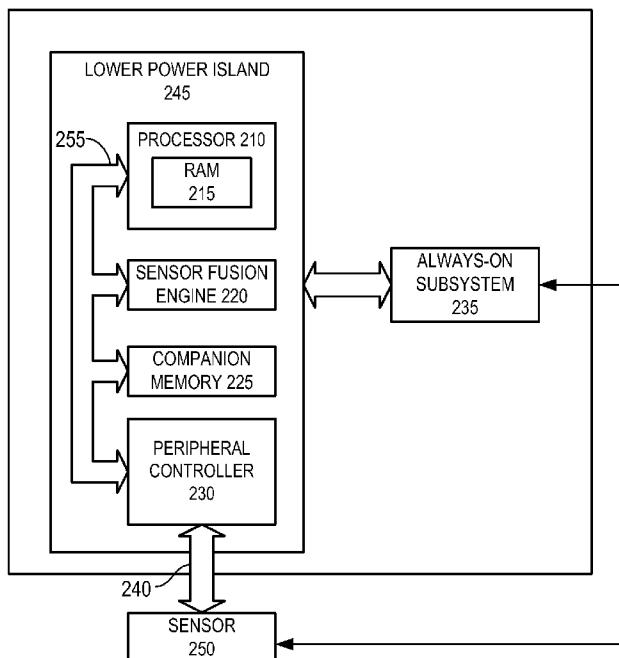
(57) **Abstract**: Disclosed is a method and apparatus for
power-efficiently processing sensor data. In one embodi-
ment, the operations implemented include: configuring a
sensor fusion engine and a peripheral controller with a gen-
eral purpose processor; placing the general purpose pro-
cessor into a low-power sleep mode; reading data from a
sensor and storing the data into a companion memory with
the peripheral controller; processing the data in the compan-
ion memory with the sensor fusion engine; and awaking the
general purpose processor from the low-power sleep mode.

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— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

ALGORITHM ENGINE FOR ULTRA LOW-POWER PROCESSING OF SENSOR DATA

RELATED APPLICATIONS

[0001]   This application claims priority to U.S. Patent Application No. 14/498,510 filed September 26, 2014, which is incorporated by reference herein in its entirety.

FIELD

[0002]   The subject matter disclosed herein relates generally to a System on a Chip comprising a hardware sensor fusion engine.

BACKGROUNDS

[0003]   The System on a Chip (SoC) is increasingly common in mobile devices such as smartphones and tablets.   A SoC is an integrated circuit comprising multiple components of a computing system.   For example, a typical SoC may contain one or more processor cores, a Graphics Processing Unit (GPU), a memory controller, and memory.   Some SoCs may also contain components such as radios and basebands for cellular communication, Wi-Fi, GPS, and Bluetooth, etc., as well as a Digital Signal Processor (DSP).

[0004]   It is desirable to improve power efficiency of SoCs used in mobile devices in order to increase battery life.   More particularly, improving power efficiency of SoCs for sensor-related tasks is important because many context-based applications demand the gathering, processing, and fusing (combining data from disparate sensors to derive information) of sensor data from multiple sensors on a continuous always-on basis. Performing these sensor-related tasks on an always-on basis with a general purpose processor core and/or a DSP is overly energy-inefficient.

SUMMARY

[0005]   An embodiment disclosed herein may include a method for power-efficiently processing sensor data comprising: configuring a sensor fusion engine and a peripheral controller with a general purpose processor; placing the general purpose processor into a low-power sleep mode; reading data from a sensor and storing the data into a companion memory with the peripheral controller; processing the data in the companion memory with the sensor fusion engine; and awaking the general purpose processor from the low-power sleep mode.

[0006]   Another embodiment disclosed herein may include a System on a Chip (SoC) comprising: a general purpose processor; a sensor fusion engine comprising one or

more hardware macros for sensor data-related algorithms; a companion memory; and a peripheral controller.

[0007]   A further embodiment disclosed herein may include a non-transitory computer-readable medium including code that, when executed by a processor, causes the processor to: configure a sensor fusion engine and a peripheral controller with a general purpose processor, place the general purpose processor into a low-power sleep mode, read data from a sensor and storing the data into a companion memory with the peripheral controller, process the data in the companion memory with the sensor fusion engine, and awake the general purpose processor from the low-power sleep mode.

[0008]   An additional embodiment disclosed herein may include an apparatus for power-efficiently processing sensor data comprising: means for processing data; means for fusing sensor data including means for executing sensor data-related algorithms; means for storing data; and means for controlling peripheral components, wherein the means for processing data is configured to provide configuration of the means for fusing sensor data and means for controlling peripheral components, the means for processing data is configured to enter a low-power sleep mode, the means for controlling peripheral components is configured to read data from a sensor and store the data into the means for storing data, and the means for processing data is configured to awaken from the low-power sleep mode.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009]   FIG. 1 illustrates an embodiment of a computing device where embodiments of the disclosure may be practiced.

[0010]   FIG. 2 illustrates a schematic diagram of an exemplary system on a chip.

[0011]   FIG. 3 is a flowchart illustrating an exemplary method for collecting and processing sensor data power-efficiently with a sensor fusion engine.

DETAILED DESCRIPTION

[0012]   The word "exemplary" or "example" is used herein to mean "serving as an example, instance, or illustration." Any aspect or embodiment described herein as "exemplary" or as an "example" in not necessarily to be construed as preferred or advantageous over other aspects or embodiments.

[0013]   As used herein, the term "computing system or device" refers to any form of programmable computer device including but not limited to laptop and desktop computers, tablets, smartphones, televisions, home appliances, cellular telephones,

personal television devices, personal data assistants (PDA's), palm-top computers, wireless electronic mail receivers, multimedia Internet enabled cellular telephones, Global Positioning System (GPS) receivers, wireless gaming controllers, receivers within vehicles (e.g., automobiles), interactive game devices, notebooks, smartbooks, netbooks, mobile television devices, wearable devices, or any data processing apparatus.

[0014]   An example computing device 100 adapted for context-based applications is illustrated in FIG. 1.   The computing device 100 is shown comprising hardware elements that can be electrically coupled via a bus 105 (or may otherwise be in communication, as appropriate).   The hardware elements may include one or more processors 110, including without limitation one or more general-purpose processors and/or one or more special-purpose processors (such as digital signal processing chips, graphics acceleration processors, and/or the like); one or more input devices 115, which can include without limitation one or more sensors, a mouse, a keyboard, keypad, touch-screen, microphone and/or the like; and one or more output devices 120, which can include without limitation a speaker, a printer, and/or the like.

[0015]   The computing device 100 may further include (an/or be in communication with) one or more non-transitory storage devices 125, which can comprise, without limitation, local and/or network accessible storage, an/or can include, without limitation, a disk drive, a drive array, an optical storage device, solid-state storage device such as a random access memory ("RAM") and/or a read-only memory ("ROM"), which can be programmable, flash-updateable, and/or the like.   Such storage devices may be configured to implement any appropriate data stores, including without limitation, various file systems, database structures, and/or the like.

[0016]   The computing device may also include a communication subsystem 130, which can include without limitation a modem, a network card (wireless or wired), an infrared communication device, a wireless communication device and/or chipset (such as a Bluetooth device, an 802.11 device, a Wi-Fi device, a WiMAX device, cellular communication devices, etc.), and/or the like. The communications subsystem 130 may permit data to be exchanged with a network, other computing devices, and/or any other devices described herein.   In one embodiment, the computing device 100 may further comprise a working memory 135, which can include a RAM or ROM device, as described above. Computing device may further comprise a battery 150. It should be

appreciated that computing device 100 may be a mobile device or a non-mobile device, and may have wireless and/or wired connections.

[0017]   The computing device 100 may also comprise software elements, shown as being currently located within the working memory 135, including an operating system 140, device drivers, executable libraries, and/or other code, such as one or more application programs 145, which may comprise or may be designed to implement methods, and/or configure systems, provided by embodiments, as will be described herein. Merely by way of example, one or more procedures described with respect to the method(s) discussed below might be implemented as code and/or instructions executable by computing device 100 (an/or a processor 110 within computing device 100); in an aspect, then, such code and/or instructions can be used to configure and/or adapt a general purpose computer (or other device) to perform one or more operations in accordance with the described methods.

[0018]   A set of these instructions and/or code might be stored on a non-transitory computer-readable storage medium, such as the storage device(s) 125 described above. In some cases, the storage medium might be incorporated within a computing device, such as the system 100. In other embodiments, the storage medium might be separate from a computing device (e.g., a removable medium, such as a compact disc), and/or provided in an installation package, such that the storage medium can be used to program, configure, and/or adapt a general purpose computer with the instructions/code stored thereon. These instructions might take the form of executable code, which is executable by the computerized computing device 100 and/or might take the form of source and/or installable code, which, upon compilation and/or installation on the computing device 100 (e.g., using any of a variety of generally available compilers, installation programs, compression/decompression utilities, etc.), then takes the form of executable code.

[0019]   Application programs 145 may include one or more context-based applications which rely on sensor data or information derived from sensor data.

[0020]   Fig. 2 illustrates a schematic diagram of an exemplary SoC 200. SoC 200 may include a general purpose processor 210, a random access memory (RAM) 215, a sensor fusion engine 220, a companion memory 225, a peripheral controller 230, and an always-on subsystem (AOSS) 235. General purpose processor 210, sensor fusion engine 220, companion memory 225, and peripheral controller 230 may be

communicatively connected via an internal interconnection 255. In one embodiment, companion memory 225 may be approximately several dozens of kilobytes in size. In another embodiment, companion memory 225 may be at least approximately 12 kilobytes in size. RAM 215 may have a dedicated connection with general purpose processor 210, or may be connected to other components via internal interconnection 255. In one embodiment, general purpose processor 210, RAM 215, sensor fusion engine 220, companion memory 225, and peripheral controller 230 may be located within a low power island 245 of SoC 200. The low power island is any section of the SoC designed for low power processing. The island may contain its own memory, clocks, PLLs, buses, dedicated voltage rails, power management circuits, memory, interfaces, digital or analog blocks, counters, microprocessors, and DSPs. In another embodiment, sensor fusion engine 220, peripheral controller 230, and companion memory 225 may be provided with a dedicated low power clock, so that data collection, buffering, and/or computation may take place when other parts of SoC 200 are in a low-power sleep mode with the system clock turned off and the main digital and memory rails for SoC 200 at retention voltage levels. In other words, in this embodiment, sensor fusion engine 220, peripheral controller 230, and companion memory 225 may have their own voltage rails (not shown) configured by the AOSS 235, or may be able to operate at retention voltage levels. In still another embodiment, peripheral controller 230 may be implemented with a dedicated programmable low-power processor, such as an ARM Cortex-M processor or a MIPS processor. SoC 200 may be in communication with one or more sensors 250 through peripheral controller 230 via a peripheral interface 240. Examples of one or more sensors 250 may include a proximity sensor, an ambient light sensor (ALS), an accelerometer, a gyroscope, a magnetometer, a barometric pressure sensor, and so on. These one or more sensors 250 may operate on an always-on basis. Sensors 250 may also be wireless connected via a connectivity chip using a protocol such as Bluetooth, Bluetooth LE, or 802.11. Peripheral interface 240 may be any of the suitable interfaces, such as I2C, SPI, UART, or SLIMbus, etc. AOSS 235 is always on and may perform multiple functions. For example, AOSS 235 may supply power to components of SoC 200 with one or more correct voltages, may receive data ready interrupt (DRI) signals from one or more sensors 250 when such interrupt signals are used, and may provide wake up signals to one or more components of SoC 200 such as peripheral controller 230. In some embodiments,

sensor fusion engine 220, companion memory 225, and peripheral controller 230 may be part of AOSS 235. In other embodiments the sensor fusion engine 220, companion memory 225, and the peripheral controller 230 may be in other domains of the SoC. SoC 200 may include additional components, which are not shown in Fig. 2 in order not to obscure the disclosure.

[0021]   Corresponding relationships may exist between elements shown in Fig. 2 and Fig. 1, and are described herein. General purpose processor 210 may be one of the one or more processors 110 shown in Fig. 1. RAM 215 may be part of the working memory 135 shown in Fig. 1. Internal interconnection 255, peripheral controller 230, peripheral interface 240, and AOSS 235 may be part of the bus 105 shown in Fig. 1. And one or more sensors 250 may be part of the one or more input devices 115.

[0022]   SOC 200 may comprise a general purpose processor 210, a sensor fusion engine 220 comprising one or more hardware macros for sensor data-related algorithm, a companion memory 225, and a peripheral controller 230, where the general purpose processor 210 may configure the sensor fusion engine 220 and the peripheral controller 230 before it enters a low-power sleep mode. Thereafter, the peripheral controller 230 may read data from a sensor 250 and may store the data into the companion memory 225 and last the general purpose processor 210 may be awoken from the low-power sleep mode.

[0023]   Sensor fusion engine 220 may have implemented therein one or more hardware macros. Hardware macros may perform sensor-related tasks with dedicated hardware circuitry and consume less energy than a general purpose processor and/or a DSP performing the same tasks does. A number of algorithms for sensor-related tasks may be implemented as hardware macros within sensor fusion engine 220. Examples include Kalman filters, motion detection algorithms, pedometer algorithms, navigation algorithms, gesture-related algorithms, sensor calibration algorithms, medical signal processing algorithms, fingerprint and/or touch algorithms, sensor data fusion algorithms, etc. The list is illustrative and does not limit the disclosure. Alternatively sensor fusion engine 220 may be an ultra-low power processor.

[0024]   Different methods for utilizing sensor fusion engine 220 to perform sensor-related tasks in a power-efficient manner will be hereinafter described. For example, sensor fusion engine 220 may be left active together with companion memory 225 and peripheral controller 230 to collect and process sensor data taking advantage of the

hardware macros while general purpose processor 210 and other components power-collapse into a sleep mode. General purpose processor 210 is awoken only when the sensor data processing is completed and general purpose processor 210 is required to perform other tasks. In an alternative embodiment, sensor fusion engine 220 acts as a math coprocessor to general purpose processor 210 to offload the tasks of executing computationally intensive sensor-related algorithms from general purpose processor 210. When a sensor fusion engine 220 is provided to act as a math coprocessor, a less powerful and likely more power-efficient general purpose processor 210 may be used.

[0025]   Fig. 3 is a flowchart illustrating an exemplary method 300 for collecting and processing sensor data power-efficiently with sensor fusion engine 220. At block 310, general purpose processor 210 configures sensor fusion engine 220 and peripheral controller 230. The particular configuration depends on the application(s) requesting sensor data and derived information. Sensor fusion engine 220 may be configured to execute one or more algorithms with the embedded hardware macros, while peripheral controller 230 is configured to read sensor data from at least one of the one or more sensors 250. At block 320, general purpose processor 210 enters a low-power sleep mode to conserve power. In some embodiments, other components such as peripheral controller 230 may also enter a sleep mode until being awoken to perform specific tasks.

[0026]   At block 330, peripheral controller 230 reads sensor data from one or more sensors 250 and stores the read sensor data into companion memory 225. Different methods for reading sensor data from one or more sensors 250 may be utilized. For example, in a polling mode, peripheral controller 230 may be configured at block 310 to periodically query one or more sensors 250. In some embodiments, sensor data is transferred in an interrupt mode: when at least one of the one or more sensor 250 have data ready to be read, it transmits a DRI signal to AOSS 235. In response, AOSS 235 then sets appropriate voltage levels and awakes peripheral controller 230. Peripheral controller 230 then configures peripheral interface 240, reads sensor data, and stores the sensor data into companion memory 225. In some other embodiments, peripheral controller 230, instead of AOSS 235, may handle the interrupts so that voltage levels do not have to change.

[0027]   At block 340, sensor fusion engine 220 processes sensor data stored in companion memory 225 with hardware macros. Processed sensor data and/or

information derived from sensor data may also be stored in companion memory 225 by sensor fusion engine 220. In some embodiments, block 330 and block 340 may overlap in time, and may be repeated when necessary. Last, at block 350, sensor fusion engine 220 awakes general purpose processor 210 when all the sensor data processing is completed and general purpose processor 210 is required for further tasks.

[0028]   Methods described herein allows for more power-efficient processing of sensor data. A computing device 100 that features a SoC 200 comprising sensor fusion engine 220, as described herein, may have a better battery life while supporting various context-based applications.

[0029]   It should be appreciated that aspects of the disclosure previously described may be implemented in conjunction with the execution of instructions (e.g., applications) by processor 101 of computing device 100, as previously described. Particularly, circuitry of the device, including but not limited to processor, may operate under the control of an application, program, routine, or the execution of instructions to execute methods or processes in accordance with embodiments of the disclosure (e.g., the processes of FIG. 3). For example, such a program may be implemented in firmware or software (e.g., stored in memory and/or other locations) and may be implemented by processors and/or other circuitry of the devices. Further, it should be appreciated that the terms processor, microprocessor, circuitry, controller, etc., refer to any type of logic or circuitry capable of executing logic, commands, instructions, software, firmware, functionality, etc.

[0030]   The teachings herein may be incorporated into (e.g., implemented within or performed by) a variety of apparatuses (e.g., devices). For example, one or more aspects taught herein may be incorporated into a general computing device, a desktop computer, a mobile computer, a mobile device, a phone (e.g., a cellular phone), a personal data assistant, a tablet, a laptop computer, a tablet, an entertainment device (e.g., a music or video device), a headset (e.g., headphones, an earpiece, etc.), a medical device (e.g., a biometric sensor, a heart rate monitor, a pedometer, an EKG device, etc.), a user I/O device, a computer, a server, a point-of-sale device, an entertainment device, a set-top box, or any other suitable device.

[0031]   In some aspects a wireless device may comprise an access device (e.g., a Wi-Fi access point) for a communication system. Such an access device may provide, for example, connectivity to another network through transceiver (e.g., a wide area

network such as the Internet or a cellular network) via a wired or wireless communication link. Accordingly, the access device may enable another device (e.g., a Wi-Fi station) to access the other network or some other functionality. In addition, it should be appreciated that one or both of the devices may be portable or, in some cases, relatively non-portable.

[0032]   It should be appreciated that when the devices are mobile or wireless devices that they may communicate via one or more wireless communication links through a wireless network that are based on or otherwise support any suitable wireless communication technology. For example, in some aspects the wireless device and other devices may associate with a network including a wireless network. In some aspects the network may comprise a body area network or a personal area network (e.g., an ultra-wideband network). In some aspects the network may comprise a local area network or a wide area network. A wireless device may support or otherwise use one or more of a variety of wireless communication technologies, protocols, or standards such as, for example, 3G, LTE, LTE Advanced, 4G, CDMA, TDMA, OFDM, OFDMA, WiMAX, and Wi-Fi. Similarly, a wireless device may support or otherwise use one or more of a variety of corresponding modulation or multiplexing schemes. A wireless device may thus include appropriate components (e.g., air interfaces) to establish and communicate via one or more wireless communication links using the above or other wireless communication technologies. For example, a device may comprise a wireless transceiver with associated transmitter and receiver components (e.g., a transmitter and a receiver) that may include various components (e.g., signal generators and signal processors) that facilitate communication over a wireless medium. As is well known, a mobile wireless device may therefore wirelessly communicate with other mobile devices, cell phones, other wired and wireless computers, Internet web-sites, etc.

[0033]   Those of skill in the art would understand that information and signals may be represented using any of a variety of different technologies and techniques. For example, data, instructions, commands, information, signals, bits, symbols, and chips that may be referenced throughout the above description may be represented by voltages, currents, electromagnetic waves, magnetic fields or particles, optical fields or particles, or any combination thereof.

[0034]   Those of skill in the art would further appreciate that the various illustrative logical blocks, modules, engines, circuits, and algorithm steps described in connection with the embodiments disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, engines, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the present disclosure.

[0035]   The various illustrative logical blocks, modules, and circuits described in connection with the embodiments disclosed herein may be implemented or performed with a general purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general-purpose processor may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

[0036]   The steps of a method or algorithm described in connection with the embodiments disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module may reside in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, hard disk, a removable disk, a CD-ROM, or any other form of storage medium known in the art. An exemplary storage medium is coupled to the processor such the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor. The processor and the storage medium may reside in an ASIC. The ASIC

may reside in a user terminal. In the alternative, the processor and the storage medium may reside as discrete components in a user terminal.

[0037]   In one or more exemplary embodiments, the functions described may be implemented in hardware, software, firmware, or any combination thereof. If implemented in software as a computer program product, the functions or modules may be stored on or transmitted over as one or more instructions or code on a non-transitory computer-readable medium. Computer-readable media can include both computer storage media and communication media including any medium that facilitates transfer of a computer program from one place to another. A storage media may be any available media that can be accessed by a computer. By way of example, and not limitation, such non-transitory computer-readable media can comprise RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that can be used to carry or store desired program code in the form of instructions or data structures and that can be accessed by a computer. Also, any connection is properly termed a computer-readable medium. For example, if the software is transmitted from a web site, server, or other remote source using a coaxial cable, fiber optic cable, twisted pair, digital subscriber line (DSL), or wireless technologies such as infrared, radio, and microwave, then the coaxial cable, fiber optic cable, twisted pair, DSL, or wireless technologies such as infrared, radio, and microwave are included in the definition of medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above should also be included within the scope of non-transitory computer-readable media.

[0038]   The previous description of the disclosed embodiments is provided to enable any person skilled in the art to make or use the claimed subject matter. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without departing from the spirit or scope of the disclosure. Thus, the claimed subject matter is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

<u>CLAIMS</u>

What is claimed is:

1. A method for power-efficiently processing sensor data comprising:

configuring, by a general purpose processor, a sensor fusion engine and a peripheral controller;

placing the general purpose processor into a low-power sleep mode;

reading data from a sensor and storing the data into a companion memory with the peripheral controller;

processing the data in the companion memory with the sensor fusion engine; and

awaking the general purpose processor from the low-power sleep mode.

2. The method of claim 1, wherein the sensor fusion engine comprises one or more hardware macros for sensor data-related algorithms.

3. The method of claim 2, wherein the sensor data-related algorithms comprise a sensor fusion algorithm.

4. The method of claim 2, wherein configuring the sensor fusion engine comprises configuring the sensor fusion engine to execute a sensor data-related algorithm with one of the one or more hardware macros.

5. The method of claim 1, wherein the data is read from the sensor in a polling mode or an interrupt mode.

6. The method of claim 1, wherein the companion memory is approximately several dozens of kilobytes in size.

7. The method of claim 1, wherein the reading of the data from the sensor with the peripheral controller is coordinated by an Always-On Subsystem (AOSS).

8. The method of claim 1, wherein the general purpose processor, the sensor fusion engine, the companion memory, and the peripheral controller are located within a low power island of a System on a Chip (SoC).

9. The method of claim 1, wherein the sensor fusion engine is part of an Always-On Subsystem (AOSS).

10. A System on a Chip (SoC) comprising:

    a general purpose processor;

    a sensor fusion engine comprising one or more hardware macros for sensor data-related algorithms;

    a companion memory; and

    a peripheral controller.

11. The System on a Chip (SoC) of claim 10, wherein

    the general purpose processor is configured to provide configuration of the sensor fusion engine and the peripheral controller,

    the general purpose processor is configured to enter a low-power sleep mode,

    the peripheral controller is configured to read data from a sensor and store the data into the companion memory, and

    the general purpose processor is configured to awaken from the low-power sleep mode.

12. The System on a Chip (SoC) of claim 10, wherein the sensor fusion engine is configured to act as a math coprocessor to the general purpose processor.

13. The System on a Chip (SoC) of claim 10, wherein the sensor data-related algorithms comprise a sensor fusion algorithm.

14. The System on a Chip (SoC) of claim 11, wherein the general purpose processor is configured to provide configuration of the sensor fusion engine by causing the sensor fusion engine to execute a sensor data-related algorithm with one of the one or more hardware macros.

15. The System on a Chip (SoC) of claim 11, wherein the data is read from the sensor in a polling mode or an interrupt mode.

16. The System on a Chip (SoC) of claim 10, wherein the companion memory is approximately several dozens of kilobytes in size.

17. The System on a Chip (SoC) of claim 11, wherein the reading of the data from the sensor with the peripheral controller is coordinated by an Always-On Subsystem (AOSS).

18. The System on a Chip (SoC) of claim 10, wherein the general purpose processor, the sensor fusion engine, the companion memory, and the peripheral controller are located within a low power island of the System on a Chip (SoC).

19. The System on a Chip (SoC) of claim 10, wherein the sensor fusion engine is part of an Always-On Subsystem (AOSS).

20. A non-transitory computer-readable medium including code that, when executed by a processor, causes the processor to:

configure a sensor fusion engine and a peripheral controller with a general purpose processor,

place the general purpose processor into a low-power sleep mode,

read data from a sensor and storing the data into a companion memory with the peripheral controller,

process the data in the companion memory with the sensor fusion engine, and

awake the general purpose processor from the low-power sleep mode.

21. The non-transitory computer-readable medium of claim 20, wherein the sensor fusion engine comprises one or more hardware macros for sensor data-related algorithms.

22. The non-transitory computer-readable medium of claim 21, wherein code for configuring the sensor fusion engine comprises code for configuring the sensor fusion engine to execute a sensor data-related algorithm with one of the one or more hardware macros.

23. The non-transitory computer-readable medium of claim 20, wherein the data is read from the sensor in a polling mode or an interrupt mode.

24. The non-transitory computer-readable medium of claim 20, wherein the reading of the data from the sensor with the peripheral controller is coordinated by an Always-On Subsystem (AOSS).

25. An apparatus for power-efficiently processing sensor data comprising:

    means for processing data;

    means for fusing sensor data including means for executing sensor data-related algorithms;

    means for storing data; and

    means for controlling peripheral components,

    wherein the means for processing data is configured to provide configuration of the means for fusing sensor data and means for controlling peripheral components,

    the means for processing data is configured to enter a low-power sleep mode,

    the means for controlling peripheral components is configured to read data from a sensor and store the data into the means for storing data, and

    the means for processing data is configured to awaken from the low-power sleep mode.

26. The apparatus of claim 25, wherein the sensor data-related algorithms comprise a sensor fusion algorithm.

27. The apparatus of claim 25, wherein the means for processing data is configured to provide configuration for the means for fusing sensor data by causing the means for fusing sensor to execute a sensor data-related algorithm.

28. The apparatus of claim 25, wherein the means for processing data, the means for fusing sensor data, the means for storing data, and the means for controlling peripheral components are located within a low power island of a System on a Chip (SoC).

29. The apparatus of claim 25, wherein the reading of the data from the sensor with the means for controlling peripheral components is coordinated by an Always-On Subsystem (AOSS).

30. The apparatus of claim 25, wherein the means for fusing sensor data is part of an Always-On Subsystem (AOSS).

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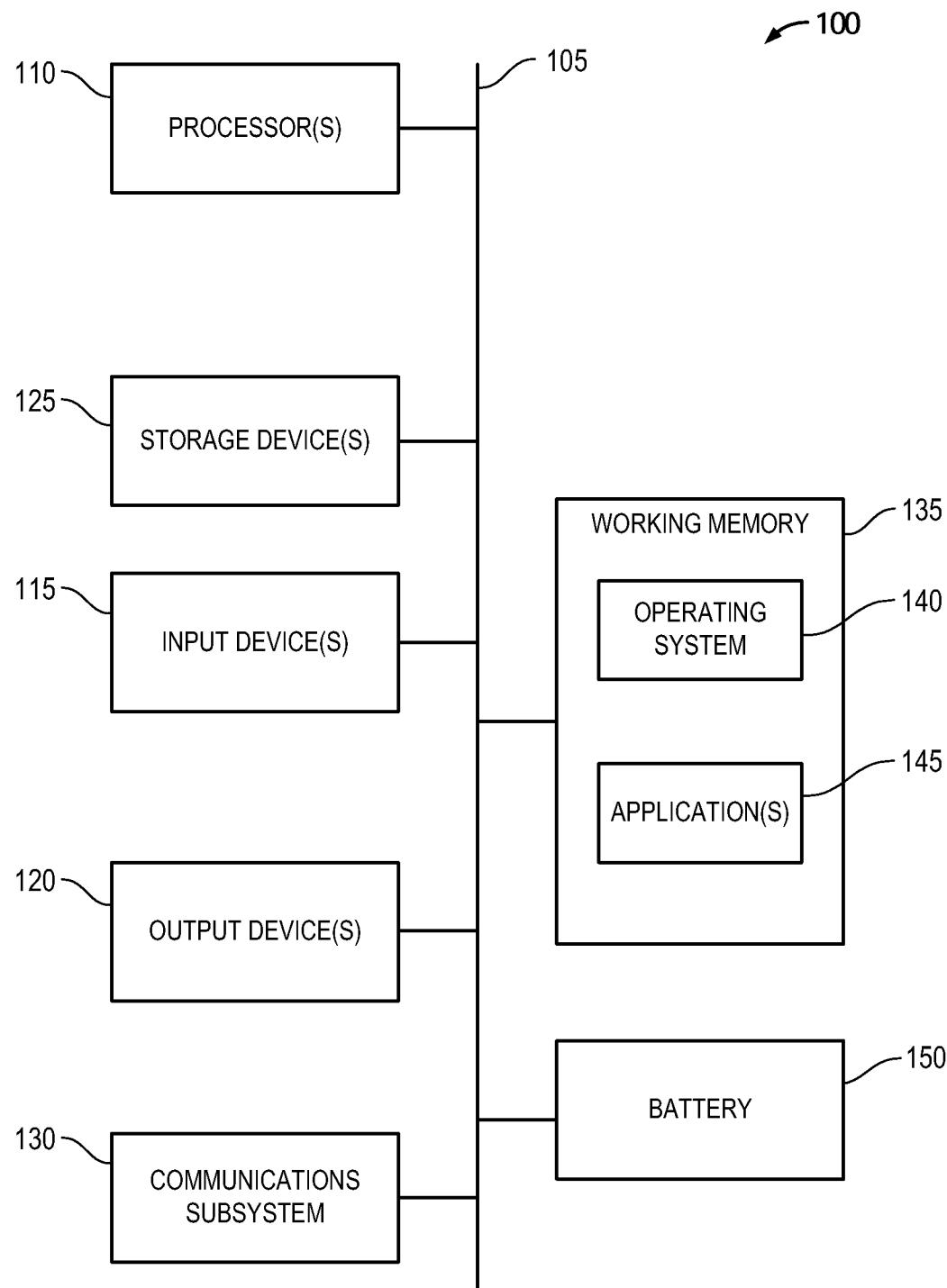
FIG. 1

2/3
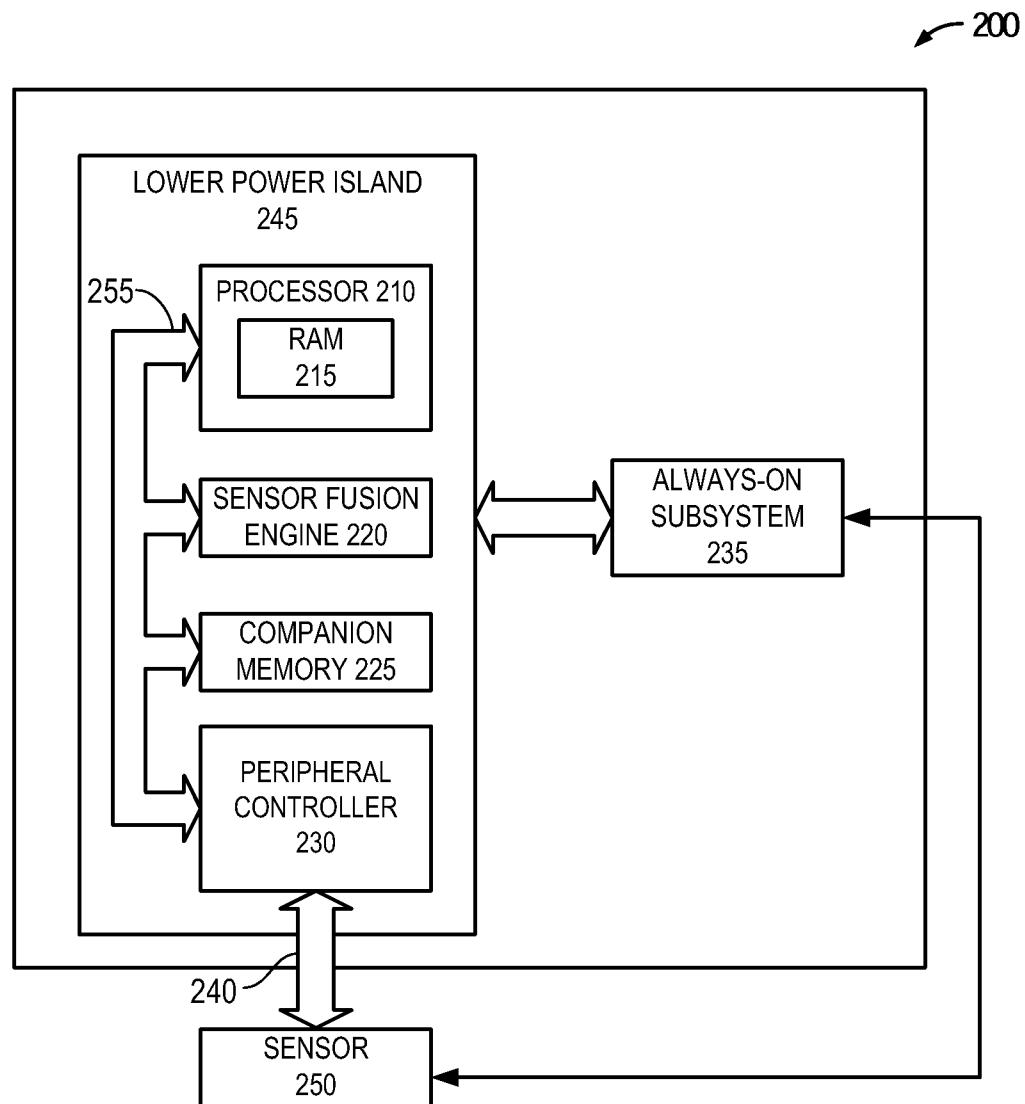
FIG. 2

3/3
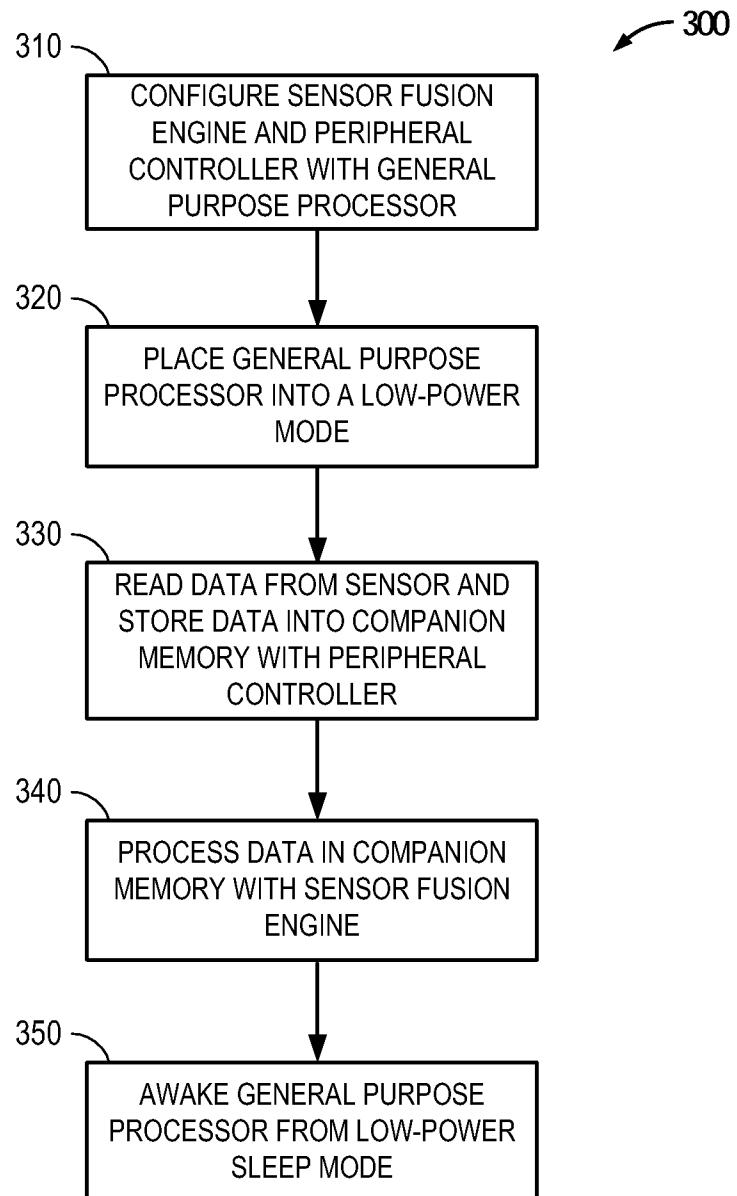
FIG. 3

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

INV. G06F1/32
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F H04W

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012/254878 A1 (INTEL CORP [US]; NACHMAN LAMA [US]; RAFFA GIUSEPPE [US]; ESSAIAN ALEXA) 4 October 2012 (2012-10-04)	1,5,6,8, 10,11, 15,16, 18,20, 23,25,28
Y	abstract; figures 1, 2, 3A, 4 paragraph [0002] paragraph [0011] - paragraph [0023] paragraph [0027] paragraph [0034] - paragraph [0037] claims 1, 6 ----- -/--	2-4,7,9, 12-14, 17,19, 21,22, 24,26, 27,29,30

[X] Further documents are listed in the continuation of Box C.   [X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
30 October 2015	09/11/2015

Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Rousset, Antoine

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C(Continuation).   DOCUMENTS CONSIDERED TO BE RELEVANT

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Y	CARLOS RODRIGUEZ-DONATE ET AL: "FPGA-Based Fused Smart Sensor for Dynamic and Vibration Parameter Extraction in Industrial Robot Links", SENSORS, vol. 10, no. 4, 26 April 2010 (2010-04-26) , pages 4114-4129, XP055224761, DOI: 10.3390/s100404114 abstract; figures 3, 4, 6, 7 page 4116, line 1 - line 10 page 4118, line 14 - page 4122, line 6 page 4127, line 1 - line 15 -----	2-4,13, 14,21, 22,26,27
A	US 2013/117769 A1 (SHARMA PIYUSH [US] ET AL) 9 May 2013 (2013-05-09) abstract; figures 2, 3, 5 paragraph [0003] - paragraph [0006] paragraph [0030] - paragraph [0033] paragraph [0037] - paragraph [0038] -----	5,15,23
Y	US 2009/259864 A1 (LI ALAN [US] ET AL) 15 October 2009 (2009-10-15) abstract; figure 1 paragraph [0020] - paragraph [0028] -----	7,9,17, 19,24, 29,30
Y	US 2007/079161 A1 (GUPTA VIKRAM [US]) 5 April 2007 (2007-04-05) abstract; figures 1-4, 7 paragraph [0014] - paragraph [0025] paragraph [0042] - paragraph [0044] -----	12
A	US 2013/238921 A1 (ALPERT YARON [IL] ET AL) 12 September 2013 (2013-09-12) abstract; figures 1-4 paragraph [0002] paragraph [0024] - paragraph [0044] -----	1-30
A	Dr P Mrs ET AL: "FPGA Implementation of Data Fusion Algorithm for Distance Measurement", International Journal of Electronics Communication and Computer Engineering Volume, 6 April 2014 (2014-04-06), pages 2249-71, XP055224767, Retrieved from the Internet: URL:http://ijecce.org/Download/conference/ Tech_Pune_2014/15.pdf [retrieved on 2015-10-30] the whole document -----	2,14,21

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C(Continuation).   DOCUMENTS CONSIDERED TO BE RELEVANT

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A	US 2009/303204 A1 (NASIRI STEVEN S [US] ET AL) 10 December 2009 (2009-12-10) abstract; figures 1, 2, 9A-C paragraph [0048] - paragraph [0060] paragraph [0182] - paragraph [0184] -----	2,14,21

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