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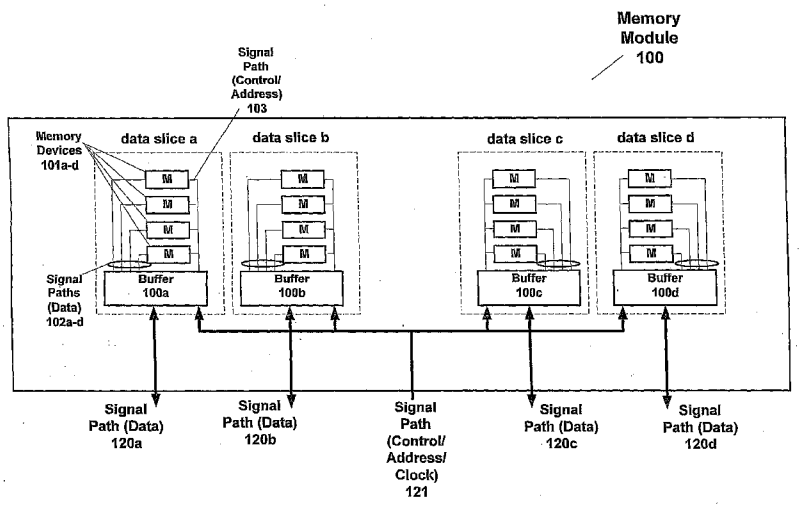
(54) **Title:** A MEMORY MODULE INCLUDING A PLURALITY OF INTEGRATED CIRCUIT MEMORY DEVICES AND A PLURALITY OF BUFFER DEVICES IN A MATRIX TOPOLOGY



(57) **Abstract:** A memory module includes a plurality of signal paths that provide data to a memory module connector interface from a plurality of respective integrated circuit buffer devices that access data from an associated plurality of integrated circuit memory devices. The memory module forms a plurality of "data slices" or a plurality of portions of the memory module data bus that is coupled to the respective integrated circuit buffer devices. Each integrated circuit buffer device is also coupled to a bus that provides control information that specifies an access to at least one integrated circuit memory devices. According to an embodiment, a SPD device stores information regarding configuration information of the memory module. In embodiments, at least one integrated circuit buffer devices access information stored in the SPD device. In a package embodiment, a package houses an integrated circuit buffer die and a plurality of integrated circuit memory dies.

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A MEMORY MODULE INCLUDING A PLURALITY OF INTEGRATED CIRCUIT MEMORY DEVICES AND A PLURALITY OF BUFFER DEVICES IN A MATRIX TOPOLOGY

FIELD OF THE INVENTION

The present invention generally relates to integrated circuit devices, high speed signaling of such devices, memory devices, and memory systems.

BACKGROUND

Some contemporary trends predict that processors, such as general purpose microprocessors and graphics processors, will continue to increase system memory and data bandwidth requirements. Using parallelism in applications such as multi-core processor architectures and multiple graphics pipelines, processors should be able to drive increases in system bandwidths at rates some predict will be doubled every three years for the next ten years. There are several major trends in dynamic random access memory ("DRAM") that may make it prohibitively costly and challenging to keep up with increasing data bandwidth and system memory requirements. For example, transistor speed relative to feature size improvements in a given DRAM technology node, and the rising costs of capital investment required to move DRAM technology to greater memory densities for a given DRAM die adversely affect the rate at which DRAM technology can keep pace with the increasing data bandwidth and system capacity requirements.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

Figure 1 illustrates a memory module topology including a plurality of integrated circuit memory devices and a plurality of integrated circuit buffer devices;

Figure 2 illustrates a memory module topology having a split multi-drop control/address bus;

Figure 3 illustrates a memory module topology having a single multi-drop control/address bus;

Figure 4 illustrates a memory module topology that provides data between each integrated circuit buffer device and a memory module connector interface;

Figure 5 illustrates a memory module topology including a plurality of integrated circuit memory devices and a plurality of integrated circuit buffer devices with an integrated circuit buffer device for control and address information;

Figure 6 illustrates termination of a control/address signal path in a memory module topology of Figure 5;

Figure 7 illustrates termination of data signal paths in a memory module topology of Figure 5;

Figure 8 illustrates termination of a split control/address signal path in a memory module topology of Figure 5;

Figure 9A illustrates a top view of a memory module topology including a plurality of integrated circuit memory devices and a plurality of integrated circuit buffer devices;

Figure 9B illustrates a side view of a memory module topology including a plurality of integrated circuit memory devices and a plurality of integrated circuit buffer devices;

Figure 9C illustrates a bottom view of a memory module topology including a plurality of integrated circuit memory devices and a plurality of integrated circuit buffer devices;

Figure 10 is a block diagram illustrating a topology of a device having a plurality of integrated circuit memory dies and an integrated circuit buffer die;

Figure 11 illustrates a multi-chip package ("MCP") device having a plurality of integrated circuit memory dies and an integrated circuit buffer die;

Figure 12 illustrates a packaged device having a plurality of integrated circuit memory dies and another packaged device having a buffer die; both packages are stacked and housed together in a single package-on-package ("POP") device;

Figure 13 illustrates a device having a plurality of integrated circuit memory devices and a buffer device that are disposed on a flexible tape;

Figure 14 illustrates a device having a plurality of integrated circuit memory dies and a buffer die that are disposed side-by-side and housed in a package;

Figure 15 illustrates a device having a plurality of integrated circuit memory dies and a buffer die that are housed in separate packages and integrated together into a larger POP device;

Figure 16 illustrates a memory module topology including a serial presence detect device ("SPD");

Figure 17 illustrates a memory module topology with each data slice having an SPD;

Figure 18 is a block diagram of an integrated circuit buffer die;

Figure 19 is a block diagram of a memory device.

DETAILED DESCRIPTION

According to embodiments, a memory module includes a plurality of signal paths that provide data to a memory module connector from a plurality of respective integrated circuit buffer devices (or dies) that access the data from an associated plurality of integrated circuit memory devices (or dies). In a specific embodiment, each integrated circuit buffer device is also coupled to a bussed signal path that provides control and/or address information that specifies an access to at least one integrated circuit memory device associated with the respective integrated circuit buffer device.

According to embodiments, a memory module connector includes a control/address interface portion and a data interface portion. A control/address bus couples a plurality of integrated circuit buffer devices to the control/address interface portion. A plurality of data signal paths couple the plurality of respective integrated circuit buffer devices to the data interface portion. Each integrated circuit buffer device includes 1) an interface to couple to at least one integrated circuit memory device, 2) an interface to couple to the control/address bus and 3) an interface to couple to a data signal path in the plurality of data signal paths.

According to embodiments, a memory module may include a non-volatile memory location, for example using an electrically erasable programmable read only memory ("EEPROM") (also known as a Serial Presence Detect ("SPD") device), to store information regarding parameters and configuration of the memory module. In embodiments, at least one integrated circuit buffer device accesses information stored in the SPD device.

In a package embodiment, a package houses an integrated circuit buffer die and the plurality of integrated circuit memory dies. In the package, a plurality of signal paths transfer data (read and/or write data)

between the integrated circuit buffer die and the plurality of integrated circuit memory dies. The integrated circuit buffer die provides control signals from an interface of the package to the plurality of integrated circuit memory dies. Data stored in memory arrays of the plurality of integrated circuit memory dies is provided to a signal path disposed on the memory module via the integrated circuit buffer die in response to the control signals. In an embodiment, the package may be a multichip package ("MCP"). In an embodiment, the plurality of integrated circuit memory dies may be housed in common or separate packages. In an embodiment described below, the memory module may include a series of integrated circuit dies (i.e., memory die and buffer die) stacked on top of one another and coupled via a signal path.

As described herein, an integrated circuit buffer device is also referred to as a buffer or buffer device. Likewise, an integrated circuit memory device is also referred to as a memory device.

In an embodiment, an integrated circuit memory device is distinguished from a memory die in that a memory die is a monolithic integrated circuit formed from semiconductor materials for storing and/or retrieving data or other memory functions, whereas an integrated circuit memory device is a memory die having at least some form of packaging or interface that allows the memory die to be accessed.

Likewise in an embodiment, an integrated circuit buffer device is distinguished from a buffer die in that a buffer die is a monolithic integrated circuit formed from semiconductor materials and performs at least one or more buffer functions described herein, whereas an integrated circuit buffer device is a buffer die having at least some form of packaging or interface that allows communication with the buffer die.

In the embodiments described in more detail below, **Figs. 1-8** illustrate control/address and data signal path topologies including a plurality of integrated circuit memory devices (or dies) and a plurality of

integrated circuit buffer devices (or dies) situated on a memory module. **Figs. 10, 18, and 19** also illustrate signal path topologies including integrated circuit memory devices (or dies) and integrated circuit buffer devices (or dies) situated on a memory module as well as the operation of an integrated circuit buffer device (or die) and memory device (or die) in embodiments among other things.

Fig. 1 illustrates a memory module topology including a plurality of integrated circuit memory devices and a plurality of associated integrated circuit buffer devices. In an embodiment, a memory module 100 includes a plurality of buffer devices 100a-d coupled to a common address/control signal path 121. Each buffer device of the plurality of buffer devices 100a-d provides access to a plurality of respective integrated circuit memory devices 101a-d via signal paths 102a-d and 103. In an embodiment, respective data slices a-d are formed by one of buffers 100a-d and sets of memory devices 101a-d. Buffer devices 100a-d are coupled to signal paths 120a-d, respectively, that transfer data (read and write data) between the buffer devices 100a-d and a memory module connector interface. In an embodiment, mask information is transferred to buffer devices 100a-d from a memory module connector interface using signal paths 120a-d, respectively.

In an embodiment, a data slice is a portion of the memory module data signal path (or bus) that is coupled to the respective integrated circuit buffer device. The data slice may include the full data path or portions of data paths to and from a single memory device disposed on the memory module.

Integrated circuit memory devices may be considered as a common class of integrated circuit devices that have a plurality of storage cells, collectively referred to as a memory array. A memory device stores data (which may be retrieved) associated with a particular address provided, for example, as part of a write or read command.

Examples of types of memory devices include dynamic random access memory ("DRAM"), including single and double data rate synchronous DRAM, static random access memory ("SRAM"), and flash memory. A memory device typically includes request or command decode and array access logic that, among other functions, decodes request and address information, and controls memory transfers between a memory array and signal path. A memory device may include a transmitter circuit to output data for example, synchronously with respect to rising and falling edges of a clock signal, (e.g., in a double data rate type of memory device). Similarly, the memory device may include a receiver circuit to receive data, for example, synchronously with respect to rising and falling edges of a clock signal or outputs data with a temporal relationship to a clock signal in an embodiment. A receiver circuit also may be included to receive control information synchronously with respect to rising and falling edges of a clock signal. In an embodiment, strobe signals may accompany the data propagating to or from a memory device and that data may be captured by a device (e.g., memory device or buffer, or controller) using the strobe signal.

In an embodiment, an integrated circuit buffer device is an integrated circuit that acts as an interface between a memory module connector interface and at least one integrated circuit memory device. In embodiments, the buffer device may store and/or route data, control information, address information and/or a clock signal to at least one integrated circuit memory device that may be housed in a common or separate package. In an embodiment, the buffer isolates, routes and/or translates data, control information and a clock signal, singly or in combination, between a plurality of memory devices and a memory module connector interface. An embodiment of a memory module connector interface is described below and shown in **Figs. 9A-C.**

At least one signal path 121, as shown in Fig. 1, disposed on memory module 100, transfers control and/or address (control/address) information between at least one of the buffer devices 100a-d and a memory module connector interface in various embodiments. In an embodiment, signal path 121 is a multi-drop bus. As illustrated in **Figs. 2-8** and described below, alternate topologies for transferring control/address information, data and clock signals between one or more buffer devices 100a-d and a memory module connector interface may be used in alternate embodiments. For example, a split multi-drop control/address bus, segmented multi-drop control/address bus, and point-to-point and/or daisy chain topologies for a data bus may be employed.

In an embodiment, clock signals and/or clock information may be transferred on at least one signal line in signal path 121. These clock signal(s) provide one or more clock signals having a known frequency and/or phase. In an embodiment, a clock signal is synchronized with or travels along side the control/address information. In an embodiment, an edge of the clock signal has a temporal relationship with an edge of a control/address signal representing the control/address information. In an embodiment, a clock signal is generated by a clock source, master device (e.g., controller device) and/or buffer device.

In an embodiment, a clock signal and/or clock information may be transferred on at least one signal line in respective signal paths 120a-d. Buffer devices 100a-d may receive and/or transmit a clock signal with data on signal paths 120a-b. In an embodiment, write data is provided to buffer devices 100a-d on signal paths 120a-d and a clock signal is provided on signal path 120a-d along side write data. In an embodiment, a clock signal (such as a clock-to-master ("CTM")) is provided from buffer devices 100a-d on signal path 120a-d along side read data on signal paths 120a-d. In an embodiment, a clock signal is synchronized

with or travels along side the write and/or read data. An edge of the clock signal has a temporal relationship or is aligned with an edge of a data signal representing write and/or read data. Clock information can be embedded in data, eliminating the use of separate clock signals along with the data signals.

In an embodiment, a read, write and/or bidirectional strobe signal may be transferred on at least one signal line in respective signal paths 120a-d. Buffer devices 100a-d may receive and/or transmit a strobe signal with data on signal paths 120a-b. In an embodiment, write data is provided to buffer devices 100a-d on signal paths 120a-d and a strobe signal is provided on signal path 120a-d along side write data. In an embodiment, a strobe signal is provided from buffer devices 100a-d on signal path 120a-d along side read data on signal paths 120a-d. In an embodiment, a strobe signal is synchronized with or travels along side the write and/or read data. An edge of the strobe signal has a temporal relationship or is aligned with an edge of a data signal representing write and/or read data.

In an embodiment, addresses (for example, row and/or column addresses) for accessing particular memory locations in a particular integrated circuit memory device and/or commands are provided on signal path 121 from a memory module connector interface. In an embodiment, a command relates to a memory operation of a particular integrated circuit memory device. For example, a command may include a write command to store write data at a particular memory location in a particular integrated circuit memory device and/or a read command for retrieving read data stored at a particular memory location from a particular integrated circuit memory device. Also, multiple memory devices in different data slices can be accessed simultaneously. In embodiments, a command may include row commands, column commands such as read or write, mask information, precharge and/or

sense command. In an embodiment, control information is transferred on signal path 121 over a common set of lines in the form of a time multiplexed packet where particular fields in the packet are used for including command operation codes and/or addresses. Likewise, packets of read data may be transferred from integrated circuit memory devices via buffers 100a-d on respective signal paths 120a-d to memory module connector interface. In an embodiment, a packet represents one or more signals asserted at particular bit windows (or a time interval) for asserting a signal on particular signal lines.

In embodiments, memory module 100 communicates (via a memory module connector interface) with a master device (e.g., a processor or controller).

Fig. 2 illustrates an embodiment of a memory module topology having a split multi-drop control/address/clock bus. In particular, memory module 200 includes a split multi-drop control/address bus 221 coupled to buffers 100a-d and a memory module connector interface. With reference to **Fig. 2**, a first portion of bus 221 is terminated by termination 230 and a second portion of bus 221 is terminated by termination 231. In an embodiment, the impedance of termination 230 matches the impedance of the first portion of bus 221 (Z0) coupled to buffers 100c-d and the impedance of termination 231 matches the impedance of the second portion of bus 221 (Z1) coupled to buffers 100a-b. In an embodiment, impedance Z0 equals impedance Z1. In embodiments, terminations 230 and 231, singly or in combination, are disposed on memory module 100, buffer devices 100a and 100d or packages used to house buffer devices 100a and100d.

Fig. 3 illustrates a memory module topology having a single multi-drop control/address/clock bus terminated by termination 330. In an embodiment, the impedance of termination 330 matches the impedance of signal path 121 (or control/address/clock bus). In embodiments,

termination 330, singly or in combination, is disposed on memory module 300 or on buffer device 100d.

Fig. 4 illustrates a memory module topology that provides data between each integrated circuit buffer device and a memory module connector interface. In an embodiment, each signal path 120a-d is terminated by an associated termination 420a-d, respectively. In an embodiment, terminations 420a-d have respective impedances that match the impedance Z0 of each of the signal paths 120a-d. In embodiments, terminations 420a-d, singly or in combination, are disposed on memory module 400, each of buffer devices 100a-d or packages used to house buffer devices 100a-d.

Referring to **Fig. 1**, a control/address signal rate ratio of signal path 121 to signal path 103 may be 2:1 (or other multiples such as 4:1, 8:1, etc.) so that a memory module connector interface is able to operate as fast as specified while memory devices 101a-d may operate at half (quarter, eighth, etc) the control/address signaling rate so that relatively lower cost memory devices may be used. Similarly, a data signal rate of one of signal paths 102a-d to one of signal paths 120a-d may be 2:1 (or other multiple such as 4:1, 8:1, etc) so that a memory module connector interface is able to operate as fast as specified while memory devices 101a-d may operate at half (quarter, eighth, etc.) the data signaling rate so that relatively lower cost memory devices may be used.

Fig. 5 illustrates a memory module topology including a plurality of integrated circuit memory devices and a plurality of integrated circuit buffer devices with an integrated circuit buffer device 501 for control, address and/or clock information. Memory module 500 is similar to memory module 100 except that buffer device 501 is coupled to signal paths 121 and 121a-b. Buffer device 501 outputs control, address and/or clock information to buffer devices 100a-b on signal path 121a and to buffer devices 100c-d on signal path 121b. In an embodiment

buffer device 501 copies control, address and/or clock information received on signal path 121 and repeats the control, address and/or clock information on signal paths 121a-b. In an embodiment, buffer device 501 is a clocked buffer device that provides a temporal relationship with control and address information provided on signal paths 121a-b. In an embodiment, signal paths 121a-b include at least one signal line to provide a clock signal and/or clock information. In an embodiment, buffer device 501 includes a clock circuit 1870 as shown in **Fig. 18**. In an embodiment, buffer device 501 receives control information, such as a packet request, that specifies an access to at least one of the integrated circuit memory devices 101a-d and outputs a corresponding control signal (on signal path 121a and/or 121b) to the specified integrated circuit memory device.

Fig. 6 illustrates a memory module topology similar to that illustrated in **Fig. 5** except that a termination 601 is coupled to signal path 121 on memory module 600. In an embodiment, the impedance of termination 601 matches the impedance Z0 of signal path 121. In embodiments, termination 601 is disposed on memory module 600, buffer device 501 or a package used to house buffer device 501.

Fig. 7 illustrates a memory module topology that provides data to and/or from each integrated circuit buffer device and terminations coupled to signal paths. In an embodiment, each signal path 120a-d is terminated by associated terminations 701a-d, respectively. In an embodiment, terminations 701a-d have respective impedances that match the impedance Z0 of each of the signal paths 120a-d. In embodiments, terminations 701a-d, singly or in combination, are disposed on memory module 700, buffer devices 100a-d or packages used to house buffer devices 100a-d.

Fig. 8 illustrates a memory module topology having a split multi-drop signal path between a buffer device for control, address and/or

clock information and the plurality of buffer devices. In particular, memory module 800 includes a split multi-drop control/address bus 121a-b coupled to buffers 100a-d and a buffer device 501. In an embodiment, a first portion of bus 121a is terminated by termination 801 and a second portion of bus 121b is terminated by termination 802. In an embodiment, the impedance of termination 801 matches the impedance of the first leg (Z0) and the impedance of termination 802 matches the impedance of the second leg (Z1). In an embodiment, impedance Z0 equals impedance Z1. In embodiments, terminations 801 and 802, singly or in combination, are disposed on memory module 800, buffer devices 100a and 100d or packages used to house buffer devices 100a and 100d.

Referring to **Fig. 5**, a control/address signal rate ratio of signal path 121 to signal path 121a (or 121b) to signal path 103 may be 2:1:1 (or other multiples such as 4:1:1, 8:1:1, etc.) so that other multi-drop bus topology embodiments using signal paths 121a (or 121b) and signal path 103 do not have to necessarily operate as high a signal rate as an embodiment that uses signal path 121 as shown in **Fig. 1**. Also like **Fig. 1**, a control/address signal rate ratio of signal path 121 to signal path 103 may be 2:1 (or other multiples such as 4:1, 8:1, etc.) so that a memory module connector interface is able to operate as fast as specified while memory devices 101a-d may operate at half (or quarter, eighth, etc.) the control/address signaling rate so that relatively lower cost memory devices may be used. Similarly, a data signal rate of one of signal paths 102a-d to one of signal paths 120a-d may be 2:1 (or other multiple such as 4:1, 8:1, etc.) so that a memory module connector interface is able to operate as fast as the specified signaling rate while memory devices 101a-d may operate at half (or quarter, eighth, etc.) the data signaling rate so that relatively lower cost memory devices may be used.

Fig. 9A illustrates a top view of a memory module topology including a plurality of integrated circuit memory devices and a plurality of integrated circuit buffer devices coupled to a connector interface. In an embodiment, memory module 900 includes a substrate 910 having a standard dual in-line memory module ("DIMM") form factor or other module form factor standards, such as small outline DIMM ("SO-DIMM") and very low profile DIMM ("VLP-DIMM"). In alternate embodiments, substrate 910 may be, but is not limited to, a wafer, printed circuit board ("PCB"), package substrate like BT epoxy, flex, motherboard, daughterboard or backplane, singly or in combination.

In an embodiment, memory module 900 includes pairs of memory devices 101a-b and buffer devices 100a-d disposed on a first side of substrate 910. In alternate embodiments, more or less memory devices and buffer devices are used. In an embodiment, pairs of memory devices 101c-d are also disposed on a second side of memory module 900 as shown in a side and bottom view of memory module 900 in **Figs. 9B and 9C**. In an embodiment, each memory device and buffer device are housed in separate packages. In alternate embodiments, memory devices and buffer devices may be housed in MCP package embodiments described herein.

Memory module 900 includes connector interface 920 that has different interface portions for transferring data and control/address/clock signals. For example, a first side of memory module 900 includes connector interface portions 920a-d used to transfer data signals and a connector interface portion 930a used to transfer control/address signals. In an embodiment, connector interface portion 930a also transfers a clock signal and/or clock information. In an embodiment, a second side of memory module 900 including connector interface portions 920e-h are used to transfer data signals and a connector interface portion 930b is used to transfer control/address signals. In an

embodiment, connector interface portion 930b also transfers a clock signal and/or clock information.

In an embodiment, connector interface 920 is disposed on an edge of substrate 910. In an embodiment, a memory module 900 is inserted into a socket 940 disposed on substrate 950. In an embodiment, substrate 950 is a main board or PCB with signal paths 960a-b for transferring signals on substrate 950. In an embodiment, signal paths 960a and 960b are signal traces or wires. In an embodiment, signal paths 960a and 960b are coupled to other sockets disposed on substrate 950 that may have another memory module inserted and/or coupled to a master.

In an embodiment, connector interface portions include at least one contact or conducting element, such as a metal surface, for inputting and/or outputting an electrical signal. In alternate embodiments, a contact may be in the form of a ball, socket, surface, signal trace, wire, a positively or negatively doped semiconductor region and/or pin, singly or in combination. In an embodiment, a connector interface as described herein, such as connector interface 920, is not limited to physically separable interfaces where a male connector or interface engages a female connector (or socket 940) or interface. A connector interface also includes any type of physical interface or connection, such as an interface used in a system-in-a-package ("SIP") where leads, solder balls or connections from a memory module are soldered to a circuit board.

In an alternate embodiment, memory module 900 is included in an embedded memory subsystem, such as one in a computer graphics card, video game console or a printer. In an alternate embodiment, memory module 900 is situated in a personal computer or server.

In an embodiment, a master communicates with memory modules illustrated in Figs. 1-9 and 16-17. A master may transmit and/or receive

signals to and from the memory modules illustrated in Figs. 1-9 and 16-17. A master may be a memory controller, peer device or slave device. In embodiments, a master is a memory controller, which may be an integrated circuit device that contains other interfaces or functionality, for example, a Northbridge chip of a chipset. A master may be integrated on a microprocessor or a graphics processor unit ("GPU") or visual processor unit ("VPU"). A master may be implemented as a field programmable gate array ("FPGA"). Memory modules, signal paths, and a master may be included in various systems or subsystems such as personal computers, graphics cards, set-top boxes, cable modems, cell phones, game consoles, digital television sets (for example, high definition television ("HDTV")), fax machines, cable modems, digital versatile disc ("DVD") players or network routers.

In an embodiment, a master, memory modules and signal paths are in one or more integrated monolithic circuits disposed in a common package or separate packages.

Fig. 10 is a block diagram illustrating and embodiment of a device 1000 having a plurality of integrated circuit memory devices 101a-d and a buffer 100a. Here, data (read and/or write) may be transferred between the plurality of integrated circuit memory devices 101a-d and buffer 100a on a signal path 1006 (data). Signal path 1006 is a signal path situated internal to device 1000 and corresponds to signal paths 1113a-d and 1114 shown in **Fig. 11**. Signal path 1006 is a bus for providing bidirectional data signals between a plurality of integrated circuit memory devices 101a-d and buffer 100a. An example of bidirectional data signals includes signals traveling from one or more of integrated circuit memory devices 101a-d to buffer 100a and also signals traveling from buffer 100a to one or more of integrated circuit memory devices 101a-d). Signal path 1005 is a signal path internal to device 1000 and corresponds to signal paths 1116a-d and 1117 shown in **Fig.**

11. Signal path 1005 is a bus for providing unidirectional control/address/clock signals from a buffer 100a to a plurality of integrated circuit memory devices 101a-d. In an example of a unidirectional bus, signals travel in only one direction, i.e., in this case, from only buffer 100a to one or more of integrated circuit memory devices 101a-d). Signal path 1005 includes individual control signal lines, for example, a row address strobe line, column address strobe line, etc., and address signal lines. Signal path 1005 may include a fly-by clock line to transfer a clock signal from buffer 100a to integrated circuit memory devices 101a-d. Signal path 1005 may transfer a clock signal from one or more integrated circuit memory devices 101a-d to buffer 100a.

In an embodiment, buffer 100a communicates with an SPD device to store and retrieve parameters and configuration information regarding device 1000 and/or memory module 900. In an embodiment, an SPD 1002 is a non-volatile storage device. Signal path 1004 couples SPD 1002 to buffer 100a. In an embodiment, signal path 1004 is an internal signal path for providing bidirectional signals between SPD 1002 and buffer 100a.

In an embodiment, SPD 1002 is an EEPROM device. However, other types of SPD 1002 are possible, including but not limited to a manual jumper or switch settings, such as pull-up or pull-down resistor networks tied to a particular logic level (high or low), which may change state when a memory module is added or removed from a system.

In an embodiment, SPD 1002 is a memory device that includes registers that stores configuration information that can be easily changed via software during system operation, allowing a high degree of flexibility, and making configuration operations that are transparent to an end user.

In an embodiment illustrated in **Fig. 18**, functionality of the SPD mentioned above may be integrated into buffer device 100a using a

register set, such as configuration register set 1881. Referring to **Fig. 18**, SPD logic and interface 1820c may be preconfigured with information pertaining to the buffer and memory devices connected to the buffer, or may store information pertaining to only one of the memory devices or the buffer device 100a. Control inputs to the buffer may determine when a storage node within the register set will sample the information to preload or preconfigure the SPD logic and interface 1820c. The term register may apply either to a single-bit-wide register or multi-bit-wide register.

In an embodiment illustrated by Fig. 10, SPD 1002 stores information relating to configuration information of memory module 900. For example, configuration information may include repair and redundancy information to repair a defective memory device, defective memory cells or peripheral circuits on a memory device, and/or signal path. In an embodiment, SPD configuration information includes memory module population topology, such as a number, a position and a type of memory device in a package and/or on a memory module, or rank, if any. In an embodiment, SPD configuration information includes a serialization ratio for interfaces in a buffer and/or information regarding configuring the width of a buffer. In an embodiment, SPD configuration information includes a first value that represents the desired width of buffer device 100a or includes multiple values that represent the range of possible widths of the buffer device 100a, and a second value that represents the desired width of interface 1820b as illustrated in **Fig. 18**.

In an embodiment, SPD configuration information includes timing information or parameters for accessing memory devices, such as a time to access a row or the memory device, a time to access a column of the memory device, a time between a row access and a column access, a time between a row access and a precharge operation, a time between a row sense applied to a first bank of a memory array and a

row sense applied to a second bank of the memory array and/or a time between a precharge operation applied to a first bank in a memory array and a precharge operation applied to a second bank of the memory array.

In an embodiment, the stored timing information may be expressed in terms of time units where a table of values maps specific time units to specific binary codes. During an initialization or calibration sequence, a master or a buffer may read SPD configuration information and determine the proper timing information for one or more memory devices. For example, a master may also read information representing the clock frequency of a clock signal from an SPD 1002, and divide the retrieved timing information by a clock period of a clock signal. (The clock period of the clock signal is the reciprocal of the clock frequency of the clock signal). Any remainder resulting from this division may be rounded up to the next whole number of clock cycles of the clock signal.

Signal paths 120a and 121, as shown in Fig. 10, are coupled to buffer 100a. In an embodiment, signal path 120a transfers unidirectional control/address/clock signals to buffer 100a. In an embodiment, signal path 121 transfers bidirectional or unidirectional data signals to and from buffer 100a. Other interconnect and external connect topologies may also be used for device 1000 in alternate embodiments. For example, buffer 100a may be coupled to a single multi-drop control bus, a split multi-drop control bus, or a segmented multi-drop bus.

In an embodiment, device 1000 has two separate power sources. Power source V1 supplies power to one or more memory devices (memory devices 101a-d) on memory module 900. Power source V2 supplies power to one or more buffers (buffer 100a) on memory module 900. In an embodiment, the buffer 100a has internal power regulation circuits to supply power to the memory devices 101a-d.

Fig. 11 illustrates a device 1100 including a plurality of integrated circuit memory dies 1101a-d and a buffer die 1100a housed in or upon a common package 1110 according to embodiments. As described herein in other embodiments and illustrated in **Figs. 12-15**, a plurality of integrated circuit memory dies 1101a-d and buffer 1100a are disposed in multiple package type embodiments. For example, a plurality of integrated circuit memory dies 1101a-d and a buffer die 1100a may be stacked, on a flexible tape, side-by-side or positioned in separate packages on a device substrate. Buffer die 1100a is used to provide signals, including control/address/clock information and data, between a plurality of integrated circuit memory dies 1101a-d and a device interface 1111 that includes contacts 1104a-f. In an embodiment, one or more contacts 1104a-f is similar to contacts of connector interface 920. Contacts 1104a-f are used to couple device 1100 to substrate 910, and in particular to signal paths 120a and 121, of memory module 100 in an embodiment. Device interface 1111 also includes signal paths 1118 and 1115 to transfer signals between contacts 1104a-f and buffer 100a via buffer interface 1103. Signals are then transferred between a plurality of memory dies 1101a-d and buffer die 1100a via buffer interface 1103 and signal paths 1117 (disposed in device interface 1111) and 1116a-d as well as signal paths 1114 (disposed in device interface 1111) and 1113a-d. In an embodiment, spacers 1102a-c are positioned between integrated circuit memory dies 1101a-d. In an embodiment, spacers 1102a-c are positioned to dissipate heat. Similarly, buffer die 1100a is disposed away from a plurality of integrated circuit memory dies 1101a-d to alleviate heat dissipation near the memory devices. In an embodiment, signal paths are coupled to each other and integrated circuit memory dies 1101a-d by a solder ball or solder structure.

Fig. 12 illustrates a stacked package device 1200 having a package 1210 containing a plurality of integrated circuit memory dies

1101a-d and a separate package 1290 having a buffer die 1100a. Both packages 1210 and 1290 are stacked and housed to make device 1200. In an embodiment, a plurality of integrated circuit memory dies has separate packages and is stacked on package 1290. Device 1200 has similar components illustrated in **Fig. 11**. Buffer die 1100a communicates with a plurality of integrated circuit memory dies 1101a-d as described herein. Device 1200 has memory dies 1101a-d stacked upon buffer die 1100a and separated by contacts 1201a-d. In an embodiment, contacts 1201a-d are solder balls that couple signal paths 1117 and 1114 to signal paths 1202 and 1203 that are coupled to buffer interface 1103.

Fig. 13 illustrates devices 1300 and 1301 having a plurality of integrated circuit memory devices 101a-b (101a-c in device 1301) and a buffer device 100a that are disposed on a flexible tape 1302 according to embodiments. Buffer device 100a communicates with a plurality of integrated circuit memory devices as described herein. Signal path 1305 disposed on or in flexible tape 1302 transfers signals between a plurality of integrated circuit memory devices 101a-c and buffer 100a. Contacts, such as a grid array of balls 1304, couple each integrated circuit memory device in a plurality of integrated circuit memory devices 101a-c and a buffer 100a to signal path 1305 in flexible tape 1302 in an embodiment. Adhesive 1303 may be used to couple a plurality of integrated circuit memory devices 101a-c to each other and to a buffer 100a in an embodiment. Device 1300 and 1301 are disposed in common package in an embodiment.

Fig. 14 illustrates a device 1400 having a plurality of integrated circuit memory dies 1101a-d and 1401a-d and a buffer die 1100a that are disposed side-by-side and housed in a package 1410. Device 1400 has similar components illustrated in **Fig. 11**. Buffer die 1100a communicates with a plurality of integrated circuit memory dies 1101a-d

and 1401a-d as described herein. In an embodiment, a plurality of integrated circuit memory dies 1101a-d and 1401a-d and a buffer die 1100a are disposed side-by-side on a substrate 1450 that is coupled to device interface 1411. A plurality of integrated circuit memory dies 1401a-d is separated by spacers 1402a-c. In an embodiment, a single integrated circuit memory die 1101d and a single integrated circuit memory die 1401d are disposed side-by-side with buffer die 1100a. Device interface 1411 includes contacts 1104a-f. Signals are transferred between buffer interface 1103 and contacts 1104a-f by signal paths 1418 and 1415. Signals are transferred between buffer interface 1103 and signal paths 1116a-d (or integrated circuit memory dies 1101a-d) by signal path 1417. Similarly, signals are transferred between buffer interface 1103 and signal paths 1113a-d (or integrated circuit memory dies 1401a-d) by signal path 1414.

Fig. 15 illustrates a device 1500 having a plurality of integrated circuit memory dies 1101a-b and a buffer die 1100a that are housed in separate packages 1501, 1505 and 1520, respectively. Device 1500 has similar components illustrated in **Fig. 11**. Buffer die 1100a communicates with integrated circuit memory dies 1101a-b as described herein. Integrated circuit memory dies 1101a-b and a buffer die 1100a are disposed on substrate 1530 that includes signal paths 1504, 1509, 1515 and 1518. Integrated circuit memory die 1101a includes memory interface 1507 having contacts 1508. Integrated circuit memory die 1101b includes memory interface 1503 having contacts 1541. Buffer die 1100a includes a buffer interface 1103 having contacts 1560. Signals are transferred between buffer interface 1103 and contacts 1104a-f by signal paths 1515 and 1518. Signals are transferred between buffer interface 1103 and integrated circuit memory die 1101a by signal path 1509 via memory interface 1507 and contacts 1508. Similarly, signals are transferred between buffer interface 1103 and integrated circuit

memory die 1101b by signal path 1504 via memory interface 1503 and contacts 1541. As described herein, device 1500 is coupled to a memory module 900 via contacts 1104a-f.

Fig. 16 illustrates a memory module having an SPD 1603 according to an embodiment. Memory module 1610 includes a plurality of integrated circuit memory devices (or dies) and buffer devices (or dies) disposed on substrate 930 along with SPD 1603. **Fig. 16** illustrates a memory module 1610 having a single SPD 1603 that can be accessed by each buffer device 100a-b positioned on substrate 930. Signal path 1601 allows access to SPD 1603 from connector interface 920 and one or more buffers 100a-b. In an embodiment, signal path 1601 is a bus. SPD 1603 may have configuration and/or parameter information written to or read by a master by way of connector interface 920 and signal path 1601. Likewise, buffers 100a-b may write to or read from SPD 1603 via signal path 1601.

Fig. 17 illustrates a memory module 1710 with each device 1711a-b or data slice a-b having an associated SPD 1720a-b, buffer device (or die) 100a-b and at least one integrated circuit memory device 101a (or die) according to an embodiment. The plurality of buffers 100a-b and associated plurality of SPDs 1720a-b are disposed on substrate 930. Configuration and/or parameter information is accessed from SPDs 1720a-b using signal path 1701, which is coupled, to connector interface 920 and each SPD 1720a-b. In particular, signal path 1701 couples SPD 1720a-b of device 1711a-b to connector interface 920. In an embodiment, signal path 1701 is a bus. In an alternate embodiment, signal path 1701 couples SPD 1720a and SPD 1720b in a daisy chain or serial topology. In an embodiment, one or more buffer devices 100a-b of devices 1711a-b may access (read and/or write) respective SPDs 1720a-b. Likewise, a master may access (read and/or write) respective SPDs 1720a-b using signal path 1701. In an embodiment, configuration

and/or parameter information is transferred using a header field or other identifier so that SPDs coupled in a daisy chain may forward the SPD information to the intended destination SPD.

Fig. 18 illustrates a block diagram of a buffer device 100a (or die, such as buffer die 1100a) according to embodiments. Buffer 100a includes buffer interface 1103a, interfaces 1820a-c, redundancy and repair circuit 1883, multiplexer 1830, request and address logic circuit 1840, data cache and tags circuit 1860, computations circuit 1865, configuration register set 1881, and clock circuit 1870, singly or in combination.

In a memory read operation embodiment, buffer 100a receives control information (including address information) that may be in a packet format from a master on signal path 121 and in response, transmits corresponding signals to one or more, or all of memory devices 101a-d on one or more signal paths 1005. One or more of memory devices 101a-d may respond by transmitting data to buffer 100a which receives the data via one or more signal paths 1006 and in response, transmits corresponding signals to a master (or other buffer). A master transmits the control information via one or more signal paths 121 and receives the data via one or more signal paths 120a.

By bundling control and address information in packets, protocols required to communicate to memory devices 101a-d are independent of the physical control/address interface implementation.

In a memory write operation embodiment, buffer 100a receives control information (including address information) that may be in a packet format from a master on signal path 121 and receives the write data for one or more memory devices 101a-d that may be in a packet format from a master on signal path 120a. Buffer 100a then transmits corresponding signals to one or more, or all of memory devices 101a-d on one or more signal paths 1006 so that the write data may be stored.

A master transmits the control/address/clock information via one or more signal paths 121 and transmits the write data via one or more signal paths 120a.

In an embodiment, simultaneous write and/or read operations may occur for different memory devices in memory devices 101a-d.

In an embodiment, control information that is provided to buffer 100a causes one or more memory operations (such as write and/or read operations) of one or more memory devices 100a-d, while the same control information may be provided to buffer 100b which causes the same memory operations of one or more memory devices 100a-d associated with buffer 100b. In another embodiment, the same control information may be provided to buffer 100a and buffer 100b, yet different memory operations occur for the one or more memory devices 100a-d associated with each buffer 100a-b.

In an embodiment, buffer interface 1103a couples signal paths 121 and 120a to buffer 100a as shown in **Fig. 10.** In an embodiment, buffer interface 1103a corresponds to buffer interface 1103 shown in **Figs. 11, 12, 14 and 15**. In an embodiment, buffer interface 1103a includes at least one transceiver 1875 (i.e. transmit and receive circuit) coupled to signal path 120a to transmit and receive data and at least one receiver circuit 1892 coupled to signal path 121 to receive control/address/clock information. In an embodiment, signal paths 121 and 120a include point-to-point links. Buffer interface 1103a includes a port having at least one transceiver 1875 that connects to a point-to-point link. In an embodiment, a point-to-point link comprises one or a plurality of signal lines, each signal line having no more than two transceiver connection points. One of the two transceiver connection points is included on buffer interface 1103a. Buffer interface 1103a may include additional ports to couple additional point-to-point links between buffer 100a and other buffer devices on other devices and/or memory

modules. These additional ports may be employed to expand memory capacity as is described in more detail below. Buffer 100a may function as a transceiver between a point-to-point link and other point-to-point links. In an embodiment, buffer interface 1103a includes a repeater circuit 1899 to repeat data, control information and/or a clock signal. In an embodiment, buffer interface 1103a includes a bypass circuit 1898 to transfer signals between connector interface portions.

In an embodiment, termination 1880 is disposed on buffer 100a and is connected to transceiver 1875 and signal path 120a. In this embodiment, transceiver 1875 includes an output driver and a receiver. Termination 1880 may dissipate signal energy reflected (i.e., a voltage reflection) from transceiver 1875. Termination 1880, as well as other termination described herein, may be a resistor or capacitor or inductor, singly or a series/parallel combination thereof. In alternate embodiments, termination 1880 may be external to buffer 100a. For example, termination 1880 may be disposed on a substrate 910 of a memory module 900 or on a package used to house buffer 100a.

Interface 1820a includes at least one transmitter circuit 1893 coupled to signal path 1005 to transmit control/address/clock information to one or more memory devices. In an embodiment, interface 1820a includes a transceiver that may transfer control/address/clock information between buffers disposed on a common memory module or different memory modules.

Interface 1820b includes a transceiver 1894 coupled to signal path 1006 to transfer data between buffer 100a and one or more memory devices 101a-d as illustrated in **Fig. 10**. SPD logic and interface 1820c includes a transceiver 1896 coupled to signal path 1004 to transfer configuration and/or parameter information between buffer 100a and an SPD 1002 as illustrated in **Fig. 10**. In an embodiment,

interface 1820c is used to transfer configuration and/or parameter information as illustrated in **Figs. 16 and 17**.

According to an embodiment, multiplexer 1830 may perform bandwidth-concentrating operations between buffer interface 100a and interface 1820b as well as route data from an appropriate source (i.e. target a subset of data from memory devices, internal data, cache or write buffer). The concept of bandwidth concentration involves combining the (smaller) bandwidth of each data path coupled to a memory device in a multiple data signal path embodiment to match the (higher) overall bandwidth utilized by buffer interface 1103a. In an embodiment, multiplexing and demultiplexing of throughput between the multiple signal paths that may be coupled to interface 1820b and buffer interface 1103a is used. In an embodiment, buffer 101a utilizes the combined bandwidth of multiple data paths coupled to interface 1820b to match the bandwidth of interface buffer interface 1103a.

In an embodiment, data cache and tags circuit 1860 (or cache 1860) may improve memory access time by providing storage of most frequently referenced data and associated tag addresses with lower access latency characteristics than those of the plurality of memory devices. In an embodiment, cache 1860 includes a write buffer that may improve interfacing efficiency by utilizing available data transport windows over an external signal path to receive write data and address/mask information. Once received, this information is temporarily stored in a write buffer until it is ready to be transferred to at least one memory device over interface 1820b.

Computations circuit 1865 may include a processor or controller unit, a compression/decompression engine, etc., to further enhance the performance and/or functionality of buffer 100a. In an embodiment, computations circuit 1865 controls the transfer of control/address/clock

information and data between buffer interface 1103a and interfaces 1820a-c.

Clock circuit 1870 may include a clock generator circuit (e.g., Direct Rambus® Clock Generator), which may be incorporated onto buffer 101a and thus may eliminate the need for a separate clock generating device.

In an alternate embodiment, clock circuit 1870 include clock alignment circuits for phase or delay adjusting an internal clock signal with respect to an external clock signal, such as a phase lock loop ("PLL") circuit or delay lock loop ("DLL") circuit. Clock alignment circuits may utilize an external clock from an existing clock generator, or an internal clock generator to provide an internal clock, to generate internal synchronizing clock signals having a predetermined temporal relationship with received and transmitted data and/or control information.

In an embodiment, clock circuit 1870 receives a first clock signal having a first frequency via signal path 121 and generates a second clock signal (via interface 1820a) to memory device 101a using the first clock signal and also generates a third clock signal (via interface 1820a) to memory device 101b using the first clock signal. In an embodiment, the second and third clock signals have a predetermined temporal (phase or delay) relationship with the first clock signal.

In an embodiment, a transmit circuit (such as in transceivers 1875, 1896 and 1894 shown in **Fig. 18**) transmits a differential signal that includes encoded clock information and a receiver circuit (such as in transceiver 1875, 1896 and 1894) receives a differential signal that includes encoded clock information. In this embodiment, a clock and data recovery circuit (such as clock circuit 1870) is included to extract the clock information encoded with the data received by the receiver circuit. Likewise, clock information may be encoded with data

transmitted by the transmit circuit. For example, clock information may be encoded onto a data signal, by ensuring that a minimum number of signal transitions occur in a given number of data bits.

In an embodiment, a transceiver 1875 transmits and receives a first type of signal (for example, a signal having specified voltage levels and timing), while transceivers 1894 (and/or transmit circuit 1893) transmits and receives a second different type of signal. For example, transceiver 1875 may transmit and receive signals for a DDR2 memory device and transceivers 1894 may transmit and receive signals for a DDR3 memory device.

In an embodiment, the control information and/or data that is provided to buffer 100a (by way of signal paths 121 and 120) may be in a different protocol format or have different protocol features than the control information and/or data provided to one or more memory devices 100a-d from buffer 100a. Logic (for example computation circuit 1865) in buffer 100a performs this protocol translation between the control information and/or data received and transmitted. A combination of the different electrical/signaling and control/data protocol constitute an interface standard in an embodiment. Buffer 100a can function as a translator between different interface standards – one for the memory module interface (for example connector interface 920) and another for one or more memory devices 100a-d. For example, one memory module interface standard may require reading a particular register in a particular memory device disposed on the memory module. Yet, a memory module may be populated with memory devices that do not include the register required by the memory module interface standard. In an embodiment, buffer 100a may emulate the register required by the memory module interface standard and thus allow for the use of memory devices 100a-d that operates under a different interface standard. This buffer functionality, combined with the module topology and architecture,

enables a memory module to be socket compatible with one interface standard, while using memory devices with a different interface standard.

In an embodiment, buffer 100a includes a redundancy and repair circuit 1883 to test and repair the functionality of memory cells, rows or banks of a memory device, entire memory devices (or periphery circuits) and/or signal paths between buffer 100a and memory devices 101a-d. In an embodiment, redundancy and repair circuit 1883 periodically, during a calibration operation and/or during initialization, tests one or more of memory devices 101a-d by writing a predetermined plurality of values to a storage location in a selected memory device (for example, using transceiver 1894 and a look-up table storing the predetermined values) using a selected data path and then reading back the stored predetermined plurality of values from the selected memory device using the selected data path. In an embodiment, when the values read from the storage location of the selected memory device do not match the values written to the storage location, redundancy and repair circuit 1883 eliminates access by buffer 100a to the selected memory device and/or selected signal path. In an embodiment, a different signal path to a different memory device may be selected and this testing function may be performed again. If selecting the different signal path results in an accurate comparison of read predetermined values to the predetermined values in redundancy and repair circuit 1883 (or a pass of the test), the different memory address to a different memory location, within or to another memory device, is selected or mapped thereafter. Accordingly, future write and/or read operations to the defective memory location will not occur.

In an embodiment, any multiplexed combination of control information (including address information) and data intended for memory devices 101a-d coupled with buffer 100a is received via buffer

interface 1103a, which may, for example extract the address and control information from the data. For example, control information and address information may be decoded and separated from multiplexed data on signal path 120a and provided on signal path 1895 to request and address logic circuit 1840 from buffer interface 1103a. The data may then be provided to configurable serialization/deserialization circuit 1891. Request and address logic circuit 1840 generates one or more control signals to transmitter circuit 1893.

Interfaces 1820a and 1820b include programmable features in embodiments. A number of control signal lines and/or data signal lines between buffer 100a and memory devices 101a-d are programmable in order to accommodate different numbers of memory devices. Thus, more dedicated control signal lines are available with an increased number of memory devices. Using programmable dedicated control lines and/or data lines avoids any possible load issues that may occur when using a bus to transfer control signals between memory devices and a buffer 100a. In another embodiment, additional data strobe signals for each byte of each memory device may be programmed at interface 1820b to accommodate different types of memory devices, such as legacy memory devices that require such a signal. In still a further embodiment, interface 1820a and 1820b are programmable to access different memory device widths. For example, interfaces 1820a and 1820b may be programmed to connect to 16 "x4" width memory devices, 8 "x8" width memory devices or 4 "x16" width memory devices. Likewise, buffer interface 1103a has a programmable width for signal path 120a.

Configurable serialization/deserialization circuit 1891 performs serialization and deserialization functions depending upon a stored serialization ratio. As a memory device access width is reduced from its maximum value, memory device access granularity (measured in quanta of data) is commensurately reduced, and an access interleaving or

multiplexing scheme may be employed to ensure that all storage locations within memory devices 101a-d can be accessed. The number of signal paths 1006 may be increased or decreased as the memory device access width changes. Signal path 1006 may be subdivided into several addressable subsets. The address of the transaction will determine which target subset of signal path 1006 will be utilized for the data transfer portion of the transaction. In addition, the number of transceiver, transmitter and/or receiver circuits included in interfaces 1820a and 1820b that are employed to communicate with one or more memory devices 101a-d may be configured based on the desired serialization ratio. Typically, configuration of the transceivers may be effectuated by enabling or disabling how many transceivers are active in a given transfer between one or more memory devices 101a-d and buffer interface 1103a. In an embodiment, a data rate of transferring data at buffer interface 1103a is a multiple or ratio of a data rate of transferring data on one or more signal paths 1006 coupled to memory devices 101a-d.

Buffer 100a provides a high degree of system flexibility. New interface standards of memory devices may be phased in to operate with a master or a memory system that supports older interface standards by modifying buffer 100a. In an embodiment, a memory module may be inserted using an older memory module interface or socket, while newer generation memory devices may be disposed on the memory module. Backward compatibility with existing generations of memory devices may be preserved. Similarly, new generations of masters, or controllers, may be phased in which exploit features of new generations of memory devices while retaining backward compatibility with existing generations of memory devices. Similarly, different types of memory devices that have different costs, power requirements and access times may be included in a single common package for specific applications.

Fig. 19 illustrates an integrated circuit memory device 1900 (or a memory die) in an embodiment. Integrated circuit memory device 1900 corresponds to one or more integrated circuit memory devices 101a-d in embodiments. Integrated circuit memory device 1900 includes a memory core 1900b and a memory interface 1900a. Signal paths 1950a-b, 1951a-b, 1952 and 1953 are coupled to memory interface 1900a. Signal paths 1950a-b transfer read and write data. Signal paths 1951a-b transfer address information, such as a row address and a column address in packets, respectively. Signal path 1952 transfers control information. Signal path 1953 transfers one or more clock signals. In an embodiment, signal paths 1950a-b correspond to signal path 120a shown in **Fig. 10** and signal paths 1951a-b, 1952 and 1953 correspond to signal path 121 in **Fig. 10**.

Memory interface 1900a includes at least one transmitter and/or receiver for transferring signals between memory device 1900 and signal paths 1950a-b, 1951a-b, 1952 and 1953. Write demultiplexer ("demux") 1920 and read multiplexer ("mux") 1922 are coupled to signal path 1950a, while write demux 1921 and read mux 1923 are coupled to signal path 1950b. Write demux 1920-21 provide write data from signal paths 1950a-b to memory core 1900b (in particular sense amplifiers 0-2a and 0-2b). Read mux 1922-23 provide read data from memory core 1900b to signal paths 1950a-b (in particular sense amplifiers Na and Nb).

Demux and row packet decoder 1910 is coupled to signal path 1951a and Demux and column packet decoder 1913 is coupled to signal path 1951b. Demux and row packet decoder 1910 decodes a packet and provides a row address to row decoder 1914. Demux and Column packet decoder 1913 provides a column address and mask information to column and mask decoder 1915.

Control registers are coupled to signal path 1952 and provide control signals to row decoder 1914 and column and mask decoder 1915 in response to register values.

A clock circuit is coupled to signal path 1953 to provide a transmit clock signal TCLK and a receive clock signal RCLK in response to one or more clock signals transferred on signal path 1953. In an embodiment, write demux 1920 and 1921 provide write data from signal paths 1950a-b to memory core 1900b in response to an edge of receive clock signal RCLK. In an embodiment, read mux 1922 and 1923 provide read data from memory core 1900b to signal paths 1950a-b in response to an edge of a transmit clock signal TCLK. In an embodiment, clock circuit generates a clock signal on signal path 1953 (to a buffer device) that has a temporal relationship with read data that are output on signal paths 1950a-b.

Row decoder 1914 and column and mask decoder 1915 provide control signals to memory core 1900b. For example, data stored in a plurality of storage cells in a memory bank is sensed using sense amplifiers in response to a row command. A row to be sensed is identified by a row address provided to row decoder 1914 from demux and row packet decoder 1910. A subset of the data sensed by a sense amplifier is selected in response to a column address (and possible mask information) provided by demux and column packet decoder 1913.

A memory bank in memory banks 0-N of memory core 1900b includes a memory array having a two dimensional array of storage cells. In embodiments, memory banks 0-N include storage cells that may be DRAM cells, SRAM cells, FLASH cells, ferroelectric RAM (FRAM) cells, magnetoresistive or magnetic RAM (MRAM) cells, or other equivalent types of memory storage cells. In an embodiment, integrated circuit memory device 1900 is a DDR integrated circuit memory device or later generation memory device (e.g., DDR2 or DDR3). In an alternate

embodiment, integrated circuit memory device 1900 is an XDR™ DRAM integrated circuit memory device or Direct Rambus® DRAM ("DRDRAM") memory device. In an embodiment, integrated circuit memory device 1900 includes different types of memory devices having different types of storage cells housed in a common package.

Signals described herein may be transmitted or received between and within devices/circuits using signal paths and generated using any number of signaling techniques including without limitation, modulating the voltage or current level of an electrical signal. The signals may represent any type of control and timing information (e.g. commands, address values, clock signals, and configuration/parameter information) as well as data. In an embodiment, a signal described herein may be an optical signal.

A variety of signals may be transferred on signal paths as described herein. For example, types of signals include differential (over a pair of signal lines), non-return to zero ("NRZ"), multi-level pulse amplitude modulation ("PAM"), phase shift keying, delay or time modulation, quadrature amplitude modulation ("QAM") and Trellis coding.

In an embodiment employing multi-level PAM signaling, a data rate may be increased without increasing either the system clock frequency or the number of signal lines by employing multiple voltage levels to encode unique sets of consecutive digital values or symbols. That is, each unique combination of consecutive digital symbols may be assigned to a unique voltage level, or pattern of voltage levels. For example, a 4-level PAM scheme may employ four distinct voltage ranges to distinguish between a pair of consecutive digital values or symbols such as 00, 01, 10 and 11. Here, each voltage range would correspond to one of the unique pairs of consecutive symbols.

In an embodiment, a clock signal is used to synchronize events in a memory module and/or device such as synchronizing receiving and transmitting data and/or control information. In an embodiment, globally synchronous clocking is used (i.e., where a single clock frequency source is distributed to various devices in a memory module/system). In an embodiment, source synchronous clocking is used (i.e., where data is transported alongside a clock signal from a source to a destination such that a clock signal and data become skew tolerant). In an embodiment, encoding data and a clock signal is used. In alternate embodiments, combinations of clocking or synchronization described herein are used.

In embodiments, signal paths described herein include one or more conducting elements, such as a plurality of wires, metal traces (internal or external), signal lines or doped regions (positively or negatively enhanced), as well as one or more optical fibers or optical pathways, singly or in combination. In embodiments, multiple signal paths may replace a single signal path illustrated in the Figures and a single signal path may replace multiple signal paths illustrated in the Figures. In embodiments, a signal path may include a bus and/or point-to-point connection. In an embodiment, signal paths include signal paths for transferring control and data signals. In an alternate embodiment, signal paths include only signals paths for transferring data signals or only signal paths for transferring control signals. In still other embodiments, signal paths transfer unidirectional signals (signals that travel in one direction) or bidirectional signals (signals that travel in two directions) or combinations of both unidirectional and bidirectional signals.

It should be noted that the various circuits disclosed herein may be described using computer aided design tools and expressed (or represented) as data and/or instructions embodied in various computer-readable media, in terms of their behavior, register transfer, logic

component, transistor, layout geometries, and/or other characteristics. Formats of files and other objects in which such circuit expressions may be implemented include, but are not limited to: formats supporting behavioral languages such as C, Verilog, and HLDL; formats supporting register level description languages like RTL; formats supporting geometry description languages such as GDSII, GDSIII, GDSIV, CIF, MEBES; and any other suitable formats and languages. Computer-readable media in which such formatted data and/or instructions may be embodied include, but are not limited to, non-volatile storage media in various forms (e.g., optical, magnetic or semiconductor storage media) and carrier waves that may be used to transfer such formatted data and/or instructions through wireless, optical, or wired signaling media or any combination thereof. Examples of transfers of such formatted data and/or instructions by carrier waves include, but are not limited to, transfers (uploads, downloads, e-mail, etc.) over the Internet and/or other computer networks via one or more data transfer protocols (e.g., HTTP, FTP, SMTP, etc.). When received within a computer system via one or more computer-readable media, such data and/or instruction-based expressions of the above described circuits may be processed by a processing entity (e.g., one or more processors) within the computer system in conjunction with execution of one or more other computer programs including, without limitation, netlist generation programs, place and route programs and the like, to generate a representation or image of a physical manifestation of such circuits. Such representation or image may thereafter be used in device fabrication, for example, by enabling generation of one or more masks that are used to form various components of the circuits in a device fabrication process.

The foregoing description of several embodiments has been provided for the purposes of illustration and description. It is not intended to be exhaustive or to limit the embodiments to the precise

forms disclosed. Modifications and variations will be apparent to practitioners skilled in the art. The embodiments were chosen and described in order to explain inventive principles and practical applications, thereby enabling others skilled in the art to understand various embodiments and with the various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the following claims and their equivalents.

What is claimed is:

1. A memory module comprising:

a connector interface;

a first signal path coupled to the connector interface;

a first integrated circuit memory die;

a first integrated circuit buffer die coupled to the first signal path, the first integrated circuit buffer die to receive control information from the first signal path, wherein the control information specifies an access to the first integrated circuit memory die such that the first integrated circuit memory die provides first data to the first integrated circuit buffer die in response to the control information;

a second integrated circuit memory die; and

a second integrated circuit buffer die coupled to the first signal path, the second integrated circuit buffer die to receive the control information from the first signal path, wherein the control information specifies an access to the second integrated circuit memory die such that the second integrated circuit memory die provides second data to the second integrated circuit buffer die in response to the control information.

2. The memory module of claim 1, further comprising:

a second signal path coupled to the first integrated circuit memory die and the first integrated circuit buffer device, wherein the second signal path is dedicated to carry the first data between the first integrated circuit memory die and first integrated circuit buffer device;

a third signal path coupled to the second integrated circuit memory die and the second integrated circuit buffer device, wherein the third signal path is dedicated to carry the second data between the

second integrated circuit memory die and second integrated circuit buffer device;

a fourth signal path coupled to the first integrated circuit buffer device and the connector interface, wherein the fourth signal path is dedicated to carry the first data between the first integrated circuit buffer device and the connector interface; and

a fifth signal path coupled to the second integrated circuit buffer device and the connector interface, wherein the fifth signal path is dedicated to carry the second data between the second integrated circuit buffer device and the connector interface.

3. The memory module of claim 1, wherein the first signal path includes a signal line to provide a clock signal to the first integrated circuit buffer die and the second integrated circuit buffer die.

4. The memory module of claim 3, wherein

the first integrated circuit buffer die generates a second clock signal using the first clock signal and provides the second clock signal to the first integrated circuit memory die; and

the second integrated circuit buffer die generates a third clock signal using the first clock signal and provides the third clock signal to the second integrated circuit memory die.

5. The memory module of claim 1, wherein the first signal path includes a first signal line to provide a first clock signal to the first integrated circuit buffer die and a second clock signal to the second integrated circuit buffer die.

6. The memory module of claim 1, wherein the first integrated circuit buffer die is disposed in a first package and the first integrated

circuit memory die is disposed in a second package, and wherein the second integrated circuit buffer die is disposed in a third package and the second integrated circuit memory die is disposed in a fourth package.

7. The memory module of claim 6, wherein the first package is stacked upon the second package.

8. The memory module of claim 6, wherein a fifth package includes a third integrated circuit memory die, and wherein the fifth package is stacked upon the first package.

9. The memory module of claim 6, wherein the first package is stacked upon the second package, and wherein a fifth package includes a third integrated circuit memory die, and wherein the fifth package is stacked upon the first package.

10. The memory module of claim 1, wherein the first integrated circuit buffer die and the first integrated circuit memory die are disposed in a first common package, and wherein the second integrated circuit buffer die and the second integrated circuit memory die are disposed in a second common package.

11. The memory module of claim 1, comprising:

a signal line in the first signal path to provide a clock signal from the first integrated circuit buffer die to the connector interface; and

a second signal path coupled to the first integrated circuit buffer device and the connector interface, the second signal path to carry the first data between the first integrated circuit buffer device and the

connector interface wherein the first data propagates in accordance with a temporal relationship to the clock signal.

12. The memory module of claim 1, comprising:

a second signal path coupled to the first integrated circuit buffer device and the connector interface, the second signal path to carry the first data between the first integrated circuit buffer device and the connector interface wherein the first data propagates in accordance with a temporal relationship to a clock signal; and

a first signal line in the second signal path to provide the clock signal.

13. The memory module of claim 1, comprising:

a second signal path coupled to the first integrated circuit buffer device and the connector interface, the second signal path to carry the first data between the first integrated circuit buffer device and the connector interface wherein the first data propagates in accordance with a temporal relationship to a strobe signal; and

a first signal line in the second signal path to provide the strobe signal.

14. The memory module of claim 13, wherein the strobe signal is bidirectional.

15. The memory module of claim 13, wherein the strobe signal is unidirectional.

16. The memory module of claim 1, comprising:

a signal line in the first signal path to provide a clock signal to the first integrated circuit buffer die from the connector interface;

a second signal path coupled to the first integrated circuit buffer device and the connector interface; and

a signal line in the second signal path to provide write data to be stored in the first integrated circuit memory die via the first integrated circuit buffer die, wherein the write data has a temporal relationship with the clock signal.

17. The memory module of claim 1, comprising:

a second signal path coupled to the first integrated circuit buffer device and the connector interface;

a signal line in the second signal path to provide a clock signal to the first integrated circuit buffer die from the connector interface; and

a signal line in the second signal path to provide write data to be stored in the first integrated circuit memory die from the connector interface via the first integrated circuit buffer die, wherein the write data has a temporal relationship with the clock signal.

18. The memory module of claim 1, comprising:

a second signal path coupled to the first integrated circuit buffer device and the connector interface;

a signal line in the second signal path to provide a strobe signal to the first integrated circuit buffer die from the connector interface; and

a signal line in the second signal path to provide write data to be stored in the first integrated circuit memory die from the connector interface via the first integrated circuit buffer die, wherein the write data has a temporal relationship with the strobe signal.

19. The memory module of claim 18, wherein the strobe signal is bidirectional.

20. The memory module of claim 18, wherein the strobe signal is unidirectional.

21. The memory module of claim 1, further comprising:

a termination coupled to the first signal path.

22. The memory module of claim 21, wherein the termination is disposed on the memory module.

23 The memory module of claim 21, wherein the termination is disposed on the first integrated circuit buffer die.

24. The memory module of claim 21, wherein the termination is disposed in a package housing the first integrated circuit buffer die.

25. The memory module of claim 1, further comprising:

a second signal path coupled to the first integrated circuit memory die and the first integrated circuit buffer device, the second signal path is to carry the first data between the first integrated circuit memory die and first integrated circuit buffer device;

a third signal path coupled to the second integrated circuit memory die and the second integrated circuit buffer device, the third signal path to carry the second data between the second integrated circuit memory die and second integrated circuit buffer device;

a first termination coupled the second signal path; and

a second termination coupled to the third signal path.

26. The memory module of claim 25, wherein the first termination is disposed on the memory module and the second termination is disposed on the memory module.

27 The memory module of claim 25, wherein the first termination is disposed on the first integrated circuit buffer die and the second termination is disposed on the second integrated circuit buffer die.

28. The memory module of claim 25, wherein the first termination is disposed on a package housing the first integrated circuit buffer die and the second termination is disposed on a package housing the second integrated circuit buffer die.

29. The memory module of claim 1, wherein the first integrated circuit buffer die is disposed in a first package and the first integrated circuit memory die is disposed in a second package,

wherein the second integrated circuit buffer die is disposed in a third package and the second integrated circuit memory die is disposed in a fourth package,

wherein the first and second packages are disposed on a first side of the memory module, and

wherein the third and fourth packages are disposed on a second side of the memory module.

30. The memory module of claim 1, wherein the first integrated circuit memory die includes a memory array having a first type of storage cells and the second integrated circuit memory die includes a memory array having a second type of storage cells, wherein the first type of storage cells is different than the second type of storage cells.

31. The memory module of claim 1, wherein:

the first and second integrated circuit buffer dies receive the control information in a DDR3 format;

the first integrated circuit buffer die provides DDR2 control signals corresponding to the control information to the first integrated buffer die; and the second integrated circuit buffer die provides DDR2 control signals corresponding to the control information to the second integrated circuit memory die.

32. The memory module of claim 1, wherein the first and second integrated circuit buffer dies receive the control information in the form of a first type of signal and provide control signals to the respective first and second integrated circuit memory dies in the form of a second type of signal, wherein the first type of signal is different that the second type of signal.

33. The memory module of claim 1, wherein the first and second integrated circuit buffer dies receive the first and second control information in a first protocol format and provide control signals to the first and second integrated circuit memory dies in a second protocol format, wherein the first protocol format is different that the second protocol format.

34 The memory module of claim 1, wherein the first and second integrated circuit buffer dies includes logic to emulate a function of the first and second memory dies.

35. The memory module of claim 1, further comprising:

at least one non-volatile storage location to store information pertaining to a configuration of the memory module.

36. A memory module comprising:

an interface;

a first package including a buffer and an integrated circuit memory device having a memory array, wherein the buffer of the first package is coupled to the interface;

a second package including a buffer and an integrated circuit memory device having a memory array, wherein the buffer of the second package is coupled to the interface; and

at least a first non-volatile storage location to store information pertaining to a configuration of the memory module.

37. The memory module of claim 36, wherein the at least first non-volatile storage location is a serial presence detect device and the information includes at least the number of integrated circuit memory devices included in the memory module and timing information of the integrated circuit memory devices.

38. The memory module of claim 36, wherein the at least first non-volatile storage location is included in the first package and at least a second non-volatile storage location containing the information is included in the second package.

39. The memory module of claim 36, wherein the at least first non-volatile storage location is included in the first package.

40. The memory module of claim 36, wherein the at least first non-volatile storage location is included in a third package disposed on the memory module.

41. The memory module of claim 36, wherein the information includes at least information to repair the integrated circuit memory device of the first package.

42. The memory module of claim 36, wherein the buffer of the first package reads the information stored in the at least first non-volatile storage location.

43. The memory module of claim 36, wherein the buffer of the first package writes the information stored in the at least first non-volatile storage location.

44. The memory module of claim 36, wherein the information is transferred between the interface and the at least first non-volatile storage location.

45. A memory module comprising:

a connector interface;

a first signal path coupled to the connector interface;

a first integrated circuit memory die;

a second integrated circuit memory die;

a first integrated circuit buffer die coupled to the first signal path, the first integrated circuit buffer die to receive first control information from the first signal path, wherein the first control information specifies an access to the first integrated circuit memory die;

a second integrated circuit buffer die coupled to the first signal path, the second integrated circuit buffer die to receive second control information from the first signal path, wherein the second control information specifies an access to the second integrated circuit memory die; and

a signal line to provide a first clock signal to the first integrated circuit buffer die and the second integrated circuit buffer die, wherein:

the first integrated circuit buffer die generates a second clock signal using the first clock signal and provides the second clock signal to the first integrated circuit memory die; and

the second integrated circuit buffer die generates a third clock signal using the first clock signal and provides the third clock signal to the first integrated circuit memory die.

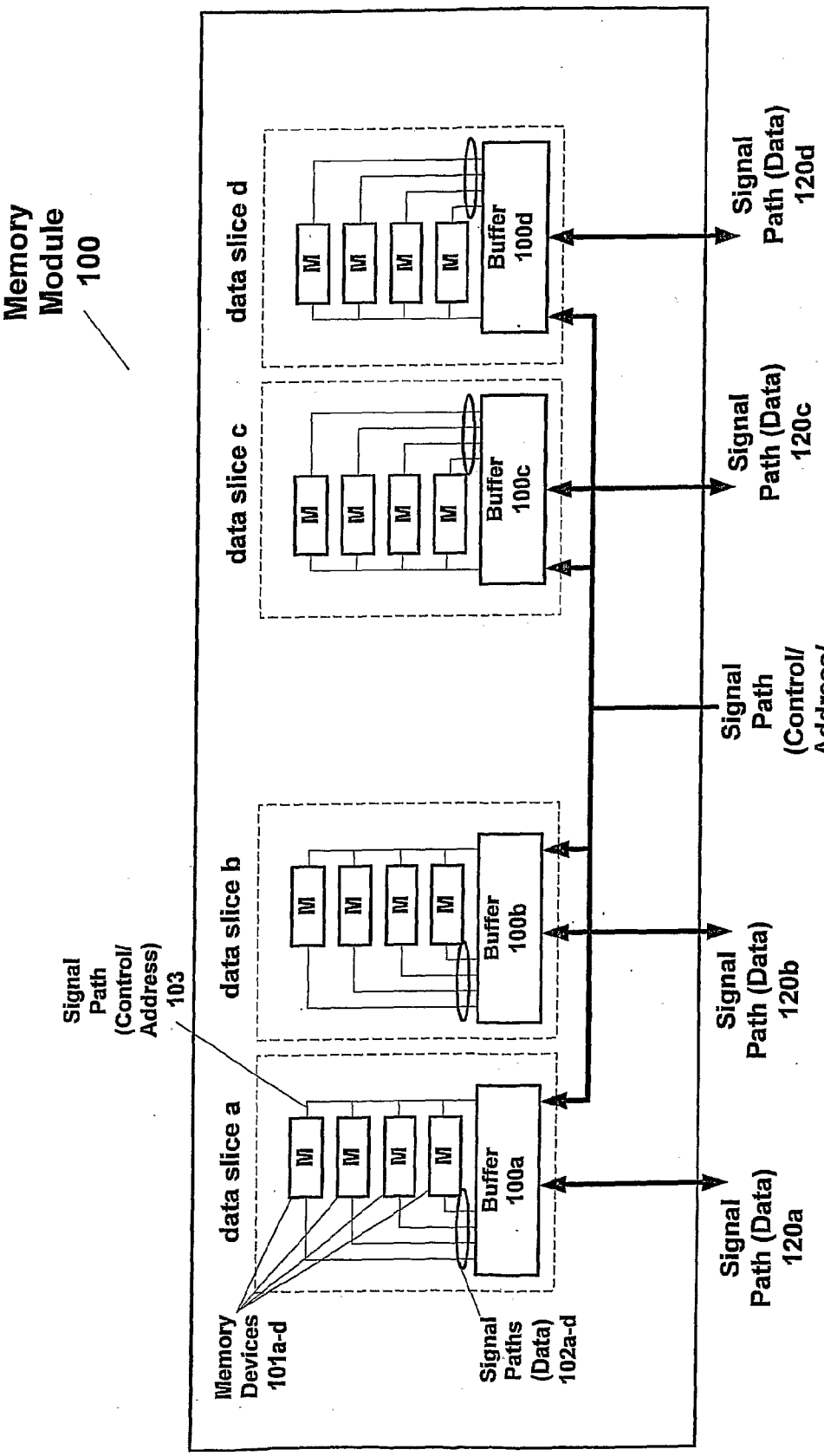
Memory Module 100
data slice a
data slice b
data slice c
data slice d
Buffer 100a
Buffer 100b
Buffer 100c
Buffer 100d
M
Signal Path (Control/ Address) 103
Memory Devices 101a-d
Signal Paths (Data) 102a-d
Signal Path (Data) 120a
Signal Path (Data) 120b
Signal Path (Data) 120c
Signal Path (Data) 120d
Signal Path (Control/ Address/ Clock) 121

Fig. 1

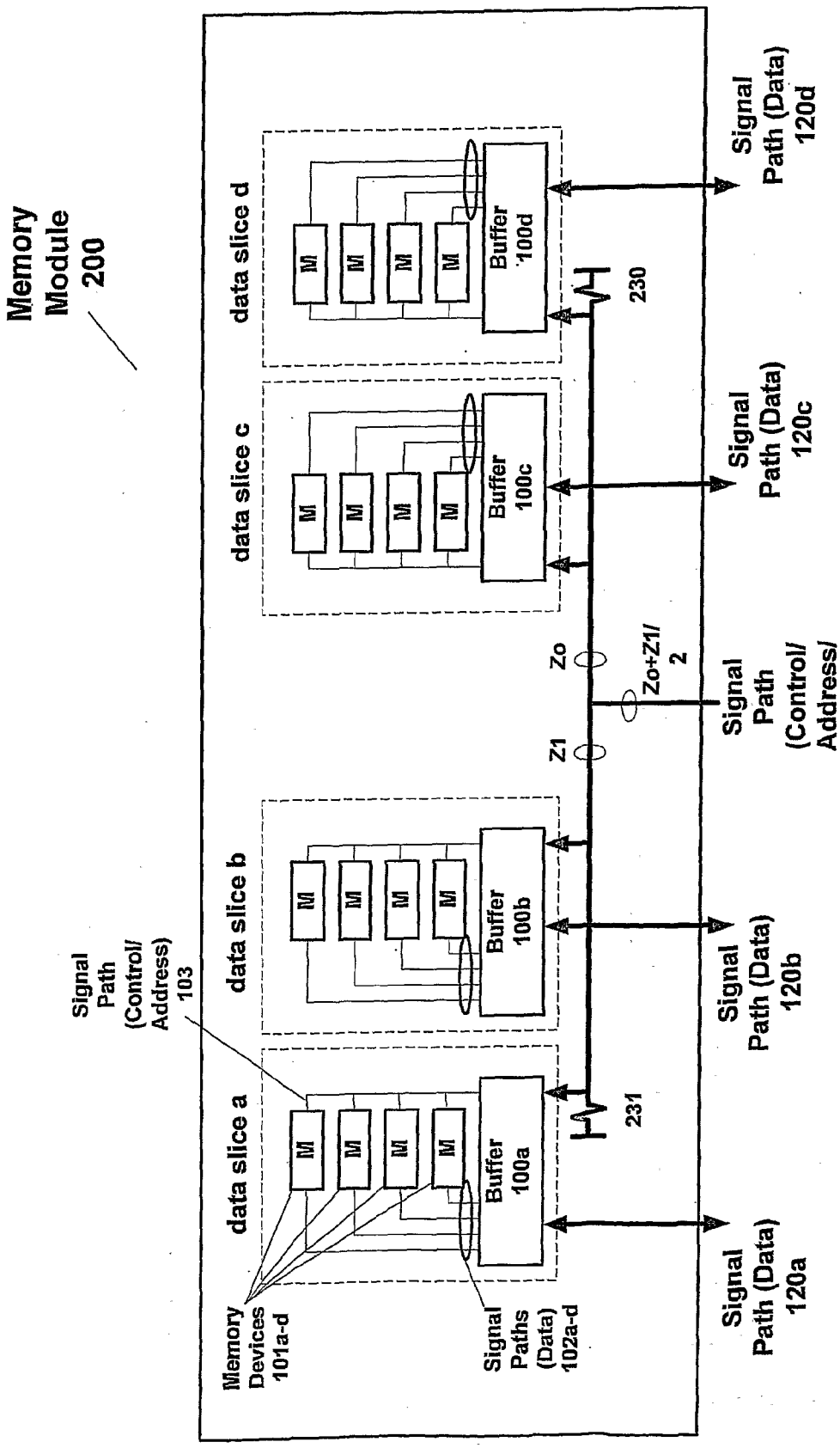
Memory Module 200
data slice a
data slice b
data slice c
data slice d
Buffer 100a
Buffer 100b
Buffer 100c
Buffer 100d
M
Memory Devices 101a-d
Signal Paths (Data) 102a-d
Signal Path (Control/ Address) 103
Signal Path (Data) 120a
Signal Path (Data) 120b
Signal Path (Data) 120c
Signal Path (Data) 120d
Signal Path (Control/ Address/ Clock) 221
231
230
Z1
Zo
Zo+Z1/ 2

Fig. 2

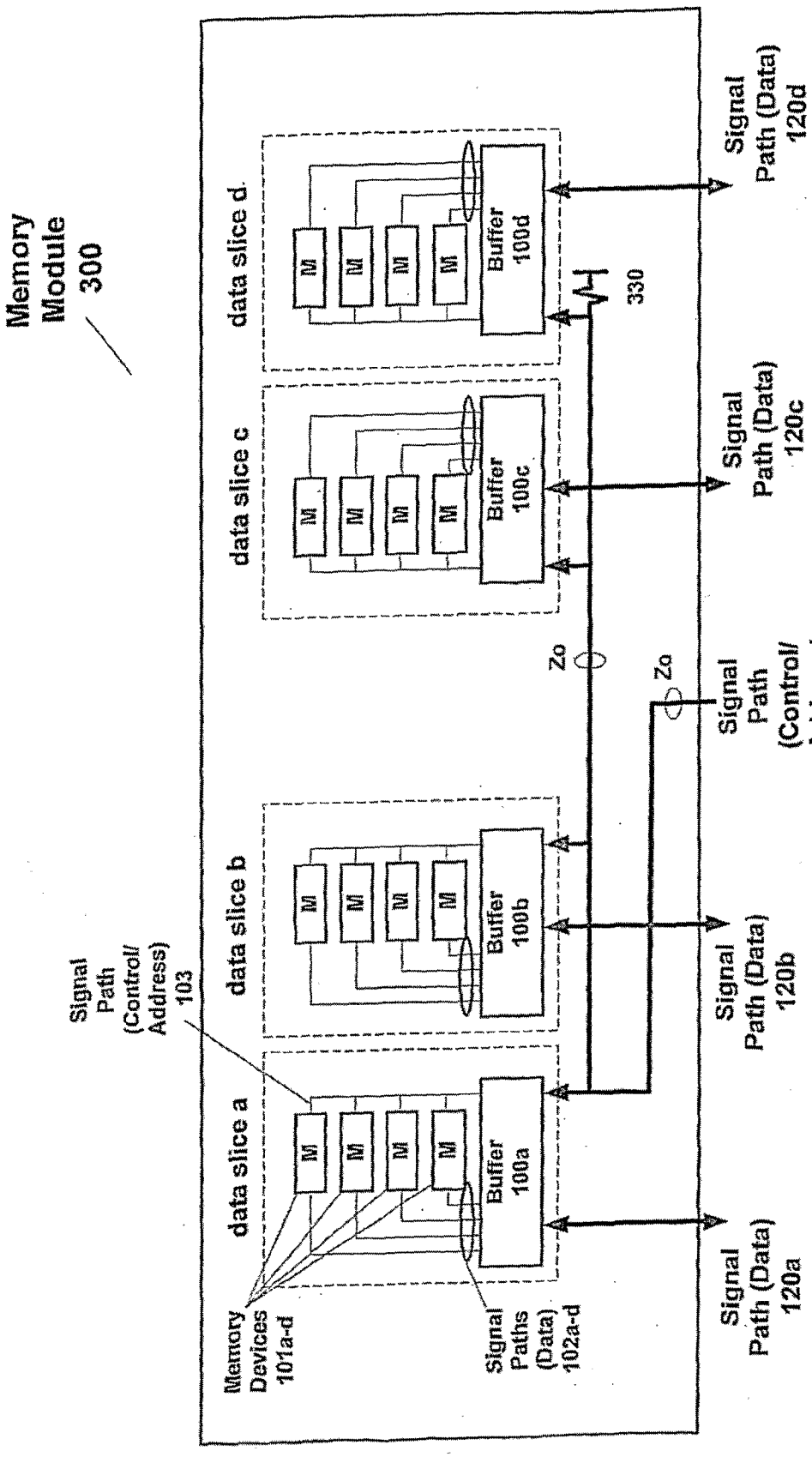
Memory Module 300
data slice a
data slice b
data slice c
data slice d
Buffer 100a
Buffer 100b
Buffer 100c
Buffer 100d
M
Memory Devices 101a-d
Signal Path (Control/ Address) 103
Signal Paths (Data) 102a-d
Signal Path (Data) 120a
Signal Path (Data) 120b
Signal Path (Data) 120c
Signal Path (Data) 120d
Signal Path (Control/ Address/ Clock) 121
Zo
Zo
330

Fig. 3

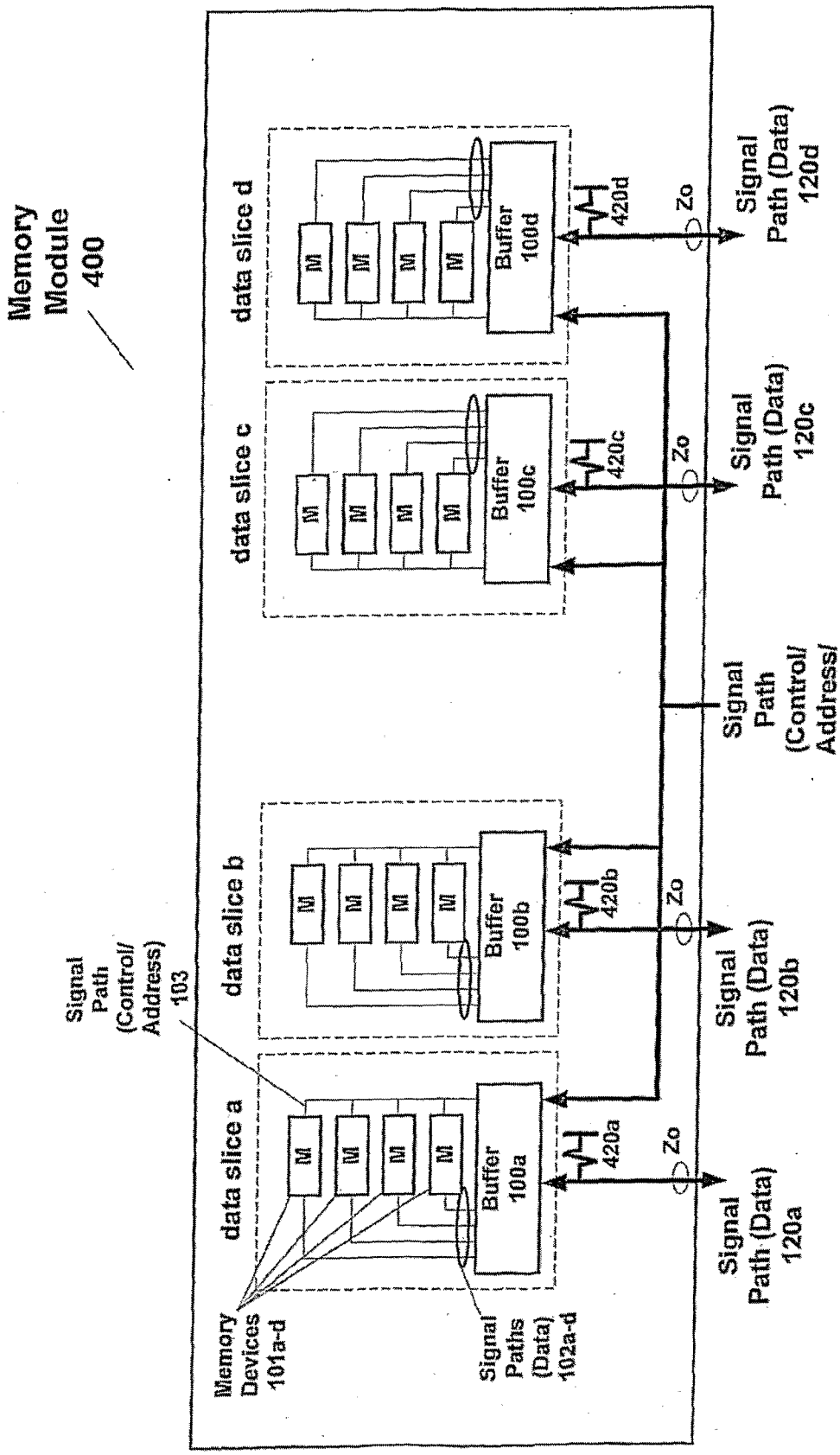
Memory Module 400
data slice a
data slice b
data slice c
data slice d
Buffer 100a
Buffer 100b
Buffer 100c
Buffer 100d
420a
420b
420c
420d
Zo
Signal Path (Control/ Address) 103
Memory Devices 101a-d
Signal Paths (Data) 102a-d
Signal Path (Data) 120a
Signal Path (Data) 120b
Signal Path (Data) 120c
Signal Path (Data) 120d
Signal Path (Control/ Address/ Clock) 121

Fig. 4

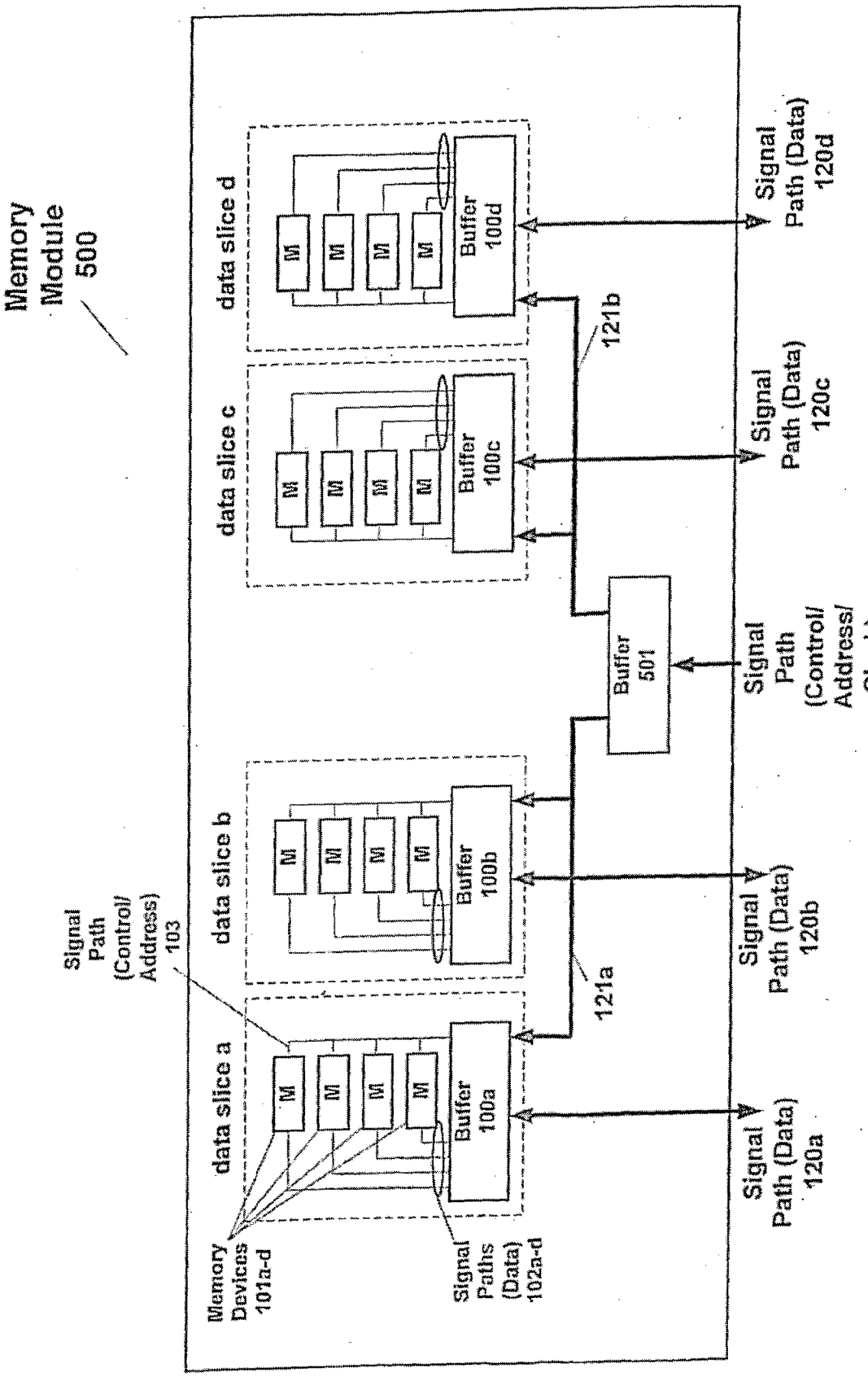
Memory Module 500
data slice a
data slice b
data slice c
data slice d
Buffer 100a
Buffer 100b
Buffer 100c
Buffer 100d
M
Memory Devices 101a-d
Signal Paths (Data) 102a-d
Signal Path (Control/ Address) 103
121a
121b
Buffer 501
Signal Path (Control/ Address/ Clock) 121
Signal Path (Data) 120a
Signal Path (Data) 120b
Signal Path (Data) 120c
Signal Path (Data) 120d

Fig. 5

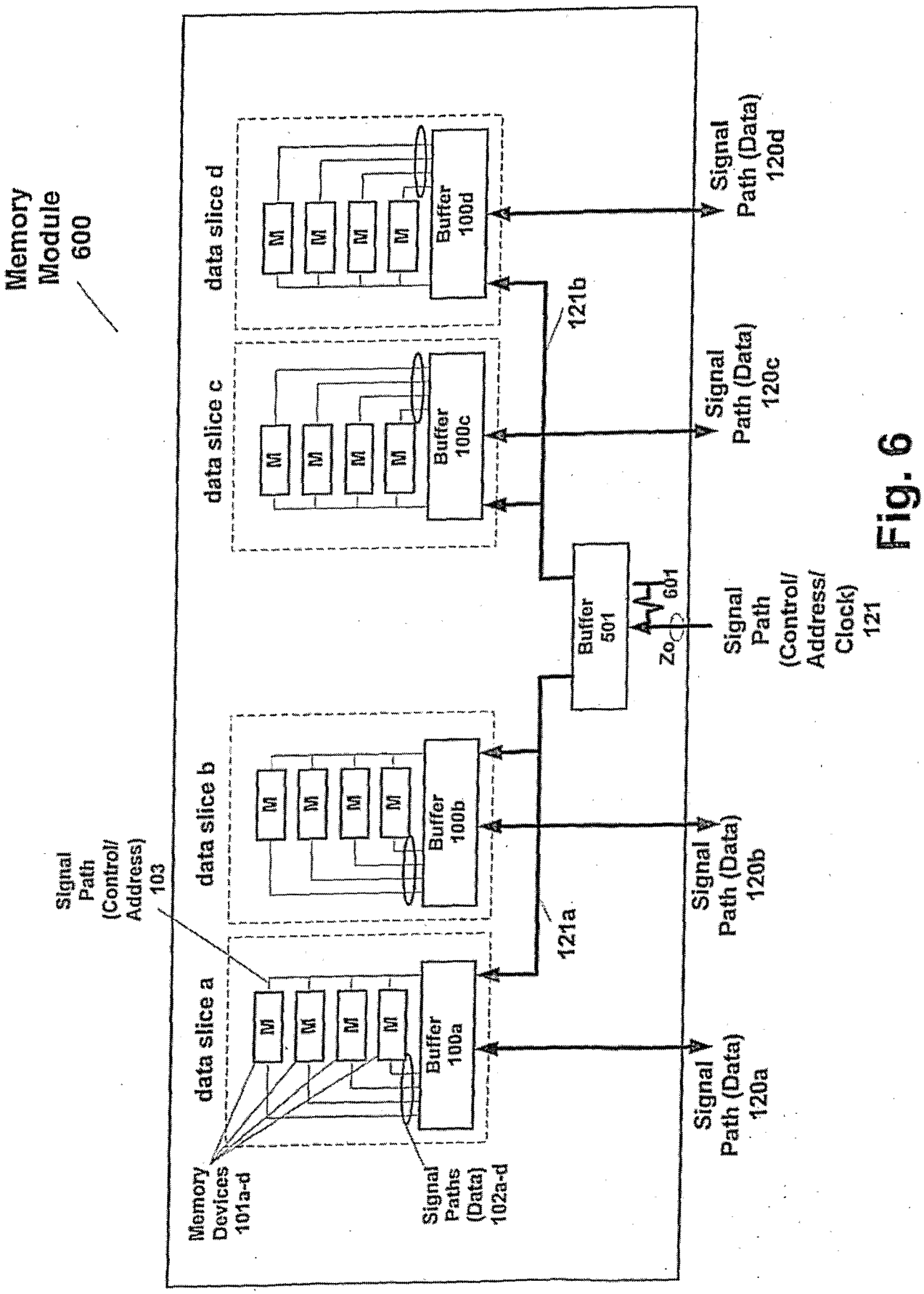
Memory Module 600
data slice a
data slice b
data slice c
data slice d
Buffer 100a
Buffer 100b
Buffer 100c
Buffer 100d
M
Buffer 501
Zo
601
Signal Path (Control/ Address) 103
Memory Devices 101a-d
Signal Paths (Data) 102a-d
121a
121b
Signal Path (Data) 120a
Signal Path (Data) 120b
Signal Path (Data) 120c
Signal Path (Data) 120d
Signal Path (Control/ Address/ Clock) 121

Fig. 6

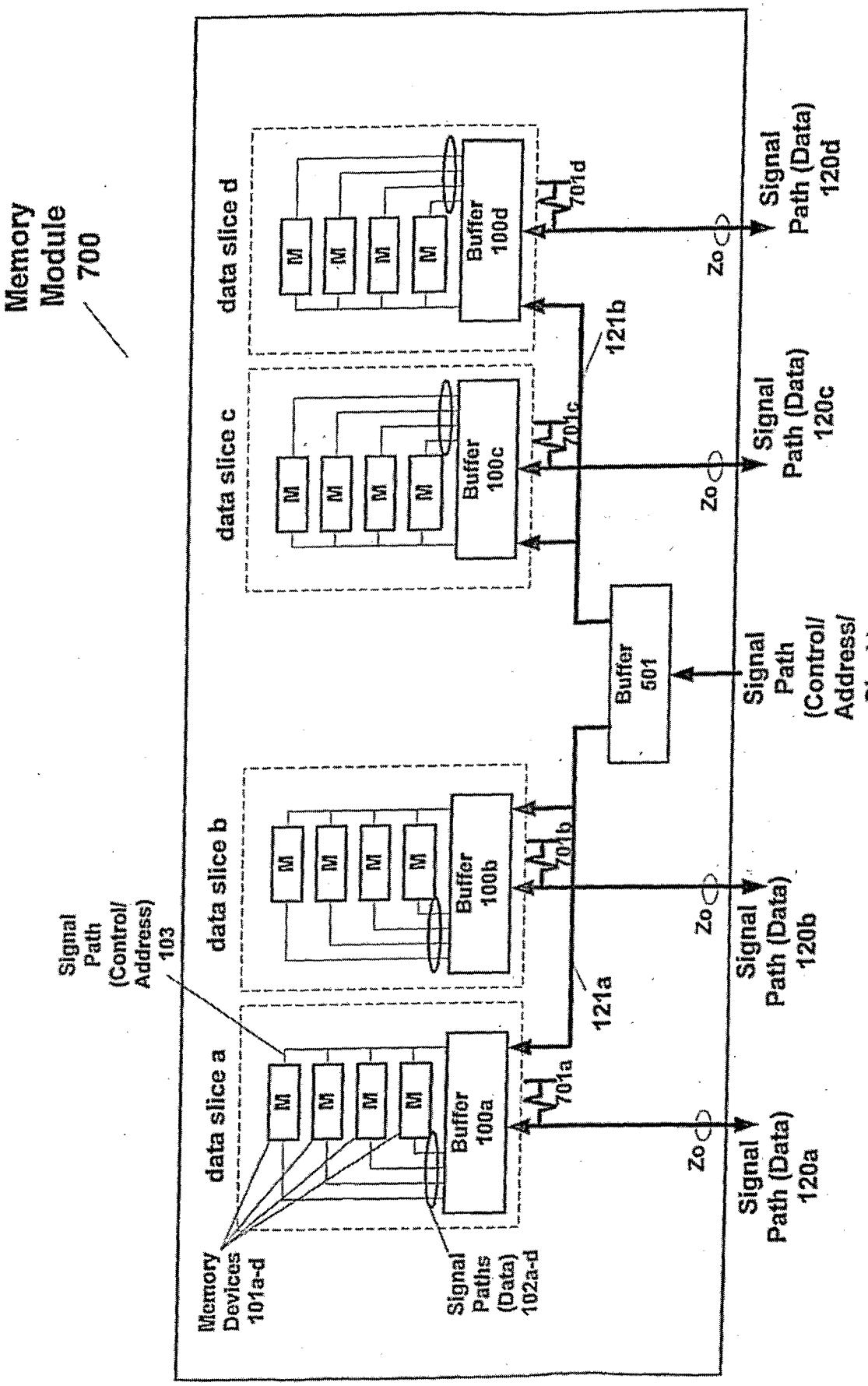
Memory Module 700
data slice a
data slice b
data slice c
data slice d
Buffer 100a
Buffer 100b
Buffer 100c
Buffer 100d
Buffer 601
M
Memory Devices 101a-d
Signal Paths (Data) 102a-d
Signal Path (Control/ Address) 103
Signal Path (Control/ Address/ Clock) 121
121a
121b
701a
701b
701c
701d
Zo
Signal Path (Data) 120a
Signal Path (Data) 120b
Signal Path (Data) 120c
Signal Path (Data) 120d

Fig. 7

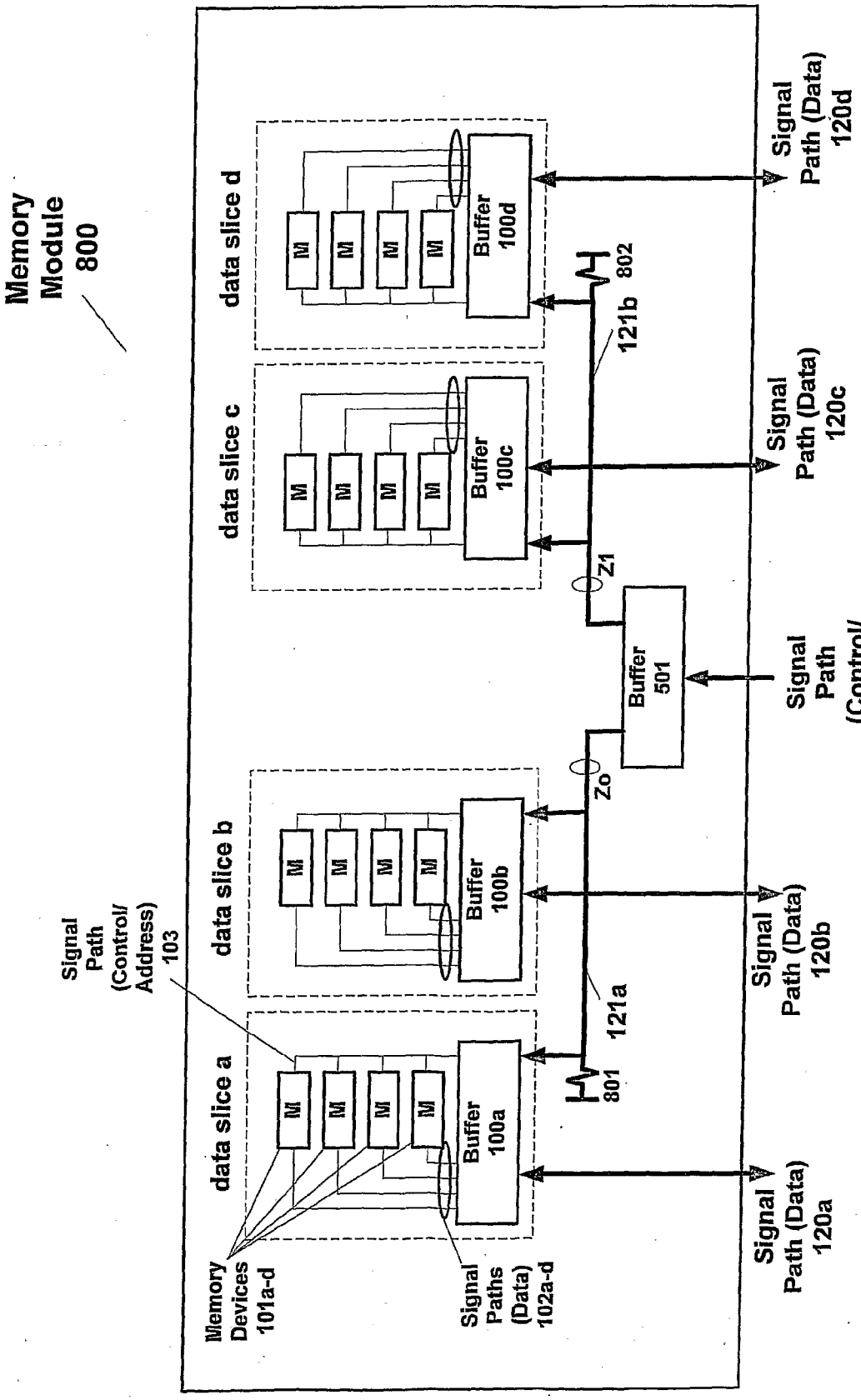
Memory Module 800
data slice a
data slice b
data slice c
data slice d
Buffer 100a
Buffer 100b
Buffer 100c
Buffer 100d
M
Memory Devices 101a-d
Signal Paths (Data) 102a-d
Signal Path (Control/ Address) 103
Buffer 501
Signal Path (Control/ Address/ Clock) 121
Signal Path (Data) 120a
Signal Path (Data) 120b
Signal Path (Data) 120c
Signal Path (Data) 120d
121a
121b
801
802
Zo
Z1

Fig. 8

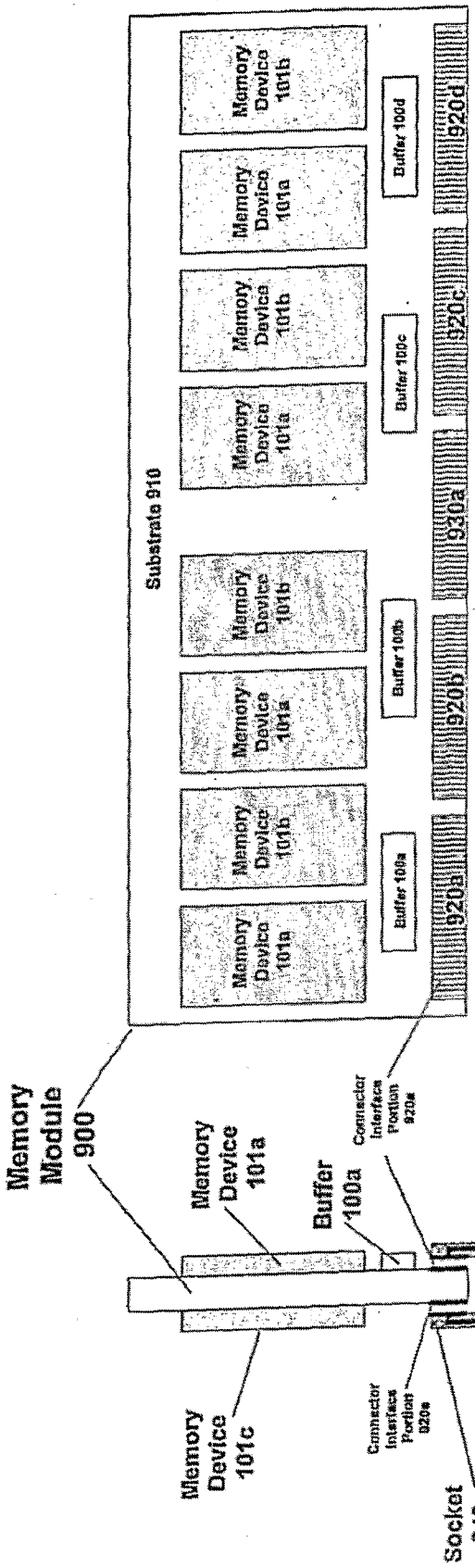

Fig. 9B

Fig. 9A

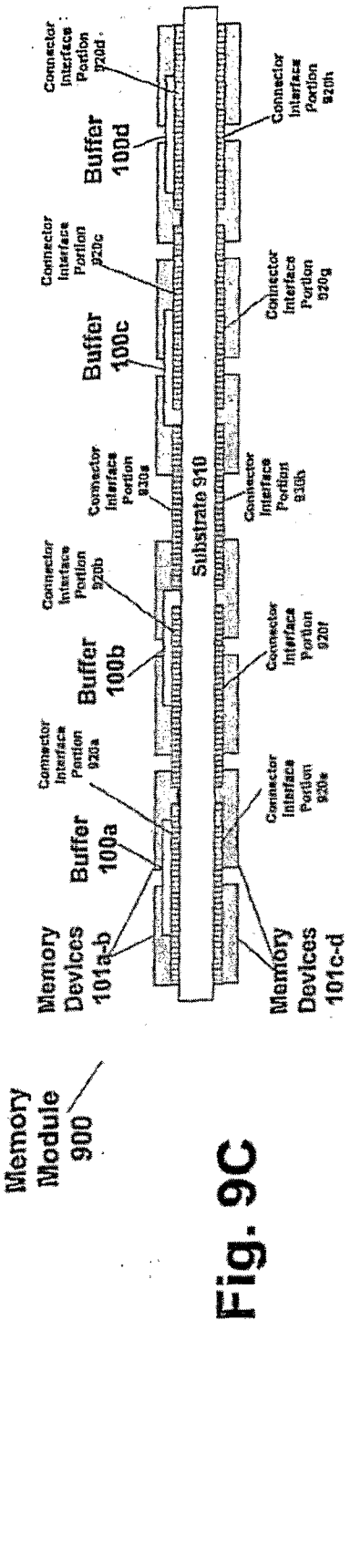

Fig. 9C

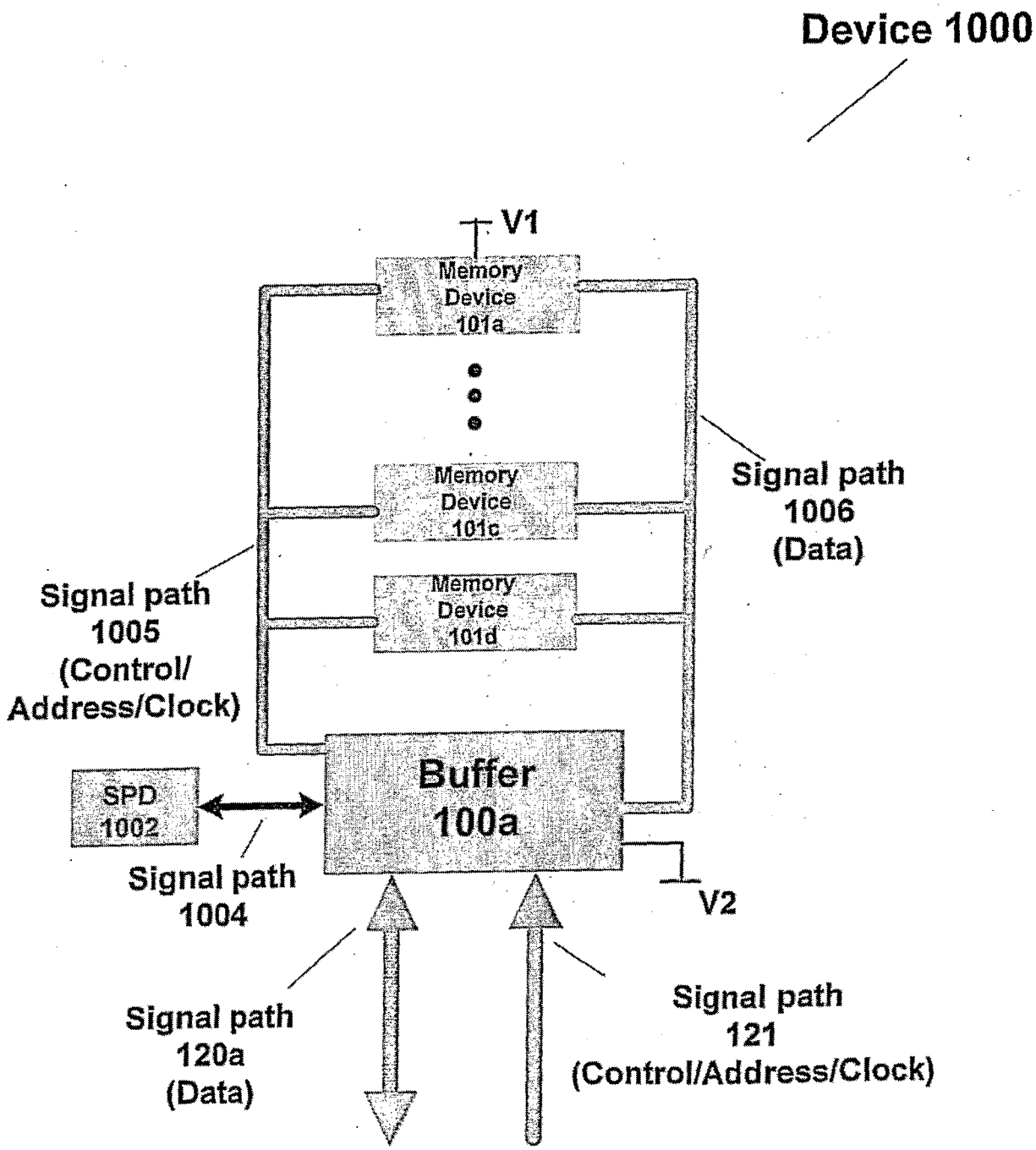
Device 1000
V1
Memory Device 101a
Memory Device 101c
Memory Device 101d
Signal path 1006 (Data)
Signal path 1005 (Control/ Address/Clock)
SPD 1002
Buffer 100a
Signal path 1004
V2
Signal path 120a (Data)
Signal path 121 (Control/Address/Clock)

Fig. 10

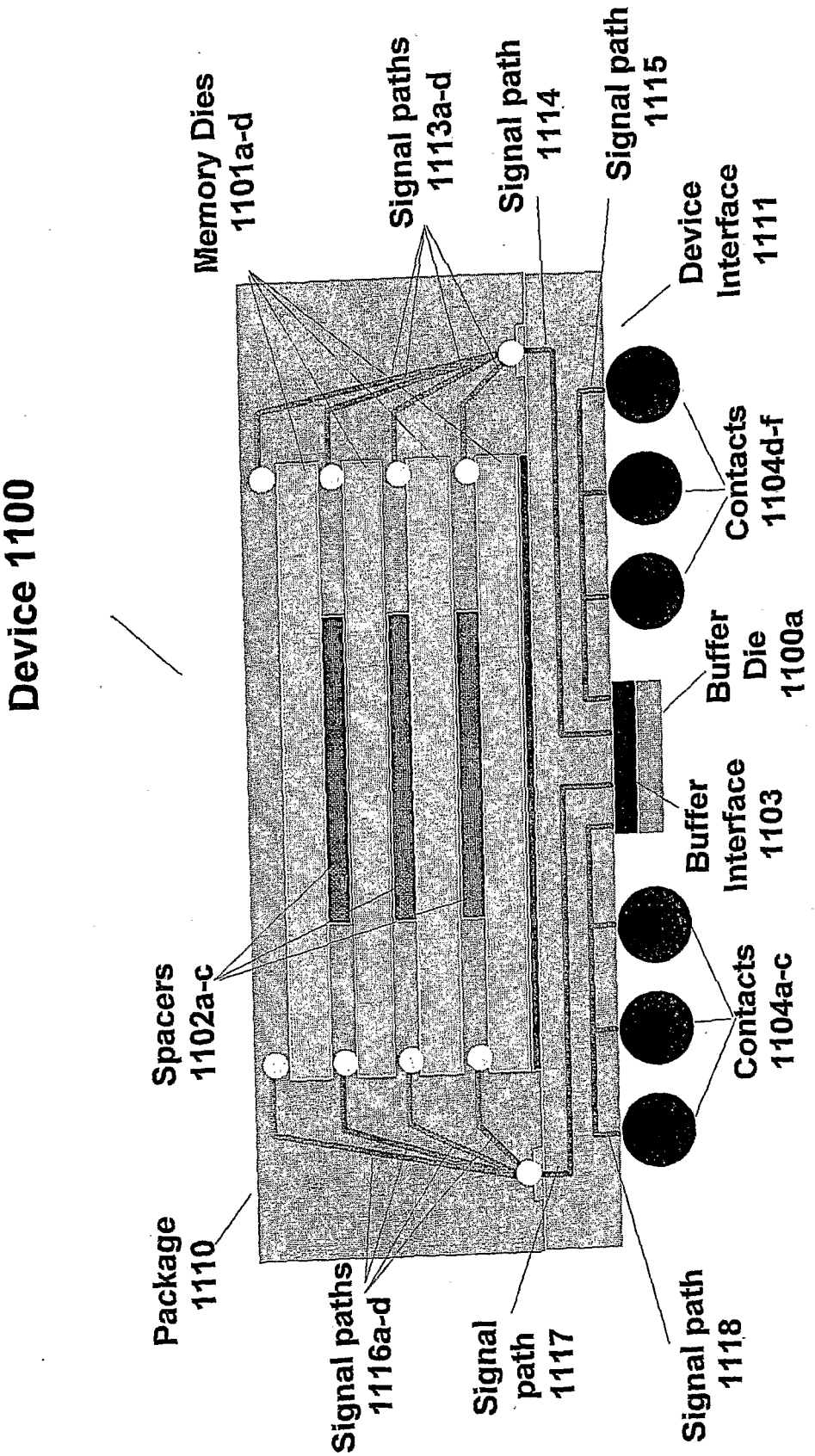
Device 1100
Memory Dies 1101a-d
Signal paths 1113a-d
Signal path 1114
Signal path 1115
Device Interface 1111
Contacts 1104d-f
Buffer Die 1100a
Buffer Interface 1103
Contacts 1104a-c
Spacers 1102a-c
Package 1110
Signal paths 1116a-d
Signal path 1117
Signal path 1118

Fig. 11

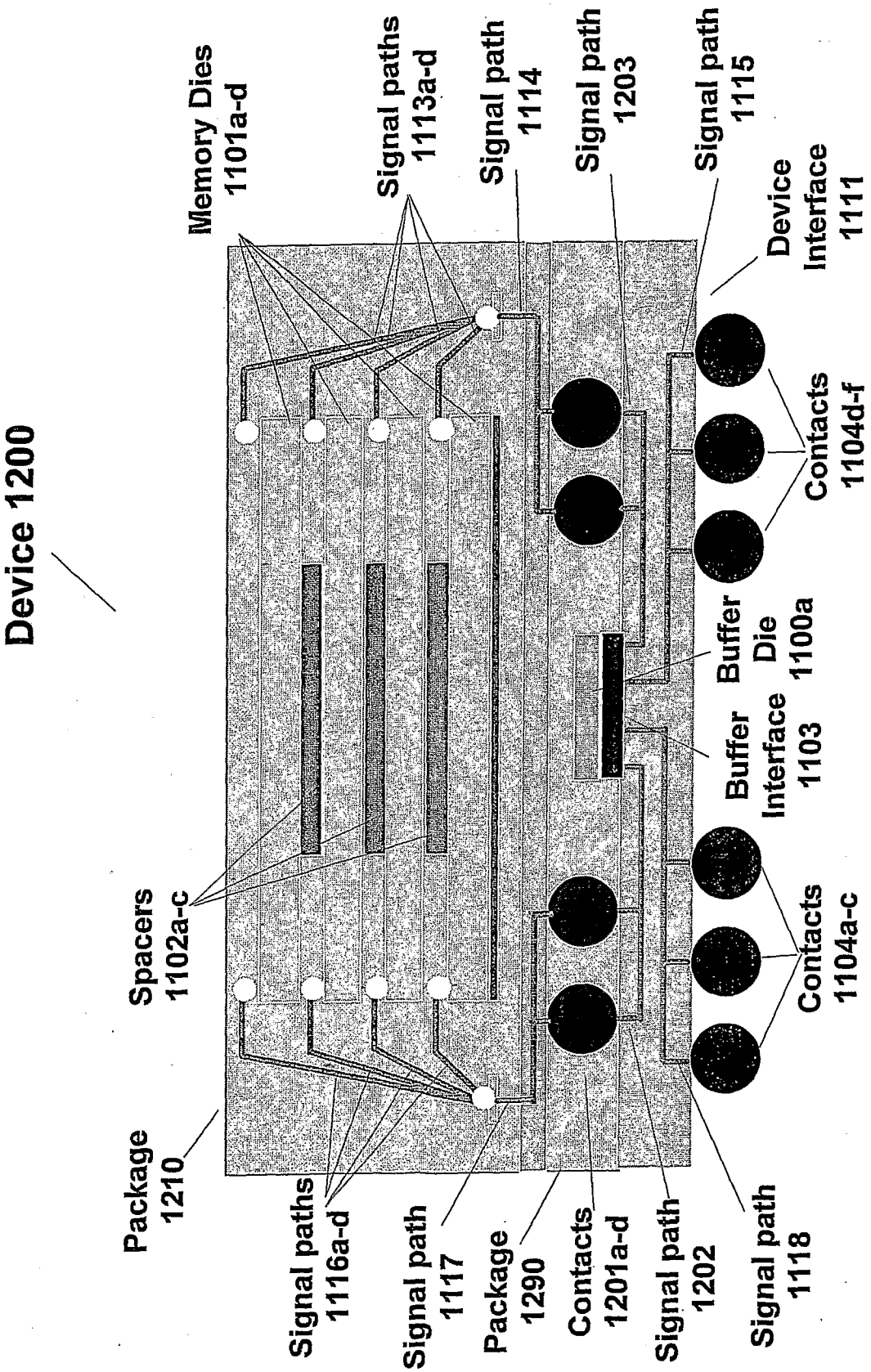
Device 1200
Memory Dies 1101a-d
Signal paths 1113a-d
Signal path 1114
Signal path 1203
Signal path 1115
Device Interface 1111
Contacts 1104d-f
Buffer Die 1100a
Buffer Interface 1103
Contacts 1104a-c
Spacers 1102a-c
Package 1210
Signal paths 1116a-d
Signal path 1117
Package 1290
Contacts 1201a-d
Signal path 1202
Signal path 1118

Fig. 12

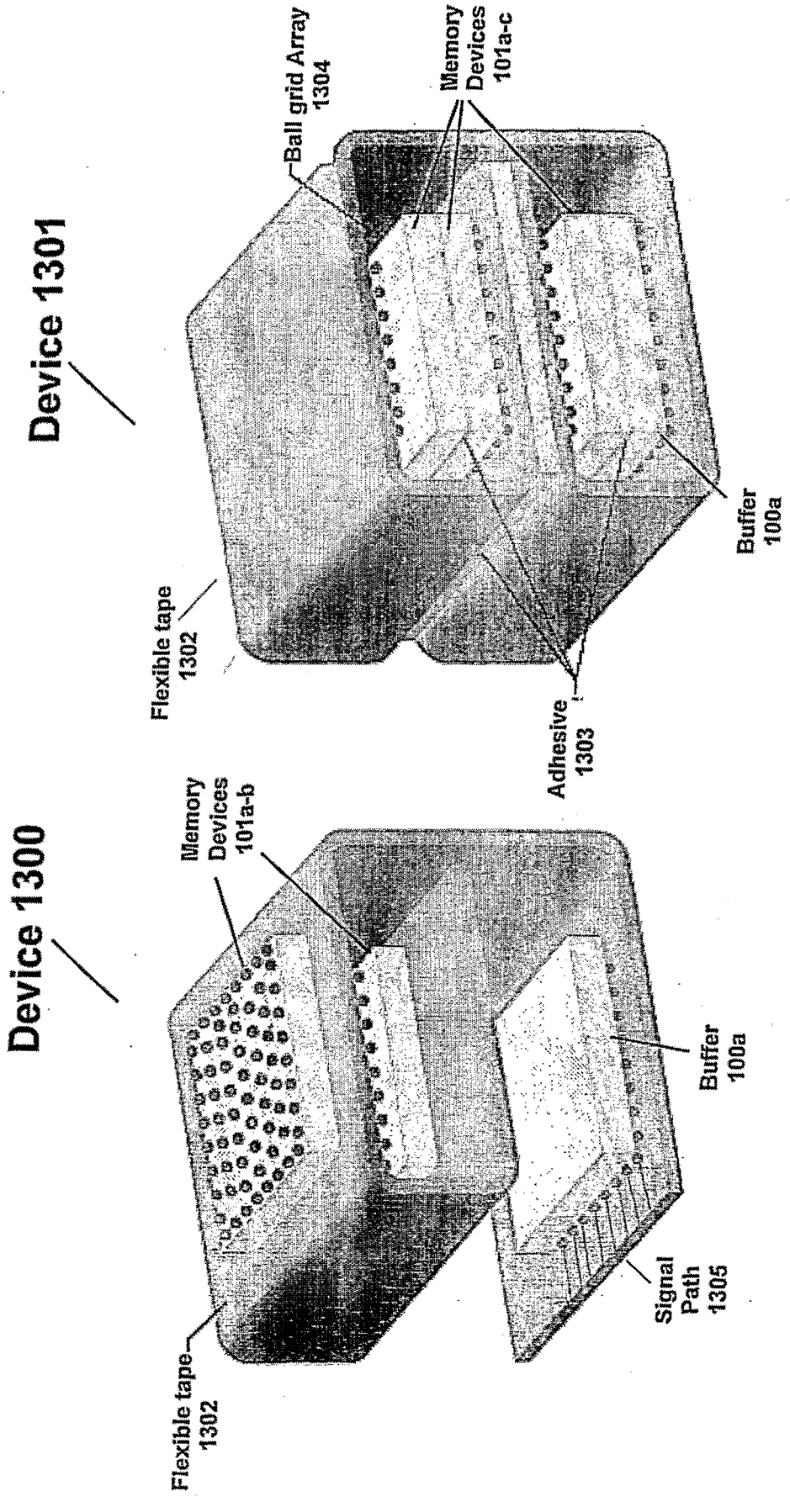
Device 1301
Ball grid Array 1304
Memory Devices 101a-c
Buffer 100a
Flexible tape 1302
Adhesive 1303
Device 1300
Memory Devices 101a-b
Buffer 100a
Signal Path 1305
Flexible tape 1302

Fig. 13

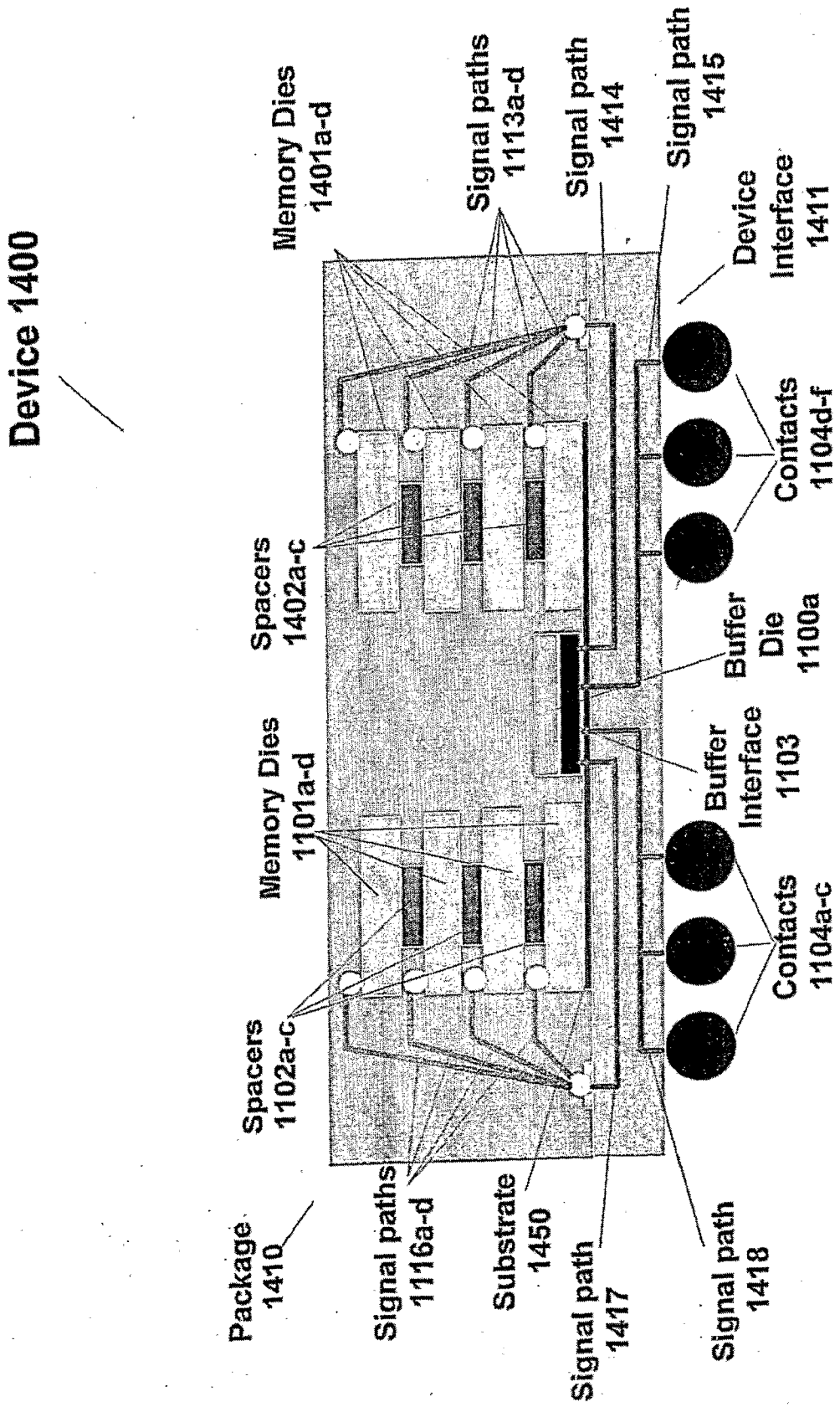
Device 1400
Memory Dies 1401a-d
Signal paths 1113a-d
Signal path 1414
Signal path 1415
Device Interface 1411
Contacts 1104d-f
Buffer Die 1100a
Buffer Interface 1103
Contacts 1104a-c
Spacers 1402a-c
Memory Dies 1101a-d
Spacers 1102a-c
Package 1410
Signal paths 1116a-d
Substrate 1450
Signal path 1417
Signal path 1418

Fig. 14

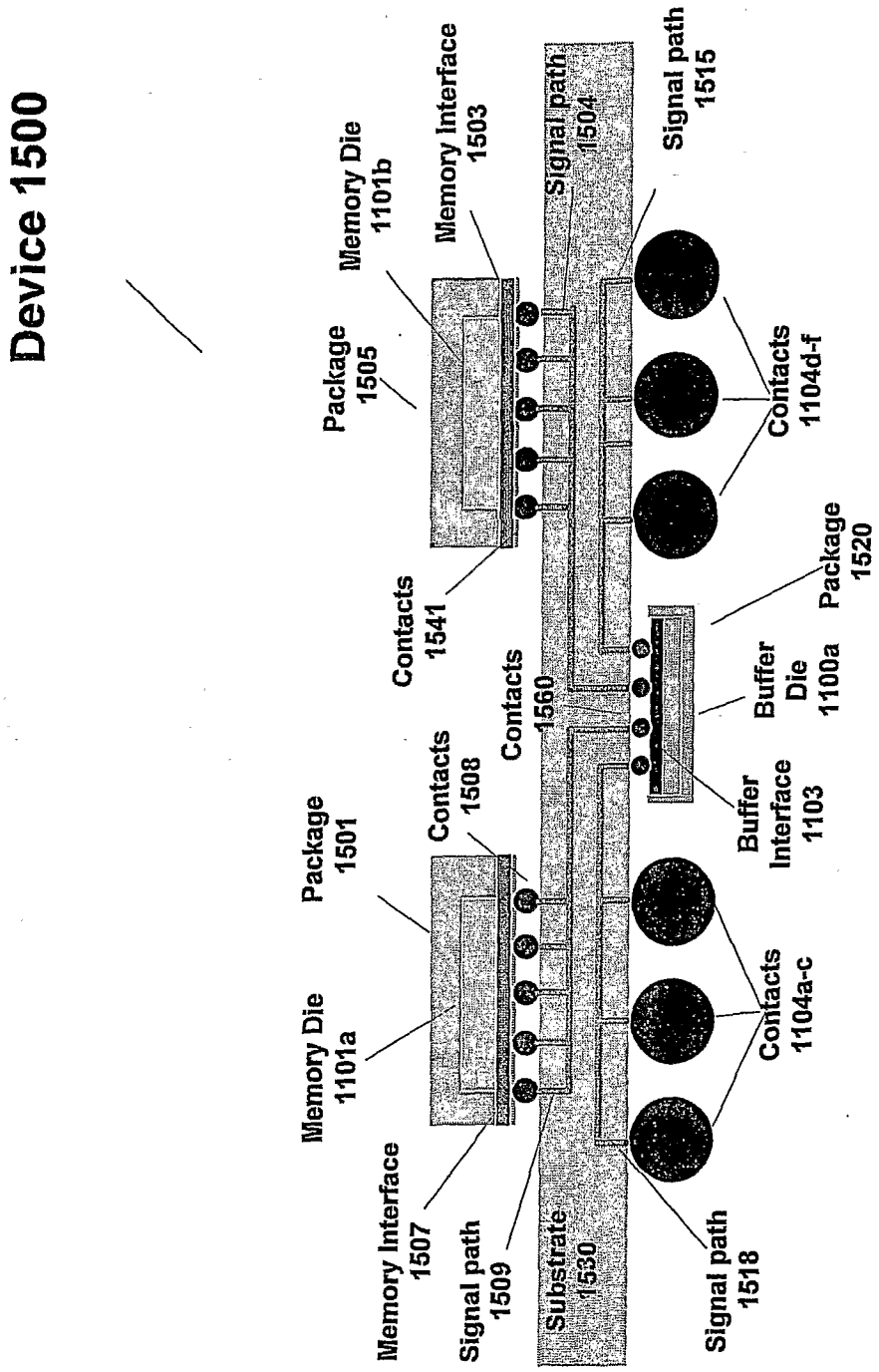
Device 1500
Memory Die 1101b
Memory Interface 1503
Signal path 1504
Signal path 1515
Package 1505
Contacts 1104d-f
Contacts 1541
Package 1520
Buffer Die 1100a
Contacts 1560
Buffer Interface 1103
Package 1501
Contacts 1508
Memory Die 1101a
Contacts 1104a-c
Memory Interface 1507
Signal path 1509
Substrate 1530
Signal path 1518

Fig. 15

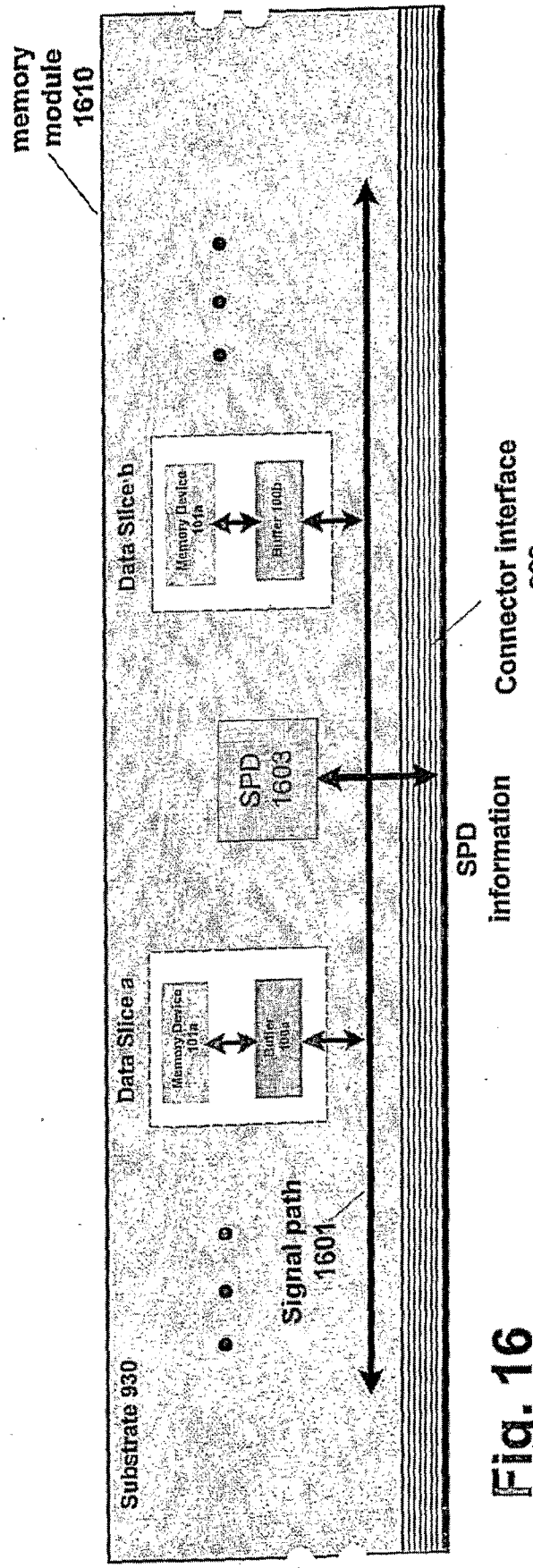
memory module 1610
Substrate 930
Data Slice a
Memory Device 101a
Buffer 100a
Data Slice b
Memory Device 101a
Buffer 100b
SPD 1603
Signal path 1601
Connector interface 920
SPD information

Fig. 16

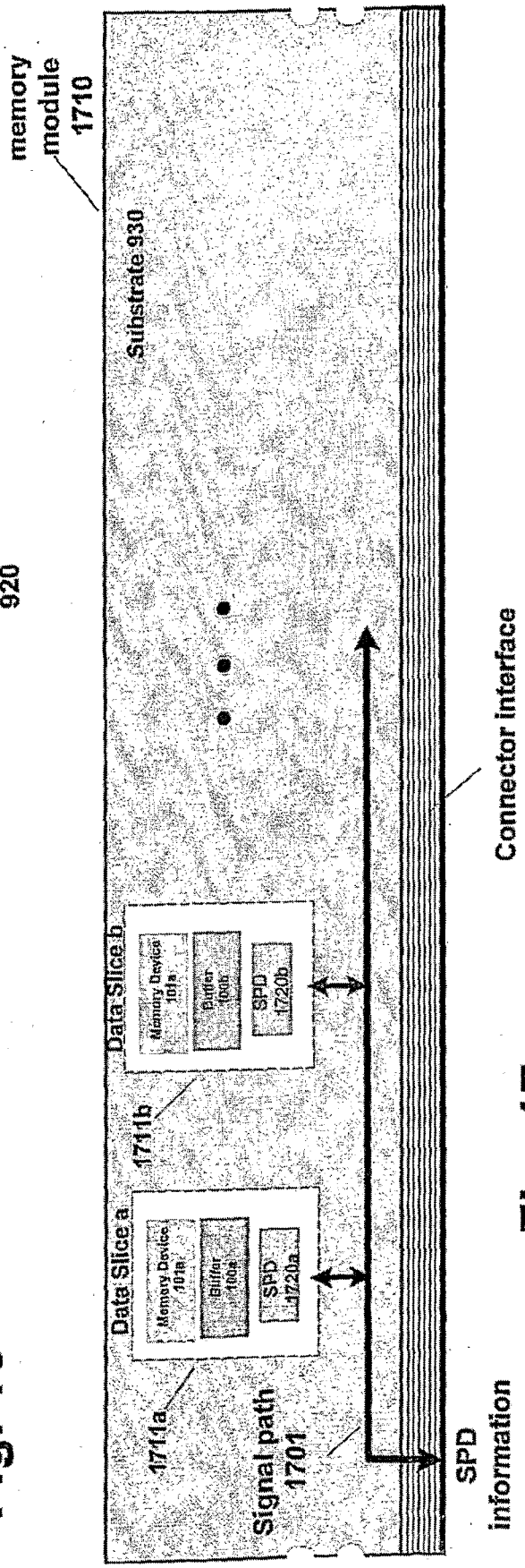
memory module 1710
Substrate 930
Data Slice a
1711a
Memory Device 101a
Buffer 100a
SPD 1720a
Data Slice b
1711b
Memory Device 101a
Buffer 100a
SPD 1720b
Signal path 1701
Connector interface 920
SPD information

Fig. 17

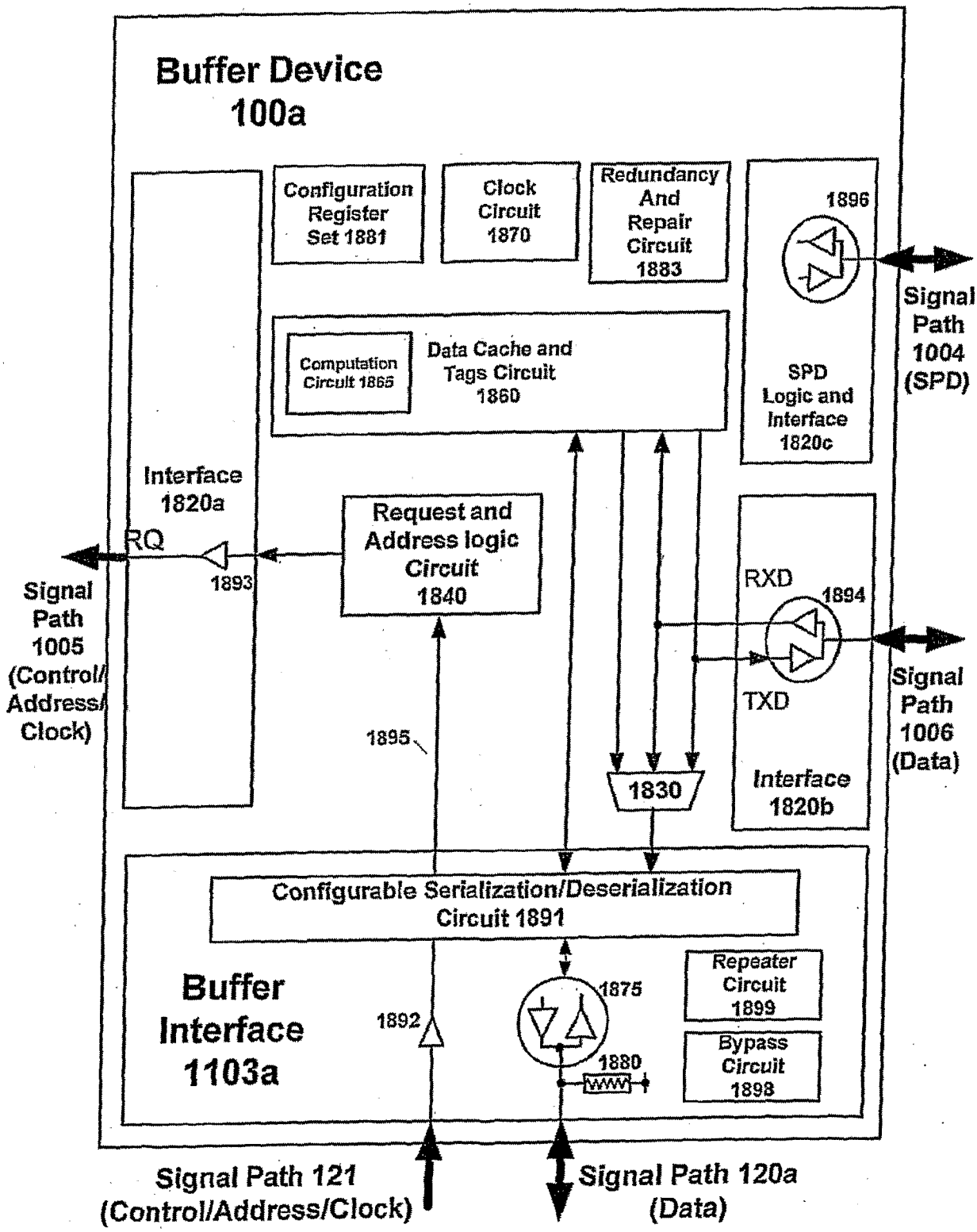
Buffer Device
100a
Configuration Register Set 1881
Clock Circuit 1870
Redundancy And Repair Circuit 1883
1896
Signal Path 1004 (SPD)
Computation Circuit 1865
Data Cache and Tags Circuit 1860
SPD Logic and Interface 1820c
Interface 1820a
RQ
1893
Request and Address logic Circuit 1840
Signal Path 1005 (Control/ Address/ Clock)
RXD
1894
TXD
Signal Path 1006 (Data)
1895
1830
Interface 1820b
Configurable Serialization/Deserialization Circuit 1891
Buffer Interface 1103a
1892
1875
1880
Repeater Circuit 1899
Bypass Circuit 1898
Signal Path 121 (Control/Address/Clock)
Signal Path 120a (Data)

Fig. 18

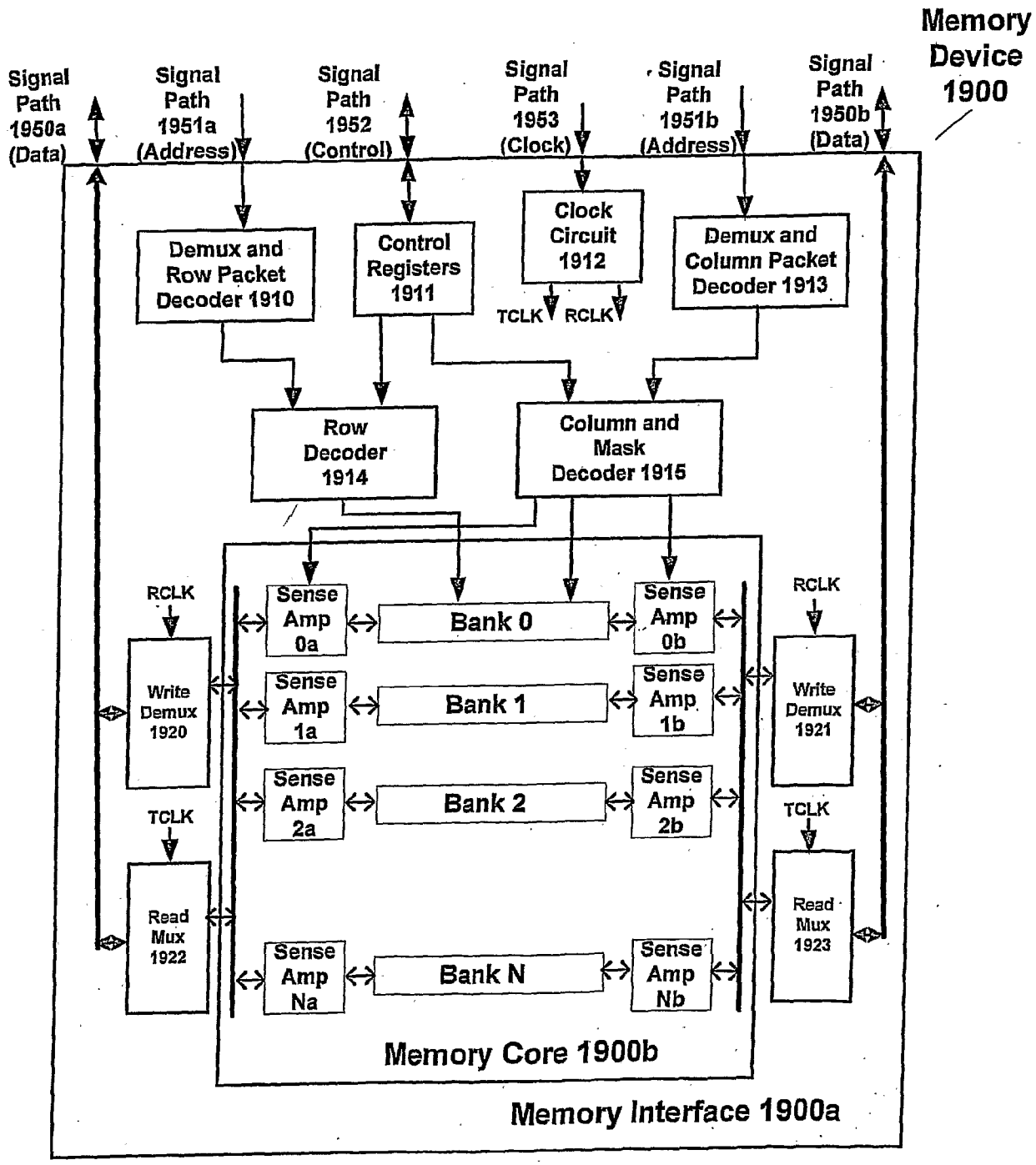
Memory Device 1900
Signal Path 1950a (Data)
Signal Path 1951a (Address)
Signal Path 1952 (Control)
Signal Path 1953 (Clock)
Signal Path 1951b (Address)
Signal Path 1950b (Data)
Demux and Row Packet Decoder 1910
Control Registers 1911
Clock Circuit 1912
TCLK
RCLK
Demux and Column Packet Decoder 1913
Row Decoder 1914
Column and Mask Decoder 1915
RCLK
Sense Amp 0a
Bank 0
Sense Amp 0b
Write Demux 1920
Sense Amp 1a
Bank 1
Sense Amp 1b
Write Demux 1921
Sense Amp 2a
Bank 2
Sense Amp 2b
TCLK
TCLK
Read Mux 1922
Sense Amp Na
Bank N
Sense Amp Nb
Read Mux 1923
Memory Core 1900b
Memory Interface 1900a

Fig. 19