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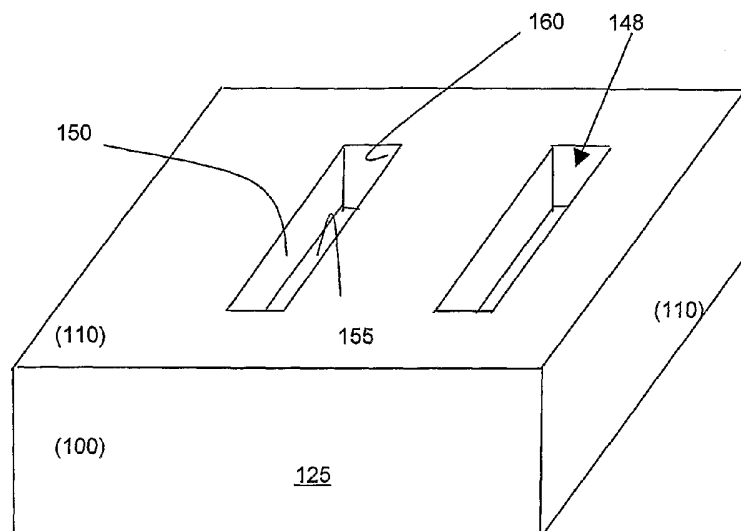
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(54) Title: IMPROVED TRENCHED MOSFETS WITH PART OF THE DEVICE FORMED ON A (110) CRYSTAL PLANE



(57) Abstract: This invention discloses an improved MOSFET devices manufactured with a trench gate by forming part of the trench on a (110) crystal orientation of a semiconductor substrate. The trench is covering with a dielectric oxide layer along the sidewalls and the bottom surface or the termination of the trench formed along different crystal orientations of the semiconductor substrate. Special manufacturing processes such as oxide annealing process, special mask or SOG processes are implemented to overcome the limitations of the non-uniform dielectric layer growth.

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IMPROVED TRENCHED MOSFETS WITH PART OF THE DEVICE FORMED ON A (110) CRYSTAL PLANE

BACKGROUND OF THE INVENTION

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1. Field of the Invention

10 The invention relates generally to the semiconductor power devices. More particularly, this invention relates to a novel and improved manufacture method and device configuration for a metal-oxide semiconductor field effect transistor (MOSFET) trench power device manufactured with part of trench oriented on a (110) crystal plane of a silicon wafer.

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2. Description of the Prior Art

20 Even though the techniques to provide improved carrier mobility for a P-channel MOSFET, i.e., metal oxide silicon field effect transistors, by forming the transistor on a (110) crystal plane is known, the difficulties of high interface state density is still a limitation for practical implementation of such configurations. Specifically, Sze disclosed in "Physics of Semiconductor Devices" (Wiley-Interscience, 1969, pp. 16, pp. 473) and B. Goebel, D. Schumann, E. Bertagnolli disclosed in IEEE Trans. Electronics Devices, Vol.48, No. 5, May 2001, pp. 897-906 that there is a thicker oxidation and higher interface state density along a (110) crystal plane. The thicker oxidation thus results in a thick gate oxide layer and lead to an adversely affected higher threshold voltage.

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Historically, the MOS devices are formed on the silicon wafer along a crystal orientation of a (100) plane because the oxide layer grown on a (100) plane has the lowest fixed charge and interface state density. For these reasons, the trench walls of the N-channel and P-channel of the trench MOSFETs are typically oriented along the (100) plane as well. Specifically, for a N-channel device, the channel formed along the (100) orientation has the benefit for achieving higher channel mobility. In contrast, the oxide layer grown along the (110) plane has greater thickness and higher interface state density. A thicker oxide layer often leads to a higher threshold voltage and

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lower transconductance. Furthermore, measured data also provide some evidence that thicker oxide layer also causes a degradation of channel mobility. Due to these concerns, forming the MOSFET power devices using a (100) crystal orientation has become a common rule in the conventional design methods. However, there are potential benefits of forming the power MOSFET devices or at least part of the transistors on the (110) plane. These potential benefits are often ignored due to the common practice as typically carried out by those of ordinary skill in the art without further exploration. Furthermore, even when there are several US Patents and Patent Applications that explored the techniques of building the MOS devices on a semiconductor substrate having a (110) crystal orientation, these disclosures are still limited by several technique difficulties due to different practical configuration and manufacture constraints due to the oxide layer thickness variations along different crystal orientations as will be discussed below.

In US Patent 4,933,298, entitled "Method of making high speed semiconductor device having a silicon-on-insulator structure", Hasegawa discloses a CMOS silicon-on-insulation structure fabricated by first forming an insulating SiO₂ layer on a silicon substrate having a (110) plane. Openings are then formed in the SiO₂ layer to expose a part of the substrate, and a polycrystalline or an amorphous silicon layer is deposited on the SiO₂ layer and in the openings. The deposited silicon layer is divided into islands so that a first island includes one of the openings and a second island does not include any openings. A laser beam is then irradiated onto the islands so as to melt the islands, and when the laser light irradiation is discontinued, the melted islands recrystallize so that the first island forms a (110) plane and the second island forms a (100) plane. A p-channel MOSFET is fabricated on the first island, and an n-channel MOSFET is fabricated on the second island. The thus paired CMOS operates at high speeds, because the p-channel MOSFET using positive holes as the carrier is fast in a (110) crystal, and the n-channel MOSFET using electrons as the carrier is fast in a (100) crystal. Hasegawa disclose the benefits of building a p-channel MOSFET in a (110) crystal plane, however the configurations and method as disclosed would be too complicate and costly with limited merits for practical application to build a commercial MOSFET product.

In another US Patent 6,245,615 entitled "Method and apparatus on

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(110) surfaces of silicon structures with conduction in the (110) direction” Noble et al. disclosed methods and structures that are lateral to surfaces with a (110) crystal plane orientation such that an electrical current of such structures is conducted in the (110) direction for the purposed of achieving improvements in hole carrier mobility. The structure's channel is oriented in a (110) plane such that the electrical current flow is in the (110) direction. A method of forming an integrated circuit includes forming a trench in a silicon wafer with the trench wall oriented to have a (110) crystal plane orientation. A semiconductor device is also formed lateral to the trench wall such that the semiconductor device is capable of conducting an electrical current in a (110) direction. The method disclosed by Noble et al. provides for forming an integrated circuit including an array of MOSFETs and another method includes forming an integrated circuit including a number of lateral transistors. The disclosure also includes structures as well as systems incorporating such structures all formed according to the methods provided in this application. Noble's disclosures are however for a lateral device. A vertical trench MOS device would require different considerations.

Fig. 1 shows a typical trench power MOSFET device that has its MOS channel vertically along the sidewall of a trench 10. The trench sidewall is covered by the gate dielectric 20, and is filled with the gate electrode material 30. Current flows from the source contact 40 to the drain contact 50, vertically down along the channel when the gate voltage is sufficient to connect the source and drain regions by an inversion layer of mobile carriers, e.g., electrons for n-channel and holes for p-channel. Many such cells operated in parallel form a power MOSFET.

Table 1 shows the measured data that summarizes the characteristics of two identical P-channel MOSFETs next to each other on the same wafer, with the channel formed on (100) and (110) interfaces respectively on a (100) wafer. An (110) orientation on the trench sidewall where the channel is formed is achieved by simply rotating the FETs by 45 degrees as can be seen from Fig. 2. The results from two wafers are shown. The only difference in process between the two wafers is the duration of gate oxidation.

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Crystal Orientation	Estimated Oxide thickness	Vth	Rds1 Vgs=10V	Rds2 Vgs=4.5V	Rds3 Vgs=2.5V	Qg
100	250 Å	0.99V	0.37 Ohm	0.37 Ohm	0.37 Ohm	1.02 nC
110	330 Å	1.33V	0.31 Ohm	0.31 Ohm	0.31 Ohm	0.82 nC

Crystal Orientation	Estimated Oxide thickness	Vth	Rds1 Vgs=10V	Rds2 Vgs=4.5V	Qg
100	450 Å	1.7V	0.37 Ohm	0.83 Ohm	
110	600 Å	2.6V	0.31 Ohm	0.78 Ohm	

5 It is clear from those measured data that there is a significant increase in threshold voltage, i.e., Vth, caused by the thicker oxide for (110) oriented device. However, there is a marked improvement in on-resistance, especially at higher gate bias, showing that there must have been a large improvement in the hole-channel mobility.

10 Therefore, a need still exists in the art of MOSFET device design and manufacture to provide new design method and device configuration in forming the MOSFET channel along the (110) plane to achieve device performances.

15 SUMMARY OF THE PRESENT INVENTION

It is therefore an object of the present invention to provide a new design and manufacturing methods and device configuration for the power MOSFET devices to take advantages of building the devices on planes of different crystal orientations such that the limitations of the conventional methods can be overcome.

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Specifically, it is an object of the present invention to provide improved MOSFET devices manufactured with a trench gate by forming part of the trench on a (110) crystal orientation of a semiconductor substrate. The trench is covering with a dielectric oxide layer along the sidewalls and the bottom surface or the termination of the trench formed along different crystal orientations of the semiconductor substrate. Special manufacturing processes such as oxide annealing process, special mask or SOG processes are

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implemented to overcome the limitations of the non-uniform dielectric layer growth. In a special preferred embodiment, forming the trenches with a stripe configuration, and choosing a different orientation of the seed crystal can produce an orientation of the trench with both sidewalls and bottom
5 surface align along a (110) crystal orientation of the semiconductor substrate.

Briefly in a preferred embodiment this invention discloses a trenched MOSFET power transistor that includes a gate disposed in a trench formed in a semiconductor substrate. The trench further includes sidewalls and a trench
10 bottom surface all formed along a (110) crystal orientation of the semiconductor substrate. In a preferred embodiment, the MOSFET power transistor is a P-channel MOSFET power transistor. In a different preferred embodiment, this invention further discloses a trenched MOSFET power transistor comprising a gate disposed in a trench formed in a semiconductor
15 substrate. The trench further includes sidewalls formed along a first crystal orientation of the semiconductor substrate and a trench bottom surface formed along a second crystal orientation of the semiconductor substrate different from the first crystal orientation. The trench further includes an oxide layer covering the sidewalls having a substantially the same thickness
20 as an oxide layer covering the bottom surface of the trench.

These and other objects and advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiment, which is
25 illustrated in the various drawing figures.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross sectional view of a MOSFET device manufactured
30 according to a process of this invention;

Fig. 2 shows two identical MOSFETs next to each other on the same wafer, with the channel formed on (100) and (110) interfaces on the vertical sidewall respectively on a (100) wafer.

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Figs. 3A and 3B are perspective views for showing the crystal orientations of a silicon ingot and the configuration of a trench;

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Fig. 4A to 4C are cross sectional views for showing the process to form the trench aligned along different crystal orientations of a semiconductor substrate;

5 Fig. 5 is a perspective view for showing the termination tip of a trench to minimize the (100) plane effect;

10 Figs. 6A to 6C are perspective views for showing manufacturing processes using SOG to thicken the oxide at the termination of a trench;

Figs. 7A and 7B are perspective views for showing an annealing process to produce trench oxide layer covering (110) and (100) planes of uniform thickness;

15 Figs. 8A to 8C show the cross sectional view of another embodiment using (100) wafer as starting material, following the steps described in Figs. 4A - 4C;

20 Fig. 9 is a perspective view of a P-channel DMOS with channel along (110) plane; and

Figs. 10 is a perspective view of a wafer and the trench for a N-channel
25
trenched MOSFET device with the bottom of the trench formed on a (110) plane and the sidewalls on the (100) plane.

DETAILED DESCRIPTION OF THE METHOD

For P-channel implementations, Fig. 3A and 3B show the orientations of the substrate and trench according to the current invention. In Fig. 3A, the
30 silicon ingot 125 is grown in the (110) plane. The silicon ingot 125 provides a configuration that four sidewalls are situated with four sidewall surfaces forming a corner with a corner angle of 90 degrees, thus these sidewall surfaces are perpendicular to each other. Two of these sidewalls are along a (100) crystal orientation and two are along a (110) crystal orientation.
35 Referring to Fig. 3A, two sidewalls 150 and bottom 155 of the trench 148 are formed along a (110) crystal orientation while the termination end surface 160 of the trench 148 is formed along a (100) crystal orientation. In Fig. 3B, the

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wafer 325 is formed by rotating a normal (100) wafer as shown in Fig. 2 by 45° thus forming two interface planes on a (110) plane while the top and bottom planes are still on the (100) plane. As can be observed from Fig. 3B, when a trench 348 is formed with the sidewalls 350 along the (110) plane, the bottom 355 of the trench is still oriented along a (100) plane. Due to these different orientations, the gate oxide layer along the sidewalls formed along the (110) will be thicker than the gate oxide layer formed on the bottom of the trench along the (100) plane during thermal oxidation process. In order to fabricate a device capable of an operating voltage at a given gate voltage, the thin oxide bottom or end surface of the trench sets the minimum oxide thickness usable. This then forces the use of a thicker oxide along the sidewall compared to a device with all trench sides along the (100), and causes a higher threshold voltage for a given channel doping profile. To minimize the effect of (100) surface, stripe structure design with round termination or round bottom is incorporated with dielectric layer thickening techniques to provide improve P-channel trench MOSFET device.

Referring to Fig. 4A, one embodiment uses (110) wafer 125 as substrate. An oxide layer 135 is formed on the top (110) surface by thermal oxidation. A trench mask 145 is used to expose the silicon dioxide in the area for forming the trenches as shown in Fig. 4C below. In one embodiment, the trench mask may have a round or oval shape where the trench ends. As shown in Fig. 5, this produces a trench with round termination therefore the section lying along the (100) plane during trench dry etching process is minimized. Referring to Fig. 4B, after the exposed oxide is removed by etching, the photoresist 145 is stripped off and the remaining oxide layer 135 forms the hard mask for forming the trenches where the oxide layer 135 is removed. Referring now to Fig. 4C, the trenches 148 are then formed along the (110) direction on the wafer by dry etching process. Thus, by using a stripe design, it is possible for the trench MOSFET to have the trench sidewalls 150 and the channel, and the trench bottom 155 along a (110) interface, making the gate oxide thickness uniform both along the sidewall and at the trench bottom. Therefore, the on resistance of the device may be reduced. However, as that shown in Fig. 5, in the area 160 where the trench terminates, some part of the tip will be in the (100) plane. The gate oxide may be thinner at the trench termination area 160 thus limiting gate maximum rating of the gate oxide.

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In order to overcome the technical difficulties caused by a non-uniform thickness of the gate dielectric layer when part of the device is formed along different crystal orientations, the thickness of oxide layer around (100) plane is enhanced to provide a gate oxide layer with uniform thickness or even thicker at the trench bottom or at the trench termination. Numerous oxide thickening techniques may be used to achieve the above design goal. Several measures are disclosed in this invention.

Figs. 6A to 6C shows another P-channel MOSFET device 200 that has a configuration with the trench sidewalls formed along the (110) plane while using a mask to form thicker oxide in the designated areas thus minimizing the effects of uneven thickness of gate oxide layer. After the trench is formed, it is filled with oxide 210 using techniques such as SOG (spin on glass) or oxide deposition as shown in Fig. 6A. Alternatively, an oxide layer may thermally be grown over the entire Silicon surface. A mask 220 is used to generate a protection area at the trench termination as that shown in Fig. 6B. The oxide is then etched back with the oxide in the terminal area intact as that shown in Fig 6C. A sacrificial oxide layer may be thermally grown and then removed by wet etch to remove the defects on silicon surface on the bottom and the sides of the trench caused by the harsh etching process during trench formation and SOG etch back. A high quality gate oxide is then thermally grown (not shown).

Figs. 7A to 7B show another embodiment, using a high temperature gate anneal to flow the oxide, so its thickness loses its orientation dependence. As seen in Fig. 7A, when following the regular process, the gate oxide layer 260 is thinner at the trench termination tip portion of (100) plan. After annealing at a temperature higher than 950°C, silicon oxide goes into viscous flow and losses its orientation dependence to yield a film with uniform thickness. Fig 7B shows the result after 1200°C of annealing for 5 minutes.

Figs. 8A to 8C show another embodiment using (100) wafer 325 as starting material. Following the steps described in Figs. 4A - 4C, a trench 348 with both side walls 350 and termination end faces (not shown) on (110) plane is obtained. The trench bottom 355 is in (100) plane. An additional ion reactive etching process is performed to round the bottom 355 of the trench. To overcome the technical difficulties caused by a non-uniform thickness of the

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gate oxide layer when part of the device is formed along different crystal orientations, the thickness of oxide layer around (100) trench bottom is enhanced to provide a gate oxide layer with uniform thickness or even thicker at the trench bottom or at the trench termination. Referring to Fig. 8B, a layer of oxide is deposited to fill the bottom of trench. Alternatively, polysilicon
5 may be deposited and then oxidized, or SOG may be used to fill the trench. The oxide is then etched back. In one embodiment, the oxide is etched with a mask. In another embodiment, the oxide is etched backed without using a mask. The etch back process goes on until the thickness of the bottom oxide
10 310 reaches a predetermined thickness (Fig. 8C). A sacrificial oxide layer may be thermally grown and then removed by wet etch to remove the defects on silicon surface on the sides of the trench caused by the harsh etching process during trench formation and oxide etch back. A high quality gate oxide is then thermally grown. As shown in Fig. 8D, this yields a layer of gate oxide
15 320 lining within the trench 348 where the oxide thickness at the bottom portion 355 has been increased so that the overall thickness is substantially the same.

Other techniques and any of combinations of these techniques
20 including those mentioned above can be used to increase the thickness of thin dielectric layer portion in the trench when part of the device is formed along different crystal orientations. This will improve the device rating without deteriorating the performance.

After the gate dielectric layer is formed in the trench, standard trench MOSFET processes are carried out to complete the fabrication of a MOSFET device 400 as that shown in Fig. 9. The processes for the formation of the gate
25 410, the body 420, the source 430, BPSG deposition 440, and contact with the substrate 405 functioning as a drain are well know in the art, to form the device as shown in Fig. 9. This invention discloses a trenched MOSFET
30 device 400 formed on a silicon substrate with sidewalls of the trench formed along a (110) crystal plane. The sidewalls and the bottom surface are covered with an dielectric layer 415 having substantially a uniform thickness on the sidewalls and the bottom surface. In one embodiment, the trench and gate is
35 formed before the formation of body or source. In another embodiment, the trench and gate is formed after the formation of body or source.

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Referring to Figs. 10 are perspective views for forming an N-channel
trenched MOSFET device with a part of the device on a (110) plane. The
wafer 510 is a (110) wafer. A stripe design is implemented wherein a
trenched N-channel MOSFET 500 is formed with the trenches 520 perpendicular to the
5 (110) direction. This orientation of the trench results in a configuration where
the sidewalls 525 of the trench 520 are formed on the (100) plane while the
bottom of the trench 530 is formed on a (110) plane. This process naturally
produces a thicker gate oxide on the bottom of the trench. The thicker oxide at
the bottom has several advantages that the thick gate oxide at the bottom
10 reduces the gate-drain capacitance, leading to a faster switching MOSFET.
Furthermore, the thicker gate oxide at the bottom of the trench reduces the
electric field at the trench bottom, increasing the breakdown voltage. This
allows the designer to increase the epitaxial layer doping, thereby lowering
the on-resistance of the MOSFET. For a stripe configuration as shown, the
15 trench termination will also lie on a 110 plane, and since the oxide is thicker
here, there is no penalty in gate voltage rating.

Thus this invention discloses a N-channel MOSFET device having a
trench wherein a sidewall of the trench is oriented along a different crystal
20 orientation than a bottom of the sidewall. In a preferred embodiment, the
bottom of the trench is oriented along a (110) crystal plane. In another
preferred embodiment, the sidewall is oriented along a (100) crystal plane. In
yet another embodiment, the trench and gate is formed before the formation
of body or source. In yet another embodiment, the trench and gate is formed
25 after the formation of body or source.

Although the present invention has been described in terms of the
presently preferred embodiment, it is to be understood that such disclosure is
not to be interpreted as limiting. Various alterations and modifications will no
30 doubt become apparent to those skilled in the art after reading the above
disclosure. Accordingly, it is intended that the appended claims be
interpreted as covering all alterations and modifications as fall within the true
spirit and scope of the invention.

CLAIMS

We claim:

1. A trench MOSFET power transistor comprising a gate disposed in a trench formed in a semiconductor substrate wherein:
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said trench further comprising sidewalls formed along a (110) crystal orientation of said semiconductor substrate.
2. The trench MOSFET power transistor of claim 1 wherein:
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said MOSFET power transistor is a P-channel MOSFET power transistor.
3. The trench MOSFET power transistor of claim 1 wherein:
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said trench further comprising a trench bottom surface formed along a (110) crystal orientation of said semiconductor substrate.
4. The trench MOSFET power transistor of claim 2 wherein:
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said trench further comprising a trench bottom surface formed along a (100) crystal orientation of said semiconductor substrate.
- 25
5. A trench MOSFET power transistor comprising a gate disposed in a trench formed in a semiconductor substrate wherein:
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said trench further comprising sidewalls formed along a first crystal orientation of said semiconductor substrate and a trench bottom surface formed along a second crystal orientation of said semiconductor substrate different from said first crystal orientation; and
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said trench further comprising an dielectric layer covering said sidewalls having a substantially same thickness as an dielectric layer covering said bottom surface of said trench.

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6. The trench MOSFET power transistor of claim 5 wherein:
said sidewall are formed along a (110) crystal orientation and
said bottom surface is formed along a (100) crystal orientation.
- 10
7. The trench MOSFET power transistor of claim 5 wherein:
said MOSFET power transistor is a P-channel MOSFET power
transistor.
- 15
8. The trench MOSFET power transistor of claim 5 wherein:
said sidewall are formed along a (100) crystal orientation and
said bottom surface is formed along a (110) crystal orientation.
- 20
9. The trench MOSFET power transistor of claim 5 wherein:
said MOSFET power transistor is a N-channel MOSFET power
transistor.
- 25
10. The trench MOSFET power transistor of claim 5 wherein:
said dielectric layer is an oxide layer having a substantially a
same thickness covering said sidewalls and said bottom surface
of said trench.

11. A trench MOSFET power transistor comprising a gate disposed in a trench formed in a semiconductor substrate wherein:

5 said trench further comprising sidewalls formed along a first crystal orientation of said semiconductor substrate and a trench bottom surface formed along a second crystal orientation of said semiconductor substrate, where both the first and second crystal orientations are (110) crystal orientation; and

10 said trench further comprising an dielectric layer covering said sidewalls having a substantially same thickness as an dielectric layer covering said bottom surface of said trench.

12. The trench MOSFET power transistor of claim 11 wherein:

15 said MOSFET power transistor is a P-channel MOSFET power transistor.

13. The trench MOSFET power transistor of claim 11 wherein:

20 said dielectric layer is an oxide layer having a substantially a same thickness covering said sidewalls and said bottom surface of said trench.

25 14. A trench MOSFET power transistor comprising a gate disposed in a trench formed in a semiconductor substrate wherein:

30 said trench further comprising sidewalls formed along a first crystal orientation of said semiconductor substrate and a trench termination end surface along a second crystal orientation of said semiconductor substrate different from said first crystal orientation.

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15. The trench MOSFET power transistor of claim 14 wherein
said termination end surface having a curved surface whereby
said termination end surface only having a small tip portion
5 formed along a second crystal orientation of said semiconductor
substrate different from said first crystal orientation.
16. The trench MOSFET power transistor of claim 14 wherein:
10 said sidewall are formed along a (110) crystal orientation and
said termination end surface is formed along a (100) crystal
orientation.
17. The trench MOSFET power transistor of claim 14 wherein:
15 said MOSFET power transistor is a P-channel MOSFET power
transistor.
18. The trench MOSFET power transistor of claim 14 wherein:
20 said sidewall are formed along a (100) crystal orientation and
said termination end surface is formed along a (110) crystal
orientation.
19. The trench MOSFET power transistor of claim 14 wherein:
25 said MOSFET power transistor is a N-channel MOSFET power
transistor.
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20. A trench MOSFET power transistor comprising a gate disposed in a trench formed in a semiconductor substrate wherein:

5 said trench further comprising sidewalls formed along a first crystal orientation of said semiconductor substrate and a trench termination end surface formed along a second crystal orientation of said semiconductor substrate different from said first crystal orientation; and

10 said trench further comprising an dielectric layer covering said sidewalls and said termination end surface wherein said dielectric layer covering said termination end surface is not thinner than said dielectric layer covering said sidewalls in the central area of the trench.

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21. The trench MOSFET power transistor of claim 20 wherein:

20 said sidewall are formed along a (110) crystal orientation and said termination end surface is formed along a (100) crystal orientation.

22. The trench MOSFET power transistor of claim 20 wherein:

25 said MOSFET power transistor is a P-channel MOSFET power transistor.

23. The trench MOSFET power transistor of claim 20 wherein:

30 said sidewall are formed along a (100) crystal orientation and said termination end surface is formed along a (110) crystal orientation.

24. The trench MOSFET power transistor of claim 20 wherein:

35 said MOSFET power transistor is a N-channel MOSFET power transistor.

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25. The trench MOSFET power transistor of claim 20 wherein:

said dielectric layer is an oxide layer having a substantially a same thickness covering said sidewalls and said termination end surface of said trench.

26. A method for manufacturing a trench MOSFET power transistor by forming a trench in a semiconductor substrate and then forming a gate in said trench wherein:

said step of forming said trench further comprising a step of forming said trench with sidewalls and a trench bottom surface all along a (110) crystal orientation of said semiconductor substrate.

27. The method of claim 26 further comprising a step of:

manufacturing said MOSFET power transistor as a P-channel MOSFET power transistor.

28. A method for manufacturing a trench MOSFET power transistor by forming a trench in a semiconductor substrate and then forming a gate in said trench wherein:

said step of forming said trench further comprising a step of forming said trench with sidewalls along a first crystal orientation of said semiconductor substrate and a trench bottom surface along a second crystal orientation of said semiconductor substrate different from said first crystal orientation; and

covering said sidewalls and said bottom surface with an dielectric layer having substantially a same thickness on said sidewalls and said bottom surface.

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29. The method of claim 28 further comprising a step of:

forming said sidewall along a (110) crystal orientation and said bottom surface along a (100) crystal orientation.

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30. The method of claim 28 further comprising a step of:

manufacturing said MOSFET power transistor as a P-channel MOSFET power transistor.

10

31. The method of claim 28 further comprising a step of:

forming said sidewall along a (100) crystal orientation and said bottom surface along a (110) crystal orientation.

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32. The method of claim 28 further comprising a step of:

manufacturing said MOSFET power transistor as a N-channel MOSFET power transistor.

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33. A method for manufacturing a trench MOSFET power transistor by forming a trench in a semiconductor substrate and then forming a gate in said trench wherein:

25

said step of forming said trench further comprising a step of forming said trench with sidewalls along a first crystal orientation of said semiconductor substrate and a trench termination end surface having a curved surface whereby said termination end surface only having a small tip portion formed along a second crystal orientation of said semiconductor substrate different from said first crystal orientation.

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34. The method of claim 33 further comprising a step of:

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forming said sidewall along a (110) crystal orientation and said termination end surface along a (100) crystal orientation.

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35. The method of claim 33 further comprising a step of:

manufacturing said MOSFET power transistor as a P-channel MOSFET power transistor.

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36. The method of claim 33 further comprising a step of:

forming said sidewall along a (100) crystal orientation and said termination end surface along a (110) crystal orientation.

10

37. The method of claim 33 further comprising a step of:

manufacturing said MOSFET power transistor as a N-channel MOSFET power transistor.

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38. A method for manufacturing a trench MOSFET power transistor by forming a trench in a semiconductor substrate and then forming a gate in said trench wherein:

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said step of forming said trench further comprising a step of forming said trench with sidewalls along a first crystal orientation of said semiconductor substrate and a trench termination end surface along a second crystal orientation of said semiconductor substrate different from said first crystal orientation; and

25

forming an dielectric layer covering said sidewalls and said termination end surface having substantially a same thickness covering said sidewalls and said termination end surface of said trench.

30

39. The method of claim 38 further comprising a step of:

forming said sidewall along a (110) crystal orientation and said termination end surface along a (100) crystal orientation.

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40. The method of claim 38 further comprising a step of:
manufacturing said MOSFET power transistor as a P-channel
MOSFET power transistor.
41. The method of claim 38 further comprising a step of:
forming said sidewall along a (100) crystal orientation and said
termination end surface along a (110) crystal orientation.
42. The method of claim 38 further comprising a step of:
manufacturing said MOSFET power transistor as a N-channel
MOSFET power transistor.

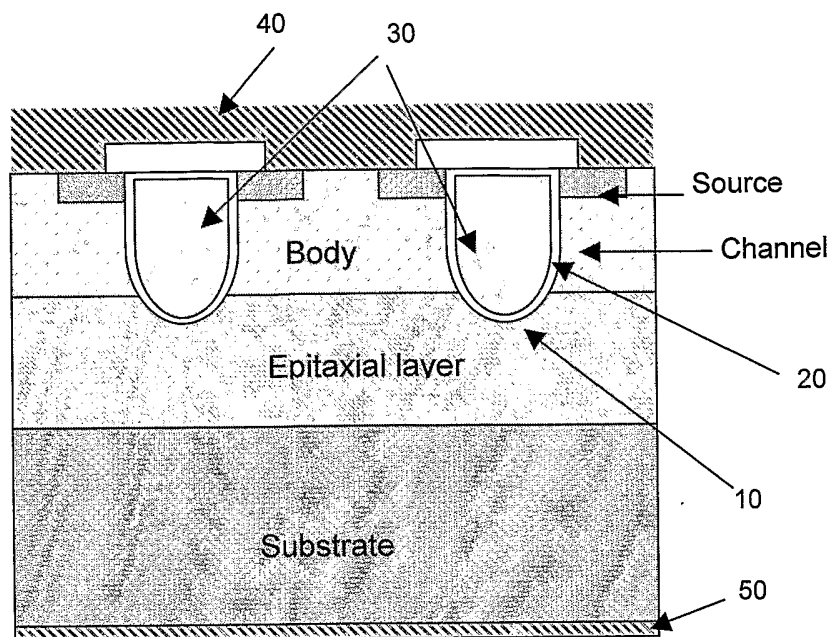


Fig. 1

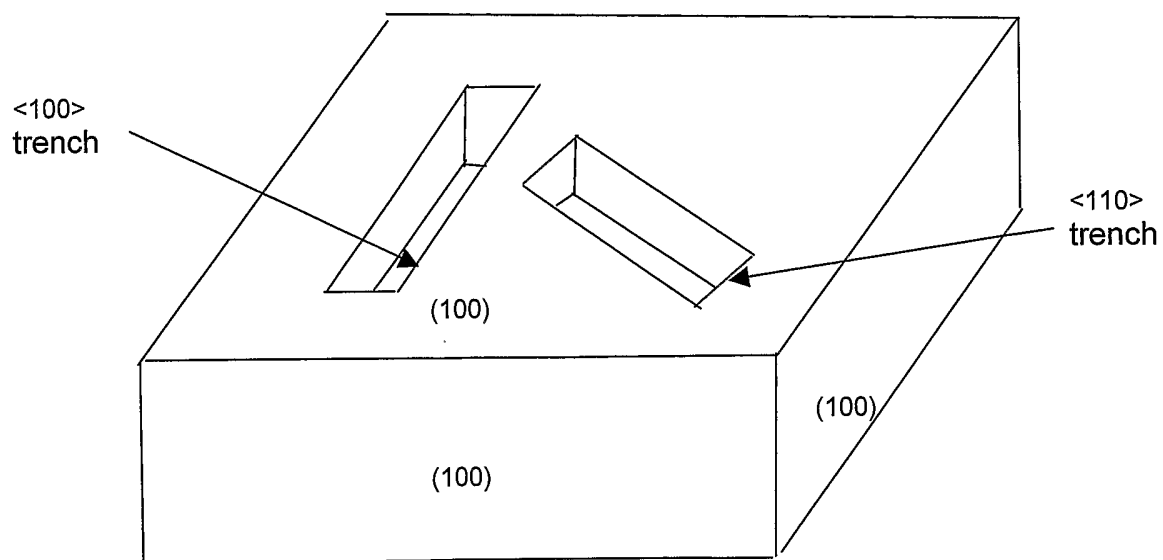
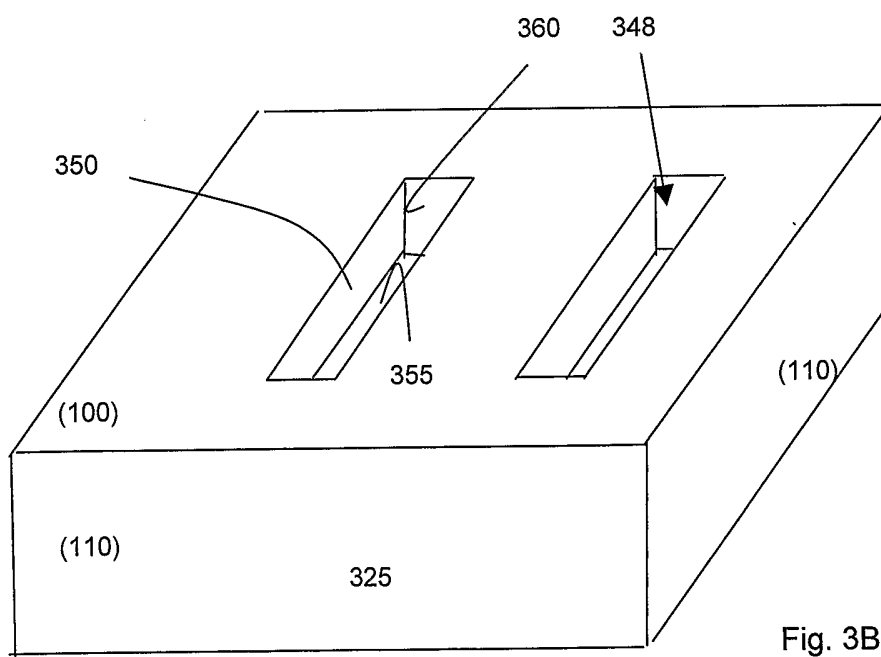
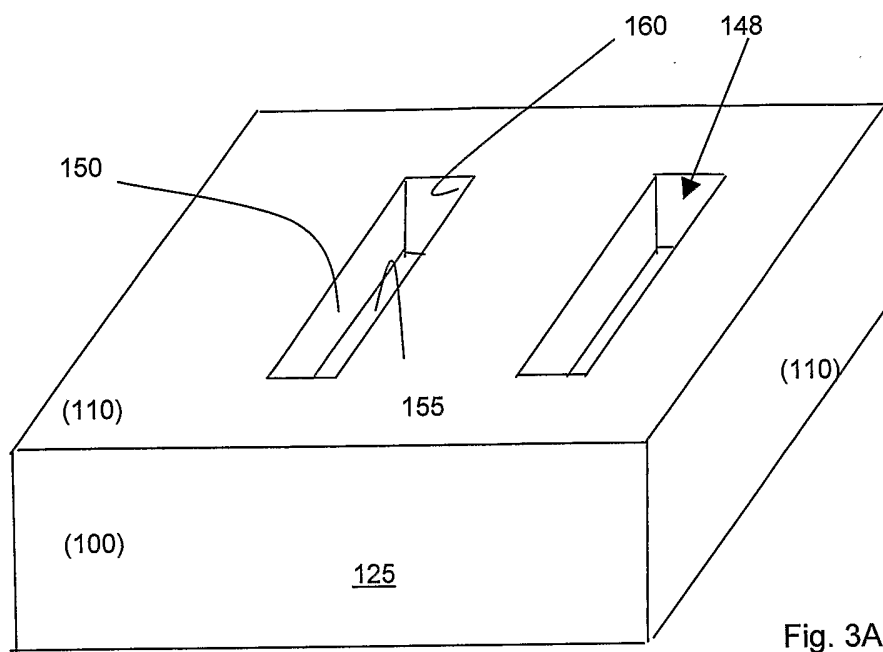


Fig. 2



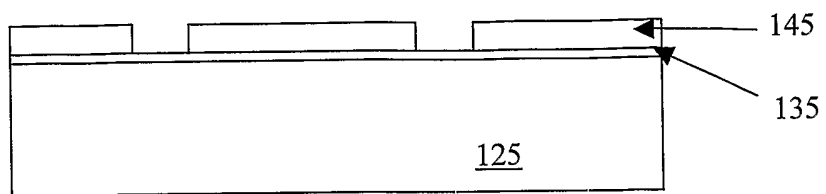


Fig. 4A

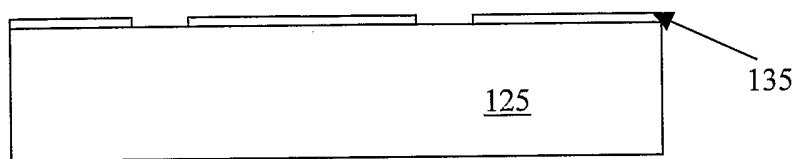


Fig. 4B

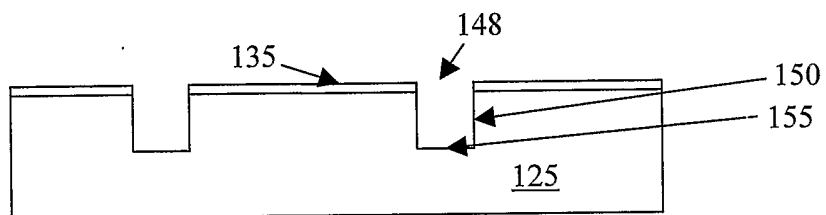


Fig. 4C

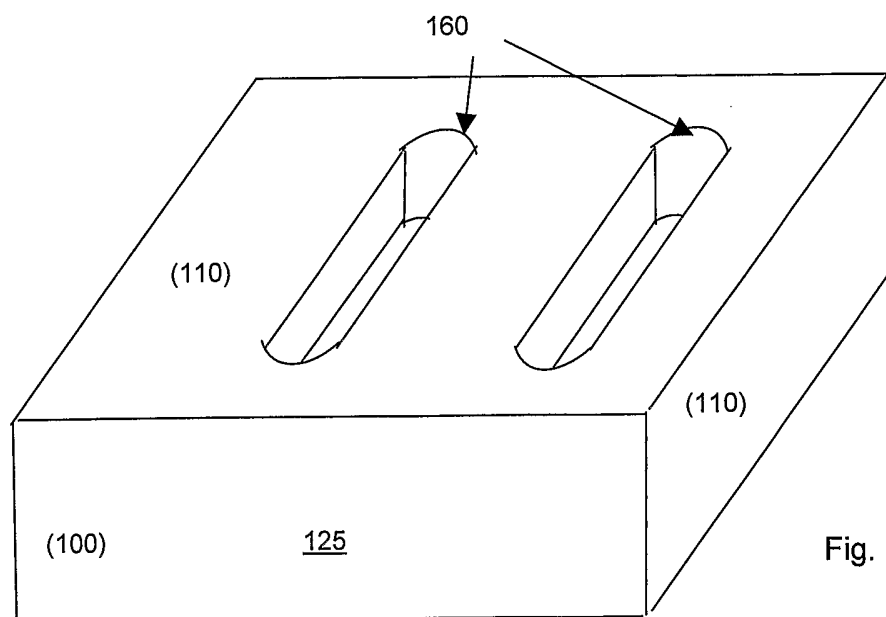


Fig. 5

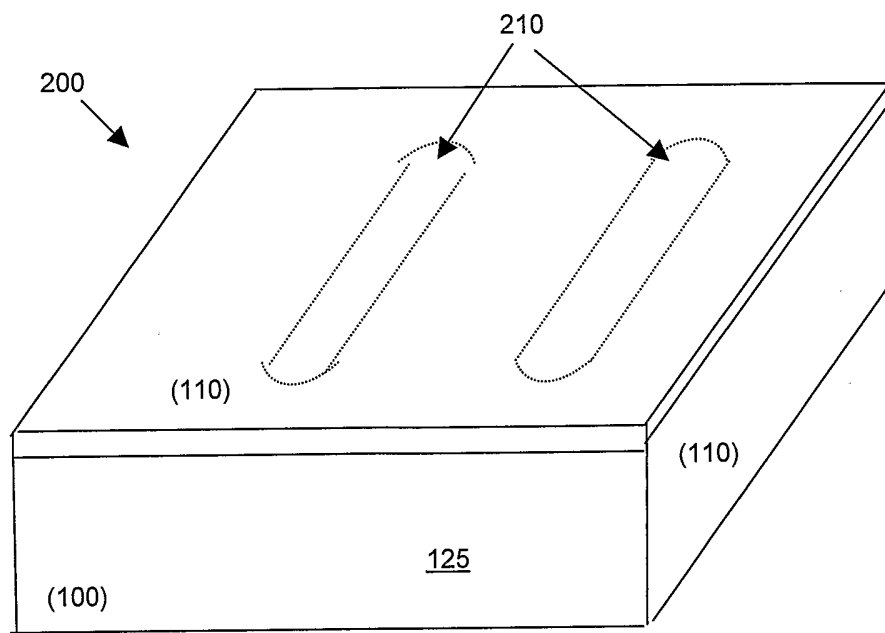
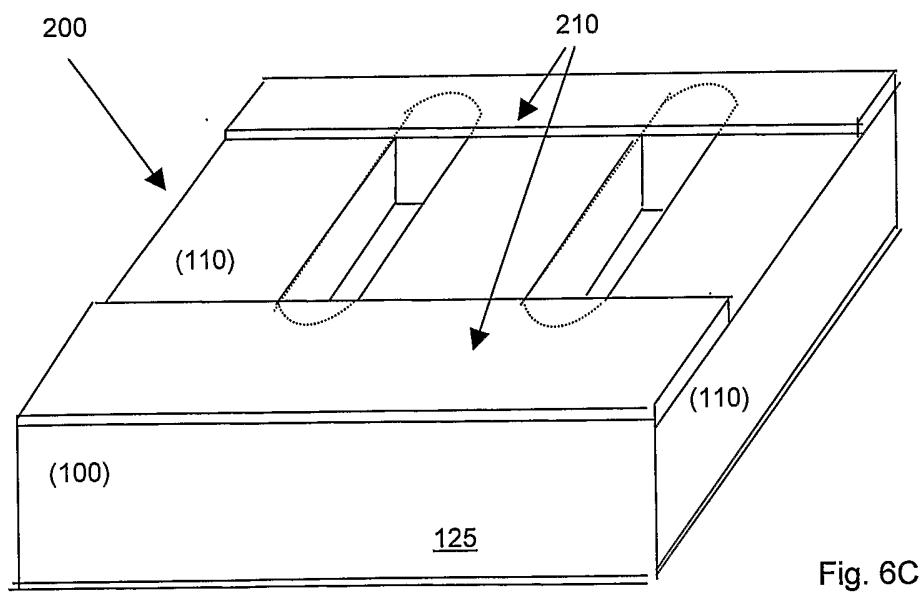
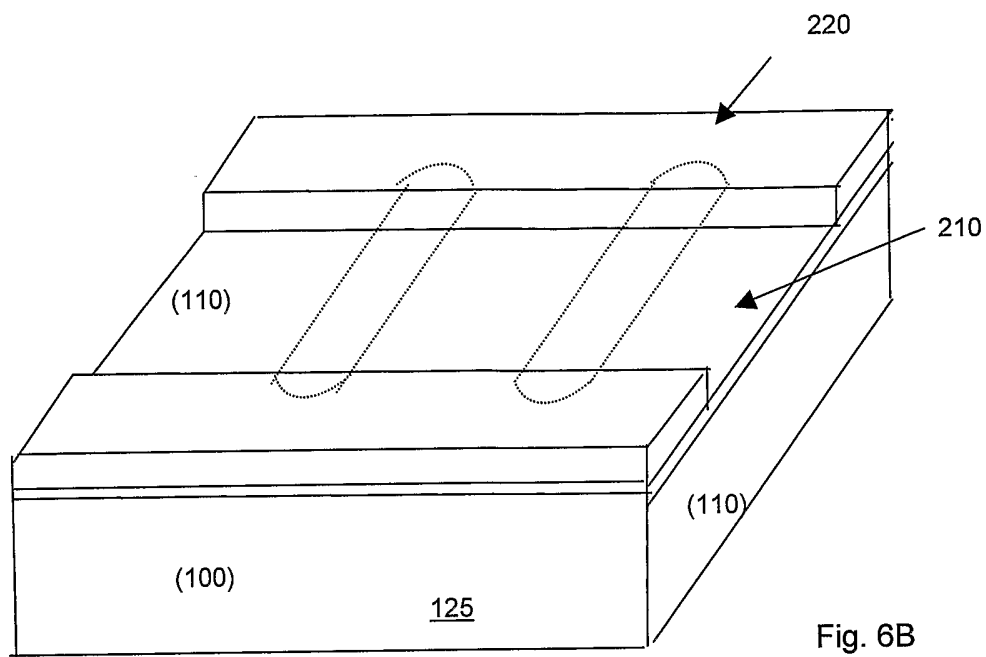


Fig. 6A



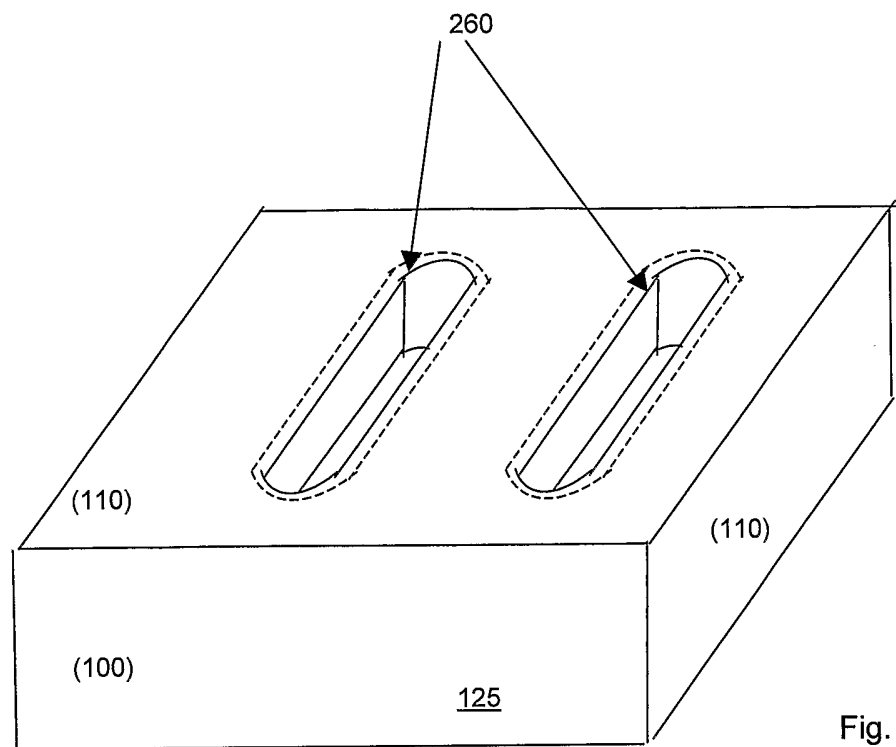


Fig. 7A

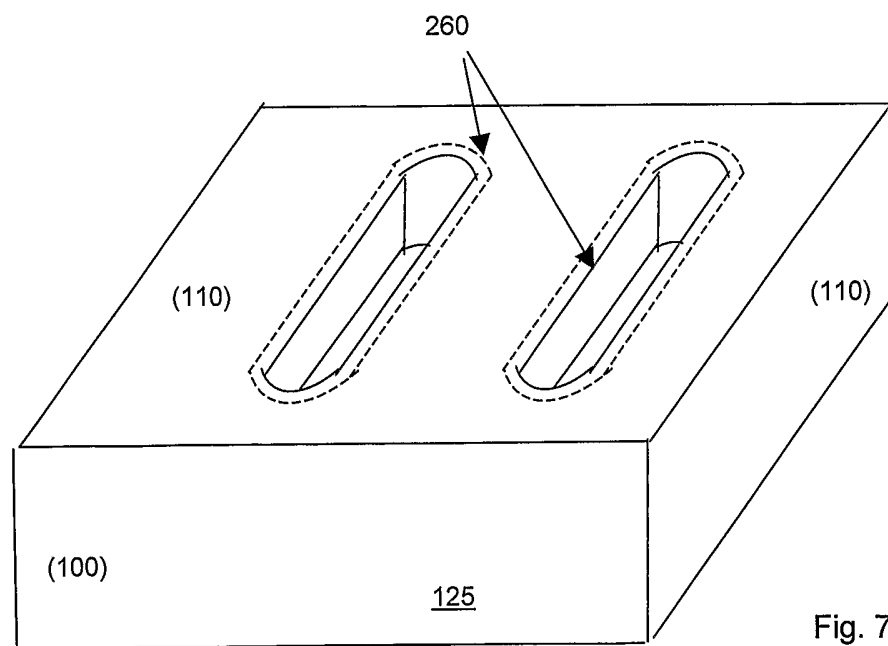


Fig. 7B

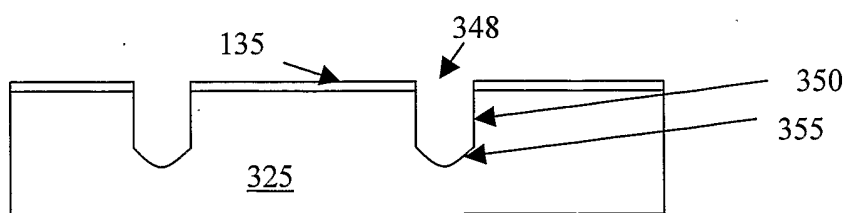


Fig. 8A

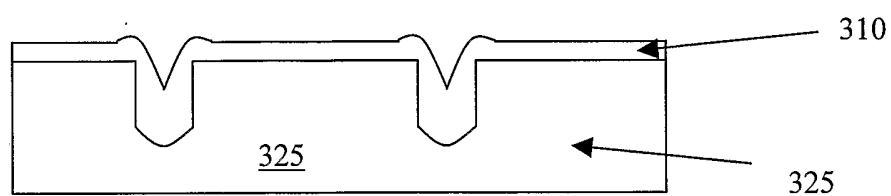


Fig. 8B

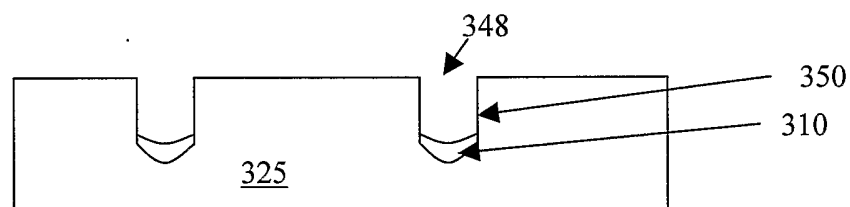


Fig. 8C

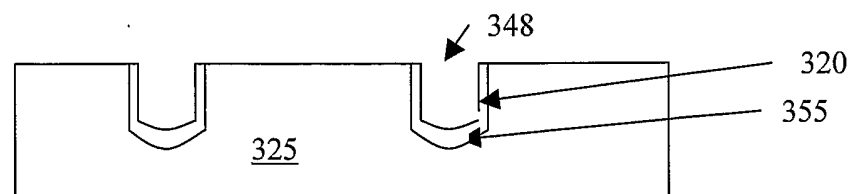


Fig. 8D

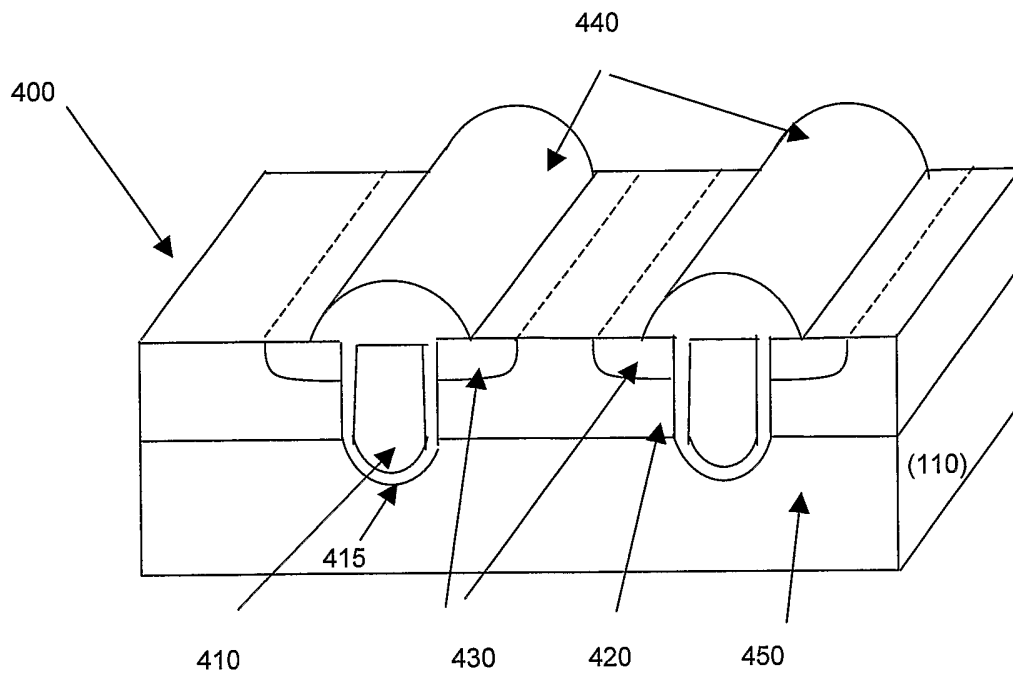


Fig. 9

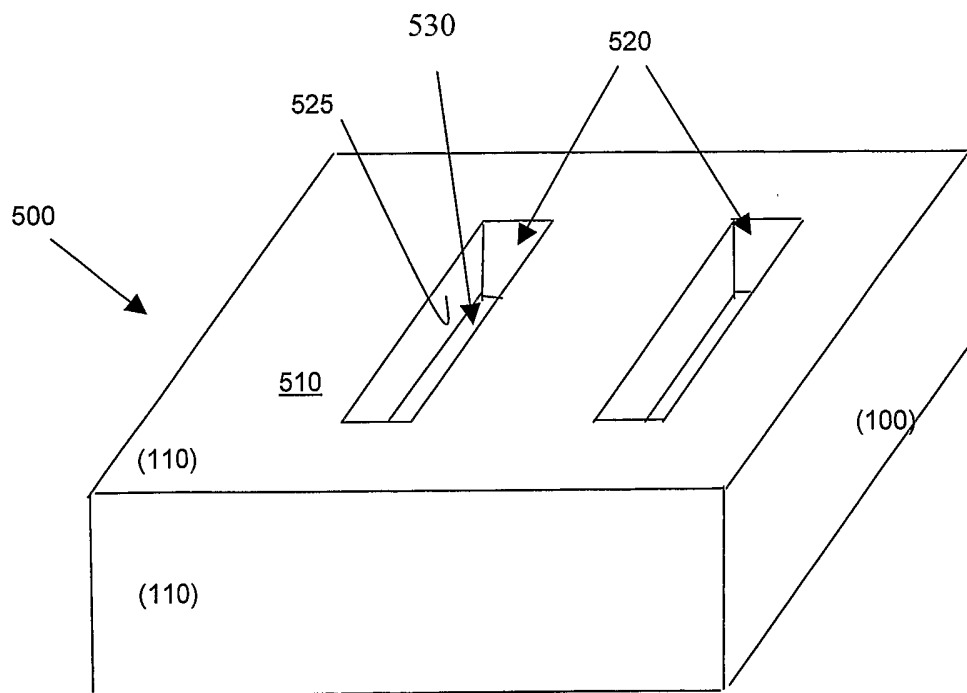


Fig. 10

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US05/42743

A. CLASSIFICATION OF SUBJECT MATTER

IPC: H01L 29/76(2006.01)

USPC: 257/329

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 257/329

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Continuation Sheet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/0036121 A1 (AOKI et al) 26 February 2004 (26.02.2004), Fig. 1; Fig. 9A; Fig. 9B.	1-42



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:		"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier application or patent published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search
28 February 2006 (28.02.2006)

Date of mailing of the international search report

Name and mailing address of the ISA/US
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Authorized officer
Jose Dees
Telephone No. 571-272-1604

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US05/42743

Continuation of B. FIELDS SEARCHED Item 3:
US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
Search Terms: gate with trench with (sidewall with "110" with (crystal or orientation or plane))