The present invention relates to a fast recovery cathode follower circuit for pulse operation and, more particularly, to a high-power cathode follower circuit adapted to operate on decreased power and incorporating apparatus to overcome the lag in fall time inherent in cathode followers under pulse conditions.

As is generally known, a conventional cathode follower comprises an electron discharge device having a plate connected to a source of B-+ potential, and a cathode connected through a series resistor to a source of B- potential. Quiescent conditions are established by the applied grid voltage and the potential drop across the cathode series resistor, the total current being dependent on the value of the series resistor during the quiescent condition. During operation the voltage and current in the output circuit follows the applied grid voltage whereby the electron discharge device employed must be capable of carrying the peak current through the cathode series resistor and the load during positive going pulse conditions.

Associated with the output circuit of the cathode follower is its own inherent distributed capacity to ground and the input capacity of the load. When the signal has a positive excursion, these capacitances charge through the electron discharge device, and when the signal has a negative excursion, these capacitances must discharge through the cathode series resistor until the quiescent state is reached. The cathode series resistor and shunt capacitances thus set up a definite time constant during intervals when the output circuit is returning to the quiescent operating condition. This time constant, designated RC, is of no consequence until it exceeds the fall time of the applied signal which is often the case during pulse operation. Usually, no control can be exercised, beyond certain limits, over the shunt capacitance, so a decrease in the resistance of the cathode series resistor is the usual resort. This leads to higher power dissipation in the electron discharge device and in the cathode series resistor. Also the direct current power supply capabilities have to be considered. Often during pulse operation, the cathode follower circuit will dissipate more power than the associated pulse generating circuitry. It is thus apparent that a conventional cathode follower circuit reproduces pulses very poorly under very fast fall conditions due to the RC time constant. Also, a conventional cathode follower has high power dissipation when an attempt is made to secure fast recovery by reducing the value of the cathode series resistance.

It is, therefore, an object of the present invention to provide an improved cathode follower circuit having a fast recovery time.

Another object of the invention is to provide a cathode follower circuit adapted to reproduce pulses under very fast rise and fall conditions.

Still another object of the present invention is to provide a cathode follower circuit capable of reproducing pulses under very fast rise and fall conditions that is adapted to operate on decreased power.

In accordance with the present invention, the cathode series resistor of the conventional cathode follower circuit is replaced with a second electron discharge device. This additional electron discharge device is biased to near cut-off at all times except during the recovery time of the output circuit. During operation, the applied pulse is differentiated and its phase reversed by means of a pulse transformer thereby to produce sharp negative pulses from the quiescent level concurrent with the rise of the applied pulses and sharp positive pulses from the quiescent level concurrent with the fall of the applied pulses. The pulse transformer thus employed may be located in the plate circuit of the cathode follower tube or, alternatively, in the plate circuit of a third electron discharge device. These sharp negative and positive pulses are applied to the control grid of the second electron discharge device in a manner to completely cut off the flow of current therethrough during the rise time of the pulse and to render the discharge device conductive during the fall time of the applied pulse. Thus, the discharge device provides a low impedance during the fall time of the applied pulse thereby to allow the shunt capacitance to discharge rapidly thereby enabling accurate reproduction of the pulse.

The above-mentioned and other features and objects of this invention and the manner of attaining them will become more apparent by reference to the following description taken in conjunction with the accompanying drawings, wherein:

Fig. 1 illustrates a schematic circuit diagram of the fast recovery cathode follower circuit of the present invention; and

Fig. 2 illustrates an alternative embodiment of the device of the present invention.

Referring now to Fig. 1 of the drawings, there is illustrated an embodiment of the device of the present invention which device comprises a cathode follower circuit including a tube 11, a control grid 12 and a plate 13, and a load impedance tube 14 including a cathode 15, a control grid 16 and a plate 17 which is connected to the cathode 11 of tube 10. In addition, the plate 13 of tube 10 is connected through the primary winding of a pulse transformer 18 to a source of B- potential which provides a potential, for example, of the order of +300 volts positive with respect to ground. The pulse transformer 18 is adapted for use with pulses of the order of 20 percent of the duration of the narrowest width of the pulses initially to be applied to the circuit of the present invention. Thus, if 0.5 microsecond pulses are to be applied to the circuit, the pulse transformer used will be designed for 0.1 microsecond pulses. One extremity of the secondary winding of the pulse transformer 18 is connected to a source of B- potential of the order of -300 volts with respect to ground and the remaining extremity extremity is connected to the control grid 16 of the tube 14 as well as being returned to the source of B- potential through a resistor 20. The polarity of the secondary winding of pulse transformer 18 is arranged in a manner such that a positive pulse provided by a pulse source 21 and applied through input terminals 22 to the control grid 12 of tube 10 to thereby produce a negative spike corresponding to the positive excursion or rise of the pulse and a positive spike corresponding to the negative excursion or fall of the pulse. These negative and positive spikes constitute a load impedance control signal which is applied to the control grid 16 of tube 14.

The cathode 11 of tube 10 in addition to being connected to the plate 17 of tube 14 is also connected to a load impedance 24, the remaining input terminal of which is returned to a terminal maintained at a substantially
fixed potential which may, for example, be ground or the source of B—potential. Cathode 15 of tube 14, on the other hand, is connected through a resistor 25 bypassed by a capacitor 26 to the source of B—potential.

The following types of tubes and values of the various parameters in the circuit have been found to be satisfactory for a device intended to translate 0.5 microsecond pulses to 20 microsecond pulses:

- Tube 10 (section A) — 5687 (dual triode).
- Tube 14 (section B) — 5667.
- Resistor 20 — 1500 ohms.
- Resistor 25 — 12,000 ohms.
- Capacitor 26 — 0.01 microfarad.

In the operation of the device of the present invention, one must consider a shunt capacitance 28 across the tube 14 to ground and a shunt capacitance 30 across the load impedance 24. Both capacitances 28 and 30 are represented by dashed lines in that they are an inherent part of the circuit and, as such, are distributed capacitances. 

During quiescent conditions a direct current flows from the source of B—potential through the primary of the pulse transformer 18, the tube 10, the tube 14 and its associated biasing resistor 25 to the source of B—potential. The flow of current through resistor 25 is such that the potential of cathode 15 of tube 14 is positive with respect to the potential of control grid 16, whereby the current through tube 14 is near cut-off.

The embodiment of the device of the present invention is designed to handle positive pulses although devices adapted to handle either positive or negative pulses are considered to be within the scope of the teachings of the present application. Thus, in operation a pulse of waveform 32 provided by source 21 is applied through the input terminals 22 to the control grid 12 of the tube 10. The positive excursion or rise of the pulse of waveform 32 increases the current flow through the tube 10, which increase in current flow produces a negative spike 34 across the secondary of the pulse transformer 18. This negative spike 34 is concurrent with the rise of the pulse of waveform 32 and is applied to the control grid 16 of the tube 14 to temporarily render it non-conductive. When non-conductive, the tube 14 represents an infinite impedance and, hence, forces all of the increase in current through the load impedance 24. In that the pulse transformer 18 is designed for 0.1 microsecond pulses, it differentiates the applied pulse whereby the negative excursion at the termination of the pulse of waveform 32 produces a positive spike 36. This positive spike 36, which occurs simultaneously with the trailing negative excursion of the pulse of waveform 32, appears at the control grid 16 of the tube 14 to render it conductive. The rendering of tube 14 conductive at the trailing edge of the positive pulse of waveform 32 provides a low resistance for the distributed capacitances 28 and 30 to discharge through, thereby to accurately reproduce the pulse of waveform 32 across the load impedance 24.

An alternate embodiment of the invention is shown in Fig. 2. In this embodiment the pulse transformer 18 is removed from the plate circuit of the tube 10 and inserted in the plate circuit of an additional tube 40 which tube includes a cathode 41, a control grid 42 and a plate 43. The plate 43 of the tube 40 is connected through the primary winding of the pulse transformer 18 to the source B—potential. The cathode 41 of tube 40 is returned to ground through a biasing resistor 44 and the control grid 42 is connected through the input terminals 22 to the pulse source 21. In the operation of the device in Fig. 2, the applied pulse is differentiated and its phase reversed by the pulse transformer 18 and the tube 40 to produce a control signal which is applied to the control grid 16 of the tube 14 in the same manner as before. The operation of the remainder of the circuit is the same as for the device of Fig. 1. The difference between the device of Fig. 2 and that of Fig. 1 is that the cathode follower tube 10 does not include the pulse transformer 18 in its plate circuit. Inasmuch as the pulse transformer 18 is in the plate circuit of tube 10 in the device of Fig. 1 and in that the impedance of the pulse transformer 18 is substantially less than the plate resistance of tube 10, the removal of the pulse transformer 18 from the plate circuit of tube 10 does not have any substantial effect on the operation of the device or its output impedance.

What is claimed is:

A pulse translation circuit for supplying an electrical load, comprising: a first electron discharge device having a direct current energized plate circuit, a cathode circuit and a control electrode circuit, the latter for receiving electrical input pulses; a control circuit including a second electron discharge device, connected in series in the cathode circuit of said first electron discharge device and adapted to be connected in parallel with said electrical load; and a pulse transformer having a primary winding connected in series in the plate circuit of said first electron discharge device and having a secondary winding connected to the grid-cathode circuit of said second electron discharge device and controlling said second electron discharge device in a sense to increase conduction of said second electron discharge device during the fall time of said electrical input pulse.

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