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(54) Title: VECTOR SIGNALING CODES WITH INCREASED SIGNAL TO NOISE CHARACTERISTICS

(57) Abstract: Vector signaling codes are synergistically combined with multi-level signaling, the increased alphabet size provided by the multi-level signaling enabling a larger codeword space for a given number of symbols, at the cost of reduced receiver detection margin for each of the multiple signal levels. Vector signaling code construction methods are disclosed in which code construction and selection of multi-level signal levels are coordinated with the design of an associated receive comparator network, wherein modified signal levels encoded and emitted by the transmitter result in increased detection margin at the receive comparators.

VECTOR SIGNALING CODES WITH INCREASED SIGNAL TO NOISE CHARACTERISTICS

[0001] This application claims priority to U.S. Provisional Patent Application 62/023,163, filed July 10, 2014, naming Amin ShokroUahi, entitled "Vector Signaling Codes with Increased Signal to Noise Characteristics" which is herein incorporated by reference in its entirety for all purposes.

REFERENCES

[0002] The following references are herein incorporated by reference in their entirety for all purposes:

[0003] U.S. Patent Publication No. 201 1/0268225 of U.S. Patent Application No. 12/784,414, filed May 20, 2010, naming Harm Cronie and Amin ShokroUahi, entitled "Orthogonal Differential Vector Signaling" (hereinafter "Cronie I");

[0004] U.S. Patent Publication No. 201 1/0302478 of U.S. Patent Application No. 13/154,009, filed June 6, 201 1, naming Harm Cronie and Amin ShokroUahi, entitled "Error Control Coding for Orthogonal Differential Vector Signaling" (hereinafter "Cronie II");

[0005] U.S. Patent Application No. 13/030,027, filed February 17, 201 1, naming Harm Cronie, Amin ShokroUahi and Armin Tajalli, entitled "Methods and Systems for Noise Resilient, Pin-Efficient and Low Power Communications with Sparse Signaling Codes" (hereinafter "Cronie III");

[0006] U.S. Patent Publication No. 201 1/0299555 of U.S. Patent Application No. 13/154,009, filed June 6, 201 1, naming Harm Cronie and Amin ShokroUahi, entitled "Error Control Coding for Orthogonal Differential Vector Signaling" (hereinafter "Cronie IV");

[0007] U.S. Provisional Patent Application No. 61/763,403, filed February 11, 2013, naming John Fox, Brian Holden, Ali Hormati, Peter Hunt, John D Keay, Amin ShokroUahi, Anant Singh, Andrew Kevin John Stewart, Giuseppe Surace, and Roger Ulrich, entitled "Methods and Systems for High Bandwidth Chip-to-Chip Communications Interface" (hereinafter called "Fox I");

[0008] U.S. Provisional Patent Application No. 61/773,709, filed March 6, 2013, naming John Fox, Brian Holden, Peter Hunt, John D Keay, Amin ShokroUahi, Andrew Kevin John Stewart, Giuseppe Surace, and Roger Ulrich, entitled "Methods and Systems for High Bandwidth Chip-to-Chip Communications Interface" (hereinafter called "Fox II");

[0009] U.S. Provisional Patent Application No. 61/812,667, filed April 16, 2013, naming John Fox, Brian Holden, Ali Hormati, Peter Hunt, John D Keay, Amin ShokroUahi, Anant Singh, Andrew Kevin John Stewart, and Giuseppe Surace, entitled "Methods and Systems for High Bandwidth Communications Interface" (hereinafter called "Fox III");

[0010] U.S. Patent Application No. 13/842,740, filed March 15, 2013, naming Brian Holden, Amin ShokroUahi, and Anant Singh, entitled "Methods and Systems for Skew Tolerance and Advanced Detectors for Vector Signaling Codes for Chip-to-Chip Communication" (hereinafter called "Holden I");

[0011] U.S. Patent Application No. 13/895,206, filed May 15, 2013, naming Roger Ulrich and Peter Hunt, entitled "Circuits for Efficient Detection of Vector Signaling Codes for Chip-to-Chip Communications using Sums of Differences" (hereinafter called "Ulrich I").

[0012] U.S. Patent Application No. 14/3 15,306, filed June 25, 2014, naming Roger Ulrich, entitled "Multilevel Driver for High Speed Chip-to-Chip Communications" (hereinafter called "Ulrich II").

[0013] U.S. Provisional Patent Application No. 61/934,804, filed February 2, 2014, naming Ali Hormati and Amin Shokrollahi, entitled "Method for Code Evaluation using ISI Ratio" (hereinafter called "Hormati I").

[0014] U.S. Provisional Patent Application No. 61/992,71 1, filed May 13, 2014, naming Amin Shokrollahi, entitled "Vector Signaling Code with Improved Noise Margin" (hereinafter called "Shokrollahi I").

TECHNICAL FIELD

[0015] Embodiments discussed herein relate to communications in general and in particular to the transmission of signals capable of conveying information and detection of those signals in chip-to-chip communication.

BACKGROUND

[0016] In communication systems, a goal is to transport information from one physical location to another. It is typically desirable that the transport of this information is reliable, is fast and consumes a minimal amount of resources. One common information transfer medium is the serial communications link, which may be based on a single wire circuit relative to ground or other common reference, or multiple such circuits relative to ground or other common reference. A common example uses singled-ended signaling ("SES"). SES operates by sending a signal on one wire, and measuring the signal relative to a fixed reference at the receiver. A serial communication link may also be based on multiple circuits used in relation to each other. A common example of the latter uses differential signaling ("DS"). Differential signaling operates by sending a signal on one wire and the opposite of that signal on a matching wire. The signal information is represented by the difference between the wires, rather than their absolute values relative to ground or other fixed reference.

[0017] There are a number of signaling methods that maintain the desirable properties of DS while increasing pin efficiency over DS. Vector signaling is a method of signaling.

With vector signaling, a plurality of signals on a plurality of wires is considered collectively although each of the plurality of signals might be independent. Each of the collective signals is referred to as a component and the number of plurality of wires is referred to as the "dimension" of the vector. In some embodiments, the signal on one wire is entirely dependent on the signal on another wire, as is the case with DS pairs, so in some cases the dimension of the vector might refer to the number of degrees of freedom of signals on the plurality of wires instead of exactly the number of wires in the plurality of wires.

[0018] With binary vector signaling, each component or "symbol" of the vector takes on one of two possible values. With non-binary vector signaling, each symbol has a value that is a selection from a set of more than two possible values. The set of values that a symbol of the vector may take on is called the "alphabet" of the vector signaling code. A vector signaling code, as described herein, is a collection C of vectors of the same length N, called codewords. Any suitable subset of a vector signaling code denotes a "subcode" of that code. Such a subcode may itself be a vector signaling code.

[0019] In operation, the coordinates of the codewords are bounded, and we choose to represent them by real numbers between -1 and 1. The ratio between the binary logarithm of the size of C and the length N is called the pin-efficiency of the vector signaling code.

[0020] A vector signaling code is called "balanced" if for all its codewords the sum of the coordinates is always zero. Balanced vector signaling codes have several important properties. For example, as is well-known to those of skill in the art, balanced codewords lead to lower electromagnetic interference (EMI) noise than non-balanced ones. Also, if common mode resistant communication is required, it is advisable to use balanced codewords, since otherwise power is spent on generating a common mode component that is cancelled at the receiver.

[0021] Additional examples of vector signaling methods are described in Cronie I, Cronie II, Cronie III, Cronie IV, Fox I, Fox II, Fox III, Holden I, Shokrollahi I, and Hormati I.

BRIEF DESCRIPTION

[0022] Vector signaling codes may be synergistically combined with multi-level signaling, the increased alphabet size provided by the multi-level signaling enabling a larger codeword space for a given number of symbols, which in turn permits introduction of additional constraints on construction of the vector signaling code to provide robust transmission results with acceptable throughput. However, introduction of additional signal levels within a fixed transmission amplitude envelope is known to reduce the available signal detection margin for each received signal level, potentially leading to degraded reception.

[0023] Vector signaling code construction methods have been disclosed in which code construction is coordinated with design of an associated receive comparator network, such that the system performance of the combination is optimized. Such methods may be extended to incorporate modified multi-level signaling values which provide consistent signal detection margin across the set of receive comparators.

BRIEF DESCRIPTION OF FIGURES

[0024] FIG. 1 shows one embodiment of a multi-input comparator producing a result from the weighted sum of multiple input values.

[0025] FIG. 2 illustrates receive eye openings for binary and ternary signals.

[0026] FIG. 3 is a block diagram in accordance with one embodiment.

[0027] FIG. 4 illustrates two embodiments of a circuit accepting six inputs w_0- w_5 which are combined in proportions [1/3 1/3 1/3 -1/3 -1/3 -1/3] respectively, producing differential results outp and outm.

[0028] FIG. 5 shows alternative embodiments of the circuits of FIG. 4.

[0029] FIG. 6 illustrates two embodiments of a circuit accepting three inputs $w_0,\ldots,w_2$ and not using the three inputs $w_3,\ldots,w_5$ in combinations representing the proportions [1/2 1/2 -1 0 0 0] respectively, producing differential results outp and outm.

[0030] FIG. 7 shows alternative embodiments of the circuits of FIG. 6.

[0031] FIG. 8 illustrates two embodiments accepting two inputs w_0, wi and not using the four inputs w_4,w_5 in combinations representing the proportions [1 -1 0 0 0 0] respectively, producing differential results outp and outm.

[0032] FIG. 9 shows one driver embodiment producing the optimized signal levels for a first example code ±(l,-l/5,-4/5),±(-l/5, 1,-4/5).

[0033] FIG. 10 shows one driver embodiment generating the signal levels of the code shown in Table 1.

[0034] FIG. 11 shows one driver embodiment generating the signal levels of the 5b6w_7_5_l code.

[0035] FIG. 12 shows one driver embodiment generating the signal levels of the 5b6w_10_5 code.

[0036] FIG. 13 shows one driver embodiment generating the signal levels of the 8b9w_8_8 code.

[0037] FIG. 14 shows a process in accordance with at least one embodiment.

[0038] FIG. 15 shows a process in accordance with at least one embodiment.

DETAILED DESCRIPTION

[0039] The concept of orthogonal vector signaling is described in [Croniel]. As presented there, an orthogonal differential vector signaling code (or ODVS code) may be obtained via the multiplication

(0,¾, ...,¾) * M/ o [Eqn. 1]

wherein M is an orthogonal n x n-matrix in which the sum of the columns is zero except at the first position, $x_2,\ldots,x_n$ belong to an alphabet S describing the original modulation of these symbols, and a is a normalization constant which ensures that all the coordinates of the resulting vector are between -1 and +1. For example, in case of binary modulation, the alphabet S may be chosen to be $\{-1,+1\}$. In case of ternary modulation, the alphabet S may be chosen as $\{-1,0,1\}$, in case of quaternary modulation, the alphabet S may be chosen as $\{-3,-1,1,3\}$, and in case of quintary modulation S may be chosen as $\{-2,-1,0,1,2\}$. In general, however, it is not necessary that all the ¾ are modulated by the same alphabet S. The vector $(x_2, \ldots, x_n)$ is often denoted by x henceforth and is called the message.

[0040] In at least one embodiment, the multiplication of Eqn. 1 represents a weighted sum of sub-channel code vectors, each sub-channel code vector weighted based on a corresponding antipodal weight of a set of antipodal weights, wherein the sub-channel code vectors are mutually orthogonal, and wherein the sub-channel code vectors represent rows of a scaled-orthogonal matrix, M.

[0041] In operation, the matrix M does not need to be orthogonal. It suffices that all its rows (also referred to herein as sub-channel code vectors) are pairwise orthogonal (even if the rows are not of Euclidean norm 1). In the following, we call such matrices *s-orthogonal* (scaled orthogonal).

[0042] Detection of the transmitted signals can be accomplished with the matrix M in the following manner. Each row of M is scaled in such a way as to ensure that the sum of the positive entries in that row is equal to 1. Then the entries of each row of this new matrix D (except for the first) are used as coefficients of a multi-input comparator as defined in [Holden I]. For example, if $n=6$, the values on the 6 wires (possibly after equalization) are denoted by a, b, c, d, e, f, and the row is [1, 1/2, -1, 1/2, -1, 0], then the multi-input comparator would calculate the value

$$\frac{a}{2}+\frac{b+d}{4}-\left(\frac{c+e}{2}\right) \qquad \text{[Eqn. 2]}$$

and would slice the result to reconstruct the original value in the alphabet *S*. The set of multi-input comparators defined by matrix *D* are said to detect the ODVS code defined by *M* if the collection of comparator outputs unambiguously identifies any message x encoded by *M* as described above.

Multi-input comparators

[0043] Following the definition of [Holden I], a multi-input comparator with coefficients $a_0, a_1, \ldots, a_{m-1}$ is a circuit that accepts as its input a vector $(x_0, x_1, \ldots, x_{m-1})$ and outputs

$$\text{sign}(a_0 * x_0 + \ldots + a_{m-i} * x_{m-i}), \qquad \text{[Eqn. 3]}$$

with the definition of the sign-function being sign(x) =+1 if x > 0, sign(x) = -1 if x < 0, and sign(x) is undefined if x = 0. As such, a simple comparator may be seen to be a two input multi-input comparator with coefficients 1 and -1, hence may be considered to be a special case of a multi-input comparator.

[0044] The weighting coefficients $a_0, a_1, \ldots, a_{m-1}$ of a multi-input comparator are rational numbers, and one example implementation is shown as FIG. 1, where input weights of 2, 4, -1, -2, -3 are associated with the input values x0 through x4 respectively, each input weight in this example providing a fractional proportion of the total number of transistors (and thus, a comparable proportion of the output result) on that differential input leg, in this case six on each side. In this example, each of the twelve input transistors 101 are identical, representing an extended differential input stage sharing current source 102, followed by differential comparator stage 105. As all transistors 101 are identical, the contributions of inputs x0 and x1 to positive summing node 103, and of inputs x2, x3, and x4 to negative summing node 104 are weighted in proportion to the number of input transistors controlled by each such input, relative to the total number of transistors 101 associated with node 103 and node 104 respectively. Resistors 106 are shown as passive pull-ups on summing nodes 103 and 104; in some embodiments their function will be incorporated in that of differential comparator 105. Assuming sufficiently high gain in differential comparator 105 to obtain a digital result, its output

represents the sign() operation taken on the difference between positive summing node 103 and negative summing node 104.

[0045] Thus, the circuit of FIG. 1 implements Eqn. 3, where inputs with positive coefficients are attached to transistors 101 associated with positive summing node 103, and inputs with negative coefficients are attached to transistors 101 associated with negative summing node 104, the coefficient values being represented by the ratio of the number of identical input transistors 101 used for each input to the total number of identical input transistors 101 associated with that input node 103 or 104.

[0046] As present embodiments primarily addresses higher order modulation, the descriptive convention herein will be to assume that each example of a multi-level comparator comprises multiple appropriately-weighted inputs and summation and difference computations, the comparator output value which (also referenced to herein as the combined input value) is presented as a linear signal to a binary or higher-order slicer or digital comparator (herein, simply called the comparator) detecting the desired multi-valued signal result.

[0047] Although scaling, summation, difference, and comparator elements of multi-input comparators may be described discretely for purposes of explanation, practical embodiments may utilize circuit functions combining aspects of multiple such elements, as further described in [Holden I] and [Ulrich I].

Eye opening

[0048] Conventionally, the receiver detection window for receiver slicing operations is described as the "eye opening" of graphs such as illustrated in FIG. 2, showing a time-superimposed representation of all possible received signal patterns (and thus, every possible inter-symbol interference or ISI condition) at the comparator or slicer input. For binary modulation, horizontal "eye" opening 210 represents the available time interval during which a stable result may be sampled, and vertical eye opening 220 represents the detectable signal over noise available to the slicer. For ternary modulated signals, there are two eye openings 231 and 232, corresponding to the signal margins for detection of the three possible signal levels. These smaller vertical openings 231 and 232 versus 220

correspond to higher susceptibility of the signal to communications channel and internal receiver noise with ternary versus binary modulation. Generalizing, the larger the size n, the larger the value of the normalization constant a in Eqn. 1 must be, leading to smaller incremental differences between output levels, and therefore to a smaller measurement window (that is, a smaller vertical "eye") at the receiver's comparator or slicer.

[0049] On the other hand, larger value of n typically lead to a higher pin-efficiency of the signaling scheme, wherein pin-efficiency is defined as the ratio of the transmitted bits on the n-wire interface within a clock cycle, and the number n of wires. For orthogonal differential vector signaling with binary modulation of the input values the pin-efficiency is $(n-l)/n$, whereas using quaternary modulation of the input values leads to a pin-efficiency of $(2n - 2)1n$. In addition to higher pin-efficiency, orthogonal differential vector signaling has the property that the ISI-ratio as defined in [Hormati I] of the resulting signaling scheme is the same as the ISI-ratio of uncoded signals from the alphabet S. Hence, when binary modulation of the input values is used, the resulting ISI-ratio is the smallest possible value 1, representing the best possible detection capability. Using values of n that are larger than 2 is thus preferable, as this allows to achieve a higher throughput on the communication wires. What is therefore needed is a method to optimize the vertical opening of the resulting eye diagrams in order to achieve the best possible tolerance against thermal and mismatch noise with the resulting reduced signal levels.

[0050] As will be apparent to one familiar with the art, the output result from each of the combined input value slicers or digital comparators is dependent on two signal levels; the reference or baseline level for the comparison, and the variable signal value (i.e. the combined signal level.) For descriptive purposes, the absolute value of the difference between these two levels is herein called the "detection margin" for that comparator. The detection margin can be measured, as may be done as the vertical component of a signal quality metric such as a receive eye diagram, or may be calculated or computed as part of a simulation. Larger margins are associated with more reliable results, especially if the variable input signal is accompanied by noise. Similar terms of art include "comparator overdrive" and "comparator input margin".

Increasing ODVS eye opening

[0051] The optimization method to increase the vertical opening of the eye diagrams corresponding to the various comparators of an orthogonal differential vector signaling code using an s-orthogonal matrix M starts by assuming that the entry j of the input vector comprises antipodal weights having values $-a_j$ and a_j, wherein a_j is positive. We define the "initial code set" to be the set of antipodal weights represented by a vector

$$(0, \pm a_2, \pm a_3, \ldots, \pm a_n) \qquad \text{[Eqn. 4]}$$

[0052] It should be noted that although the values in Eqn. 4 illustrate binary modulation for descriptive convenience, the same procedure described here is also applicable to optimization of vertical eye opening for higher-order modulation, such as PAM-X modulation of the input vectors.

[0053] The code obtained from the input set is

$$(0, \pm a_2, \pm a_3, \ldots, \pm a_n) \ * \ M/\mu \qquad \text{[Eqn. 5]}$$

where

$$\mu = \max_{2 \le i \le n} \sum_{j=1}^{n} |M_{ij}| a_i \qquad \text{[Eqn. 6]}$$

[0054] In other words, μ is the codeword symbol normalization constant used to ensure that the coordinates of the codewords are between -1 and +1.

[0055] The detection matrix corresponding to the vector signaling code is the matrix comprising rows 2, 3, .., n, of M wherein each sub-channel code vector is chi-normalized so that the sum of the positive entries in the row is 1. Each such sub-channel code vector corresponds to a multi-input sub-channel comparator as defined in [Holden I], and the fact that the sum of the positive entries is equal to 1 means that the sub-channel comparator (also referred to herein as a "comparator" or "multi-input comparator") does not introduce additional gain. For a real number a we define chi(a) to be equal to a if a is positive, and equal to 0 otherwise. Then the chi-normalization constant for row i of M is equal to

$\sum_{j=1}^{n}$ **Chi**(My). [Eqn. 7]

[0056] We denote by D the detection matrix corresponding to M. If L denotes the matrix comprising the rows 2, 3, …, n of M, then

$$\boldsymbol{D} = \text{diag}(1/\ \sum_{j=1}^{n} \text{chi}(M_{2j}), \ldots, 1/\sum_{j=1}^{n} \text{chi}(M_{nj}))\ *\ \boldsymbol{L} \qquad \text{[Eqn. 8]}$$

wherein diag(. ..) denotes the diagonal matrix with diagonal entries given by the vector in the argument. As can be easily verified by anyone of moderate skill in the art, application of the multi-input sub-channel comparators leads to the values

$$\pm\frac{a_2 s_2}{\mu\sum_{j=1}^{n}\text{chi}(M_{2j})}, \pm\frac{a_3 s_3}{\mu\sum_{j=1}^{n}\text{chi}(M_{3j})}, \ldots, \pm\frac{a_n s_n}{\mu\sum_{j=1}^{n}\text{chi}(M_{nj})}, \qquad \text{[Eqn. 9]}$$

wherein s_i is the squared Euclidean norm of the ż-th row of M. The goal is to maximize the minimum of the absolute values of the above expressions.

[0057] To check whether this maximum is greater than or equal to a given vertical opening threshold δ, the following Basic Linear Program (BLP) needs to be solved:

Maximize

$a_2 + \ldots + \boldsymbol{a_n}$ [Eqn. 10]

Subject to:

$$\text{For all } 1 \le j \le n, 2 \le i \le n\text{: } a_i s_i \ \ge\ \delta * \sum_{l=2}^{n} |M_{lj}|\, a_l * \sum_{k=1}^{n} \text{chi}(M_{ik})$$

[Eqn. 11]

And

For all $2 \le \boldsymbol{I} \le \boldsymbol{n}\boldsymbol{:}\ \boldsymbol{a}_i \ge 0$ [Eqn. 12]

[0058] If this BLP is feasible, then the maximum vertical opening threshold is at least δ, and if not, it is definitely strictly smaller than δ. The optimal value of the vertical

opening can then be found using a binary search on δ. At each step of the binary search the BLP needs to be solved for the particular value of δ relevant in that step.

Examples

[0059] As a first example embodiment, we start with the case *n=3.* In this case the only possible choice for the scaled-orthogonal matrix *M* (up to a permutation of rows/columns and scaling of rows) is

$$M = \begin{pmatrix} 1 & 1 & 1 \\ 1 & -1 & 0 \\ 1 & 1 & -2 \end{pmatrix} \qquad \text{[Eqn. 13]}$$

and the corresponding detection matrix is

$$D = \begin{pmatrix} 1 & -1 & 0 \\ \frac{1}{2} & \frac{1}{2} & -1 \end{pmatrix} \qquad \text{[Eqn. 14]}$$

[0060] Using standard binary modulation of the initial code set, the resulting codewords would equal ±(1,0,-1), ±(0,1,-1). Applying the detection matrix of Eqn. 14 at the receiver, the first receive sub-channel comparator will generate a comparator output value of ± 1 while the second receive sub-channel comparator will generate a comparator output value of ±3/2. As the lesser of the two values limits the overall signal to noise limit, the reduction of vertical eye opening compared to differential signaling is therefore 20*logio(2/l) = ~6 dB. Applying the procedure above, the optimal initial code set (i.e. the optimal set of antipodal weights) is the set (0,±3/5,±2/5) which leads to the resulting codewords ±(1,-1/5,-4/5),±(-l/5, 1,-4/5). One embodiment of a driver generating these signal levels is shown as FIG. 9.

[0061] Applying the detection matrix of Eqn. 14 to this code, it may be observed that both sub-channel comparators will now generate comparator output values of ±6/5, providing an increase in vertical eye opening compared to the previous case of 20*logio (1.2/1) = ~ 1.58 dB. As an additional benefit, the termination power (total power required for transmission) using these modified signal levels is less than that of the previous ternary code.

[0062] In a second example embodiment, *n=5* and the matrix *M* is

$$M = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 \\ 1 & 1 & -1 & -1 & 0 \\ 1 & 1 & 1 & 1 & -4 \end{pmatrix} \qquad \text{[Eqn. 15]}$$

with a corresponding detection matrix of

$$\begin{pmatrix} 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 \\ 1/2 & 1/2 & -1/2 & -1/2 & 0 \\ 1/4 & 1/4 & 1/4 & 1/4 & -1 \end{pmatrix}. \qquad \text{[Eqn. 16]}$$

[0063] Using standard binary modulation of the initial code set, the resulting code has an alphabet of size 6 comprising the elements 1, ¾, ¼, -¼, -¾, -1. Applying the detection matrix of Eqn. 16, it may be seen that the first three comparators generate comparator output values of ±1/2, whereas the fourth comparator generates comparator output values of ±5/4. The loss in vertical eye opening compared to differential signaling is therefore 20* logio(2/0.5) = -12 dB.

[0064] Applying the procedure above, the optimal initial code set is calculated to be

(0, ±5/12, ±5/12, ±5/12, ±1/6) and the corresponding code is shown in Table 1. One embodiment of a driver generating these signal levels is shown as FIG. 10.

± [1, 1/6, 1/6, -2/3, -2/3]	± [1/6, -2/3, 1, 1/6, -2/3]
± [1/6, 1, 1/6, -2/3, -2/3]	± [-2/3, 1/6, 1, 1/6, -2/3]
± [1, 1/6, -2/3, 1/6, -2/3]	± [1/6, -2/3, 1/6, 1, -2/3]
± [1/6, 1, -2/3, 1/6, -2/3]	± [-2/3, 1/6, 1/6, 1, -2/3]

Table 1

[0065] As may be seen, when using this code with the detection matrix of Eqn. 16 all four comparators generate comparator output values of ±5/6. The increase in vertical eye

opening compared to the previous code is 20*logio(5/3) = ~ 4.43 dB. As the termination power of this code is a factor of 10/9 worse than the previous code, one may wish to normalize these results to the same termination power as the original code, in which case the new code still has a vertical eye opening that is 1.581 dB better than the vertical eye opening of the original code.

[0066] In a third example embodiment, $n=6$ and the matrix M is

$$M = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 \\ 1 & 1 & -1 & -1 & 0 & 0 \\ 1 & 1 & 1 & 1 & -2 & -2 \end{pmatrix} \qquad \text{[Eqn. 17]}$$

with a corresponding detection matrix of

$$\begin{pmatrix} 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 \\ 1/2 & 1/2 & -1/2 & -1/2 & 0 & 0 \\ 1/4 & 1/4 & 1/4 & 1/4 & -1/2 & -1/2 \end{pmatrix}. \qquad \text{[Eqn. 18]}$$

[0067] Using standard binary modulation of the initial code set the result, herein called the 5b6w_4_5_l code, has an alphabet of size 4 comprising the elements 1, 1/3, -1/3, -1 and its codewords are shown in Table 2.

± [1, 1/3, 1/3, -1/3, -1/3, -1]	± [1/3, -1/3, 1, 1/3, -1/3, -1]
± [1/3, 1, 1/3, -1/3, -1/3, -1]	± [-1/3, 1/3, 1, 1/3, -1/3, -1]
± [1, 1/3, -1/3, 1/3, -1/3, -1]	± [1/3, -1/3, 1/3, 1, -1/3, -1]
± [1/3, 1, -1/3, 1/3, -1/3, -1]	± [-1/3, 1/3, 1/3, 1, -1/3, -1]
± [1, 1/3, 1/3, -1/3, -1, -1/3]	± [1/3, -1/3, 1, 1/3, -1, -1/3]
± [1/3, 1, 1/3, -1/3, -1, -1/3]	± [-1/3, 1/3, 1, 1/3, -1, -1/3]
± [1, 1/3, -1/3, 1/3, -1, -1/3]	± [1/3, -1/3, 1/3, 1, -1, -1/3]

± [1/3, 1, -1/3, 1/3, -1, -1/3]	± [-1/3, 1/3, 1/3, 1, -1, -1/3]

Table 2

[0068] When this code is detected using the detection matrix of Eqn. 18, the first four comparators generate comparator output values of ±2/3, whereas the fifth comparator generates a comparator output value of ±1. The loss in vertical eye opening compared to differential signaling is therefore 20* logio(3) = -9.5 dB. Applying the procedure above, the optimal initial code set is calculated to be (0, ±3/8, ±3/8, ±1/2, ±3/8, ±1/4) and the corresponding code has an alphabet of size 7 given by 1, ½, ¼, 0, -¼, -½, -1. The codewords of this new code herein called 5b6w_7_5_l code are shown in Table 3. One embodiment of a driver generating these signal levels is shown as FIG. 11.

± [1, 1/4, 1/4, -1/2, 0, -1]	± [1/4, -1/2, 1, 1/4, 0, -1]
± [1/4, 1, 1/4, -1/2, 0, -1]	± [-1/2, 1/4, 1, 1/4, 0, -1]
± [1, 1/4, -1/2, 1/4, 0, -1]	± [1/4, -1/2, 1/4, 1, 0, -1]
± [1/4, 1, -1/2, 1/4, 0, -1]	± [-1/2, 1/4, 1/4, 1, 0, -1]
± [1, 1/4, 1/4, -1/2, -1, 0]	± [1/4, -1/2, 1, 1/4, -1, 0]
± [1/4, 1, 1/4, -1/2, -1, 0]	± [-1/2, 1/4, 1, 1/4, -1, 0]
± [1, 1/4, -1/2, 1/4, -1, 0]	± [1/4, -1/2, 1/4, 1, -1, 0]
± [1/4, 1, -1/2, 1/4, -1, 0]	± [-1/2, 1/4, 1/4, 1, -1, 0]

Table 3

[0069] Using this new code with the detection matrix of Eqn. 18, all comparators except for the third generate comparator output values of ±3/4 and the third comparator generates a comparator output value of ±1. The increase in vertical eye opening compared to the previous code is 20*logl0((3/4)/(2/3)) = ~ 1 dB. The termination power of the 5b6w_7_5_l code is about 97% of the termination power of 5b6w_4_5_l code, so even at a smaller termination power, 5b6w_7_5_l leads to a bigger vertical eye opening.

[0070] In a fourth example embodiment, $n=6$ and the matrix M is

$$M = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 1 & 1 & -2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 1 & 1 & -2 \\ 1 & 1 & 1 & -1 & -1 & -1 \end{pmatrix} \qquad \text{[Eqn. 19]}$$

with a corresponding detection matrix of

$$\begin{pmatrix} 1 & -1 & 0 & 0 & 0 & 0 \\ 1/2 & 1/2 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 1/2 & 1/2 & -1 \\ 1/3 & 1/3 & 1/3 & -1/3 & -1/3 & -1/3 \end{pmatrix}. \qquad \text{[Eqn. 20]}$$

[0071] Using standard binary modulation of the initial code set, the resulting code has an alphabet of size 4 comprising the elements 1, 1/3, -1/3, -1 and is herein called the 5b6w_4_5_2 code, with its codewords shown in Table 4.

± [1, 1/3, -1/3, 1/3, -1/3, -1]	± [1, 1/3, -1/3, -1/3, -1, 1/3]
± [1/3, 1, -1/3, 1/3, -1/3, -1]	± [1/3, 1, -1/3, -1/3, -1, 1/3]
± [1/3, -1/3, 1, 1/3, -1/3, -1]	± [1/3, -1/3, 1, -1/3, -1, 1/3]
± [-1/3, 1/3, 1, 1/3, -1/3, -1]	± [-1/3, 1/3, 1, -1/3, -1, 1/3]
± [1, 1/3, -1/3, -1/3, 1/3, -1]	± [1, 1/3, -1/3, -1, -1/3, 1/3]
± [1/3, 1, -1/3, -1/3, 1/3, -1]	± [1/3, 1, -1/3, -1, -1/3, 1/3]
± [1/3, -1/3, 1, -1/3, 1/3, -1]	± [1/3, -1/3, 1, -1, -1/3, 1/3]
± [-1/3, 1/3, 1, -1/3, 1/3, -1]	± [-1/3, 1/3, 1, -1, -1/3, 1/3]

Table 4

[0072] With this code and the detection matrix of Eqn. 20, it may be observed that comparators 1, 3, and 5 generate comparator output values of ±2/3, whereas comparators 2 and 4 generate comparator output values of ±1. The loss in vertical eye opening compared to differential signaling is therefore 20* logio(3) = -9.5 dB. Applying the procedure above, the optimal initial code set is calculated to be (0, ±3/8, ±1/4, ±3/

8, ±1/4, ±3/8) with the corresponding code having an alphabet of size 10 given by (1, 7/8, 1/2, 1/4, 1/8, -1/8, -1/4, -1/2, -7/8, -1). The resulting codewords are shown in Table 5, with the new code herein called the 5b6w_10_5 code. One embodiment of a driver generating these signal levels is shown as FIG. 12.

± [1, 1/4, -1/8, 1/4, -1/2, -7/8]	± [1, 1/4, -1/8, -1/4, -1, 1/8]
± [1/4, 1, -1/8, 1/4, -1/2, -7/8]	± [1/4, 1, -1/8, -1/4, -1, 1/8]
± [1/2, -1/4, 7/8, 1/4, -1/2, -7/8]	± [1/2, -1/4, 7/8, -1/4, -1, 1/8]
± [-1/4, 1/2, 7/8, 1/4, -1/2, -7/8]	± [-1/4, 1/2, 7/8, -1/4, -1, 1/8]
± [1, 1/4, -1/8, -1/2, 1/4, -7/8]	± [1, 1/4, -1/8, -1, -1/4, 1/8]
± [1/4, 1, -1/8, -1/2, 1/4, -7/8]	± [1/4, 1, -1/8, -1, -1/4, 1/8]
± [1/2, -1/4, 7/8, -1/2, 1/4, -7/8]	± [1/2, -1/4, 7/8, -1, -1/4, 1/8]
± [-1/4, 1/2, 7/8, -1/2, 1/4, -7/8]	± [-1/4, 1/2, 7/8, -1, -1/4, 1/8]

Table 5

[0073] For this code all comparators generate comparator output values of ±3/4. The increase in vertical eye opening compared to 5b6w_4_5_2 is 20*logio((3/4)/(2/3)) = ~ 1 dB. The termination power of 5b6w_10_5 is about 88% of the termination power of 5b6w_4_5_2, so even at a smaller termination power, 5b6w_10_5 leads to a bigger vertical eye opening.

[0074] In a fifth example embodiment $n=9$, and the matrix M is

$$M = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 \\ 1 & 1 & -1 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & -1 & -1 & 0 \\ 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 & 0 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & -8 \end{pmatrix} \quad \text{[Eqn. 21]}$$

with a corresponding detection matrix of

$$\begin{pmatrix} 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 \\ 1/2 & 1/2 & -1/2 & -1/2 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1/2 & 1/2 & -1/2 & -1/2 & 0 \\ 1/4 & 1/4 & 1/4 & 1/4 & -1/4 & -1/4 & -1/4 & -1/4 & 0 \\ 1/8 & 1/8 & 1/8 & 1/8 & 1/8 & 1/8 & 1/8 & 1/8 & -1 \end{pmatrix}. \quad \text{[Eqn. 22]}$$

[0075] Using standard binary modulation of the initial code set, the resulting code has an alphabet of size 7 composed of the elements (1, 1/2, 1/4, 0, -1/4, -1/2, -1). For this code all the comparators except the generate comparator output values of ±1/4 and the last comparator generates a comparator output value of ±9/8.

[0076] Applying the procedure above, the optimal initial code set is calculated to be (0,±3/10,±3/10,±3/10,±3/10,±3/10,±3/10,±3/10,±l/10) and the corresponding code has an alphabet of size 8 given by (1, 4/5, 2/5, 1/5, -1/5, -2/5, -4/5, -1). This code is herein called 8b9w_8_8 code and its codewords are shown in Table 7. One embodiment of a driver generating these signal levels is shown as FIG. 13.

[0077] Using this code with the detection matrix of Eqn. 22 all but the last comparator generate comparator output values of ±3/5, and the last generates a comparator output value of ±9/10. The increase in vertical opening compared to the non-optimized code is 20*logio((3/5)/(l/4)) = ~ 7.6 dB. The termination power of 8b9w_8_8 is about 1.9 times the termination power of the non-optimized code. At equal termination power, 8b9w_8_8 has a vertical opening that is about 2 dB better than the opening of the non-optimized code.

±[1,2/5, 2/5, -1/5, 2/5, -1/5,-1/5, -4/5, -4/5]	±[2/5,-1/5, -1/5, -4/5, 1,2/5, 2/5, -1/5, -4/5]
±[2/5, 1, 2/5, -1/5, 2/5, -1/5,-1/5, -4/5, -4/5]	±[-1/5, 2/5, -1/5, -4/5, 1,2/5, 2/5, -1/5, -4/5]
±[1,2/5, -1/5, 2/5, 2/5, -1/5,-1/5, -4/5, -4/5]	±[2/5,-1/5, -4/5, -1/5, 1,2/5, 2/5, -1/5, -4/5]
±[2/5, 1, -1/5, 2/5, 2/5, -1/5,-1/5, -4/5, -4/5]	±[-1/5, 2/5, -4/5, -1/5, 1,2/5, 2/5, -1/5, -4/5]
±[1,2/5, 2/5, -1/5,-1/5, 2/5, -1/5, -4/5, -4/5]	±[2/5,-1/5, -1/5, -4/5,2/5, 1, 2/5, -1/5, -4/5]
±[2/5, 1, 2/5, -1/5,-1/5, 2/5, -1/5, -4/5, -4/5]	±[-1/5, 2/5, -1/5, -4/5, 2/5, 1, 2/5, -1/5, -4/5]
±[1,2/5, -1/5, 2/5, -1/5, 2/5,-1/5, -4/5, -4/5]	±[2/5,-1/5, -4/5, -1/5,2/5, 1, 2/5, -1/5, -4/5]
±[2/5, 1, -1/5, 2/5, -1/5, 2/5,-1/5, -4/5, -4/5]	±[-1/5, 2/5, -4/5, -1/5, 2/5, 1, 2/5, -1/5, -4/5]
±[1,2/5, 2/5, -1/5, 2/5, -1/5, -4/5, -1/5, -4/5]	±[2/5,-1/5, -1/5, -4/5, 1,2/5, -1/5, 2/5, -4/5]
±[2/5, 1, 2/5, -1/5, 2/5, -1/5, -4/5, -1/5, -4/5]	±[-1/5,2/5, -1/5, -4/5, 1,2/5, -1/5, 2/5, -4/5]
±[1,2/5, -1/5, 2/5, 2/5, -1/5, -4/5, -1/5, -4/5]	±[2/5,-1/5, -4/5, -1/5, 1,2/5, -1/5, 2/5, -4/5]
±[2/5, 1, -1/5, 2/5, 2/5, -1/5, -4/5, -1/5, -4/5]	±[-1/5,2/5, -4/5, -1/5, 1,2/5, -1/5, 2/5, -4/5]
±[1,2/5, 2/5, -1/5,-1/5, 2/5, -4/5, -1/5, -4/5]	±[2/5,-1/5, -1/5, -4/5,2/5, 1, -1/5, 2/5, -4/5]
±[2/5, 1, 2/5, -1/5,-1/5, 2/5, -4/5, -1/5, -4/5]	±[-1/5,2/5, -1/5, -4/5,2/5, 1, -1/5, 2/5, -4/5]
±[1,2/5, -1/5, 2/5, -1/5, 2/5, -4/5, -1/5, -4/5]	±[2/5,-1/5, -4/5, -1/5,2/5, 1, -1/5, 2/5, -4/5]
±[2/5, 1, -1/5, 2/5, -1/5, 2/5, -4/5, -1/5, -4/5]	±[-1/5,2/5, -4/5, -1/5,2/5, 1, -1/5, 2/5, -4/5]
±[2/5, -1/5, 1, 2/5, 2/5, -1/5,-1/5, -4/5, -4/5]	±[-1/5, -4/5, 2/5, -1/5, 1,2/5, 2/5, -1/5, -4/5]
±[-1/5, 2/5, 1, 2/5, 2/5, -1/5,-1/5, -4/5, -4/5]	±[-4/5,-1/5, 2/5, -1/5, 1,2/5, 2/5, -1/5, -4/5]
±[2/5, -1/5, 2/5, 1, 2/5, -1/5,-1/5, -4/5, -4/5]	±[-1/5, -4/5,-1/5, 2/5, 1,2/5, 2/5, -1/5, -4/5]
±[-1/5, 2/5, 2/5, 1, 2/5, -1/5,-1/5, -4/5, -4/5]	±[-4/5, -1/5,-1/5, 2/5, 1,2/5, 2/5, -1/5, -4/5]
±[2/5, -1/5, 1, 2/5, -1/5, 2/5,-1/5, -4/5, -4/5]	±[-1/5, -4/5, 2/5, -1/5,2/5, 1, 2/5, -1/5, -4/5]
±[-1/5, 2/5, 1, 2/5, -1/5, 2/5,-1/5, -4/5, -4/5]	±[-4/5,-1/5, 2/5, -1/5,2/5, 1, 2/5, -1/5, -4/5]
±[2/5, -1/5, 2/5, 1, -1/5, 2/5,-1/5, -4/5, -4/5]	±[-1/5, -4/5,-1/5, 2/5, 2/5, 1, 2/5, -1/5, -4/5]
±[-1/5, 2/5, 2/5, 1, -1/5, 2/5,-1/5, -4/5, -4/5]	±[-4/5, -1/5,-1/5, 2/5, 2/5, 1, 2/5, -1/5, -4/5]
±[2/5, -1/5, 1, 2/5, 2/5, -1/5, -4/5, -1/5, -4/5]	±[-1/5, -4/5, 2/5, -1/5, 1,2/5, -1/5, 2/5, -4/5]
±[-1/5, 2/5, 1, 2/5, 2/5, -1/5, -4/5, -1/5, -4/5]	±[-4/5,-1/5, 2/5, -1/5, 1,2/5, -1/5, 2/5, -4/5]
±[2/5, -1/5, 2/5, 1, 2/5, -1/5, -4/5, -1/5, -4/5]	±[-1/5, -4/5, -1/5, 2/5, 1,2/5, -1/5, 2/5, -4/5]
±[-1/5, 2/5, 2/5, 1, 2/5, -1/5, -4/5, -1/5, -4/5]	±[-4/5,-1/5, -1/5, 2/5, 1,2/5, -1/5, 2/5, -4/5]
±[2/5, -1/5, 1, 2/5, -1/5, 2/5, -4/5, -1/5, -4/5]	±[-1/5, -4/5, 2/5, -1/5,2/5, 1, -1/5, 2/5, -4/5]
±[-1/5, 2/5, 1, 2/5, -1/5, 2/5, -4/5, -1/5, -4/5]	±[-4/5,-1/5, 2/5, -1/5,2/5, 1, -1/5, 2/5, -4/5]
±[2/5, -1/5, 2/5, 1, -1/5, 2/5, -4/5, -1/5, -4/5]	±[-1/5, -4/5, -1/5, 2/5,2/5, 1, -1/5, 2/5, -4/5]
±[-1/5, 2/5, 2/5, 1, -1/5, 2/5, -4/5, -1/5, -4/5]	±[-4/5,-1/5, -1/5, 2/5,2/5, 1, -1/5, 2/5, -4/5]
±[1,2/5, 2/5, -1/5, -1/5, -4/5, 2/5, -1/5, -4/5]	±[2/5,-1/5, -1/5, -4/5,2/5, -1/5, 1, 2/5, -4/5]
±[2/5, 1, 2/5, -1/5, -1/5, -4/5, 2/5, -1/5, -4/5]	±[-1/5,2/5, -1/5, -4/5,2/5, -1/5, 1, 2/5, -4/5]
±[1,2/5, -1/5, 2/5, -1/5, -4/5, 2/5, -1/5, -4/5]	±[2/5,-1/5, -4/5, -1/5,2/5, -1/5, 1, 2/5, -4/5]
±[2/5, 1, -1/5, 2/5, -1/5, -4/5, 2/5, -1/5, -4/5]	±[-1/5,2/5, -4/5, -1/5,2/5, -1/5, 1, 2/5, -4/5]
±[1,2/5, 2/5, -1/5, -4/5, -1/5, 2/5, -1/5, -4/5]	±[2/5,-1/5, -1/5, -4/5,-1/5, 2/5, 1, 2/5, -4/5]
±[2/5, 1, 2/5, -1/5, -4/5, -1/5, 2/5, -1/5, -4/5]	±[-1/5,2/5, -1/5, -4/5,-1/5, 2/5, 1, 2/5, -4/5]
±[1,2/5, -1/5, 2/5, -4/5, -1/5, 2/5, -1/5, -4/5]	±[2/5,-1/5, -4/5, -1/5,-1/5, 2/5, 1, 2/5, -4/5]
±[2/5, 1, -1/5, 2/5, -4/5, -1/5, 2/5, -1/5, -4/5]	±[-1/5,2/5, -4/5, -1/5,-1/5, 2/5, 1, 2/5, -4/5]
±[1,2/5, 2/5, -1/5,-1/5, -4/5, -1/5,2/5, -4/5]	±[2/5,-1/5, -1/5, -4/5,2/5, -1/5, 2/5, 1, -4/5]
±[2/5, 1, 2/5, -1/5,-1/5, -4/5, -1/5,2/5, -4/5]	±[-1/5,2/5, -1/5, -4/5,2/5, -1/5, 2/5, 1, -4/5]
±[1,2/5, -1/5, 2/5, -1/5, -4/5, -1/5,2/5, -4/5]	±[2/5,-1/5, -4/5, -1/5,2/5, -1/5, 2/5, 1, -4/5]
±[2/5, 1, -1/5, 2/5, -1/5, -4/5, -1/5,2/5, -4/5]	±[-1/5,2/5, -4/5, -1/5,2/5, -1/5, 2/5, 1, -4/5]
±[1,2/5, 2/5, -1/5, -4/5, -1/5, -1/5,2/5, -4/5]	±[2/5,-1/5, -1/5, -4/5,-1/5, 2/5, 2/5, 1, -4/5]
±[2/5, 1, 2/5, -1/5, -4/5, -1/5, -1/5,2/5, -4/5]	±[-1/5,2/5, -1/5, -4/5,-1/5, 2/5, 2/5, 1, -4/5]
±[1,2/5, -1/5, 2/5, -4/5, -1/5, -1/5,2/5, -4/5]	±[2/5,-1/5, -4/5, -1/5,-1/5, 2/5, 2/5, 1, -4/5]
±[2/5, 1, -1/5, 2/5, -4/5, -1/5, -1/5,2/5, -4/5]	±[-1/5,2/5, -4/5, -1/5,-1/5, 2/5, 2/5, 1, -4/5]
±[2/5, -1/5, 1, 2/5, -1/5, -4/5, 2/5, -1/5, -4/5]	±[-1/5, -4/5, 2/5, -1/5,2/5, -1/5, 1, 2/5, -4/5]
±[-1/5, 2/5, 1, 2/5, -1/5, -4/5, 2/5, -1/5, -4/5]	±[-4/5,-1/5, 2/5, -1/5,2/5, -1/5, 1, 2/5, -4/5]
±[2/5, -1/5, 2/5, 1, -1/5, -4/5, 2/5, -1/5, -4/5]	±[-1/5, -4/5, -1/5, 2/5,2/5, -1/5, 1, 2/5, -4/5]
±[-1/5, 2/5, 2/5, 1, -1/5, -4/5, 2/5, -1/5, -4/5]	±[-4/5,-1/5, -1/5, 2/5,2/5, -1/5, 1, 2/5, -4/5]
±[2/5, -1/5, 1, 2/5, -4/5, -1/5, 2/5, -1/5, -4/5]	±[-1/5, -4/5, 2/5, -1/5,-1/5, 2/5, 1, 2/5, -4/5]
±[-1/5, 2/5, 1, 2/5, -4/5, -1/5, 2/5, -1/5, -4/5]	±[-4/5,-1/5, 2/5, -1/5,-1/5, 2/5, 1, 2/5, -4/5]
±[2/5, -1/5, 2/5, 1, -4/5, -1/5, 2/5, -1/5, -4/5]	±[-1/5, -4/5, -1/5, 2/5,-1/5, 2/5, 1, 2/5, -4/5]
±[-1/5, 2/5, 2/5, 1, -4/5, -1/5, 2/5, -1/5, -4/5]	±[-4/5,-1/5, -1/5, 2/5,-1/5, 2/5, 1, 2/5, -4/5]
±[2/5, -1/5, 1, 2/5, -1/5, -4/5, -1/5,2/5, -4/5]	±[-1/5, -4/5, 2/5, -1/5,2/5, -1/5, 2/5, 1, -4/5]
±[-1/5, 2/5, 1, 2/5, -1/5, -4/5, -1/5,2/5, -4/5]	±[-4/5,-1/5, 2/5, -1/5,2/5, -1/5, 2/5, 1, -4/5]
±[2/5, -1/5, 2/5, 1, -1/5, -4/5, -1/5,2/5, -4/5]	±[-1/5, -4/5, -1/5, 2/5,2/5, -1/5, 2/5, 1, -4/5]
±[-1/5, 2/5, 2/5, 1, -1/5, -4/5, -1/5,2/5, -4/5]	±[-4/5,-1/5, -1/5, 2/5,2/5, -1/5, 2/5, 1, -4/5]
±[2/5, -1/5, 1, 2/5, -4/5, -1/5, -1/5,2/5, -4/5]	±[-1/5, -4/5, 2/5, -1/5,-1/5, 2/5, 2/5, 1, -4/5]
±[-1/5, 2/5, 1, 2/5, -4/5, -1/5, -1/5,2/5, -4/5]	±[-4/5,-1/5, 2/5, -1/5,-1/5, 2/5, 2/5, 1, -4/5]
±[2/5, -1/5, 2/5, 1, -4/5, -1/5, -1/5,2/5, -4/5]	±[-1/5, -4/5, -1/5, 2/5,-1/5, 2/5, 2/5, 1, -4/5]
±[-1/5, 2/5, 2/5, 1, -4/5, -1/5, -1/5,2/5, -4/51	±[-4/5,-1/5, -1/5, 2/5,-1/5, 2/5, 2/5, 1, -4/51

Table 7

Receiver circuits

[0078] As previously mentioned, the multi-input comparator detector circuits described in [Holden I] and [Ulrich I] are advantageously utilized with the described codes. As an example, embodiments of both methods are shown in FIGs 4-8.

[0079] FIG. 4 illustrates two embodiments of the [Holden I] circuit accepting six inputs w_0 - w_5 which are combined in proportions [1/3 1/3 1/3 -1/3 -1/3 -1/3] respectively, producing differential results outp and outm. The first embodiment incorporates high-frequency equalization via adjustable or selectable resistor/capacitor elements. The second embodiment does not provide equalization.

[0080] The alternative embodiment of FIG. 5 illustrates two embodiments of the [Ulrich I] circuit accepting the same six inputs w_0,…, w_5 which are c

[0081] d in proportions [1/3 1/3 1/3 -1/3 -1/3 -1/3] respectively, producing equivalent differential results outp and outm. As in FIG. 4, the first embodiment incorporates high-frequency equalization via adjustable or selectable resistor/capacitor elements, and the second embodiment does not provide equalization.

[0082] FIG. 6 illustrates two embodiments of the [Holden I] circuit accepting three inputs w_0 - w_2 and not using the three inputs w_3,…, w_5 in combinations representing the proportions [1/2 1/2 -1 0 0 0] respectively, producing differential results outp and outm. The first embodiment incorporates high-frequency equalization via adjustable or selectable resistor/capacitor elements. The second embodiment does not provide equalization.

[0083] The alternative embodiment of FIG. 7 illustrates two embodiments of the [Ulrich I] circuit accepting the same inputs as FIG. 6 and producing the same producing differential results outp and outm. As in FIG. 6, the first embodiment incorporates high-frequency equalization via adjustable or selectable resistor/capacitor elements, and the second embodiment does not provide equalization.

[0084] FIG. 8 illustrates two embodiments accepting two inputs w_0, w_1 and not using the four inputs w_4, w_5 in combinations representing the proportions [1 -1 0 0 0 0] respectively, producing differential results outp and outm. The first embodiment incorporates high-frequency equalization via adjustable or selectable resistor/capacitor elements. The second embodiment does not provide equalization. As one familiar with the art will note, the two circuit topologies of [Holden I] and [Ulrich I] reduce to a single differential stage in this two input case.

Driver embodiments

[0085] Generation of the desired output signal levels described in accordance with at least one embodiment may be obtained using the driver circuit of [Ulrich II]. As specific examples of the approach, driver embodiments capable of generating the particular output signal levels associated with each of the previous examples are illustrated.

[0086] FIG. 9 shows one driver embodiment in accordance with at least one embodiment producing the optimized signal levels determined in the first example embodiment above. Encoder 901 encodes the data to be transmitted using the matrix M of Eqn. 13, and passes the encoded control signal result to the set of output wire drivers 910. As this is a three wire code, there are three instances of 910 shown, herein called a wire driver slice, each taking the appropriate encoded element from 901 and producing the correct signal levels for its output wire.

[0087] As is common practice in high-speed communications systems, multiple processing phases may be used to increase throughput of processing-intensive operations such as encoding. Thus, digital multiplexers 911 are shown, taking the individual phase outputs and switching between them to produce a single full wire rate encoded data stream. As will be apparent to one familiar with the art, a single phase omitting the multiplexer to many phases of data supported by wider or deeper multiplexer configurations may be incorporated in this design. Subsequent driver embodiment examples incorporate the same illustrative encoder and multiplexer design, varying only in the width of the resulting output which is determined by the number of individual output wire drivers utilized.

[0088] The full wire rate encoded values are presented to digital output drivers 912 which are interconnected by series source resistors 913, 914, 915 to the common output wire producing a digitally controlled analog output. Because each of the series source resistors has a particular predetermined value, the steps produced in this digital-to-analog converter need not be identical. For the particular values illustrated in FIG. 9, the output values are shown in Table 6.

Value	Output	Comments
000	-1	
001	-4/5	
010	-2/5	Not used by this code
011	-1/5	
100	1/5	
101	2/5	Not used by this code
110	4/5	
111	1	

Table 6

[0089] Following good integrated circuit design practices, the value of resistor 913 would preferably be obtained by paralleling six 500 ohm resistors, the value of resistor 914 by paralleling three 500 ohm resistors, and the value of resistor 915 by using a single 500 ohm resistor, all resistors being of identical design, size, and composition.

[0090] As taught by [Ulrich II], multiple instances of a wire driver slice such as 910 may be also be advantageously paralleled to drive a single wire with appropriate adjusted component values in some alternative embodiments. In one such alternative embodiment, each wire driver slice 910 of FIG. 9 is replaced by, as a numeric example presented without implying a limitation, thirty-two identical wire driver slices receiving the same encoded control signal result. Because the wire driver slices are in parallel, each need drive a much smaller current into the common wire output, thus the transistors of digital drivers 912 may be smaller, and the values of series source resistors 913, 914, 915 will be

in this example 32 times larger than required for a single wire driver slice, significantly simplifying implementation in an integrated circuit device.

[0091] Similarly, alternative embodiments may utilize any known encoding of the control information passing from encoder 901 through multiplexers (if used) to control digital output drivers with series source resistors, including without limitation unary or thermometer encoding and binary or other weighted-bit encoding.

[0092] The embodiment of FIG. 10 shows the same three wire driver design as the previous example, using series source resistors of 300/4 ohms, 300 ohms, and 300 ohms respectively, producing output signal levels of [-1, 2/3, 1/6, -1/6, -2/3, 1].

[0093] The embodiment of FIG. 11 incorporates a fourth digital output driver and series source resistor in each wire driver slice, as well as a total of six wire driver slices to drive six wire outputs with signals of [1, ½, ¼, 0, -1/4, -1/2, 1]. The series source resistors used are 400/3 ohms, 400/2 ohms, 400/2 ohms, and 400 ohms.

[0094] The embodiment of FIG. 12 also utilizes four digital output drivers per wire driver slice and six wire driver slices to drive six wires with signals of [1, 7/8, ½, ¼, 1/8, -1/8, -1/4, -1/2, -1] using series source resistors of 800/6 ohms, 800/5 ohms, 800/4 ohms, and 800 ohms.

[0095] The embodiment of FIG. 13 utilizes only three digital output drivers per slice, but uses eight slices to drive eight wire outputs with signals of [1, 4/5, 2/5, 1/5, -1/5, -2/5, -4/5, -1] using series resistor values of 500/6 ohms, 500/3 ohms, and 500 ohms.

Embodiments

In at least one embodiment, an apparatus comprises a multi-wire bus configured to receive a set of symbols of a codeword, the set of symbols representing a weighted sum of sub-channel code vectors, each sub-channel code vector weighted according to a corresponding antipodal weight of a set of antipodal weights, the set of antipodal weight set containing at least two unique magnitudes, wherein the sub-channel code vectors are mutually orthogonal, and wherein the sub-channel code vectors form a scaled-orthogonal

matrix, and a decoder, connected to the multi-wire bus, comprising a plurality of sub-channel comparators configured to generate a respective plurality of comparator output values based on the received set of symbols of the codeword, each comparator comprising a set of chi-normalized input weights, wherein each set of chi-normalized input weights is selected according to a respective sub-channel code vector, and wherein the antipodal weight set is selected such that each subchannel comparator generates antipodal values greater than a minimum value. In some embodiments, the antipodal weight set is selected such that each subchannel comparator generates antipodal values of substantially similar magnitudes.

[0096] In at least one embodiment, the set of antipodal weights comprises at least two antipodal weights having distinct magnitudes.

[0097] In at least one embodiment, each of the antipodal weights in the set of antipodal weights has a magnitude less than 1.

[0098] In at least one embodiment, the set of antipodal weights is based on a codeword symbol normalization constant, μ.

[0100] In at least one embodiment, the codeword symbol normalization constant μ normalizes the symbols of the codeword to values having magnitudes less than or equal to 1.

[0101] In at least one embodiment, a sum of the antipodal weights in the set of antipodal weights is maximized according to the antipodal value corresponding a minimum vertical opening threshold. In at least one embodiment, the sum of the antipodal weights in the set of antipodal weights is also maximized according to the codeword symbol normalization constant μ.

[0102] In at least one embodiment, the antipodal value is greater than a predetermined vertical opening threshold, .

[0103] As shown in FIG. 14, a method 1400 in accordance with at least one embodiment comprises receiving, at step 1402, a set of symbols of a codeword on a

multi-wire bus, the set of symbols representing a weighted sum of sub-channel code vectors, each sub-channel code vector weighted based on a corresponding antipodal weight of a set of antipodal weights, wherein the sub-channel code vectors are mutually orthogonal, and wherein the sub-channel code vectors form a scaled-orthogonal matrix, and generating, at step 1404, a plurality of comparator output values based on the received set of symbols of the codeword using a plurality of sub-channel comparators, wherein each sub-channel comparator comprises a set of chi-normalized input weights, each set of chi-normalized input weights selected according to a respective sub-channel code vector, and wherein each comparator output value is represented as an antipodal value.

[0104] In at least one embodiment, the set of antipodal weights comprises at least two antipodal weights having distinct magnitudes.

[0105] In at least one embodiment, each of the antipodal weights in the set of antipodal weights has a magnitude less than 1.

[0106] In at least one embodiment, the set of antipodal weights is based on a codeword symbol normalization constant, μ.

[0107] In at least one embodiment, the codeword symbol normalization constant μ normalizes the symbols of the codeword to values having magnitudes less than or equal to 1.

[0108] In at least one embodiment, the antipodal value is greater than a predetermined vertical opening threshold, δ.

[0109] As shown in FIG. 15, a method 1500 in accordance with at least one embodiment comprises receiving, at step 1502, a vector corresponding to a set of antipodal weights, generating, at step 1504, a set of symbols of a codeword, the codeword representing a weighted sum of a plurality of sub-channel vectors, wherein a weighting of each sub-channel vector is determined by a corresponding antipodal weight of the set of antipodal weights, and wherein the plurality of sub-channel vectors form a scaled-

orthogonal matrix, and, transmitting, at step 1506, the set of symbols of the codeword on a multi-wire bus.

[0110] In at least one embodiment, the scaled-orthogonal matrix is represented as

$$M = \begin{pmatrix} 1 & 1 & 1 \\ 1 & -1 & 0 \\ 1 & 1 & -2 \end{pmatrix}$$

and the vector corresponding to the set of antipodal weights is represented as (0,±3/5,±2/5).

[0111] In at least one embodiment, the scaled-orthogonal matrix is represented as

$$M = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 \\ 1 & 1 & -1 & -1 & 0 \\ 1 & 1 & 1 & 1 & -4 \end{pmatrix}$$

and the vector corresponding to the set of antipodal weights is represented as (0, ±5/12, ±5/12, ±5/12, ±1/6).

[0112] In at least one embodiment, the scaled-orthogonal matrix is represented as

$$M = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 \\ 1 & 1 & -1 & -1 & 0 & 0 \\ 1 & 1 & 1 & 1 & -2 & -2 \end{pmatrix}$$

and the vector corresponding to the set of antipodal weights is represented as (0, ±3/8, ±3/8, ±1/2, ±3/8, ±1/4).

[0113] In at least one embodiment, the scaled-orthogonal matrix is represented as

$$M = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 1 & 1 & -2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 1 & 1 & -2 \\ 1 & 1 & 1 & -1 & -1 & -1 \end{pmatrix}$$

and the vector corresponding to the set of antipodal weights is represented as (0, ±3/8, ±1/4, ±3/8, ±1/4, ±3/8).

[0114] In at least one embodiment, the scaled-orthogonal matrix is represented as

$$M = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 \\ 1 & 1 & -1 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & -1 & -1 & 0 \\ 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 & 0 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & -8 \end{pmatrix}$$

and the vector corresponding to the set of antipodal weights is represented as (0,±3/10,±3/10,±3/10,±3/10,±3/10,±3/10,±3/10,±l/10) .

CLAIMS

We claim:

1. An apparatus comprising:

a multi-wire bus configured to receive a set of symbols of a codeword, the set of symbols representing a weighted sum of sub-channel code vectors, each sub-channel code vector weighted according to a corresponding antipodal weight of a set of antipodal weights, the set of antipodal weight set containing at least two unique magnitudes, wherein the sub-channel code vectors are mutually orthogonal, and wherein the sub-channel code vectors form a scaled-orthogonal matrix;

a decoder, connected to the multi-wire bus, comprising a plurality of sub-channel comparators configured to generate a respective plurality of comparator output values based on the received set of symbols of the codeword, each comparator comprising a set of chi-normalized input weights, wherein each set of chi-normalized input weights is selected according to a respective sub-channel code vector, and

wherein the antipodal weight set is selected such that each subchannel comparator generates antipodal values greater than a minimum value.

2. The apparatus of claim 1, wherein the antipodal weight set is selected such that each subchannel comparator generates antipodal values of substantially similar magnitudes.

3. The apparatus of claim 1, wherein each of the antipodal weights in the set of antipodal weights has a magnitude less than 1.

4. The apparatus of claim 1, wherein the set of antipodal weights is based on a codeword symbol normalization constant, μ.

5. The apparatus of claim 4, wherein the codeword symbol normalization constant μ normalizes the symbols of the codeword to values having magnitudes less than or equal to 1.

6. The apparatus of claim 1, wherein a sum of the antipodal weights in the set of antipodal weights is maximized according to the antipodal value corresponding a minimum vertical opening threshold.

7. The apparatus of claim 6, wherein the sum of the antipodal weights in the set of antipodal weights is also maximized according to the codeword symbol normalization constant μ.

8. The apparatus of claim 1, wherein the antipodal value is greater than a predetermined vertical opening threshold, δ.

9. A method comprising:

receiving a vector corresponding to a set of antipodal weights;

generating a set of symbols of a codeword, the codeword representing a weighted sum of a plurality of sub-channel vectors, wherein a weighting of each sub-channel vector is determined by a corresponding antipodal weight of the set of antipodal weights, and wherein the plurality of sub-channel vectors form a scaled-orthogonal matrix; and,

transmitting the set of symbols of the codeword on a multi-wire bus.

10. The method of claim 9, wherein the scaled-orthogonal matrix is represented as

$$M = \begin{pmatrix} 1 & 1 & 1 \\ 1 & -1 & 0 \\ 1 & 1 & -2 \end{pmatrix}$$

and the vector corresponding to the set of antipodal weights is represented as (0,±3/5,±2/5

11. The method of claim 9, wherein the scaled-orthogonal matrix is represented as

$$M = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 \\ 1 & 1 & -1 & -1 & 0 \\ 1 & 1 & 1 & 1 & -4 \end{pmatrix}$$

and the vector corresponding to the set of antipodal weights is represented as (0, ±5/12, ±5/12, ±5/12, ±1/6).

12. The method of claim 9, wherein the scaled-orthogonal matrix is represented as

$$M = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 \\ 1 & 1 & -1 & -1 & 0 & 0 \\ 1 & 1 & 1 & 1 & -2 & -2 \end{pmatrix}$$

and the vector corresponding to the set of antipodal weights is represented as (0, ±3/8, ±3/8, ±1/2, ±3/8, ±1/4).

13. The method of claim 9, wherein the scaled-orthogonal matrix is represented as

$$M = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 1 & 1 & -2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 1 & 1 & -2 \\ 1 & 1 & 1 & -1 & -1 & -1 \end{pmatrix}$$

and the vector corresponding to the set of antipodal weights is represented as (0, ±3/8, ±1/4, ±3/8, ±1/4, ±3/8).

14. The method of claim 9, wherein the scaled-orthogonal matrix is represented as

$$M = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 \\ 1 & 1 & -1 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & -1 & -1 & 0 \\ 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 & 0 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & -8 \end{pmatrix}$$

and the vector corresponding to the set of antipodal weights is represented as (0,+3/10,+3/10,+3/10,+3/10,+3/10,+3/10,+3/10,+1/10).

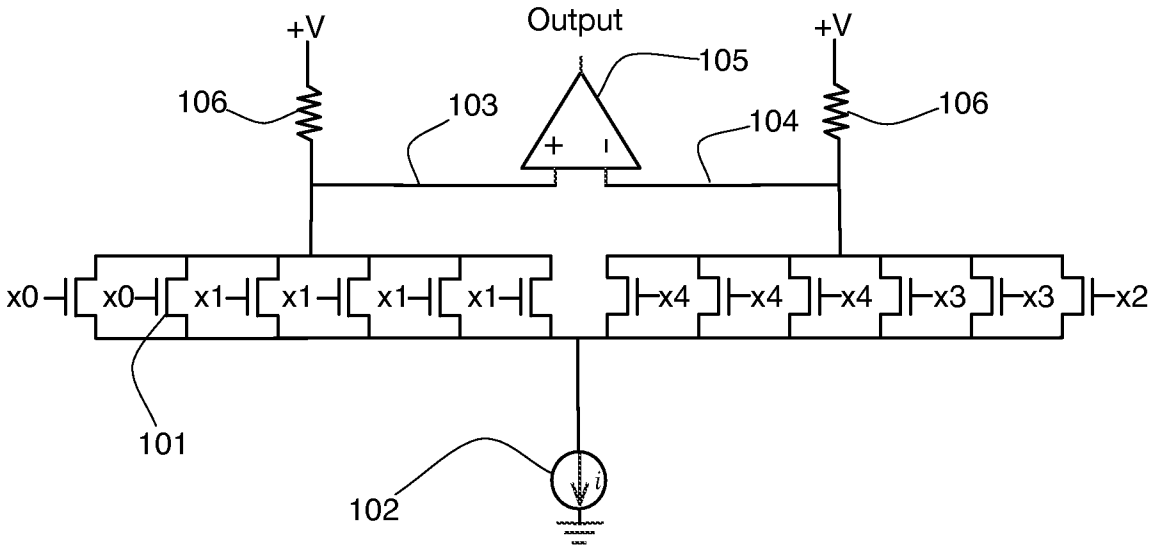

+V
Output
+V
105
106
103
104
106
x0
x0
x1
x1
x1
x1
x4
x4
x4
x3
x3
x2
101
102

FIG. 1

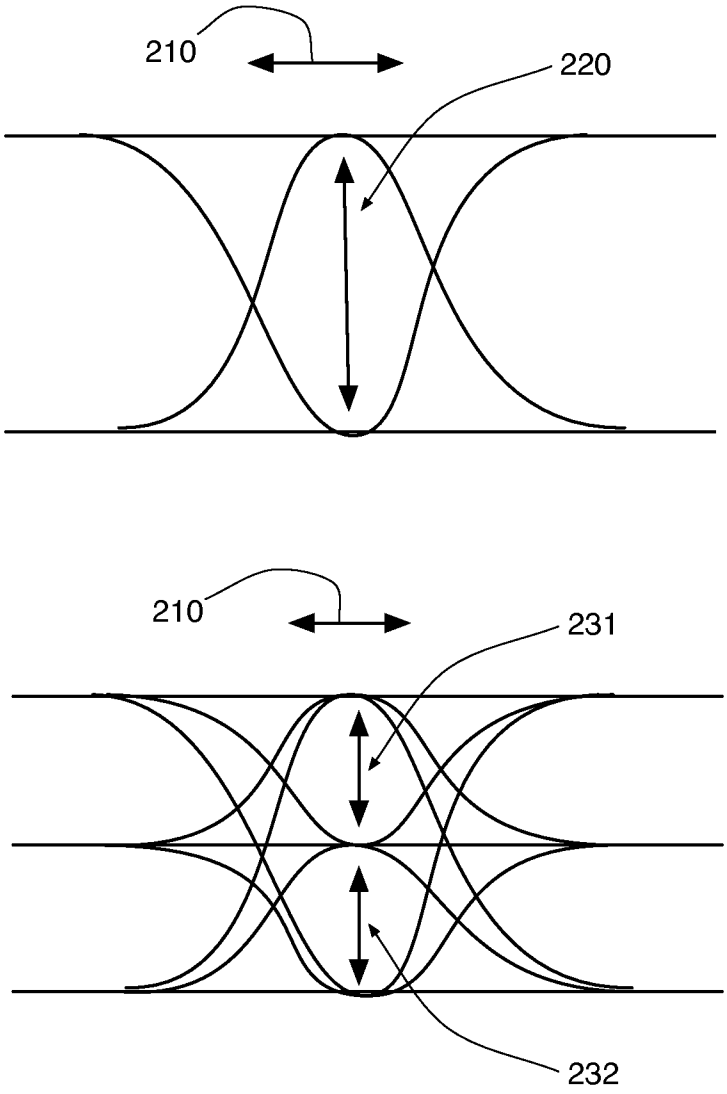


FIG. 2

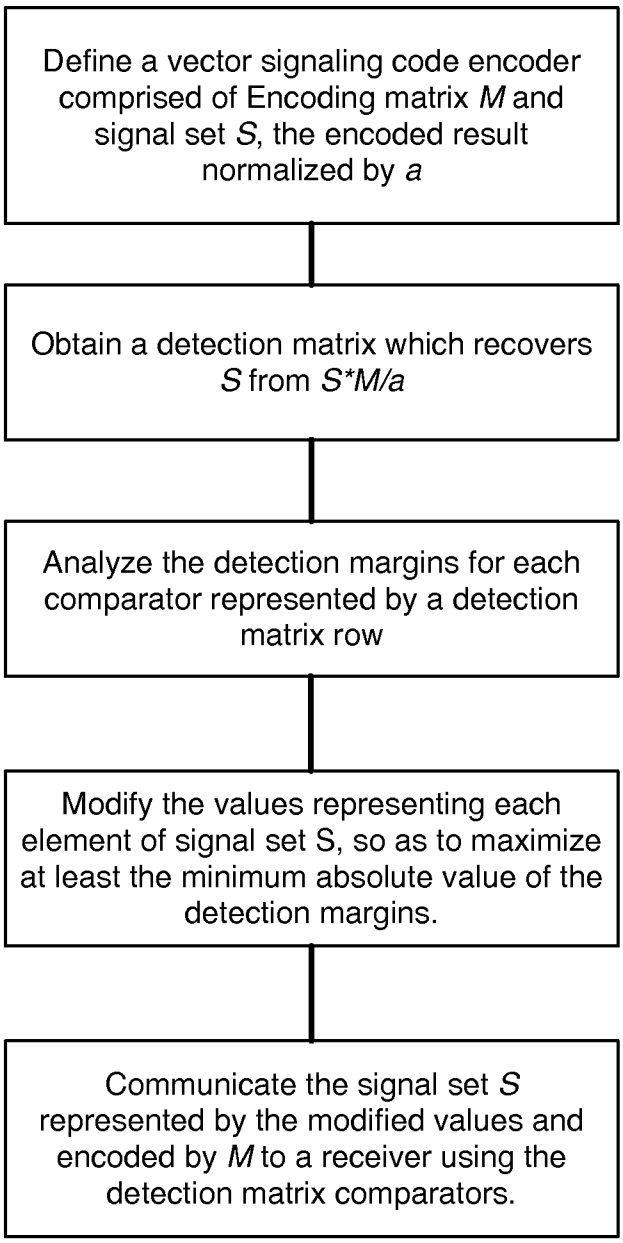
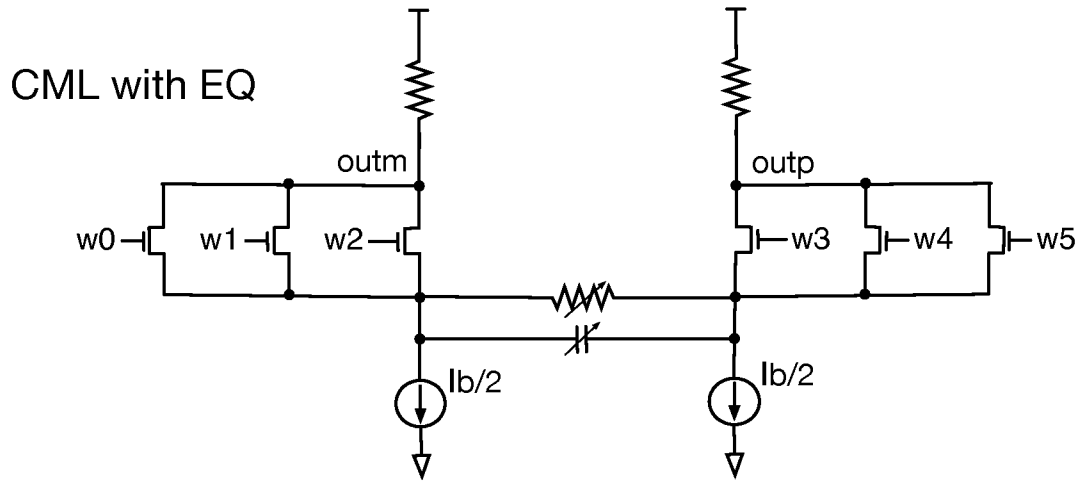

Define a vector signaling code encoder comprised of Encoding matrix *M* and signal set *S*, the encoded result normalized by *a*
Obtain a detection matrix which recovers *S* from *S*M/a*
Analyze the detection margins for each comparator represented by a detection matrix row
Modify the values representing each element of signal set S, so as to maximize at least the minimum absolute value of the detection margins.
Communicate the signal set *S* represented by the modified values and encoded by *M* to a receiver using the detection matrix comparators.

FIG. 3

Mix [1/3 1/3 1/3 -1/3 -1/3 -1/3]



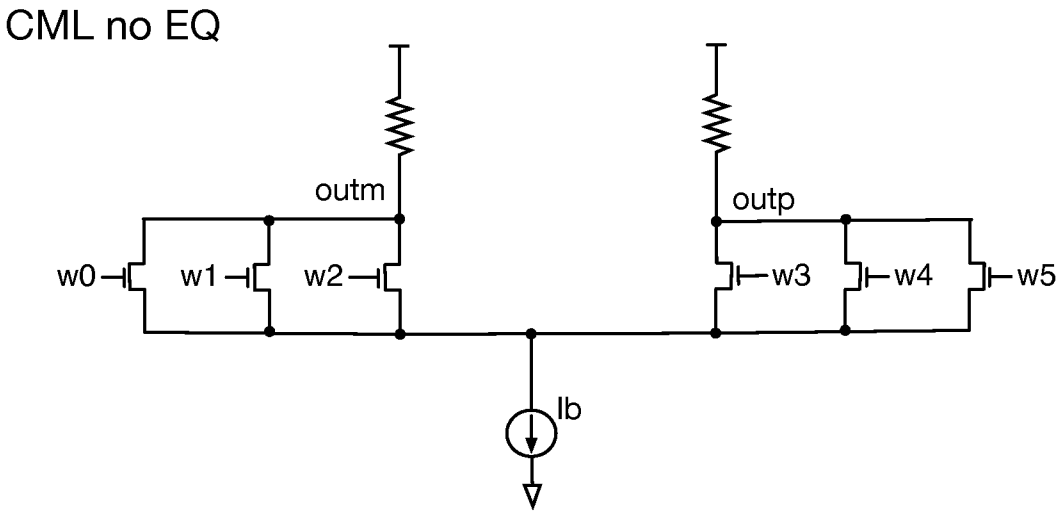


FIG. 4

Mix [1/3 1/3 1/3 -1/3 -1/3 -1/3]

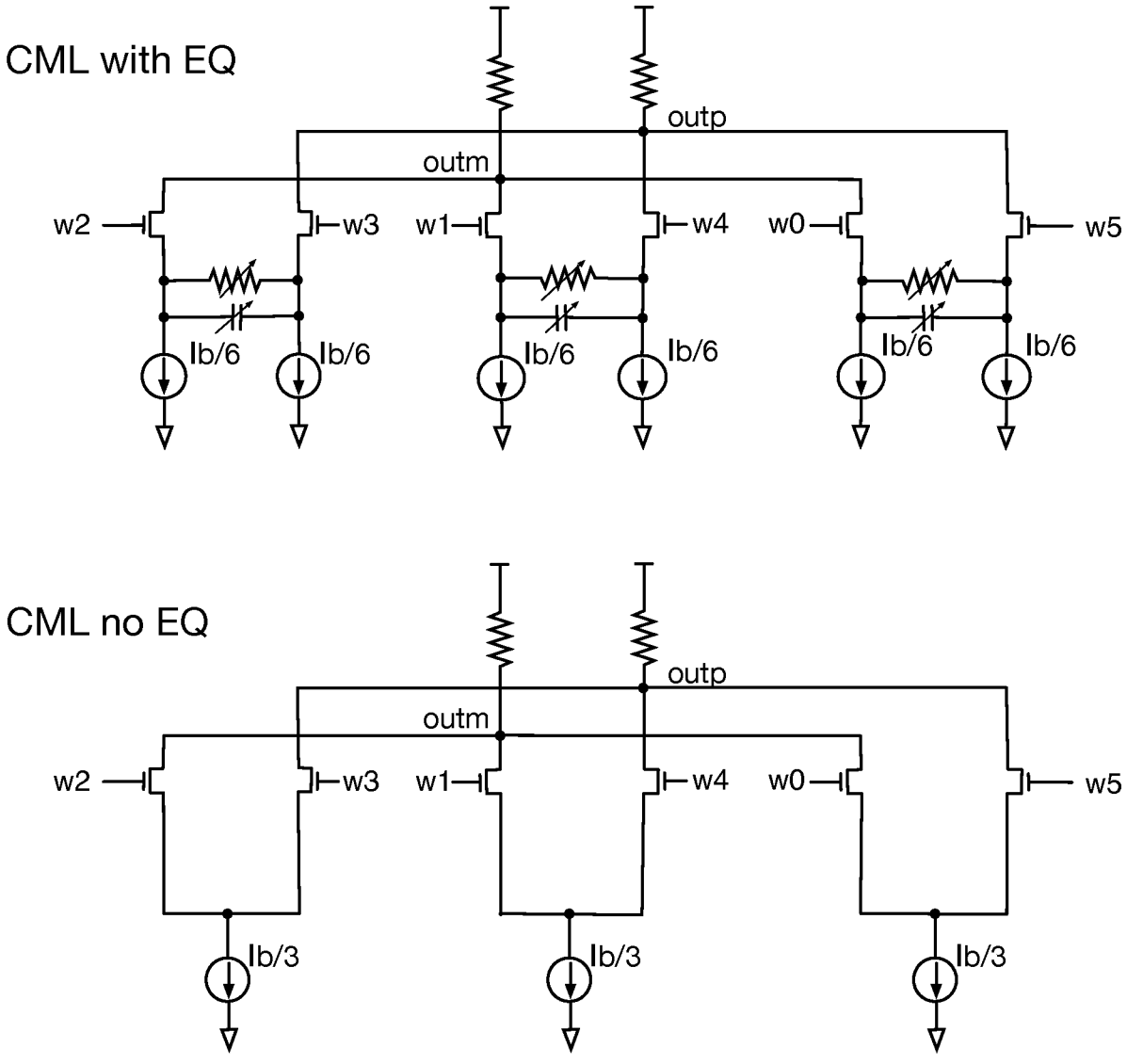


FIG. 5

Mix [1/2 1/2 -1 0 0 0]

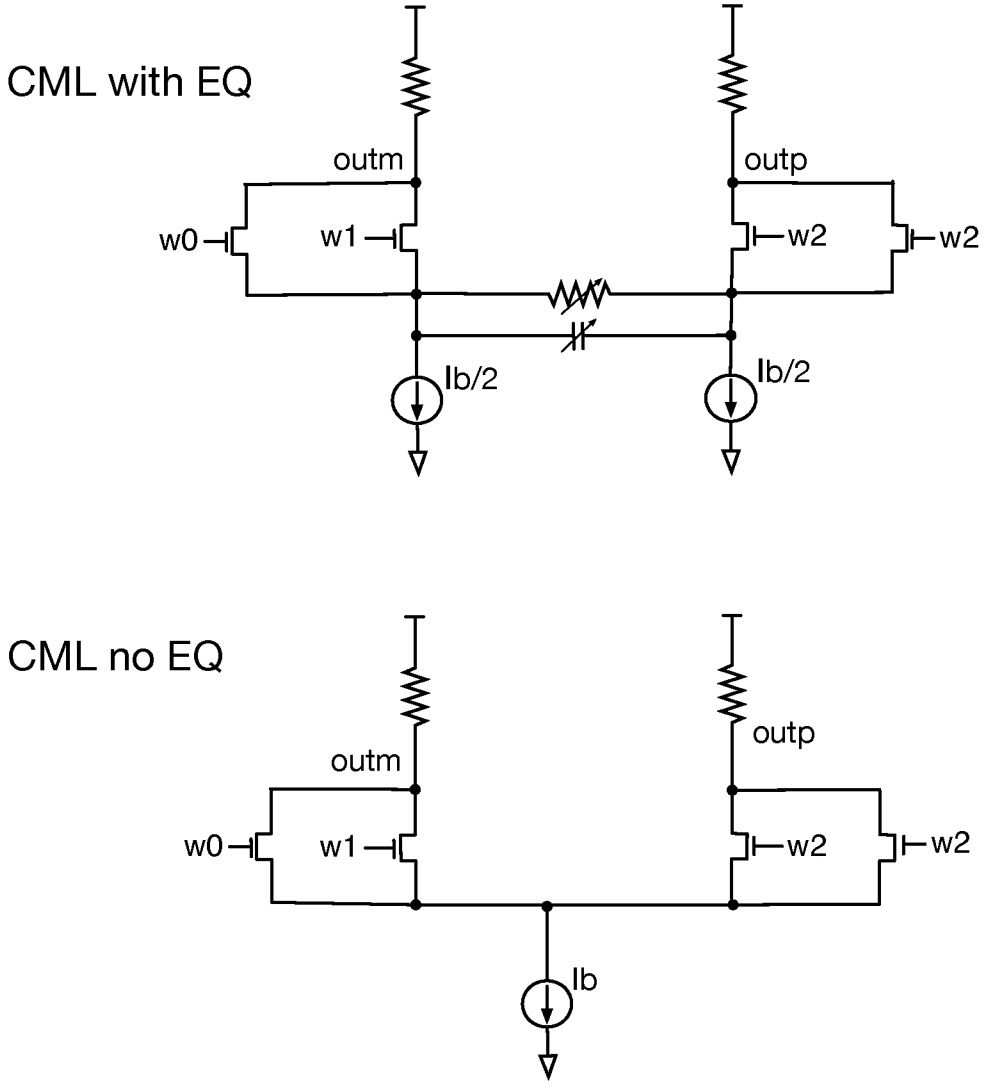


FIG. 6

Mix [1/2 1/2 -1 0 0 0]

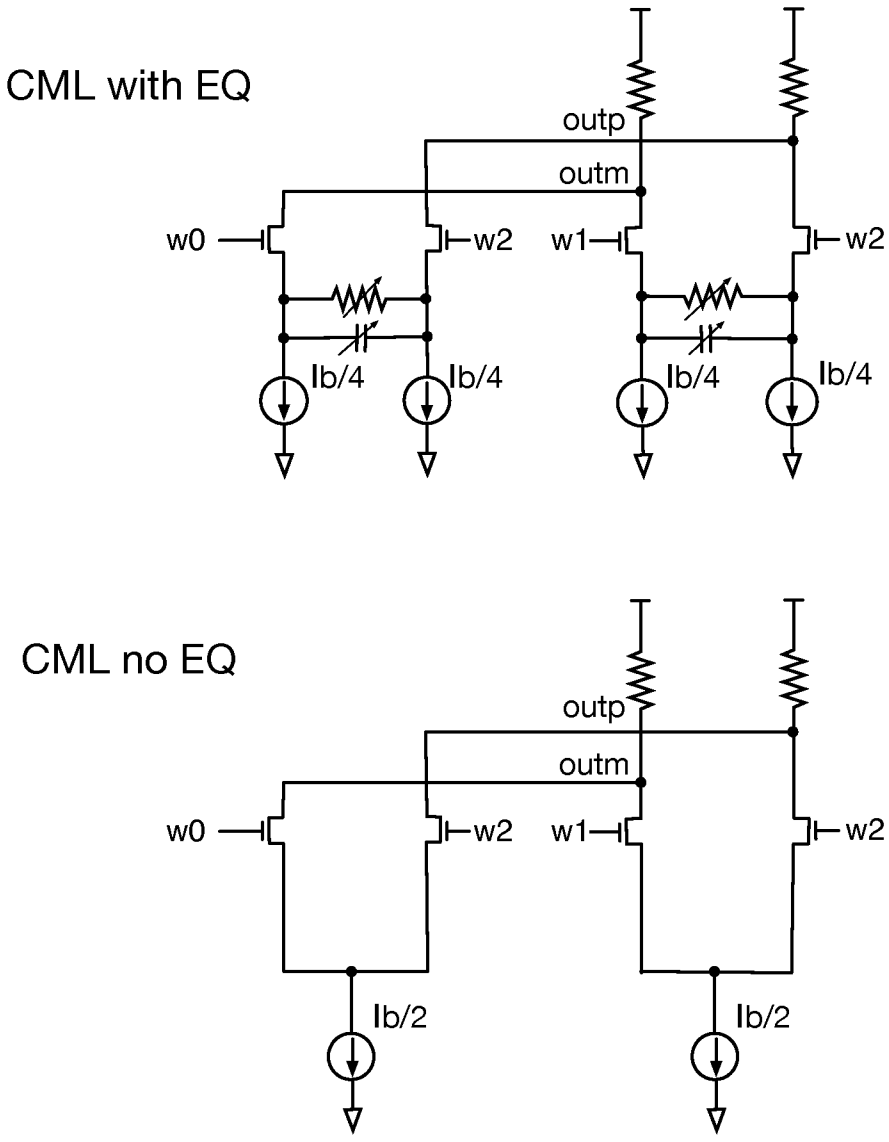
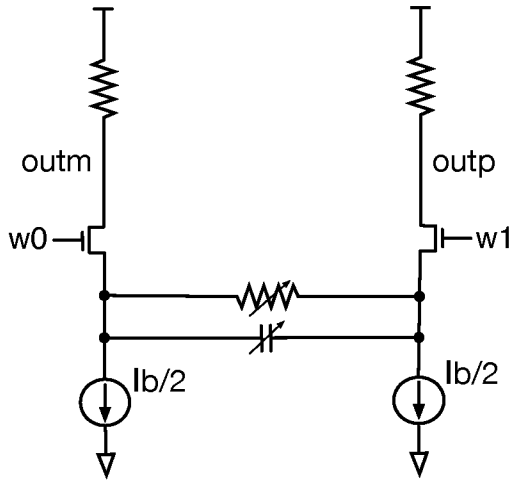


FIG. 7

Mix [1 -1 0 0 0 0]

CML with EQ



CML no EQ

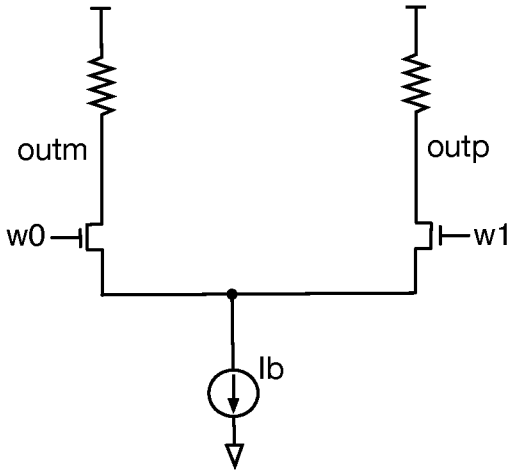


FIG. 8

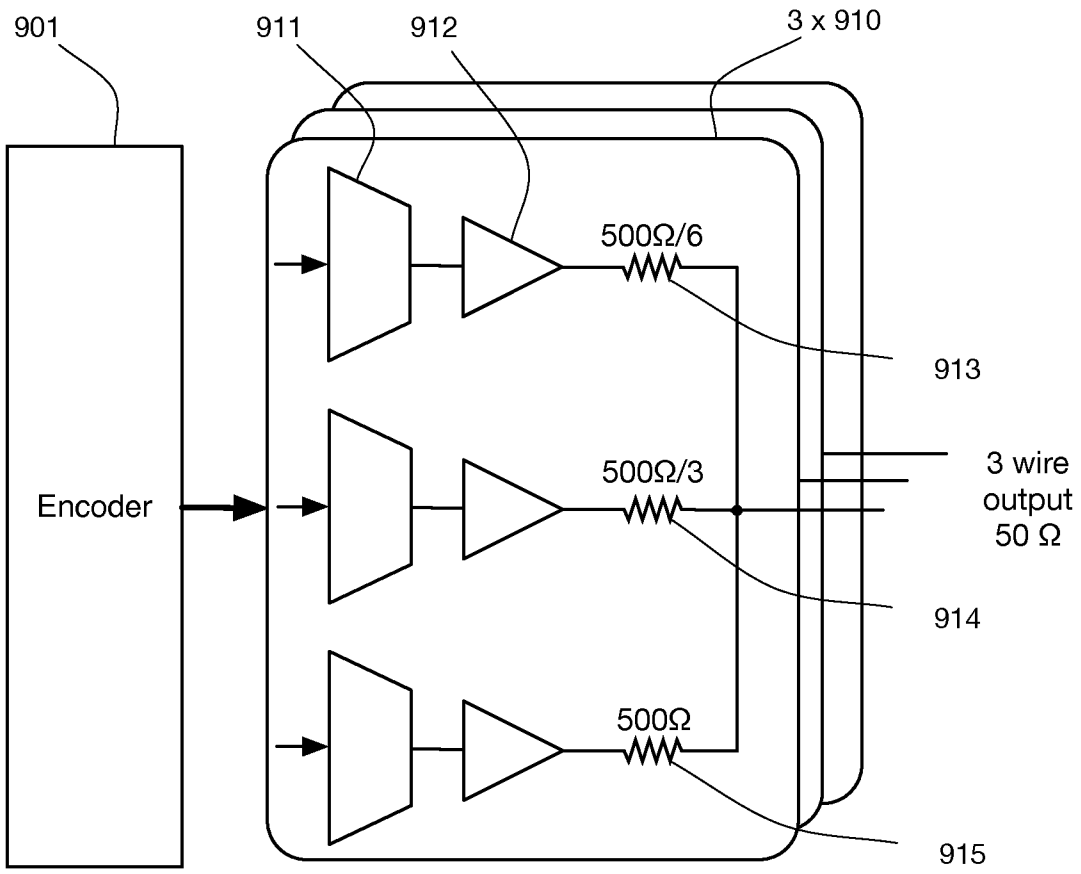

901
911
912
3 x 910
500Ω/6
913
Encoder
500Ω/3
3 wire
output
50 Ω
914
500Ω
915

FIG. 9

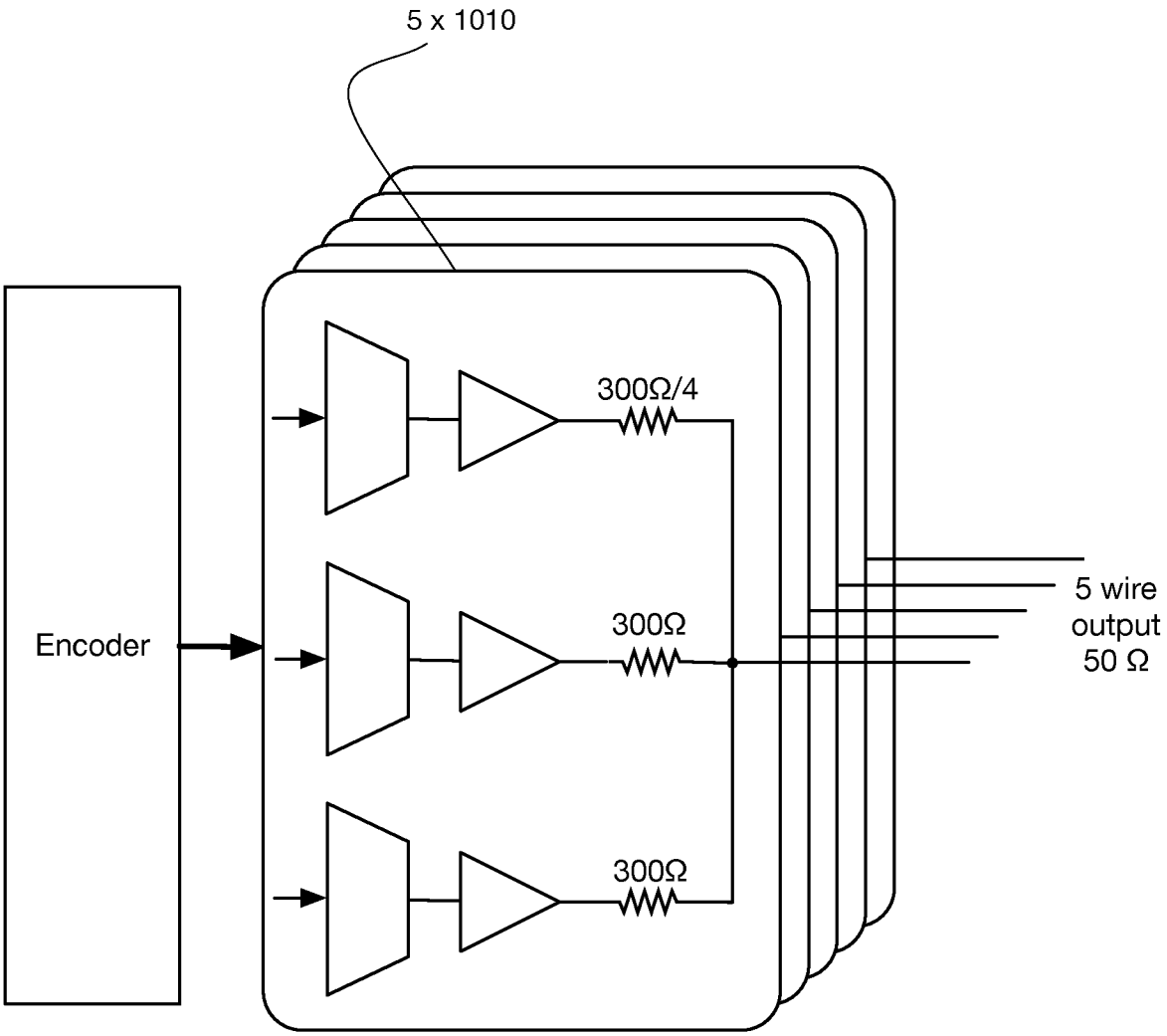


FIG. 10

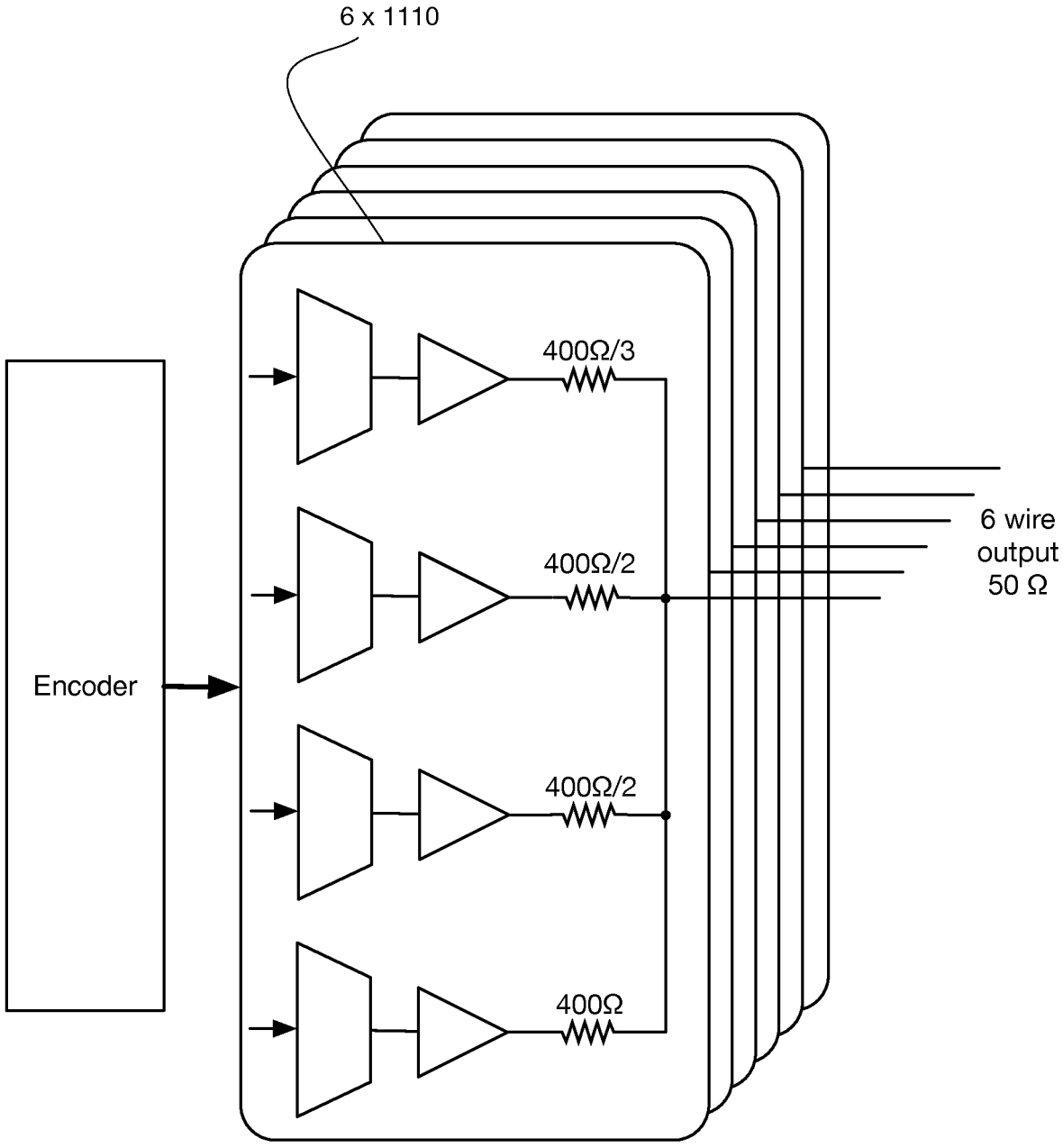


FIG. 11

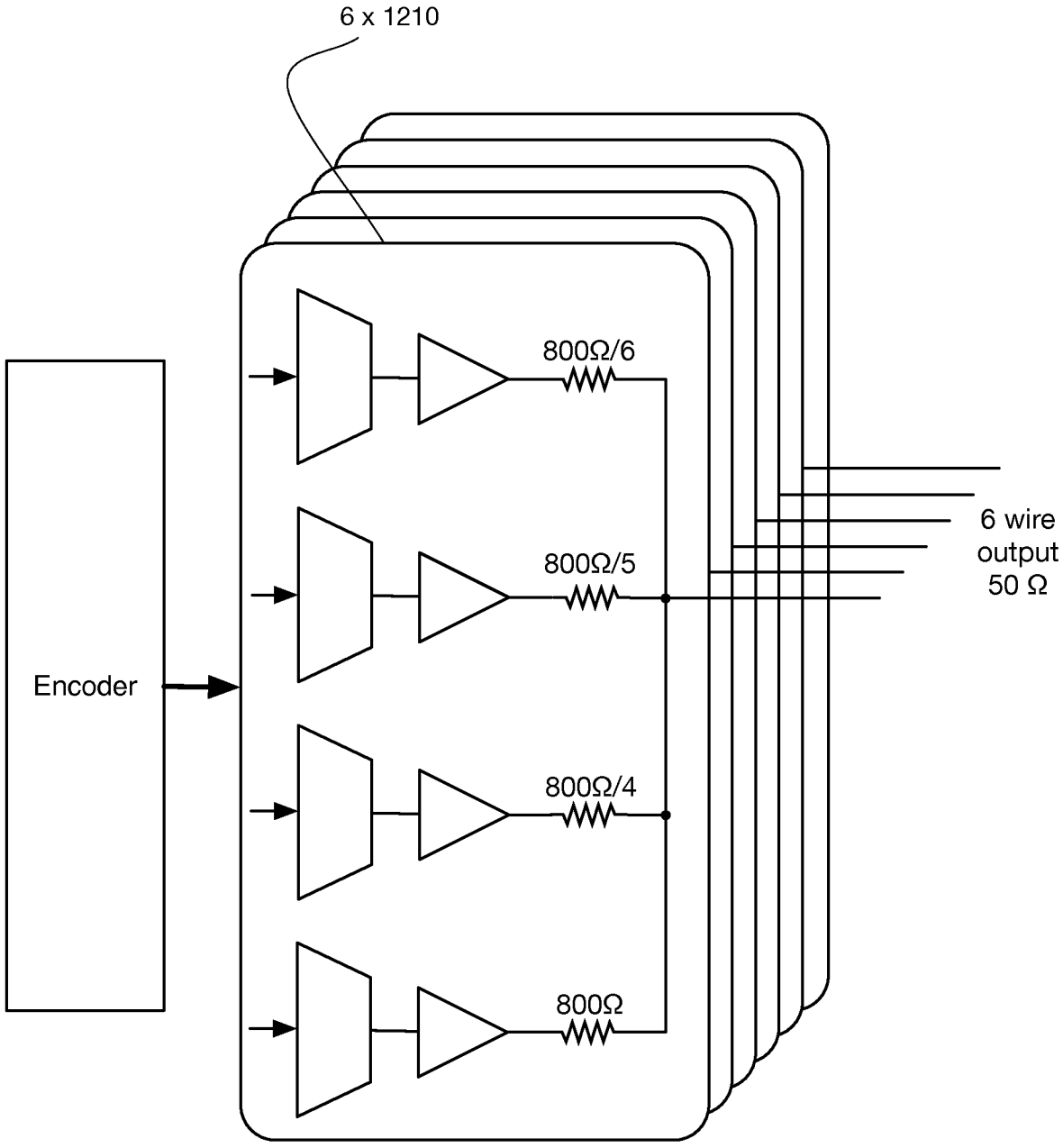


FIG. 12

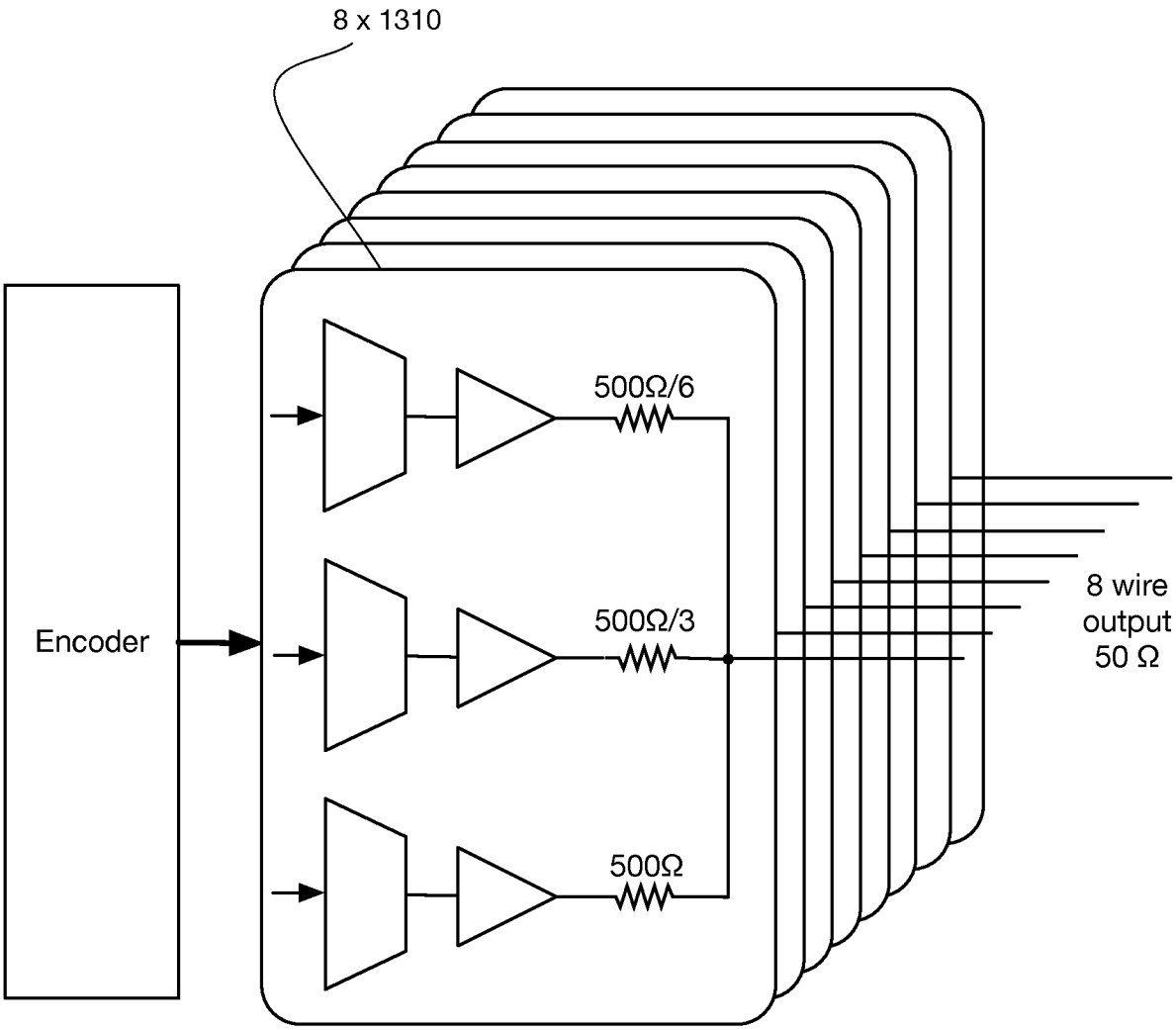


FIG. 13

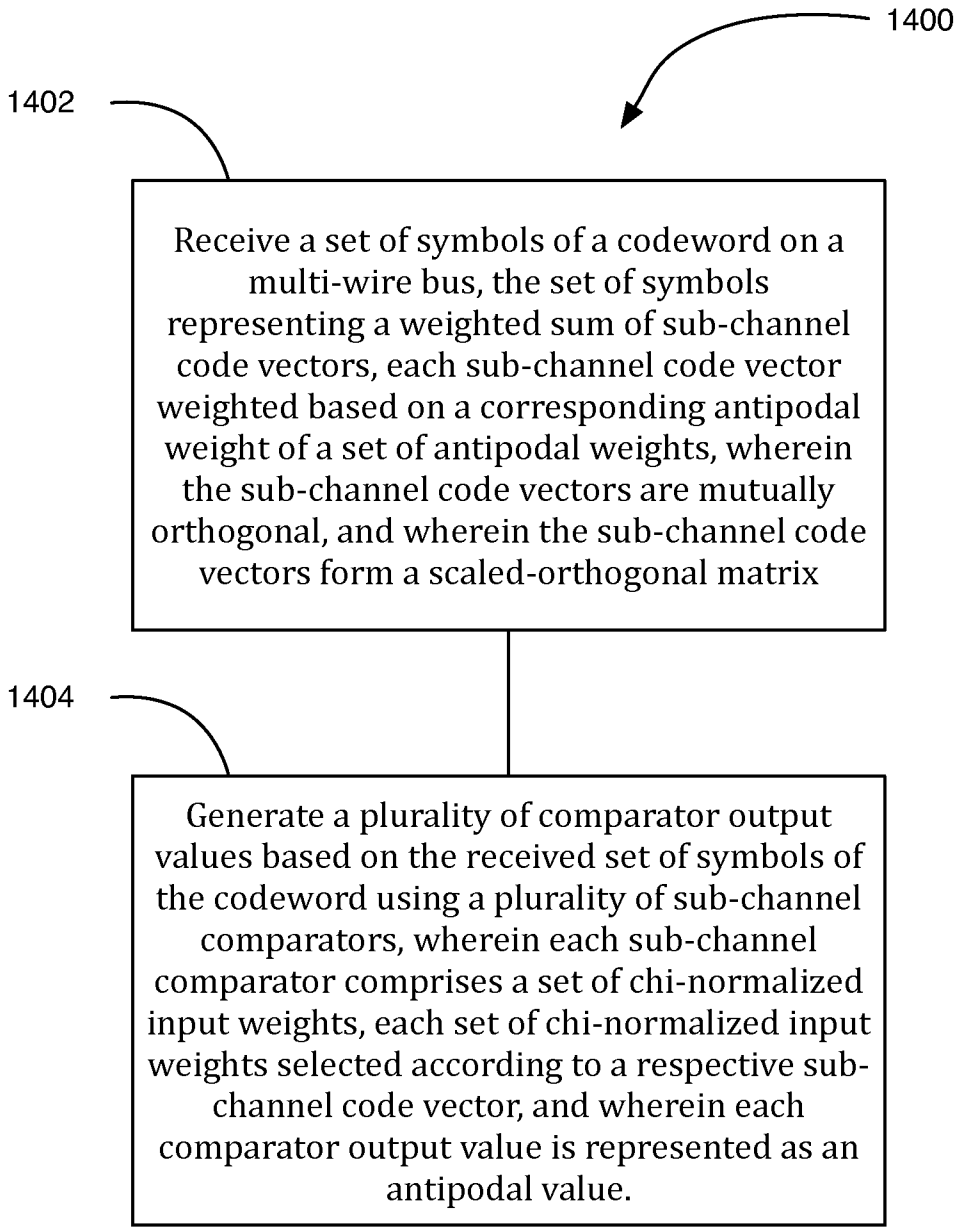

1400
1402
Receive a set of symbols of a codeword on a multi-wire bus, the set of symbols representing a weighted sum of sub-channel code vectors, each sub-channel code vector weighted based on a corresponding antipodal weight of a set of antipodal weights, wherein the sub-channel code vectors are mutually orthogonal, and wherein the sub-channel code vectors form a scaled-orthogonal matrix
1404
Generate a plurality of comparator output values based on the received set of symbols of the codeword using a plurality of sub-channel comparators, wherein each sub-channel comparator comprises a set of chi-normalized input weights, each set of chi-normalized input weights selected according to a respective sub-channel code vector, and wherein each comparator output value is represented as an antipodal value.

FIG. 14

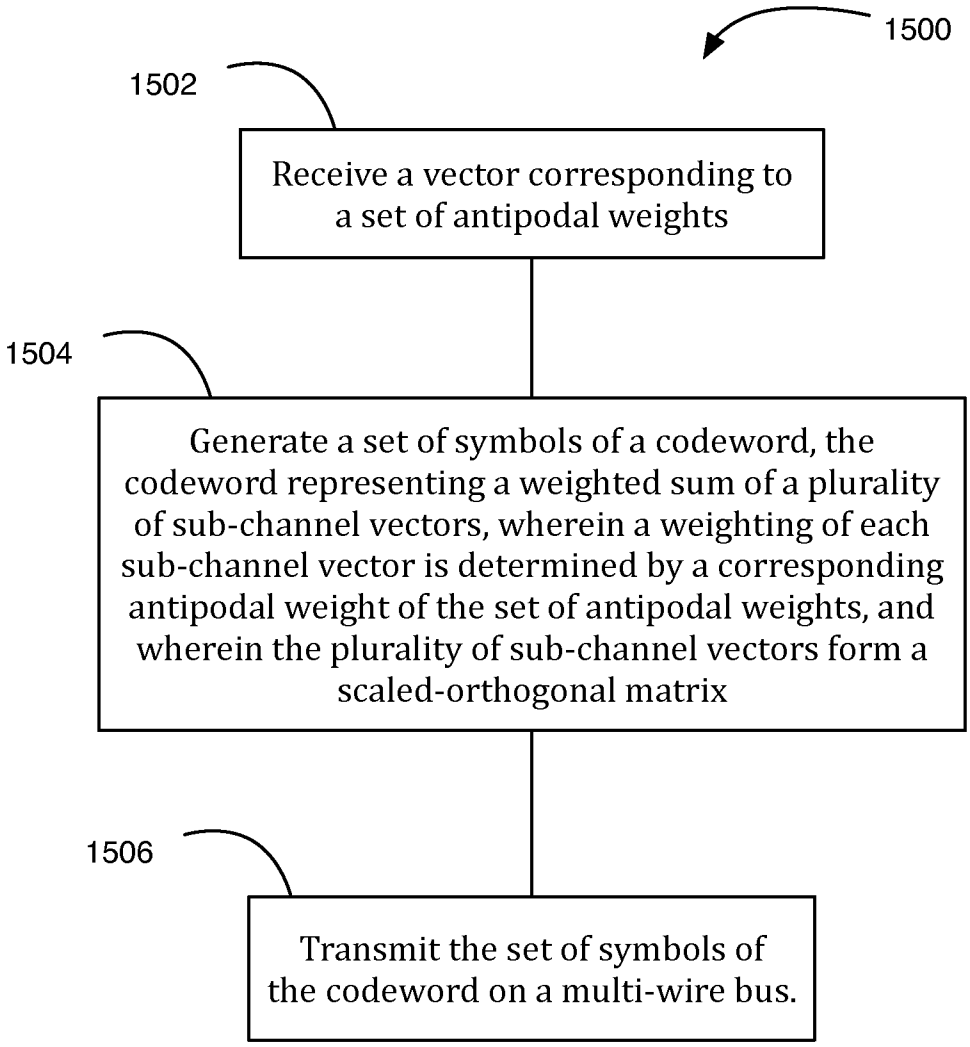

1500
1502
Receive a vector corresponding to a set of antipodal weights
1504
Generate a set of symbols of a codeword, the codeword representing a weighted sum of a plurality of sub-channel vectors, wherein a weighting of each sub-channel vector is determined by a corresponding antipodal weight of the set of antipodal weights, and wherein the plurality of sub-channel vectors form a scaled-orthogonal matrix
1506
Transmit the set of symbols of the codeword on a multi-wire bus.

FIG. 15