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## STRUCTURES WITH THROUGH-SUBSTRATE VIAS AND METHODS FOR FORMING THE SAME

### CROSS-REFERENCE TO RELATED APPLICATIONS

**[0001]** This application claims priority to U.S. Provisional Patent Application No. 63/216,389, filed June 29, 2021, titled “STRUCTURES WITH THROUGH-SUBSTRATE VIAS AND METHODS FOR FORMING THE SAME,” and to U.S. Provisional Patent Application No. 63/131,263 filed December 28, 2020, titled “STRUCTURES WITH THROUGH-SUBSTRATE VIAS AND METHODS FOR FORMING THE SAME,” the entire contents of each of which are hereby incorporated herein by reference.

### BACKGROUND

#### Field

**[0002]** The field relates to structures with through-substrate vias and methods for forming the same.

#### Description of the Related Art

**[0003]** Semiconductor elements, such as integrated device dies or chips, may be mounted or stacked on other elements. For example, a semiconductor element can be mounted to a carrier, such as a package substrate, an interposer, a reconstituted wafer or element, or other semiconductor element. As another example, a semiconductor element can be stacked on top of another semiconductor element, *e.g.*, a first integrated device die can be stacked on a second integrated device die. In some arrangements, a through-substrate via (TSV) can extend vertically through a thickness of the semiconductor element to transfer electrical signals through the semiconductor element, *e.g.*, from a first surface of the semiconductor element to a second opposing surface of the semiconductor element. There is a continuing need for improved methods of forming TSVs.

### BRIEF DESCRIPTION OF THE DRAWINGS

**[0004]** Specific implementations will now be described with reference to the following drawings, which are provided by way of example, and not limitation.

**[0005]** Figures 1A-1F show conventional processing steps for forming TSVs in an element.

**[0006]** Figure 2 shows an etch depth map of a processed wafer.

**[0007]** Figures 3A and 3B are example wafer maps of etched wafers.

**[0008]** Figures 4A-4I illustrate a method for forming a microelectronic structure, according to various embodiments.

**[0009]** Figures 5A-I illustrate a method for forming a microelectronic structure, according to various embodiments.

**[0010]** Figures 6A-6H illustrate a method for forming a microelectronic structure, according to various embodiments.

#### DETAILED DESCRIPTION

**[0011]** Figures 1A-F illustrate various conventional processing steps for forming TSVs in a microelectronic structure. Conventionally, the formation of TSVs can be performed using via-middle or front side via-last processing methods. Both of these methods are high volume manufacturing processes for different dies, including e.g. 40 um thick dies. Both of these processes involve etching through the TSVs into the bulk silicon after integrated circuit fabrication. Technical challenges of these processes increase with a reduction in the die thickness. These challenges can include TSV etch uniformity, die thickness uniformity, and the overall quality of the backside dielectric layer that is formed.

**[0012]** In Figure 1A, the microelectronic structure comprises a portion of a semiconductor wafer 102. The illustrated via structures comprise via-middle structures in which active circuitry 106, e.g., transistors or other active circuit elements, can be formed on or in the active surface of a bulk semiconductor portion 102, one or more insulating layers 112 and 113 can be formed over the active circuitry 106, and an opening 104 for the TSV can be formed through the one or more insulating layers 112 and 113 and a portion of the bulk semiconductor portion 102. In some arrangements, a metallization layer 110, for instance a back-end-of line (BEOL) or redistribution layer (RDL), can be provided over or within one or more insulating layers.

**[0013]** In Figure 1B, a via structure 108 can be provided. The via structure 108 can extend into the opening and over insulating layers 112 and 113. In Figure 1C, a

conductive pad 114 can be provided over one or more of the insulating layers and electrically connected to the metallization layer 110. Conductive overburden from electroplating the via structure 108 in Figure 1B can be removed (*e.g.*, polished away) in Figure 1C. As shown in Figure 1D, a conductive pad 117 can be provided over the one or more insulating layers 112 and 113 and electrically connected to the via structure 108. The conductive pad 117 can also be configured to electrically connect to another element. In some arrangements, the conductive pad 117 can be part of a BEOL or RDL.

**[0014]** As shown in Figure 1E, a frontside of the microelectronic structure 114 can be attached to a carrier 120 by way of an adhesive 118. The carrier 120 can comprise a temporary handle wafer that is used to support the microelectronic structure 114 during processing. In some embodiments, the adhesive 118 can comprise an organic adhesive and can be sensitive to high temperatures. Accordingly, the use of the adhesive 118 to attach the carrier 120 to the microelectronic structure 114 may limit the temperatures that can be applied during processing. In other embodiments, however, the carrier 120 can be directly bonded to the frontside of the microelectronic structure 114 without an adhesive 118. While the frontside 114 is attached to the carrier 120, the backside of the semiconductor portion 124 can be grinded or ground down to expose the vias 108. As shown in Figure 1F, a dielectric layer 122 may be deposited on the back side surface of the semiconductor 124. A backside metallization layer 116, for instance a back-end-of line (BEOL) or redistribution layer (RDL), can be provided over the dielectric layer 122 and can be configured to electrically connect to the via structure 108.

**[0015]** The conventional via formation process has several problems that lead to non-uniform via lengths. For example, the etch process used to form the openings for the vias is non-uniform across the substrate, *e.g.*, wafer, particularly for the high aspect ratio openings used for vias, which leads to via openings having different depths. This non-uniformity in produced vias causes yield loss during the TSV reveal process. Moreover, dielectric deposition, which is part of the TSV reveal process, may be limited by the temporary bond material used to adhere the die to a carrier. The adhesive limits the backside dielectric deposition temperature and can cause various processing complications. Furthermore, temporary bond layer thickness non-uniformity can add to the thinned silicon wafer thickness uniformity. Indeed, as shown in Figure 2, for a 12 inch wafer, the etch

process that is used to form the via openings can have a non-uniformity of approximately 7 microns. In some areas of the wafer, the etch depth may be higher 202, while some areas of the wafer will have low etch depths 206, other areas of the wafer will have etch depths 204 between the low 206 and high 202 etch depths. The varying depth of the via openings leads to different via structure lengths once the conductive material, for instance copper, is filled into the openings.

**[0016]** As shown in Figure 3A, the different via lengths can lead to a significant loss in yield. This loss of thickness, for example, when combined with wafer thickness variations caused by the temporary processes can further decrease the TSV yield. For instance, dies that have TSVs that are too short 304 to be effective and dies that have TSVs that are too long 302 to be effective may not be used. For example, some dies within the wafer may have TSVs that are too long 302 and break off during grinding or polishing. Other vias are too short 304 and are buried in the semiconductor portion of the device. Additionally, in some processes, non-uniform TSVs may result from incomplete or non-uniform plating procedures. For example, in such processes, the via openings may be etched uniformly, but the plating process through the high aspect ratio openings may not uniformly fill the via openings. This process variation reduces the number of dies that are effective 306. Accordingly, non-uniform TSV lengths may result from a variety of different processing methods.

**[0017]** Figure 3B illustrates the thickness variation on an 8" wafer that can be measured after TSV planarization. As can be seen, the thickness of the wafer can vary by 4 microns. Some regions of the wafer can have a thickness of up to 58.09 microns, while other regions of the wafer can have a thickness of 56.09 microns, while other regions of the wafer can have lower thicknesses around 54.67 microns. Wafer thickness variation can also cause some TSVs to be rendered ineffective and lead to lower levels of process control.

**[0018]** As explained above, due to, *e.g.*, die thickness non-uniformity and TSV opening etch non-uniformity, the lengths of the TSVs may vary considerably across the wafer after grinding the backside of the semiconductor portion to reveal the TSVs. Accordingly, as the backside of the bulk semiconductor portion is ground or otherwise thinned, the exposed vias may protrude from the backside of the thinned semiconductor portion by varying lengths and some vias, as explained above, may remain unexposed and

buried in the semiconductor portion. To reduce the non-uniform lengths of the TSVs while preventing breakage of the protruding TSVs, one or more backside dielectric layers can be provided over the backside of the semiconductor portion and over the TSVs. While it may be possible to employ solder bumping despite some degree of TSV height variability, the variability leads to a lack of levelness and makes stacking difficult. Some stacking technologies, such as direct hybrid bonding, are especially sensitive to topographical variations.

**[0019]** For example, in some processes, about 6 to 7 microns of the TSV protrudes from the backside of the semiconductor portion after initial backside silicon grinding and selective removal of silicon relative to the liner of the TSV by wet or dry etching methods. A barrier layer, *e.g.*, a dielectric barrier layer, such as silicon nitride, silicon oxynitride, silicon carbonitride, diamond-like carbon, or any other suitable dielectric barrier material layer, can be deposited over the backside of the semiconductor portion, over a sidewall of the exposed TSVs, and over the exposed end surfaces of the exposed TSVs. A second dielectric layer, such as silicon oxide or any other suitable dielectric, can be deposited over the dielectric barrier layer, including over the upper surface of the barrier layer, over the portion of the barrier layer that extends along the sidewall of the exposed TSVs, and over the portion of the barrier layer that is disposed along the end surface of the exposed TSVs. After depositing the backside dielectric layer(s), the vias and portion(s) of the dielectric layer(s) can be polished, or otherwise removed, to planarize the vias and reduce non-uniformities.

**[0020]** In other processes, thinner layer(s) of the first dielectric barrier layer and/or the second dielectric barrier layer may be deposited over the thinned semiconductor portion and the vias. For example, in other processes, the dielectric layer(s) may be only 1 or 2 microns thick, *e.g.*, significantly thinner than the length of the protruding portions of the vias. When the vias and dielectric layer(s) are polished, some of the vias may break off, such that the ends of the vias are embedded in the semiconductor portion and recessed relative to the backside of the semiconductor portion. Broken TSVs can reduce device yield.

**[0021]** In some of these processes, the chosen metal within the TSVs can lead to significant changes in TSV performance. For instance, in some processes, copper (Cu) can be an effective deposition metal. Copper, when used in TSVs, is an alloy metal that may be used and may change expansion and polishing characteristics of the TSV. Copper at the

bottom of the etch via may be generally confined and may not anneal at the same rates or the same temperatures as free copper. These different properties can lead to a Cu TSV that does not have a stabilized crystallography prior to the revealing of the TSV in the deposition processes. Furthermore, TSV metallization may include metallic or organic impurities that are unsuitable for reliable direct bonding by, for example, Direct Bond Interconnect® processes. Furthermore, shrinkage of TSVs during storage or thermal processing has been shown to cause topographical issues, e.g. the formation of rims or trenches, in the isolation oxide which may surround the TSV.

**[0022]** Some major issues that reduce the yield of conventional TSV formation processes include non-uniformity in TSV etch depths and TSV breakage during polishing. TSV can have a typical depth variation of 2 to 4 um over a 300 mm wafer out of a total of a 55 um depth. This variation in depth may create challenges for achieving uniform surface bonding. Moreover, non uniform TSVs can cause breakage during processing leading to lower yields. Silicon wafers may be planarized using chemical mechanical processing (CMP) planarization. Some TSVs may be broken off during CMP planarization. This breaking may be in part caused by excessive TSV reveal which often is caused by the depth variation in TSVs.

**[0023]** Conventionally, backside TSV processing has not been used for direct bonding in high volume manufacturing. Conventional procedures for planarizing TSVs on the back side of wafers may also rely on patterning copper pads and adding solder bumps to the wafers. Conventional backside processing also does not protect against breaking off of TSVs and may not achieve planarity suitable for direct bonding. These processes may not be suitable for high volume manufacturing because of the length of polishing time, the number of polish cycles – which may range from 4 to 6 cycles and take up to 2 hours of machine time, the amount of material that is deposited (5 um), the amount of material removed (2-4 um depending on the oxide deposited), and the total annealing time used between polishes (3-5 one hour annealing cycles).

**[0024]** Various embodiments disclosed herein can improve device yield by ensuring that TSV length is uniform throughout the thinned wafer. Some embodiments may use a copper wet etch to lower the copper TSV surface up to a few microns below the silicon surface. In some embodiments, surrounding silicon bulk will help to restrain and stabilize

the copper within the TSVs. In some embodiments, barrier layers are deposited before the deposition of copper seed layers. In some embodiments electroplating techniques are used to fill the vias. In some embodiments, some TSVs may be deeper than other TSVs and electroplating processes may be used to accommodate broken TSV additional depths.

**[0025]** In some embodiments, the annealing processes stabilize the copper plug material so as to provide it with similar chemical and structural properties as device-side copper used for bonding. In some embodiments, the annealing processes stabilizes the copper plug material to have the same impurity and texturing characteristics of the device side bonding copper. In some embodiments, plated copper can be annealed as a direct bonding interface. This annealing may stabilize the copper plug material, making the plug material chemically and physically resemble the device side direct bonding interface copper pad.

**[0026]** In some embodiments, CMP used on the copper layers can comprise a standard direct bond interface CMP slurry and process. In some embodiments, the CMP for TSVs can be the same as the device side CMP in terms of slurry usage and machine time. In some embodiments, the CMP parameters may be the same or similar to the device side CMP parameters. In some embodiments, this CMP uniformity can be achieved with or without the use of additional photolithography steps. In some embodiments, the only photolithography steps that are used during the CMP process may be blanket backside processing.

**[0027]** Figures 4A-4I illustrate a method for forming a microelectronic structure, according to one embodiment. As shown in Figure 4A, and as explained above, TSV structures 410 can be provided at least partially through a thickness of substrate that includes a bulk semiconductor portion 404. In some embodiments, the bulk semiconductor portion 404 can comprise silicon, germanium, silicon carbide or any other suitable semiconductor material. One or multiple lining layers 412 can be provided in the openings from a front surface 406 of a substrate. The one or more lining layers 412 can comprise a dielectric liner 415 in some embodiments. The dielectric liner 415 of the one or more lining layers 412 can comprise silicon nitride, silicon oxynitride, silicon carbonitride, diamond-like carbon, and any other suitable dielectric material. In some embodiments, the one or more lining layers 412 can additionally or alternatively include a first lining barrier layer 413. Although Figure 4A schematically illustrates the layer 412 as a single layer, it should be appreciated that the

layer 412 can comprise multiple layers or sub-layers, including, *e.g.*, a dielectric liner 415 and a lining barrier layer 413. A first conductive via 402 can be provided in the openings over the lining layer(s) 412. In some embodiments the first conductive via 402 can comprise copper, although other suitable metals may be used. The first conductive via portion 402 can be provided from the front surface of the substrate 406. The first lining barrier layer 413 can comprise a conductive barrier for reducing diffusion of the conductive via material. The first lining barrier layer 413 may be a different material from the conductive material of the first 402 and second 424 conductive via portions. The first lining barrier layer 413 may be configured to reduce diffusion of the conductive material of the first 402 and/or second 424 conductive via portions into the surrounding dielectric and/or semiconductor materials. Examples of materials used for the first lining barrier layer 413 include, metal and metal nitride materials, such as titanium nitride, tantalum nitride, and any other suitable metal and metal nitride material. The first conductive via portion 402 can be electroplated within the opening over a seed layer. The front surface or side of the wafer, *e.g.*, the first surface 406 may comprise an active side of the semiconductor portion with active integrated circuitry, such as transistors, formed in or on the active side. The front or first surface 406 of the wafer can be mounted to a carrier 414. The carrier 414 may serve as a temporary handle wafer in some embodiments. In some embodiments, the microelectronic structure can be attached to the carrier 414 with an adhesive. In other embodiments, the microelectronic structure can be directly bonded to the carrier 414 without an intervening adhesive, using the direct bonding techniques described in more detail below. As shown in Figure 4A-C, the TSVs 410 can have variable heights across the substrate due to variable etching through a significant depth through bulk semiconductor.

**[0028]** In Figure 4B, the backside of the semiconductor portion, the second side, 408, also a back surface of the substrate at this stage, can be thinned, by dry etching or otherwise removed, to reveal the TSVs. 410. As shown, the TSVs 410 can protrude beyond the backside of the semiconductor portion 408. As explained above, the lengths of the TSVs 410 may be non-uniform across the wafer, such that the TSVs 410 protrude by varying lengths above the semiconductor portion 416. The etch process may leave the via structures 410 intact, such that the one or more lining layer(s) 412, including dielectric liner 415 and first lining barrier layer 413, remain disposed over and along a sidewall 411 of the first

conductive via portion. In Figure 4C, one or more dielectric layers 418 can be provided, *e.g.*, deposited, over the upper surface 408 of the bulk semiconductor portion 416, along sidewalls 411 of the via structures 410, and over end surfaces of the via structures 410 to define a back surface of the substrate 408. Although Figure 4C schematically illustrates the layer 418 as a single layer, it should be appreciated that the layer 418 can comprise multiple layers or sub-layers. In various embodiments, dielectric layer(s) 418 can be a first dielectric barrier layer 419 provided on the bulk semiconductor portion 416 and on the via structure 410. The dielectric layer(s) 418 can further comprise a second dielectric layer 421 over the first dielectric barrier layer 419. In various embodiments, the first dielectric barrier layer 419 can comprise a material to reduce copper migration, such as, *e.g.*, silicon nitride, silicon oxynitride, silicon carbide, silicon carbonitride, diamond-like carbon (DLC), or any other suitable dielectric barrier layer material. The second dielectric layer 421 can comprise a lower k dielectric material, and can be an inorganic dielectric, such as silicon oxide. As shown in Figure 4C, the TSVs 410 can protrude beyond the semiconductor portion 408 by a distance in a range of about 0 to 10 microns, 1 to 7 microns, or 5 to 6 microns. Further as explained herein, the TSVs 410 can break off, as seen in TSV 420, and be recessed within the semiconductor portion 416 and/or the dielectric layer(s) 418 by a distance in a range of 0 to 10 microns, 1 to 7 microns, or 2-6 microns. The thickness of the dielectric layer(s) 418 can be in a range of about 2 to 7 microns, in a range of about 3 to 7 microns, or in a range of 4 to 6 microns, or about 5 microns in one embodiment.

**[0029]** In Figure 4D, the via structures 410 and dielectric layer(s) 418 can be planarized, for example, using a chemical-mechanical polishing (CMP) process applied to the back surface of the substrate 408. As explained herein, the planarization process may break off one or more of the TSVs 410, for instance the middle TSV 420. In Figure 4D, for example, the middle TSV 420 is shown as having broken off such that the TSV 420 is embedded within and recessed below the surface of the dielectric layer(s) 418 and/or semiconductor portion 416. As explained above, broken TSVs, like the middle TSV 420, can reduce device yield for the wafer. Depending upon selected chemistries for the CMP slurry, some or all other TSV's 410 may also be recessed below dielectric layer(s) and/or semiconductor portion.

**[0030]** In Figure 4E, the first conductive via portion 402 can be selectively etched so as to be recessed below the back surface of the substrate 408, *e.g.*, below the dielectric layer(s) 418 and/or the semiconductor portion 408. Because the middle TSV 420 broke off, the depth of the etch for the middle via structure 420 is deeper than the etch for the other via structures 410. In various embodiments, a selective copper wet etch can be performed to etch only a portion of the first conductive via portion 402. Advantageously, in the illustrated embodiment, all of the TSVs 410 across the substrate 416 are recessed to some degree, at least below the upper surface of the added dielectric layer(s) 418. In other embodiments, recessing of the TSVs 410 can be accomplished during the CMP described above with respect to Figure 4D. In still other embodiments, not all TSVs 410 are recessed, and only some TSVs 410 are recessed, whether or not a separate recessing process is employed. For example, in some embodiments, a conventional CMP process is employed in which some TSVs 410 are substantially recessed below the surface 408, *e.g.*, due to breaking off.

**[0031]** As shown in Figure 4F, to improve yield and to provide a planarized, high quality bonding surface, a second barrier layer 422 can be provided over the exposed end surface of the first conductive via portions 402 and along the lining barrier layer 412. A seed layer (not illustrated) can be provided over the second barrier layer 422, and a second conductive via portion 424 can be provided, by for instance, electroplating, over the second barrier layer 422 from the back surface of the substrate 416. The microelectronic structure can be annealed, which can beneficially promote grain growth to improve direct bonding. Advantageously, the deposition process, for instance, electroplating, and an anneal process can both be selected to prepare for direct hybrid bonding, as opposed to the plating process that was used to fill the TSV 410 vias in the first place, which is selected to improve filling of high aspect ratio, deep vias.

**[0032]** In various embodiments, alloying additives can be provided to the conductive material of the TSV 410. The alloying additives can be provided to control thermal expansion and/or improve corrosion resistance of the conductor. In some embodiments, the conductor is copper, silver, gold, or any other suitable conductive material. The alloying additive material(s) can include metallic elements, for example, beryllium, indium, gallium, nickel, and manganese, typically representing less than 5 atomic % and more particularly less than 2 atomic % of the TSV 410. The alloying additive may be provided as

part of the seed layer or the second barrier layer 422 and diffuse therefrom. Such alloying elements can be present in different amounts to affect the TSV 410 hardness, corrosion resistance and/or to pin grain formation during subsequent anneal. Because larger grains are desirable in the second conductive portion to aid interdiffusion in a direct metal-to-metal bonding process, the first conductive portion 402 may contain a smaller percentage of the alloying elements as compared to the second conductive portion 424. For example, in some embodiments, the second conductive via portion 424 can have at least 5% less, at least 10% less, at least 15% less, or at least 20% less of the alloying element(s) as compared to the first conductive via portion.

**[0033]** In addition, one or more organic additives, such as levelers, suppressors, accelerators, can be provided to the plating bath during formation of the TSV 410 to improve filling. In various embodiments, different additives and/or different proportions of additives, *e.g.*, fewer additives, may be provided when plating the second conductive via portion 424 as compared to the type or amount of additives used when plating the first conductive via portion 402 that fills the opening. For example, in some embodiments, additives may be used when plating both the first 402 and second 424 conductive via portions, but the amount of additives used for the first conductive via portion 402 may be substantially different than the amount used for the second conductive via portion 424. In some embodiments, more additives may be used when plating the first conductive via portion 402 than when plating the second conductive via portion 424. In some embodiments, additives, such as organic additives, may be provided during electroplating of the first conductive via portion 402 to, *e.g.*, improve filling, but different proportions or different types of organic additives may be provided during electroplating of the second conductive via portion 424. In various embodiments, the plating bath for the first conductive via portion 402 can include a higher percentage of organic additives as compared to the plating bath for forming the second conductive via portion 424. Accordingly, the first conductive via portion 402 may have a higher percentage of impurities, such as sulfur, oxygen, nitrogen, and/or carbon, as compared to the second conductive via portion 424. In various embodiments, the first conductive via portion 402 can be formed in a plating bath have a higher concentration of leveler, *e.g.*, Janus Green, which introduces more impurities, such as nitrogen, carbon, and/or oxygen, as

compared to the second conductive via portion 424. In both portions 402 and 424, the impurities from additives may be measured in part per million (ppm).

**[0034]** After electroplating, impurities from the plating additives, *e.g.*, carbon, nitrogen, sulfur, oxygen, amongst other impurities, may be incorporated in the first 402 and/or second 424 conductive via portions. In some embodiments, the amount of impurities present in the first conductive via portion 402 may be more than the amount of impurities present in the second conductive via portion 424. In some embodiments, only trace amounts of the impurities may be present in the second conductive via portion 424. Further, the impurities present in the second conductive via portion 424 can have a different composition and/or concentrations compared to the first conductive via portion 402. These compositions may be selected to influence the grain size, orientation or thermal stability of the interconnect that can be formed by the second conductive portion. Impurities can include other material elements present within the conductive vias with concentrations less than 2 atm. %, *e.g.*, less than 100 ppm or less than 50 ppm. In one embodiment, the impurities in the second conductive via portion 424 can be less than the impurities in the first conductive via portion 402. For example, in some embodiments, the second conductive via portion 424 can have at least 5% less, at least 10% less, or at least 20% less non-copper elements (*e.g.*, such as metallic alloying elements, or impurities from plating bath additives) than the first conductive via portion 402.

**[0035]** In Figure 4G, portions of the second conductive via portion 424 and the second barrier layer 422 that overlie the dielectric layer 418 can be removed, for example, using a CMP process applied to the back surface of the substrate. The polishing process can expose and planarize the dielectric layer(s) 418, and can serve as a preparatory step for direct bonding, *i.e.*, a very high degree of polishing accomplishes planarity sufficient for direct bonding. Beneficially, the middle broken TSV 420 has been repaired, the metal recess is provided at a suitable depth, and the polished dielectric layer(s) 418 and second conductive via portions 424 can be used in a direct bonding process. For example, the plating and annealing process can form grains, *e.g.*, copper, gold, or silver grains, or metal texture, *e.g.*, copper, oriented along a 111 crystal plane primarily perpendicular to the bond surface, which can enhance metal diffusion and bonding during a direct bonding process. In various embodiments, the metal texture can be oriented so as to have a geometric component that is

generally perpendicular to the bond surface. In some embodiments, the second conductive via portion 424 can have a first proportion of 111 planes oriented within 30° of vertical, *e.g.*, within 30° of a vertical axis extending along a longitudinal dimension of the via structure, within 20° of vertical, or within 10° of vertical. The second conductive via portion 424 can have a second proportion of 111 planes oriented within 30° of vertical, *e.g.*, within 30° of a vertical axis extending along a longitudinal dimension of the via structure, within 20° of vertical, or within 10° of vertical. In some embodiments, the second proportion can be greater than the first portion. In the illustrated embodiment, where either CMP selection, see Figure 4D and corresponding description, or subsequent recessing, see Figure 4E and corresponding description, are selected to ensure some degree of recessing across the substrate, each TSV 410 may include both first 402 and second 424 conductive via portions. In other embodiments, not all TSVs 410 are recessed across the substrate at the stage of Figure 4E, and only some TSVs 410 include the second conductive via portion 424. In any case, the CMP process selected to achieve the structure of Figure 4G can be selected to facilitate subsequent direct hybrid bonding. Accordingly, each of the TSVs 410 may be recessed below the dielectric layer(s) 418 upper surface, for example, by less than 40 nm, less than 30 nm, less than 20 nm, less than 15 nm or less than 10 nm, but more than or equal to about 5 nm, *e.g.*, more than or equal to about 2 nm.

**[0036]** As shown in Figure 4H, the microelectronic elements described above can be utilized in a multi-die or multi-element stack. For example, a first stacked die 434 can be directly bonded to a base wafer 432 without an adhesive. In some embodiments, the front active surface can be bonded to the base wafer. As explained below, contact pads 426 of the first die can be directly bonded to contact pads 426 of the wafer without an adhesive, and nonconductive regions can be directly bonded to corresponding nonconductive regions of the wafer without an adhesive 430. Additional devices can be stacked and directly bonded to the backside of the microelectronic structure. For example, as shown contact pads 426 of a second element or die 436 can be directly bonded to the exposed TSV structures 410 of the first element 434 without an adhesive. Nonconductive regions of the second element or die 436 can be directly bonded to the dielectric layer(s) 418 without an adhesive. Additional elements can be directly bonded to the second element or die to form any number of elements in the stacked and directly bonded structure. In some other applications, processed wafers

with the methods described herein may be assembled or stacked and directly bonded to each other without an intervening adhesive layer.

**[0037]** Figure 4I illustrates the via structure 410 formed using various disclosed embodiments. As shown, the microelectronic structure can include a bulk semiconductor portion 404 having a first/front surface 406 and a second/back surface opposite the first surface 408. In some embodiments, the second surface 408 can comprise an active surface having active circuitry formed in or on the second surface. Additionally or alternatively, in some embodiments, the first surface 406 may comprise an active surface having active circuitry formed in or on the second surface. In other embodiments, the first surface 406 may comprise an inactive surface devoid of active circuitry. The via structure 410 can be disposed in an opening extending at least partially through, *e.g.*, completely through, the bulk semiconductor portion 404 along a direction non-parallel to the first surface. The via structure can include a first conductive via portion 402, a second conductive via portion 424, and a second barrier layer 422. The second barrier layer 422 includes a first portion 440 disposed between the first conductive via portion 402 and the second conductive via portion 424. The second barrier layer 422 can also include a second portion 442 disposed along the sidewall 411 of the second conductive portion 402. The second conductive via portion 424 can extend from the second barrier layer 440 to at least the surface of the substrate 408. As noted above, the second conductive via portion 424 can have a different composition from the first conductive via portion 402.

**[0038]** Both the first 402 and second 424 conductive via portions can be formed of copper, for example, but have different types and/or concentrations of alloying elements and impurities, *e.g.*, originating from the types of levelers, suppressors, accelerators, plating current densities, used in the electroplating process, and/or different grain sizes and/or orientations. For example, the first 402 and/or second 424 conductive via portion can have different proportions of non-copper elements, such as metallic alloying elements, or impurities from plating bath additives. The first via portion 402 can have more non-copper elements than the second 424 via portion. In some embodiments, the first via portion 402 can have alloying elements, such as Be, Mn, Ni, incorporated via diffusion from the barrier layer 412 or via the seed layer. The second via portion 424 may not have such non-copper elements, or only trace levels of such impurities. The second via portion 424 may have such

non-copper elements but a smaller amount as compared to the first via portion. The alloying material(s) incorporated via the barrier layer(s) 412 and/or the seed layer during plating can be provided in some arrangements to pin grains of the first via portion 402. In addition, one or more organic additives can be provided during plating of the first via portion 402 to improve filling, and the additive may not be used in the second 424 conductive via portion. In other embodiments, the organic or other additives may be provided for both the first 402 and second 424 via portions, but the first via portion 402 may have higher concentrations of impurities left by the additives after plating. As explained herein, impurities such as sulfur, oxygen, carbon, or nitrogen may be present in the TSVs 410 in higher concentrations in the first via portion 402 as compared to the second via portion 424. In some embodiments, the non-copper elements, including alloying elements and impurities from additives, composition in the first conductive via portion 402 is higher than those in the second conductive via portion 424. For example, in some embodiments, the second conductive via portion 424 can have at least 5% less, at least 10% less, at least 15% less, or at least 20% less of the non-copper elements, as compared to the first conductive via portion 402. The composition and grain structure of the first conductive portion 402 can be the result of processing selected to optimize filling of deep, high aspect ratio vias, wherein the composition and grain structure of the second conductive portion 424 can be selected to optimize subsequent direct hybrid bonding.

**[0039]** As shown in Figure 4I, a dielectric layer 418 can be disposed on the bulk semiconductor portion 404, with the second 424 conductive via portion extending through the dielectric layer 418 such that an end of the second conductive via portion 424 is flush with an upper surface of the dielectric layer 418, or is slightly recessed relative to the upper surface of the dielectric layer 418, e.g., by less than about 40 nm, by less than about 30 nm, by less than about 20 nm, by less than about 10 nm, or by less than about 5 nm. The dielectric layer 418 can include a planarized dielectric bonding layer configured for direct bonding to another element. The dielectric layer 418 can further comprise a dielectric barrier layer on the bulk semiconductor portion 404, the planarized dielectric bonding layer disposed on the dielectric barrier layer. A first lining barrier layer 412 can extend along a sidewall 411 of the first 402 and second 424 conductive portions. As shown, the second barrier layer 440 can include a second portion 442 extending along the first barrier layer 412 between the first

barrier layer 412 and the second conductive via portion 424. Thus, the overall barrier thickness is greater between the second conductive portion 424 and the bulk substrate 404, as compared to that between the first conductive portion 402 and the bulk substrate 404, and may include two identifiable barrier layers, which may or may not have different compositions.

**[0040]** Figures 5A-5I illustrate a method for forming a microelectronic structure, according to another embodiment. Unless otherwise noted, the embodiment of Figures 5A-5I may be the same as or generally similar to like components of Figures 4A-4I. For example, the steps of Figures 5A-5E may be the same as those set forth above in connection with Figures 4A-4E. In Figure 5F, however, there may not be a barrier layer provided over the first conductive via portion 410. Rather, the second conductive via portion 424 may be plated directly onto the first conductive via portion 410, or onto an intervening seed layer only, and the bulk semiconductor portion 416 without an intervening barrier layer. As explained above, the structure of Figure 5F may be annealed, which can promote copper grain growth that is conducive to direct bonding.

**[0041]** In various embodiments, the buried conductive material of the first conductive via portion 402 may be more constrained than the upper portions of conductive material of the second conductive via portion 424. During annealing, the first 402 and second 424 conductive via portions can form different metal textures and/or have different concentrations of non-copper elements, such as alloying elements and/or impurities from plating additives. For example, a first metal texture of the first conductive via portion 402 can be different from a second metal texture of the second conductive via portion 424. In various embodiments, including the embodiments disclosed in Figures 4A-4I and 5A-5I, the crystal structure of the second conductive via portion 424 can have grains oriented vertically along a 111 crystal plane non-parallel to, *e.g.*, generally perpendicular to, the bond interface to enhance metal diffusion, *e.g.*, copper diffusion, during direct bonding. The grains can have geometric components that are generally perpendicular to the bond interface. In some embodiments, the first 402 and second 424 conductive via portions can comprise different metals or different alloys. For example, in some embodiments, the first conductive via portion 402 can comprise a copper alloy, and the second conductive via portion 424 can comprise substantially pure copper.

[0042] Figures 5G and 5H may be generally similar to the steps set forth in Figures 4G and 4H. Figure 5I illustrates the microelectronic structure without the intervening barrier layer of Figure 4I. As shown in Figure 5I, the second conductive via portion 424 can be formed after and separately from the first conductive via portion 402. Unlike in Figure 4I, there is no intervening barrier layer 440 between the first conductive via portion 402 and the second conductive via portion 424.

[0043] Figures 6A-6H illustrate another embodiment that enables the formation of conductive vias 606 having generally uniform lengths, while avoiding degradation of the vias 606, *e.g.*, copper vias or other suitable conductive metal, and/or contamination of the semiconductor portion 604, *e.g.*, silicon or other suitable semiconductor. Unless otherwise noted, the components of Figures 6A-6H may be generally similar to the components of Figures 4A-5I. For example, as explained above, and as shown in Figure 6A, a semiconductor element 604, *e.g.*, a semiconductor wafer, can have a plurality of conductive vias 606 formed in a semiconductor portion 604, *e.g.*, a silicon bulk or device portion. The front side of the bulk semiconductor 610 is shown facing upwardly, and the opposite back side of the bulk semiconductor 612 is shown facing downwardly. In various embodiments, the front side 610 can comprise an active side of the semiconductor element, such that active circuitry can be formed at or near the front side 610. A dielectric liner and/or a barrier layer 608 can line the openings in which the vias 606 are disposed. One or more frontside dielectric layer(s) 602 can be provided over the front side of the semiconductor portion 610. Although Figure 6A schematically illustrates the layer 602 as a single layer, it should be appreciated that the layer 602 can comprise multiple layers or sub-layers. The frontside dielectric layer(s) 602 can comprise any suitable type of dielectric material(s), including, *e.g.*, silicon oxide, silicon nitride, silicon oxynitride, silicon oxycarbonitride, diamond-like carbon (DLC), and any other suitable dielectric material.

[0044] As explained above, the depth of the openings in which the conductive via 606 material is deposited, *e.g.*, electroplated, may vary which can lead to the formation of vias having non-uniform lengths. The lack of uniformity can make it challenging to reveal the vias from the back side of the semiconductor element 612. Indeed, the etch variation of the via openings 606 can be on the order of 2-3 microns or more, such that there may be a 50% or more variation in TSV heights. In the process of Figures 4B and 5B, the

semiconductor portion 604 is dry etched to expose the vias 606, which may protrude above the semiconductor material 604 at different heights. However, dry etching a semiconductor material 604 such as silicon with an etchant such as SF<sub>6</sub> may cause severe erosion of the copper via material, particularly if the dielectric liner and/or the lining barrier layer 608 are etched before the via 606 is adequately revealed. Moreover, processing of the conductive vias 606, *e.g.*, by CMP, grinding, and other processing methods, may cause some of the conductive material of the via, *e.g.*, copper material, to contaminate the semiconductor portion 604, *e.g.*, silicon.

**[0045]** Accordingly, unlike the process of Figures 4B and 5B, in Figure 6B, the back side of the semiconductor portion 612 can be grinded and polished, *e.g.*, with CMP, to reveal the vias 606. The grinding and polishing processes can uniformly reveal the conductive vias 606, which can accommodate for the non-uniform lengths of the vias 606 before grinding and polishing. For example, the back side of the semiconductor element 612 can be grinded and polished until all of the vias 606 are revealed at the planarized, grinded and polished back side of the semiconductor element 614. Accordingly, in the illustrated embodiment, the grinding and polishing processes can be used to reveal vias 606 having a generally uniform length. In other embodiments, such as those described above in connection with Figures 4A-5I, it may not be desirable to utilize CMP to reveal the vias 606, since exposing the vias 606, which can comprise copper among other materials, to CMP may contaminate the semiconductor portion, *e.g.*, silicon. In such embodiments, as explained above, an etch process, *e.g.*, an SF<sub>6</sub> etch, can be used to initially reveal the vias 606.

**[0046]** Turning to Figure 6C, the conductive via 606 can be etched from the backside 614 to form an etched recess in the conductive material, which can comprise copper. For example, the conductive material can be etched at a depth in a range of 0.25 microns to 3 microns, in a range of 0.5 microns to 3 microns, *e.g.*, about 1 micron in an embodiment. In Figure 6D, a first backside dielectric layer 616 can be provided, *e.g.*, deposited, over the grinded and polished back side of the semiconductor portion 618 and into the etched recesses formed in the vias 620. As shown, the first backside dielectric layer 616 can extend within the recesses over the copper vias and abutting the dielectric liner and/or barrier layers disposed in the openings 620. In some embodiments, the first backside dielectric layer 616 can comprise a plurality of layers. For example, in the illustrated

embodiment, the first backside dielectric layer 616 can comprise a first dielectric layer 617, *e.g.*, a low temperature silicon nitride dielectric layer, disposed on the back side of the semiconductor portion and on the vias 606 and a second dielectric layer 619, *e.g.*, a low temperature silicon oxide dielectric layer, over the first dielectric layer 617. For example, in various embodiments, the first 617 and/or second 619 dielectric layers can be formed using a low-temperature chemical vapor deposition (CVD) process. In other embodiments, however, the first backside dielectric layer 616 can comprise only a single dielectric layer, or more than two dielectric layers.

**[0047]** Turning to Figure 6E, the back side of the semiconductor element 614 can be polished (*e.g.*, with CMP) to remove first portions of the first backside dielectric layer 616 that overlie the semiconductor portion 604 so as to expose the semiconductor portion 604. Second portions of the first backside dielectric layer 620 may remain disposed in the recess over the conductive vias 606 as shown in Figure 6E. The remaining second portion of the first backside dielectric layer 620 may serve to protect the conductive via material during a subsequent dry etch of the semiconductor portion 604, shown in Figure 6F. The dry etch of Figure 6F can accordingly uniformly reveal the vias 606, and the second portion of the first backside dielectric layer 620 can serve to protect the copper of the vias during the dry etch, *e.g.*, using SF<sub>6</sub>. Further, the step of Figure 6F can use an etchant, *e.g.*, SF<sub>6</sub>, that is highly selective to silicon over the first backside dielectric layer 620, which can include silicon oxide at the exposed surface. As shown after the dry etch of Figure 6F, therefore, the vias 606, first portion of the first backside dielectric layer 620, and dielectric liner/barrier layers 608 can protrude relative to an etched surface at the back side of the semiconductor portion 604. In various embodiments, the vias can protrude by an amount in a range of 3 microns to 4 microns.

**[0048]** Turning to Figure 6G, a second backside dielectric layer(s) 624 can be provided, *e.g.*, deposited over the etched surface 622 of the semiconductor portion 604, along sidewalls of the exposed lining layers of the vias 606, over end portions of the lining layers 608, and over the second portions of the first backside dielectric layer 620. In some embodiments, the second backside dielectric layer 624 can comprise a plurality of layers. For example, in the illustrated embodiment, the second backside dielectric layer can comprise a first dielectric layer 625, *e.g.*, a low temperature silicon nitride dielectric layer,

disposed on the etched surface of the semiconductor portion 622 and on the second portion of the first backside dielectric layer 620 and a second dielectric layer 627, *e.g.*, a low temperature silicon oxide dielectric layer, over the first dielectric layer 625. In other embodiments, however, the second backside dielectric layer 624 can comprise only a single dielectric layer, or more than two dielectric layers. A thickness of the second backside dielectric layer 624 can be any suitable thickness, *e.g.*, in a range of 4 microns to 5 microns in various embodiments. Beneficially, a thickness of one or both of the first 625 and second 627 backside dielectric layer(s) can be selected so as to provide adequate support or stress compensation, particularly for thinned dies.

**[0049]** As shown in Figure 6H, the back side of the semiconductor element can be polished (*e.g.*, with CMP) to expose the vias 606. In particular, the polishing can remove portions of the second backside dielectric layer 624 that are disposed over the first backside dielectric layer 616, the remaining second portion of the first backside dielectric layer 620, and can thin the portion of the second backside layer that overlies the semiconductor portion. Thus, in the structure of Figure 6H, the second backside dielectric layer 624 can be disposed over the etched surface 622 of the semiconductor portion 604 and can be about the via lining layer(s) 608, *e.g.*, the lining dielectric layer and/or lining barrier layer. In various embodiments, the polishing can also serve to recess the conductive material within the via 606 relative to the second backside dielectric 624 layer so as to prepare the back side of the semiconductor element for direct bonding. In various embodiments, the polishing can recess the conductive material by an amount in a range of 1 nm to 20 nm, or in a range of 1 nm to 10 nm. As explained above, the semiconductor element can be directly bonded and/or stacked to another element. The frontside dielectric layer(s) 602 can also be removed to expose the vias 606 at the front side, and one or more additional elements can be stacked on and directly bonded to the front side of the semiconductor element.

#### Examples of Direct Bonding Methods and Directly Bonded Structures

**[0050]** Various embodiments disclosed herein relate to directly bonded structures in which two elements can be directly bonded to one another without an intervening adhesive. Two or more semiconductor elements, such as integrated device dies, wafers, and other semiconductor elements, may be stacked on or bonded to one another to form a bonded structure. Conductive contact pads of one element may be electrically connected to

corresponding conductive contact pads of another element. Any suitable number of elements can be stacked in the bonded structure.

**[0051]** In some embodiments, the elements are directly bonded to one another without an adhesive. In various embodiments, a non-conductive or dielectric material of a first element can be directly bonded to a corresponding non-conductive or dielectric field region of a second element without an adhesive. The non-conductive material can be referred to as a nonconductive bonding region or bonding layer of the first element. In some embodiments, the non-conductive material of the first element can be directly bonded to the corresponding non-conductive material of the second element using dielectric-to-dielectric bonding techniques. For example, dielectric-to-dielectric bonds may be formed without an adhesive using the direct bonding techniques disclosed at least in U.S. Patent Nos. 9,564,414; 9,391,143; and 10,434,749, the entire contents of each of which are incorporated by reference herein in their entirety and for all purposes.

**[0052]** In various embodiments, hybrid direct bonds can be formed without an intervening adhesive. For example, dielectric bonding surfaces can be polished to a high degree of smoothness. The bonding surfaces can be cleaned and exposed to a plasma and/or etchants to activate the surfaces. In some embodiments, the surfaces can be terminated with a species after activation or during activation, *e.g.*, during the plasma and/or etch processes. Without being limited by theory, in some embodiments, the activation process can be performed to break chemical bonds at the bonding surface, and the termination process can provide additional chemical species at the bonding surface that improves the bonding energy during direct bonding. In some embodiments, the activation and termination are provided in the same step, *e.g.*, a plasma or wet etchant to activate and terminate the surfaces. In other embodiments, the bonding surface can be terminated in a separate treatment to provide the additional species for direct bonding. In various embodiments, the terminating species can comprise nitrogen. Further, in some embodiments, the bonding surfaces can be exposed to fluorine. For example, there may be one or multiple fluorine peaks near layer and/or bonding interfaces. Thus, in some embodiments, in the directly bonded structures, the bonding interface between two dielectric materials can comprise a very smooth interface with higher nitrogen content and/or fluorine peaks at the bonding interface. Additional examples of activation and/or termination treatments may be found throughout U.S. Patent Nos.

9,564,414; 9,391,143; and 10,434,749, the entire contents of each of which are incorporated by reference herein in their entirety and for all purposes.

**[0053]** In various embodiments, conductive contact pads of the first element can also be directly bonded to corresponding conductive contact pads of the second element. For example, a hybrid bonding technique can be used to provide conductor-to-conductor direct bonds along a bond interface that includes covalently direct bonded dielectric-to-dielectric surfaces, prepared as described above. In various embodiments, the conductor-to-conductor, *e.g.*, contact pad to contact pad, direct bonds and the dielectric-to-dielectric hybrid bonds can be formed using the direct bonding techniques disclosed at least in U.S. Patent Nos. 9,716,033 and 9,852,988, the entire contents of each of which are incorporated by reference herein in their entirety and for all purposes.

**[0054]** For example, dielectric bonding surfaces can be prepared and directly bonded to one another without an intervening adhesive as explained above. Conductive contact pads, which may be surrounded by nonconductive dielectric field regions, may also directly bond to one another without an intervening adhesive. In some embodiments, the respective contact pads can be recessed below exterior (*e.g.*, upper) surfaces of the dielectric regions or nonconductive bonding regions, for example, recessed by less than 30 nm, less than 20 nm, less than 15 nm, or less than 10 nm, for example, recessed in a range of 2 nm to 20 nm, or in a range of 4 nm to 10 nm. The nonconductive bonding regions can be directly bonded to one another without an adhesive at room temperature in some embodiments and, subsequently, the bonded structure can be annealed. Upon annealing, the contact pads can expand and contact one another to form a metal-to-metal direct bond. Beneficially, the use of hybrid bonding techniques, such as Direct Bond Interconnect, or DBI<sup>®</sup>, available commercially from Xperi of San Jose, CA, can enable high density of pads connected across the direct bond interface, *e.g.*, small or fine pitches for regular arrays. In some embodiments, the pitch of the bonding pads, or conductive traces embedded in the bonding surface of one of the bonded elements, may be less than 40 microns or less than 10 microns or even less than 2 microns. For some applications the ratio of the pitch of the bonding pads to one of the dimensions of the bonding pad is less than 5, or less than 3 and sometimes desirably less than 2. In other applications the width of the conductive traces embedded in the bonding surface of one of the bonded elements may range between 0.3 to 3 microns. In various

embodiments, the contact pads and/or traces can comprise copper, although other metals may be suitable.

**[0055]** Thus, in direct bonding processes, a first element can be directly bonded to a second element without an intervening adhesive. In some arrangements, the first element can comprise a singulated element, such as a singulated integrated device die. In other arrangements, the first element can comprise a carrier or substrate (*e.g.*, a wafer) that includes a plurality, *e.g.*, tens, hundreds, or more, of device regions that, when singulated, form a plurality of integrated device dies. Similarly, the second element can comprise a singulated element, such as a singulated integrated device die. In other arrangements, the second element can comprise a carrier or substrate (*e.g.*, a wafer).

**[0056]** As explained herein, the first and second elements can be directly bonded to one another without an adhesive, which is different from a deposition process. In one application, a width of the first element in the bonded structure can be similar to a width of the second element. In some other embodiments, a width of the first element in the bonded structure can be different from a width of the second element. The width or area of the larger element in the bonded structure may be at least 10% larger than the width or area of the smaller element. The first and second elements can accordingly comprise non-deposited elements. Further, directly bonded structures, unlike deposited layers, can include a defect region along the bond interface in which nanovoids are present. The nanovoids may be formed due to activation of the bonding surfaces, *e.g.*, exposure to a plasma. As explained above, the bond interface can include concentration of materials from the activation and/or last chemical treatment processes. For example, in embodiments that utilize a nitrogen plasma for activation, a nitrogen peak can be formed at the bond interface. In embodiments that utilize an oxygen plasma for activation, an oxygen peak can be formed at the bond interface. In some embodiments, the bond interface can comprise silicon oxynitride, silicon oxycarbonitride, or silicon carbonitride. As explained herein, the direct bond can comprise a covalent bond, which is stronger than van Der Waals bonds. The bonding layers can also comprise polished surfaces that are planarized to a high degree of smoothness.

**[0057]** In some embodiments, metal-to-metal bonds are formed between contact pads. In some embodiments, the contact pads comprise copper or a copper alloy. In various embodiments, the metal-to-metal bonds between the contact pads can be joined such that

copper grains grow into each other across the bond interface. In some embodiments, the copper can have grains oriented along the 111 crystal plane for improved copper diffusion across the bond interface. The bond interface can extend substantially entirely to at least a portion of the bonded contact pads, such that there is substantially no gap between the nonconductive bonding regions at or near the bonded contact pads. In some embodiments, a barrier layer may be provided under the contact pads, *e.g.*, which may include copper. In other embodiments, however, there may be no barrier layer under the contact pads, for example, as described in US 2019/0096741, which is incorporated by reference herein in its entirety and for all purposes.

**[0058]** In one embodiment, a microelectronic structure is disclosed. The microelectronic structure can include a bulk semiconductor portion having a first surface and a second surface opposite the first surface; and a via structure disposed in an opening extending at least partially through the bulk semiconductor portion along a direction non-parallel to the first surface, the via structure comprising a first conductive via portion, a second conductive via portion, a first barrier layer extending along a sidewall of the first conductive via portion, and a second barrier layer the second barrier layer including a first portion disposed between the first conductive via portion and the second conductive via portion, the second conductive via portion extending from the second barrier layer to at least the first surface.

**[0059]** In some embodiments, the microelectronic structure includes a dielectric layer on the bulk semiconductor portion, the second conductive via portion extending through the dielectric layer such that an end of the second conductive via portion is flush with or recessed from an upper surface of the dielectric layer. In some embodiments, the dielectric layer comprises a planarized dielectric bonding layer configured for direct bonding to another element. In some embodiments, the dielectric layer further comprises a dielectric barrier layer on the bulk semiconductor portion, the planarized dielectric bonding layer disposed on the dielectric barrier layer. In some embodiments, the second barrier layer includes a second portion extending along the first barrier layer between the first barrier layer and the second conductive via portion. In some embodiments, a first metal texture of the first conductive via portion is different from a second metal texture of the second conductive via portion. In some embodiments, the second metal texture has grains oriented along a 111

crystal plane non-parallel to a bond interface. In some embodiments, the first and second conductive via portions comprises copper, the copper of the first conductive via portion having an impurity material therein. In some embodiments, the first conductive via portion has a higher impurity concentration than the second conductive via portion. In some embodiments, the first conductive via portion further comprises one or more alloying elements including one or more of beryllium (Be), indium (In), gallium (Ga), manganese (Mn), and nickel (Ni). In some embodiments, the impurity material comprises one or more of sulfur, oxygen, carbon, or nitrogen. In some embodiments, the first and second conductive via portions comprise different metals or different alloys. In some embodiments, the second surface comprises an active surface including active integrated circuitry formed in or on the second surface. In some embodiments, the microelectronic structure is directly bonded to another element without an intervening adhesive. In some embodiments, an end surface of the second conductive via portion is directly bonded to a contact pad of the another element without an intervening adhesive. In some embodiments, nonconductive bonding regions of the microelectronic element and the another element are directly bonded without an intervening adhesive. In some embodiments, the microelectronic structure can include a second via structure having a first conductive via portion, a second conductive via portion, a first barrier layer extending along a sidewall of the first conductive via portion, and a second barrier layer, the second barrier layer including a first portion disposed between the first conductive via portion and the second conductive via portion, wherein the second conductive via portion of the via structure extends along a length different from a length of the second conductive via portion of the second via structure.

**[0060]** In another embodiment, a microelectronic structure is disclosed. The microelectronic structure can include a bulk semiconductor portion having a first surface and a second surface opposite the first surface; and a via structure disposed in an opening extending at least partially through the bulk semiconductor portion through the first surface along a direction non-parallel to the first surface, the via structure comprising a first conductive via portion and a second conductive via portion disposed directly onto and contacting the first conductive via portion without an intervening barrier layer, the second conductive via portion disposed between the first surface and the first conductive via portion,

the first conductive via portion having a different material composition from the second conductive via portion.

**[0061]** In some embodiments, the microelectronic structure includes a barrier layer extending along a sidewall of the first and second conductive portions. In some embodiments, the microelectronic structure includes a dielectric layer on the bulk semiconductor portion, the second conductive via portion extending through the dielectric layer such that an end of the second conductive via portion is flush with or recessed below an upper surface of the dielectric layer. In some embodiments, the dielectric layer comprises a planarized dielectric bonding layer configured for direct bonding to another element. In some embodiments, the dielectric layer further comprises a dielectric barrier layer on the bulk semiconductor portion, the planarized dielectric bonding layer disposed on the dielectric barrier layer. In some embodiments, a first metal texture of the first conductive via portion is different from a second metal texture of the second conductive via portion. In some embodiments, the second metal texture has grains oriented along a 111 crystal plane. In some embodiments, the first and second conductive via portions comprises copper, the copper of the first conductive via portion having an impurity material therein. In some embodiments, the first conductive via portion comprises one or more alloying elements including one or more of beryllium (Be), indium (In), gallium (Ga), manganese (Mn), and nickel (Ni). In some embodiments, the impurity material comprises one or more of sulfur, oxygen, carbon, or nitrogen. In some embodiments, the first and second conductive via portions comprise different metals or different alloys. In some embodiments, the microelectronic device is directly bonded to another element without an intervening adhesive. In some embodiments, an end surface of the second conductive via portion is directly bonded to a contact pad of the another element without an intervening adhesive. In some embodiments, nonconductive bonding regions of the microelectronic element and the another element are directly bonded without an intervening adhesive.

**[0062]** In another embodiment, a microelectronic structure is disclosed. The microelectronic structure can include a bulk semiconductor portion having a first surface and a second surface opposite the first surface; and a via structure disposed in an opening extending at least partially through the bulk semiconductor portion through the first surface along a direction non-parallel to the first surface, the via structure comprising a first

conductive via portion and a second conductive via portion disposed directly onto and contacting the first conductive via portion without an intervening barrier layer, the second conductive via portion disposed between the first surface and the first conductive via portion, the first conductive via portion being formed before, and separately from, the second conductive via portion.

**[0063]** In some embodiments, the microelectronic structure includes a barrier layer extending along a sidewall of the first and second conductive portions. In some embodiments, a first metal texture of the first conductive via portion is different from a second metal texture of the second conductive via portion. In some embodiments, the second metal texture has grains oriented along a 111 crystal plane. In some embodiments, the first metal texture has a first proportion of 111 planes oriented within 30° of vertical, wherein the second metal texture has a second proportion of 111 planes oriented within 30° of vertical, the second proportion greater than the first portion. In some embodiments, the first and second conductive via portions comprises copper, the copper of the first conductive via portion having an impurity material therein. In some embodiments, the first conductive portion has a higher percentage of alloying elements as compared to the second conductive via portion. In some embodiments, the microelectronic device is directly bonded to another element without an intervening adhesive. In some embodiments, an end surface of the second conductive via portion is directly bonded to a contact pad of the another element without an intervening adhesive. In some embodiments, nonconductive bonding regions of the microelectronic element and the another element are directly bonded without an intervening adhesive.

**[0064]** In another embodiment, a method of forming a microelectronic structure is disclosed. The method can include forming an opening at least partially through a substrate having a front surface and a back surface opposite the front surface, the opening extending through the front surface along a direction non-parallel to the second surface; providing a first conductive via portion in the opening from the front surface; revealing the first conductive via portion by removing material from the back surface; and after the revealing, providing a filling structure in the opening over the first conductive via portion from the back surface.

[0065] In some embodiments, providing the filling structure comprises providing a second conductive via portion in the opening over the first conductive via portion from the back surface. In some embodiments, the method includes after revealing, recessing the first conductive via portion from the back surface. In some embodiments, the method includes after providing the first conductive via portion but before providing the second conductive via portion, providing a second barrier layer over the first conductive via portion. In some embodiments, the method includes providing a first barrier layer along a sidewall of the first conductive via portion. In some embodiments, the method includes providing the first barrier layer before providing the first conductive via portion. In some embodiments, providing the second barrier layer comprises providing the second barrier layer along the first barrier layer between the first barrier layer and the second conductive via portion. In some embodiments, the method includes providing a dielectric layer on the bulk semiconductor portion, the dielectric layer at least partially defining the back surface of the substrate, the second conductive via portion extending through the dielectric layer such that an end of the second conductive via portion is flush with or recessed from the back surface of the substrate. In some embodiments, the method includes preparing the dielectric layer for direct bonding to another element. In some embodiments, the method includes providing a dielectric barrier layer on the bulk semiconductor portion, the dielectric bonding layer disposed on the dielectric barrier layer. In some embodiments, the method includes directly bonding the dielectric layer to another element without an intervening adhesive. In some embodiments, the method includes directly bonding an end surface of the second conductive via portion to a contact pad of another element without an intervening adhesive. In some embodiments, providing the filling structure comprises providing a dielectric layer in a recess over the first conductive via portion. In some embodiments, the method can include removing a portion of the substrate from the back surface such that the first conductive via portion protrudes from the back surface of the substrate, and removing the dielectric layer to expose the conductive via. In some embodiments, removing the portion of the substrate comprises etching the back surface of the substrate. In some embodiments, the method can include providing a second backside dielectric layer over at least the etched back surface of the substrate and a portion of the dielectric layer disposed in the recess. In some embodiments, the method can include removing at least portions of the second backside dielectric layer that overlie the portion of

the dielectric layer disposed in the recess. In some embodiments, the method can include planarizing the second backside dielectric layer and recessing the first conductive via portion relative to the second backside dielectric layer.

**[0066]** In another embodiment, a method of forming a microelectronic structure is disclosed. The method can include forming an opening partially through a substrate having a front surface and a back surface opposite the first surface, the opening extending through the front surface along a direction non-parallel to the front surface; filling the opening with a first conductive via portion; revealing the first conductive via portion by removing material from the back surface; and refilling a portion of the opening with a filling structure after revealing the first conductive portion.

**[0067]** In some embodiments, refilling the portion of the opening with the filling structure comprises providing a second conductive via portion in the opening over the first conductive via portion from the back surface. In some embodiments, the method includes recessing the first conductive portion after revealing to define the portion of the opening. In some embodiments, the method includes depositing a second barrier layer on the first conductive via portion after recessing and before refilling. In some embodiments, the method includes depositing a first barrier layer to line the opening prior to filling. In some embodiments, depositing the second barrier layer comprises depositing the second barrier layer on the first barrier layer in the portion of the opening. In some embodiments, refilling the portion of the opening with the filling structure comprises providing a dielectric layer in a recess over the first conductive via portion. In some embodiments, the method can include removing a portion of the substrate from the back surface such that the first conductive via portion protrudes from the back surface of the substrate, and removing the dielectric layer to expose the conductive via. In some embodiments, removing the portion of the substrate comprises etching the back surface of the substrate. In some embodiments, the method can include providing a second backside dielectric layer over at least the etched back surface of the substrate and a portion of the dielectric layer disposed in the recess. In some embodiments, removing at least portions of the second backside dielectric layer that overlie the portion of the dielectric layer disposed in the recess. In some embodiments, the method can include planarizing the second backside dielectric layer and recessing the first conductive via portion relative to the second backside dielectric layer.

**[0068]** In another embodiment, a bonded structure is disclosed. The bonded structure can include a first element having a first bonding surface and a second element having a second bonding surface, the first element having a third surface opposite the first bonding surface; and a via structure disposed in an opening extending at least partially through the first element from the first bonding surface along a direction non-parallel to the first bonding surface, the via structure comprising a first conductive via portion and a second conductive via portion contacting one another, the second conductive via portion at least partially embedded within a bonding material at the bonding surface of the first element, the bonding material and the second conductive via portion directly bonded to the bonding surface of the second element without an intervening adhesive. In some embodiments, nonconductive bonding regions of the first and second elements are directly bonded without an intervening adhesive.

**[0069]** In another embodiment, a method of forming a microelectronic structure is disclosed. The method can include: providing a substrate having an opening and a conductive via disposed in the opening, the conductive via extending partially through the substrate from a first side of the substrate towards the second side; removing a portion of the substrate from the second side to expose the conductive via; removing a portion of the conductive via from the second side of the substrate to form a recess; providing a dielectric layer in the recess over the conductive via; further removing a portion of the substrate from the second side such that the conductive via protrudes from the second side of the substrate; and removing the dielectric layer to expose the conductive via.

**[0070]** In some embodiments, removing the portion of the substrate comprises at least one of grinding and polishing the second side. In some embodiments, at least one of grinding and polishing comprises planarizing the substrate and the conductive via. In some embodiments, removing the portion of the conductive via comprises etching the conductive via. In some embodiments, providing the dielectric layer comprises providing a first backside dielectric layer over the back side of the substrate and in the recess. In some embodiments, providing the first backside dielectric layer comprises providing a plurality of dielectric layers. In some embodiments, providing the plurality of dielectric layers comprises providing a first silicon nitride layer over the back side of the substrate and over the conductive via and providing a second silicon oxide layer over the first silicon nitride layer.

In some embodiments, the method can include, before further removing the portion of the substrate, removing a portion of the first backside dielectric layer that is disposed over the back side of the substrate. In some embodiments, further removing the portion of the substrate comprises etching the back side of the substrate. In some embodiments, the method can include providing a second backside dielectric layer over at least the etched back side of the substrate and a portion of the first backside dielectric layer disposed in the recess. In some embodiments, the method can include removing at least portions of the second backside dielectric layer that overlie the portion of the first backside dielectric layer disposed in the recess. In some embodiments, the method can include planarizing the second backside dielectric layer and recessing the conductive via relative to the second backside dielectric layer.

**[0071]** Unless the context clearly requires otherwise, throughout the description and the claims, the words “comprise,” “comprising,” “include,” “including” and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of “including, but not limited to.” The word “coupled”, as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Likewise, the word “connected”, as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Additionally, the words “herein,” “above,” “below,” and words of similar import, when used in this application, shall refer to this application as a whole and not to any particular portions of this application. Moreover, as used herein, when a first element is described as being “on” or “over” a second element, the first element may be directly on or over the second element, such that the first and second elements directly contact, or the first element may be indirectly on or over the second element such that one or more elements intervene between the first and second elements. Where the context permits, words in the above Detailed Description using the singular or plural number may also include the plural or singular number respectively. The word “or” in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

**[0072]** Moreover, conditional language used herein, such as, among others, “can,” “could,” “might,” “may,” “e.g.,” “for example,” “such as” and the like, unless specifically stated otherwise, or otherwise understood within the context as used, is generally intended to convey that certain embodiments include, while other embodiments do not include, certain features, elements and/or states. Thus, such conditional language is not generally intended to imply that features, elements and/or states are in any way required for one or more embodiments.

**[0073]** While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosure. Indeed, the novel apparatus, methods, and systems described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the disclosure. For example, while blocks are presented in a given arrangement, alternative embodiments may perform similar functionalities with different components and/or circuit topologies, and some blocks may be deleted, moved, added, subdivided, combined, and/or modified. Each of these blocks may be implemented in a variety of different ways. Any suitable combination of the elements and acts of the various embodiments described above can be combined to provide further embodiments. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the disclosure.

WHAT IS CLAIMED IS:

1. A microelectronic structure comprising:
  - a bulk semiconductor portion having a first surface and a second surface opposite the first surface; and
  - a via structure disposed in an opening extending at least partially through the bulk semiconductor portion along a direction non-parallel to the first surface, the via structure comprising a first conductive via portion, a second conductive via portion, a first barrier layer extending along a sidewall of the first conductive via portion, and a second barrier layer the second barrier layer including a first portion disposed between the first conductive via portion and the second conductive via portion, the second conductive via portion extending from the second barrier layer to at least the first surface.
2. The microelectronic device of Claim 1, further comprising a dielectric layer on the bulk semiconductor portion, the second conductive via portion extending through the dielectric layer such that an end of the second conductive via portion is flush with or recessed from an upper surface of the dielectric layer.
3. The microelectronic device of Claim 2, wherein the dielectric layer comprises a planarized dielectric bonding layer configured for direct bonding to another element.
4. The microelectronic device of Claim 3, wherein the dielectric layer further comprises a dielectric barrier layer on the bulk semiconductor portion, the planarized dielectric bonding layer disposed on the dielectric barrier layer.
5. The microelectronic device of any one of Claims 1 to 4, wherein the second barrier layer includes a second portion extending along the first barrier layer between the first barrier layer and the second conductive via portion.
6. The microelectronic device of any one of Claims 1 to 5, wherein a first metal texture of the first conductive via portion is different from a second metal texture of the second conductive via portion.
7. The microelectronic device of Claim 6, wherein the second metal texture has grains oriented along a 111 crystal plane non-parallel to a bond interface.

8. The microelectronic device of any one of Claims 1 to 7, wherein the first and second conductive via portions comprises copper, the copper of the first conductive via portion having an impurity material therein.

9. The microelectronic device of Claim 8, wherein the first conductive via portion has a higher impurity concentration than the second conductive via portion.

10. The microelectronic device of Claim 8, wherein the first conductive via portion further comprises one or more alloying elements including one or more of beryllium (Be), indium (In), gallium (Ga), manganese (Mn), and nickel (Ni).

11. The microelectronic device of Claim 8, wherein the impurity material comprises one or more of sulfur, oxygen, carbon, or nitrogen.

12. The microelectronic device of any one of Claims 1 to 11, wherein the first and second conductive via portions comprise different metals or different alloys.

13. The microelectronic device of any one of Claims 1 to 12, wherein the second surface comprises an active surface including active integrated circuitry formed in or on the second surface.

14. A bonded structure comprising the microelectronic device of any one of Claims 1 to 13, wherein the microelectronic device is directly bonded to another element without an intervening adhesive.

15. The bonded structure of Claim 14, wherein an end surface of the second conductive via portion is directly bonded to a contact pad of the another element without an intervening adhesive.

16. The bonded structure of Claim 14 or Claim 15, wherein nonconductive bonding regions of the microelectronic element and the another element are directly bonded without an intervening adhesive.

17. The microelectronic device of any one of Claims 1 to 16, further comprising a second via structure having a first conductive via portion, a second conductive via portion, a first barrier layer extending along a sidewall of the first conductive via portion, and a second barrier layer, the second barrier layer including a first portion disposed between the first conductive via portion and the second conductive via portion, wherein the second conductive via portion of the via structure extends along a length different from a length of the second conductive via portion of the second via structure.

18. A microelectronic structure comprising:  
a bulk semiconductor portion having a first surface and a second surface opposite the first surface; and  
a via structure disposed in an opening extending at least partially through the bulk semiconductor portion through the first surface along a direction non-parallel to the first surface, the via structure comprising a first conductive via portion and a second conductive via portion disposed directly onto and contacting the first conductive via portion without an intervening barrier layer, the second conductive via portion disposed between the first surface and the first conductive via portion, the first conductive via portion having a different material composition from the second conductive via portion.
19. The microelectronic device of Claim 18, further comprising a barrier layer extending along a sidewall of the first and second conductive portions.
20. The microelectronic device of any one of Claims 18 to 19, further comprising a dielectric layer on the bulk semiconductor portion, the second conductive via portion extending through the dielectric layer such that an end of the second conductive via portion is flush with or recessed below an upper surface of the dielectric layer.
21. The microelectronic device of Claim 20, wherein the dielectric layer comprises a planarized dielectric bonding layer configured for direct bonding to another element.
22. The microelectronic device of Claim 21, wherein the dielectric layer further comprises a dielectric barrier layer on the bulk semiconductor portion, the planarized dielectric bonding layer disposed on the dielectric barrier layer.
23. The microelectronic device of any one of Claims 18 to 22, wherein a first metal texture of the first conductive via portion is different from a second metal texture of the second conductive via portion.
24. The microelectronic device of Claim 23, wherein the second metal texture has grains oriented along a 111 crystal plane.
25. The microelectronic device of any one of Claims 18 to 24, wherein the first and second conductive via portions comprises copper, the copper of the first conductive via portion having an impurity material therein.

26. The microelectronic device of Claim 25, wherein the first conductive via portion comprises one or more alloying elements including one or more of beryllium (Be), indium (In), gallium (Ga), manganese (Mn), and nickel (Ni).

27. The microelectronic device of Claim 25, wherein the impurity material comprises one or more of sulfur, oxygen, carbon, or nitrogen.

28. The microelectronic device of any one of Claims 18 to Claim 27, wherein the first and second conductive via portions comprise different metals or different alloys.

29. A bonded structure comprising the microelectronic device of any one of Claims 18 to 28, wherein the microelectronic device is directly bonded to another element without an intervening adhesive.

30. The bonded structure of Claim 29, wherein an end surface of the second conductive via portion is directly bonded to a contact pad of the another element without an intervening adhesive.

31. The bonded structure of Claim 29 or Claim 30, wherein nonconductive bonding regions of the microelectronic element and the another element are directly bonded without an intervening adhesive.

32. A microelectronic structure comprising:

a bulk semiconductor portion having a first surface and a second surface opposite the first surface; and

a via structure disposed in an opening extending at least partially through the bulk semiconductor portion through the first surface along a direction non-parallel to the first surface, the via structure comprising a first conductive via portion and a second conductive via portion disposed directly onto and contacting the first conductive via portion without an intervening barrier layer, the second conductive via portion disposed between the first surface and the first conductive via portion, the first conductive via portion being formed before, and separately from, the second conductive via portion.

33. The microelectronic device of Claim 32, further comprising a barrier layer extending along a sidewall of the first and second conductive portions.

34. The microelectronic device of Claim 32 or 33, wherein a first metal texture of the first conductive via portion is different from a second metal texture of the second conductive via portion.

35. The microelectronic device of Claim 34, wherein the second metal texture has grains oriented along a 111 crystal plane.

36. The microelectronic device of Claim 35, wherein the first metal texture has a first proportion of 111 planes oriented within 30° of vertical, wherein the second metal texture has a second proportion of 111 planes oriented within 30° of vertical, the second proportion greater than the first portion.

37. The microelectronic device of any one of Claims 32 to 36, wherein the first and second conductive via portions comprises copper, the copper of the first conductive via portion having an impurity material therein.

38. The microelectronic device of any one of Claims 32 to Claim 37, wherein the first conductive portion has a higher percentage of alloying elements as compared to the second conductive via portion.

39. A bonded structure comprising the microelectronic device of any one of Claims 32 to 38, wherein the microelectronic device is directly bonded to another element without an intervening adhesive.

40. The bonded structure of Claim 39, wherein an end surface of the second conductive via portion is directly bonded to a contact pad of the another element without an intervening adhesive.

41. The bonded structure of Claim 39 or Claim 40, wherein nonconductive bonding regions of the microelectronic element and the another element are directly bonded without an intervening adhesive.

42. A method of forming a microelectronic structure, the method comprising:  
forming an opening at least partially through a substrate having a front surface and a back surface opposite the front surface, the opening extending through the front surface along a direction non-parallel to the second surface;  
providing a first conductive via portion in the opening from the front surface;  
revealing the first conductive via portion by removing material from the back surface; and

after the revealing, providing a filling structure in the opening over the first conductive via portion from the back surface.

43. The method of Claim 42, wherein providing the filling structure comprises providing a second conductive via portion in the opening over the first conductive via portion from the back surface.

44. The method of Claim 43, further comprising, after revealing, recessing the first conductive via portion from the back surface.

45. The method of Claim 44, further comprising, after providing the first conductive via portion but before providing the second conductive via portion, providing a second barrier layer over the first conductive via portion.

46. The method of Claim 45, further comprising providing a first barrier layer along a sidewall of the first conductive via portion.

47. The method of Claim 46, further comprising providing the first barrier layer before providing the first conductive via portion.

48. The method of Claim 46 or Claim 47, wherein providing the second barrier layer comprises providing the second barrier layer along the first barrier layer between the first barrier layer and the second conductive via portion.

49. The method of any one of Claims 43 to 48, further comprising providing a dielectric layer on the bulk semiconductor portion, the dielectric layer at least partially defining the back surface of the substrate, the second conductive via portion extending through the dielectric layer such that an end of the second conductive via portion is flush with or recessed from the back surface of the substrate.

50. The method of Claim 49, further comprising preparing the dielectric layer for direct bonding to another element.

51. The method of Claim 50, further comprising providing a dielectric barrier layer on the bulk semiconductor portion, the dielectric bonding layer disposed on the dielectric barrier layer.

52. The method of Claim 50 or Claim 51, further comprising directly bonding the dielectric layer to another element without an intervening adhesive.

53. The method of Claim 52, further comprising directly bonding an end surface of the second conductive via portion to a contact pad of the another element without an intervening adhesive.

54. The method of Claim 42, wherein providing the filling structure comprises providing a dielectric layer in a recess over the first conductive via portion.

55. The method of Claim 54, further comprising removing a portion of the substrate from the back surface such that the first conductive via portion protrudes from the back surface of the substrate, and removing the dielectric layer to expose the conductive via.

56. The method of Claim 55, wherein removing the portion of the substrate comprises etching the back surface of the substrate.

57. The method of Claim 56, further comprising providing a second backside dielectric layer over at least the etched back surface of the substrate and a portion of the dielectric layer disposed in the recess.

58. The method of Claim 57, further comprising removing at least portions of the second backside dielectric layer that overlie the portion of the dielectric layer disposed in the recess.

59. The method of Claim 57 or 58, further comprising planarizing the second backside dielectric layer and recessing the first conductive via portion relative to the second backside dielectric layer.

60. A method of forming a microelectronic structure, the method comprising:  
forming an opening partially through a substrate having a front surface and a back surface opposite the first surface, the opening extending through the front surface along a direction non-parallel to the front surface;  
filling the opening with a first conductive via portion;  
revealing the first conductive via portion by removing material from the back surface; and  
refilling a portion of the opening with a filling structure after revealing the first conductive portion.

61. The method of Claim 60, wherein refilling the portion of the opening with the filling structure comprises providing a second conductive via portion in the opening over the first conductive via portion from the back surface

62. The method of Claim 61, further comprising recessing the first conductive portion after revealing to define the portion of the opening.

63. The method of Claim 62, further comprising depositing a second barrier layer on the first conductive via portion after recessing and before refilling.

64. The method of Claim 63, further comprising depositing a first barrier layer to line the opening prior to filling.

65. The method of Claim 64, wherein depositing the second barrier layer comprises depositing the second barrier layer on the first barrier layer in the portion of the opening.

66. The method of Claim 60, wherein refilling the portion of the opening with the filling structure comprises providing a dielectric layer in a recess over the first conductive via portion.

67. The method of Claim 66, further comprising removing a portion of the substrate from the back surface such that the first conductive via portion protrudes from the back surface of the substrate, and removing the dielectric layer to expose the conductive via.

68. The method of Claim 67, wherein removing the portion of the substrate comprises etching the back surface of the substrate.

69. The method of Claim 68, further comprising providing a second backside dielectric layer over at least the etched back surface of the substrate and a portion of the dielectric layer disposed in the recess.

70. The method of Claim 69, further comprising removing at least portions of the second backside dielectric layer that overlie the portion of the dielectric layer disposed in the recess.

71. The method of Claim 69 or 70, further comprising planarizing the second backside dielectric layer and recessing the first conductive via portion relative to the second backside dielectric layer.

72. A bonded structure comprising:  
a first element having a first bonding surface and a second element having a second bonding surface, the first element having a third surface opposite the first bonding surface; and

a via structure disposed in an opening extending at least partially through the first element from the first bonding surface along a direction non-parallel to the first bonding surface, the via structure comprising a first conductive via portion and a second conductive via portion contacting one another, the second conductive via portion at least partially embedded within a bonding material at the bonding surface of the first element, the bonding material and the second conductive via portion directly bonded to the bonding surface of the second element without an intervening adhesive.

73. The bonded structure of Claim 72, wherein nonconductive bonding regions of the first and second elements are directly bonded without an intervening adhesive.

74. A method of forming a microelectronic structure, the method comprising:

providing a substrate having an opening and a conductive via disposed in the opening, the conductive via extending partially through the substrate from a first side of the substrate towards the second side;

removing a portion of the substrate from the second side to expose the conductive via;

removing a portion of the conductive via from the second side of the substrate to form a recess;

providing a dielectric layer in the recess over the conductive via;

further removing a portion of the substrate from the second side such that the conductive via protrudes from the second side of the substrate; and

removing the dielectric layer to expose the conductive via.

75. The method of Claim 74, wherein removing the portion of the substrate comprises at least one of grinding and polishing the second side.

76. The method of Claim 75, wherein at least one of grinding and polishing comprises planarizing the substrate and the conductive via.

77. The method of Claim 74, wherein removing the portion of the conductive via comprises etching the conductive via.

78. The method of Claim 74, wherein providing the dielectric layer comprises providing a first backside dielectric layer over the back side of the substrate and in the recess.

79. The method of Claim 78, wherein providing the first backside dielectric layer comprises providing a plurality of dielectric layers.

80. The method of Claim 79, wherein providing the plurality of dielectric layers comprises providing a first silicon nitride layer over the back side of the substrate and over the conductive via and providing a second silicon oxide layer over the first silicon nitride layer.

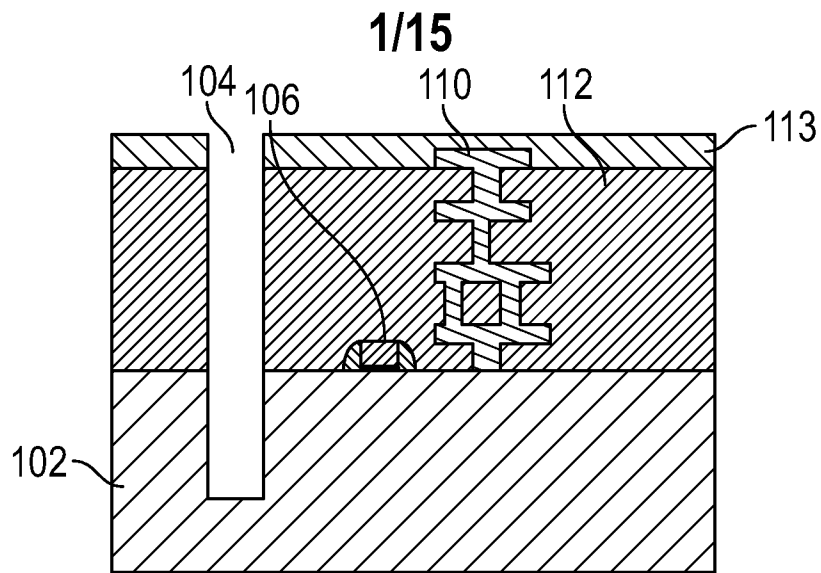
81. The method of any one of Claims 78 to 80, further comprising, before further removing the portion of the substrate, removing a portion of the first backside dielectric layer that is disposed over the back side of the substrate.

82. The method of Claim 78, wherein further removing the portion of the substrate comprises etching the back side of the substrate.

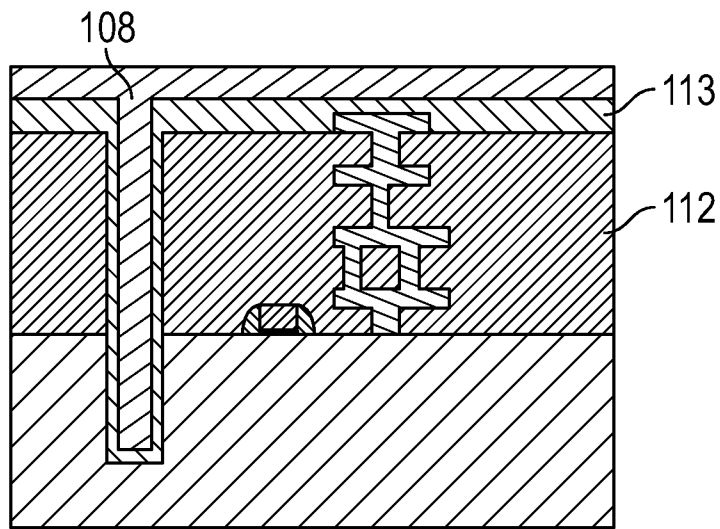
83. The method of Claim 82, further comprising providing a second backside dielectric layer over at least the etched back side of the substrate and a portion of the first backside dielectric layer disposed in the recess.

84. The method of Claim 83, further comprising removing at least portions of the second backside dielectric layer that overlie the portion of the first backside dielectric layer disposed in the recess.

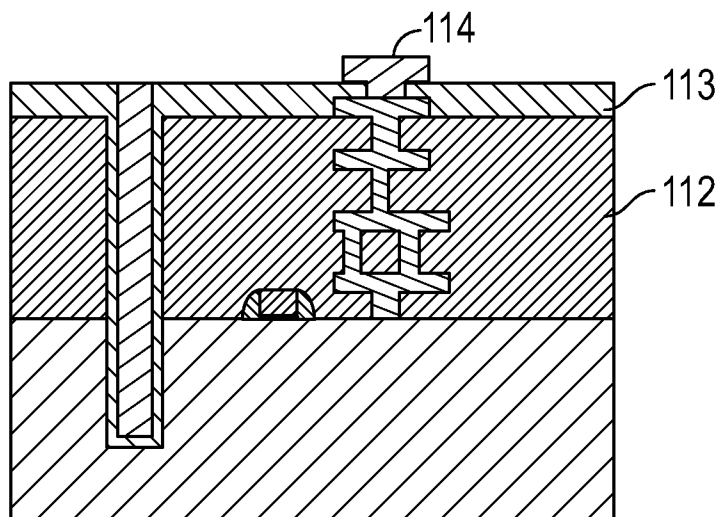
85. The method of Claim 83 or 84, further comprising planarizing the second backside dielectric layer and recessing the conductive via relative to the second backside dielectric layer.



**FIG. 1A**



**FIG. 1B**



**FIG. 1C**

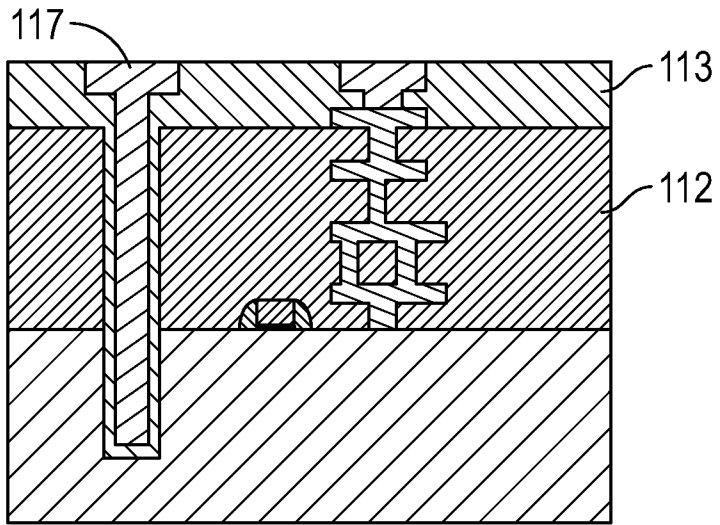


FIG. 1D

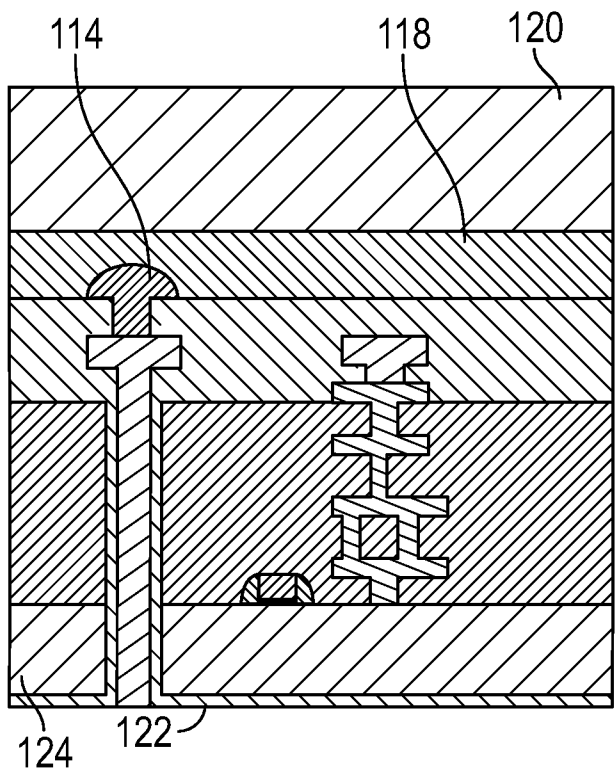


FIG. 1E

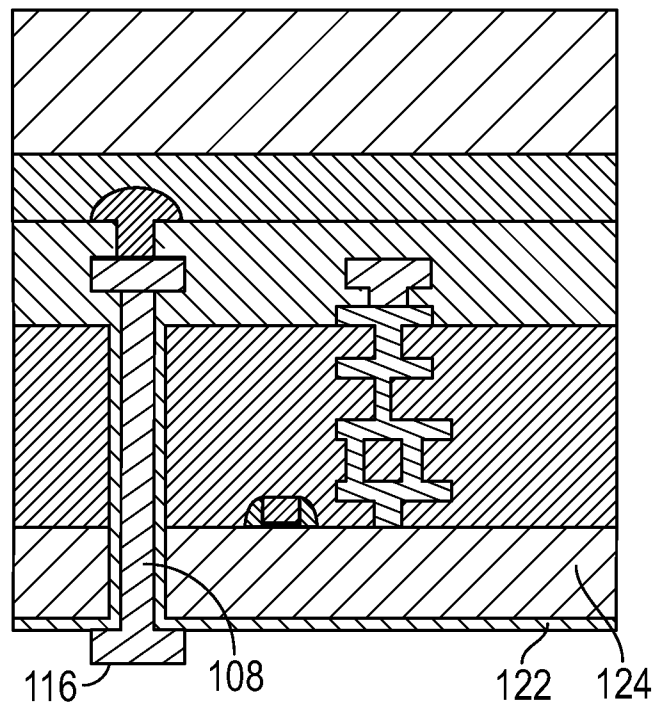


FIG. 1F

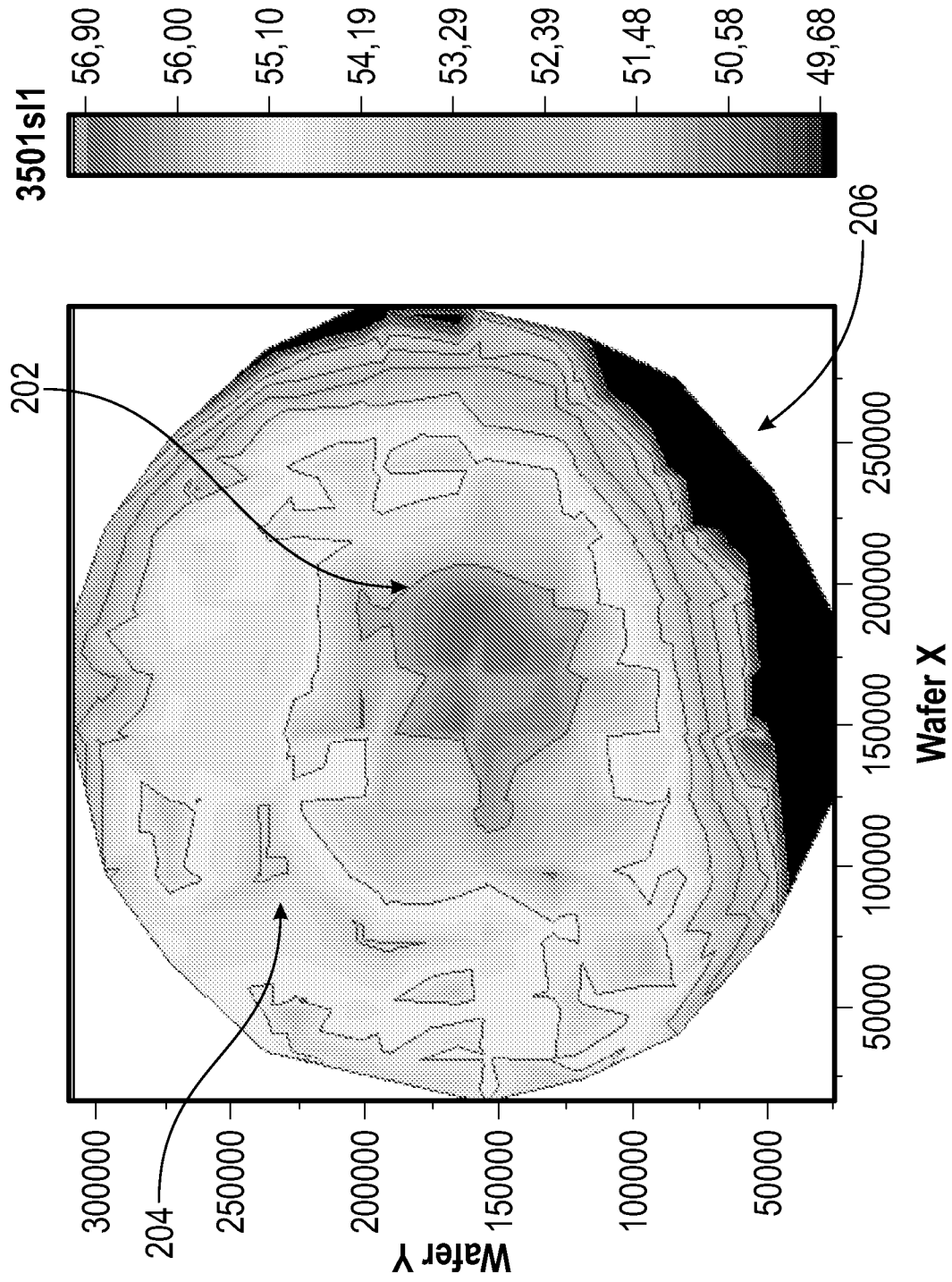


FIG. 2

304

ASPEN DIE 200MM WAFER: DIE NUMBERING (BACKSIDE)

ROW	CD	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	# OF DIE				
1											2	1														2				
2						3	4	5	6	7	8	9	10	11		12	13	14								12				
3						29	27	26	25	24	23	22	21	20		19	18	17	16	15						16				
4						31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48			18				
5						68	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49		20			
6						70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	22			
7						114	113	112	111	110	109	108	107	106	105	104	103	102	101	99	98	97	96	95	94	93	92	91	24	
8						115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	24
9						162	161	160	159	158	157	156	155	154	153	152	151	150	149	148	147	146	145	144	143	142	141	140	139	24
10						163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	24
11						208	207	206	205	204	203	202	201	200	199	198	197	196	195	194	193	192	191	190	189	188	187	186	185	24
12						209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	229	228	22
13						250	249	248	247	246	245	244	243	242	241	240	239	238	237	236	235	234	233	232	231				20	
14						251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266								16	
15						278	277	276	275	274	273	272	271	270	269	268	267												12	
16						279	280	281	282	283	284	?																6		
																												284		
																												TOTAL		

306

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FIG. 3A

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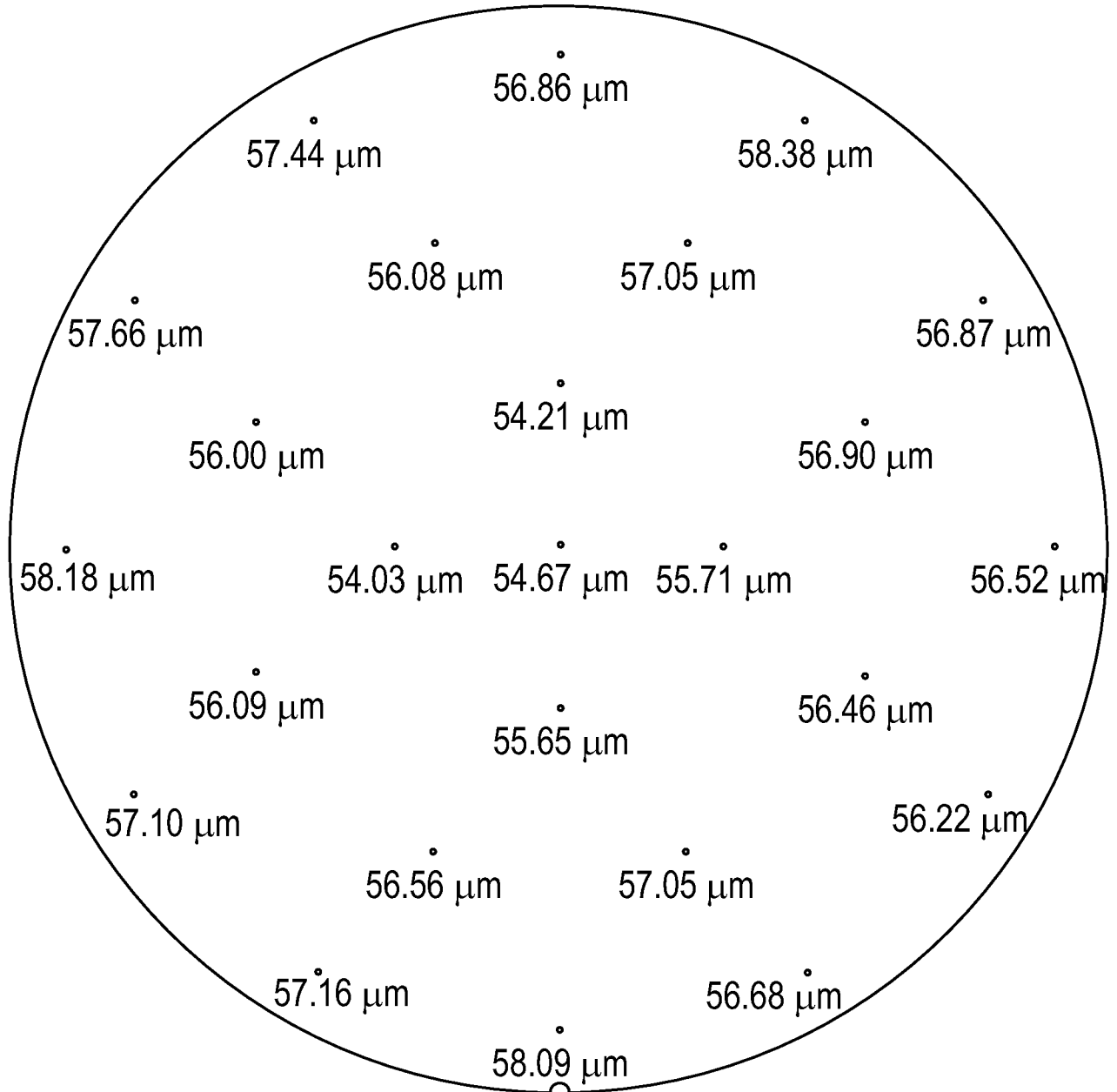


FIG. 3B

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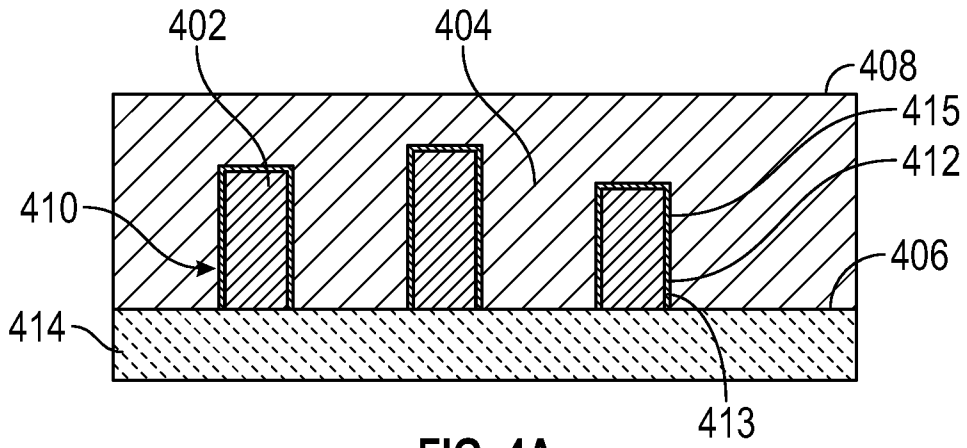


FIG. 4A

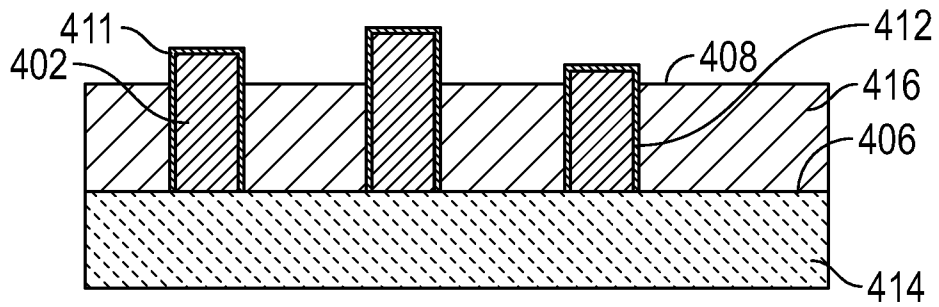


FIG. 4B

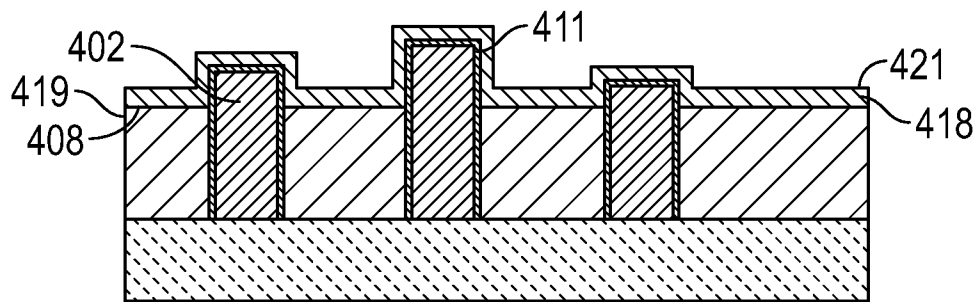


FIG. 4C

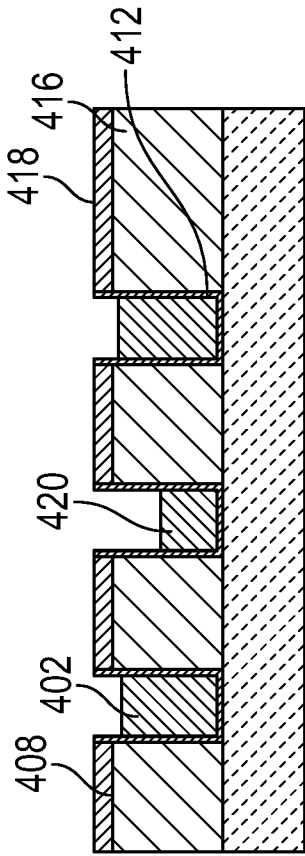


FIG. 4E

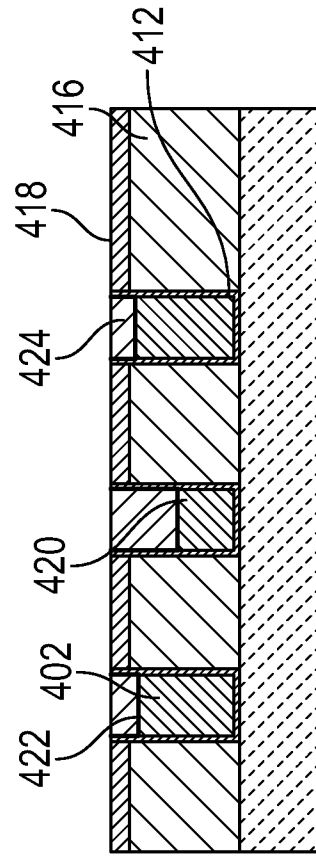


FIG. 4G

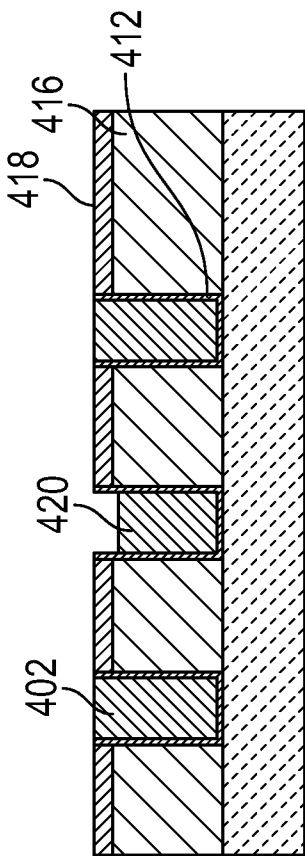


FIG. 4D

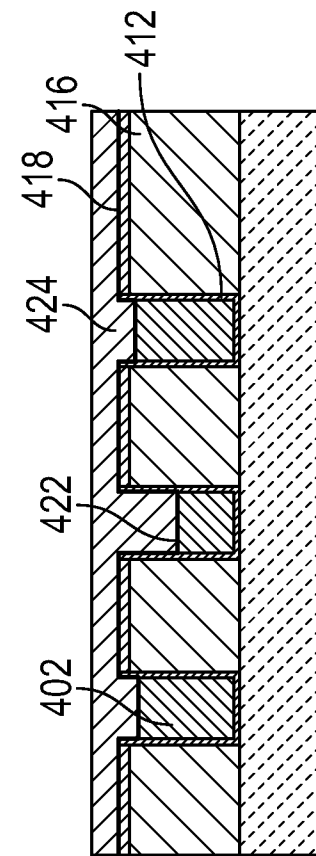


FIG. 4F

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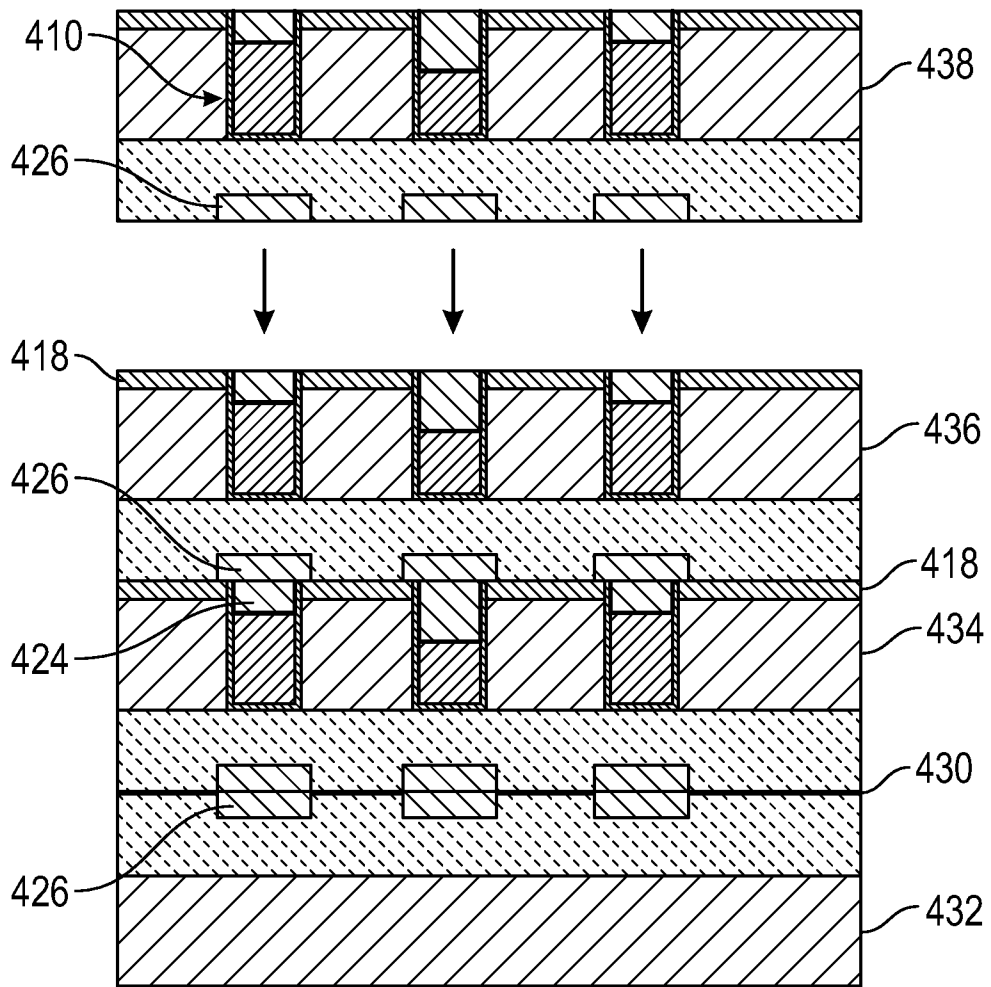


FIG. 4H

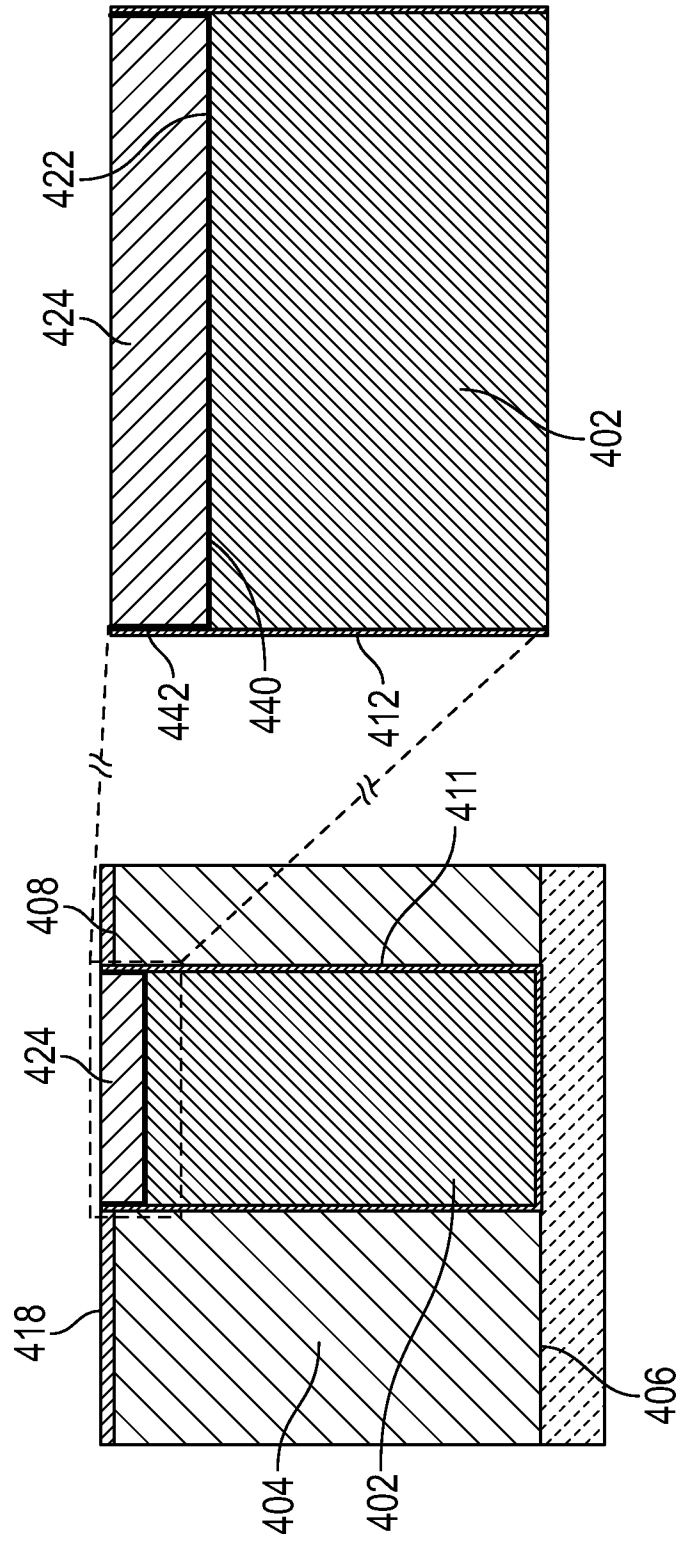


FIG. 4I

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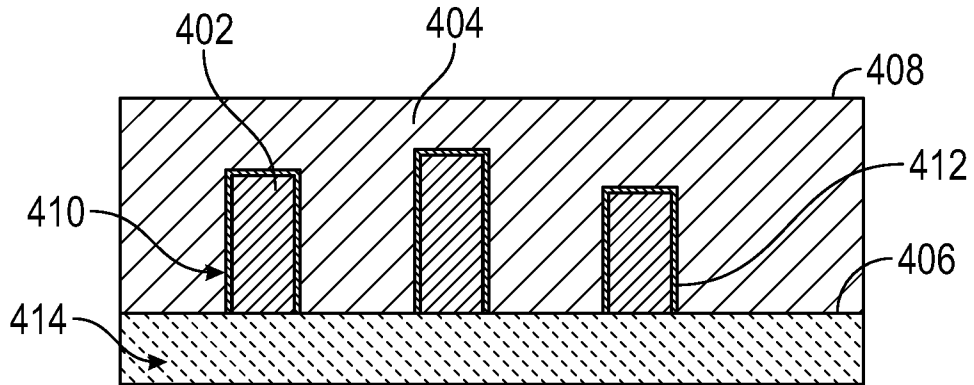


FIG. 5A

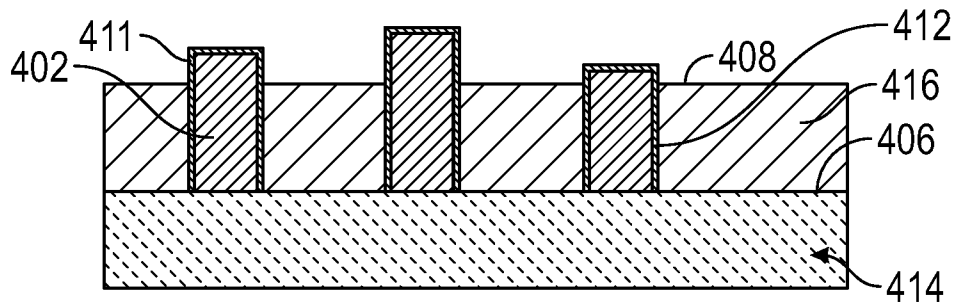


FIG. 5B

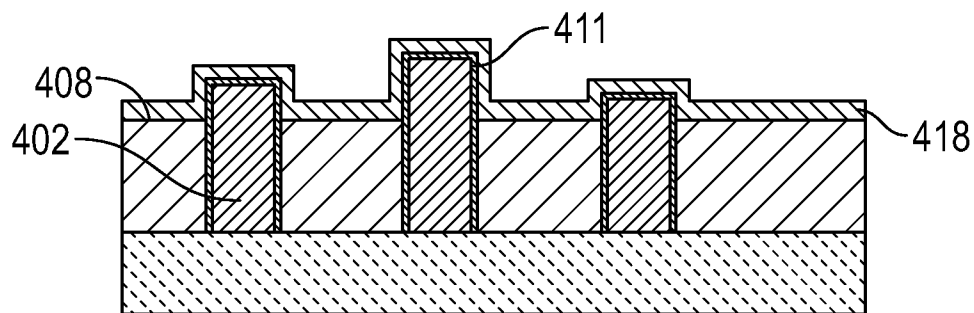


FIG. 5C

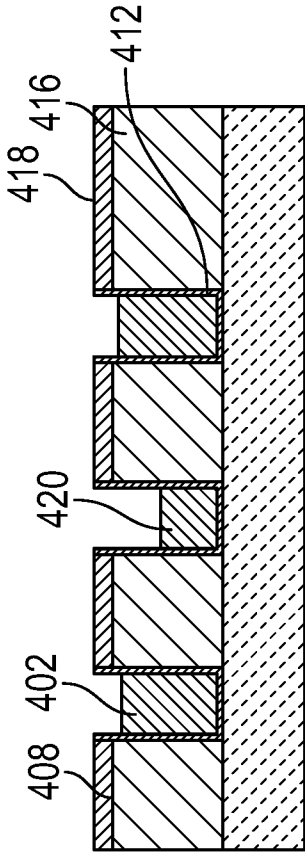


FIG. 5E

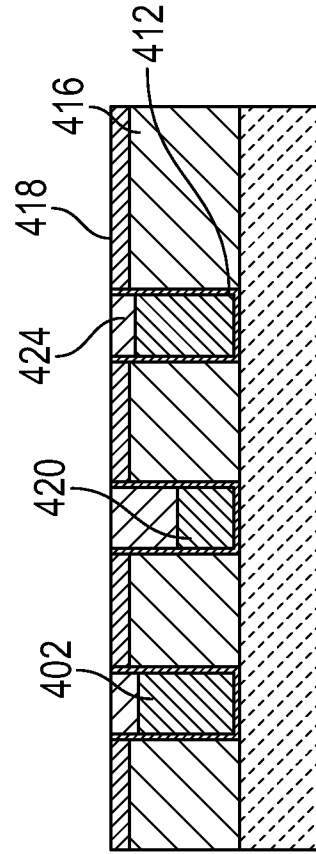


FIG. 5G

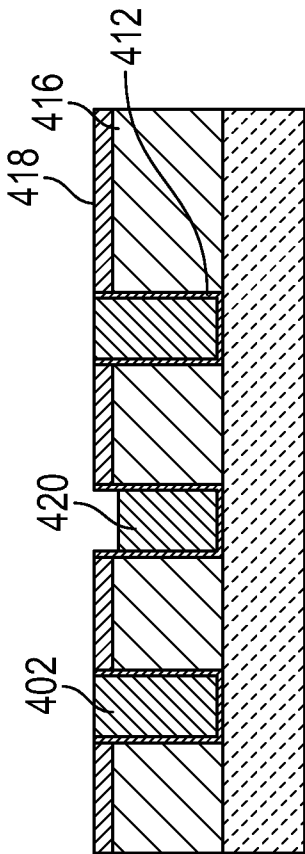


FIG. 5D

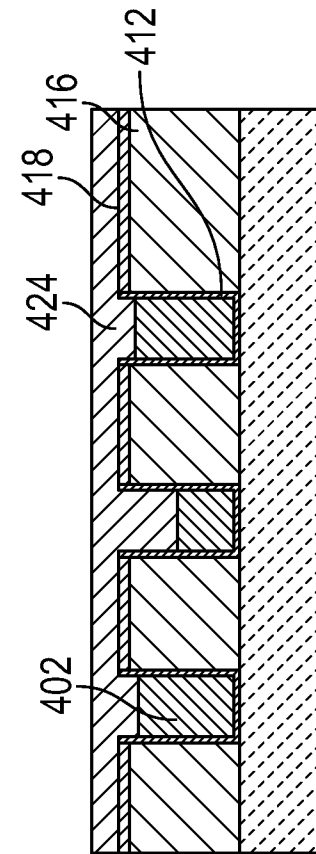


FIG. 5F

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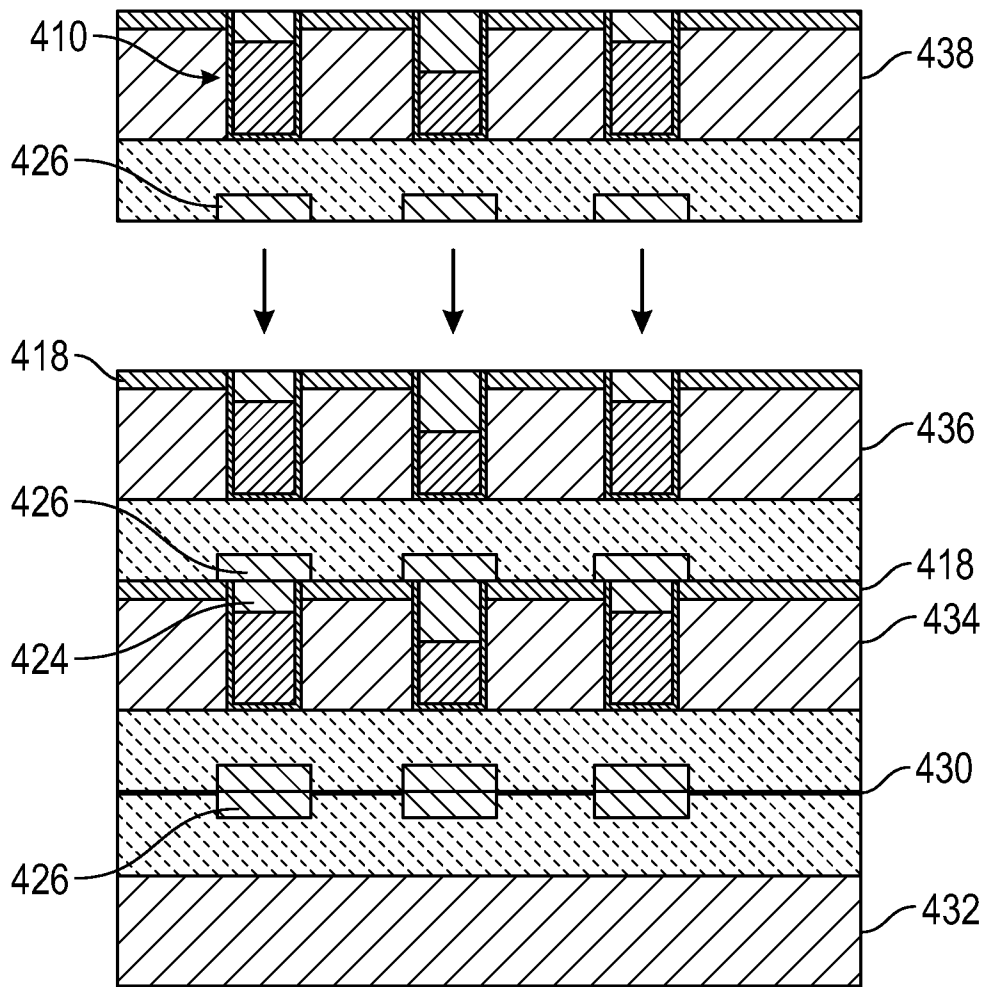


FIG. 5H

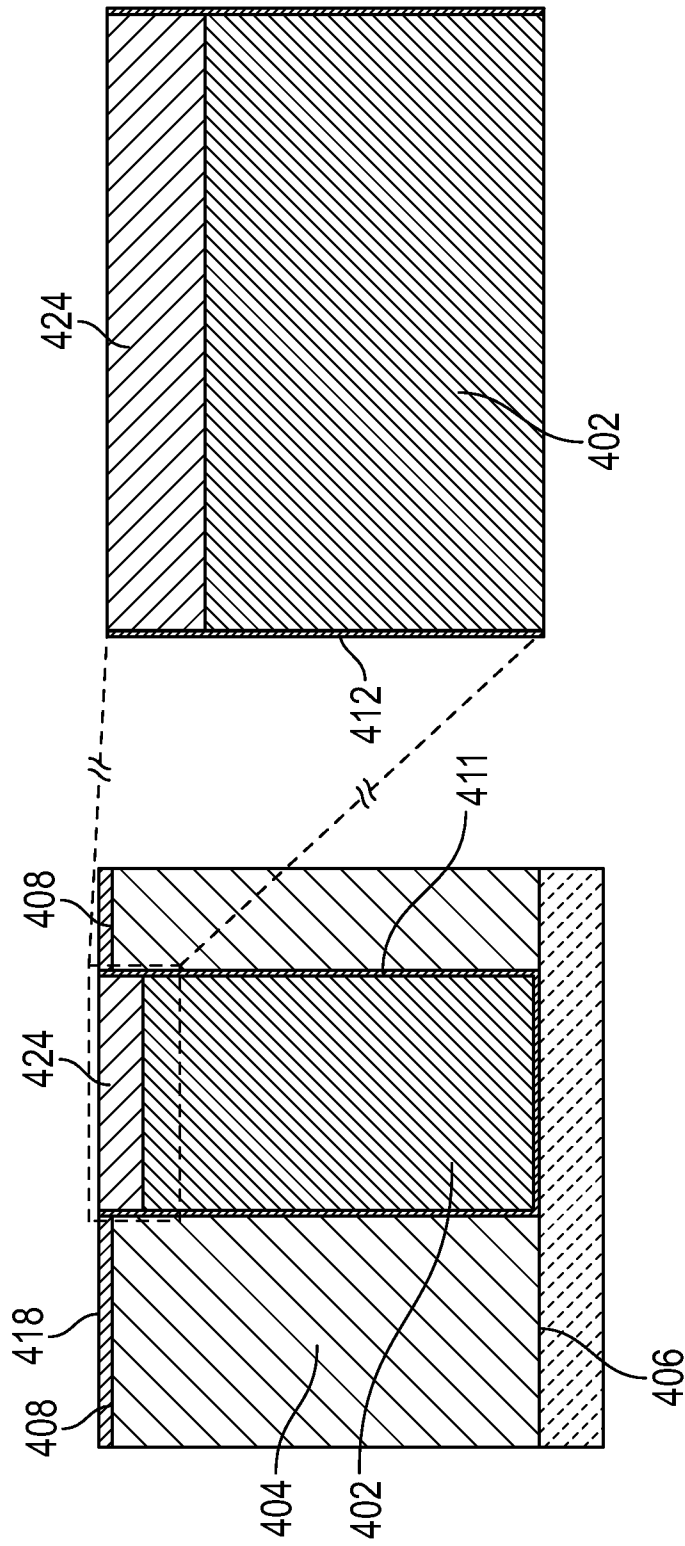


FIG. 5I

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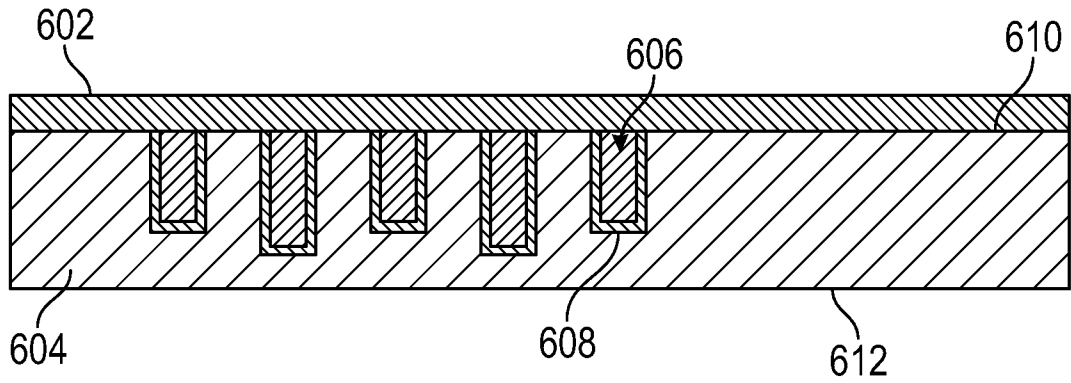


FIG. 6A

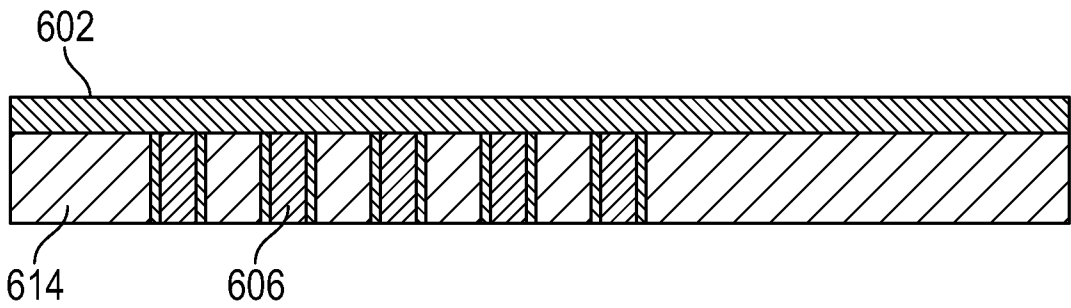


FIG. 6B

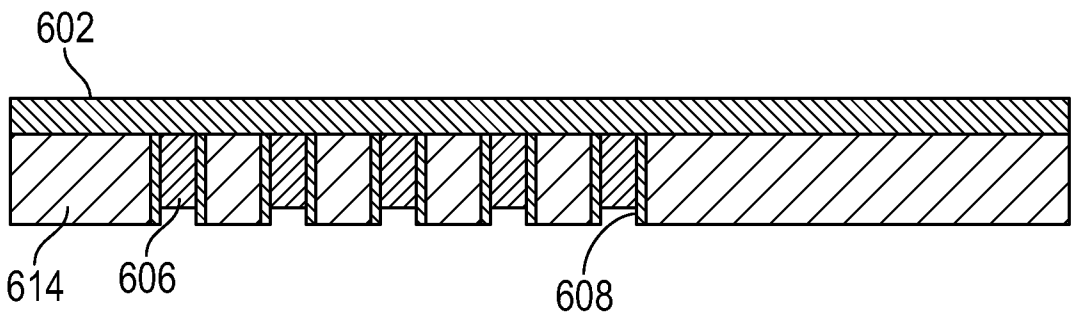


FIG. 6C

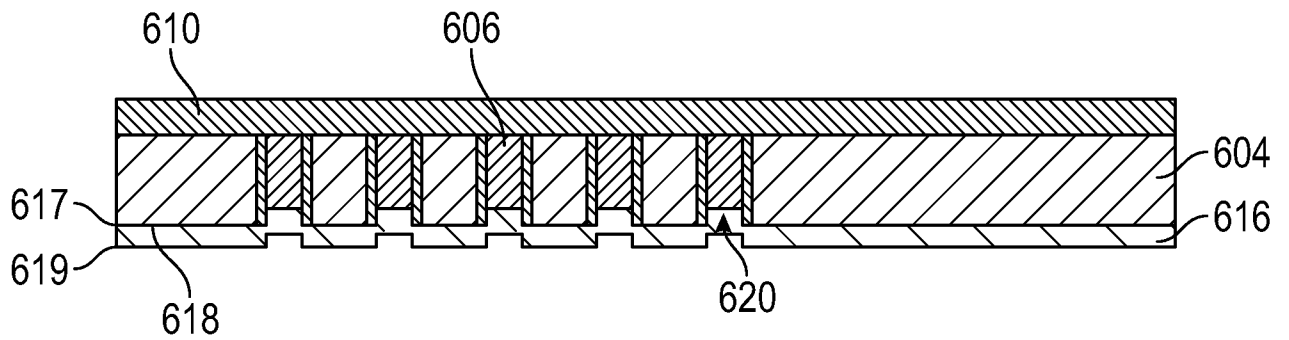


FIG. 6D

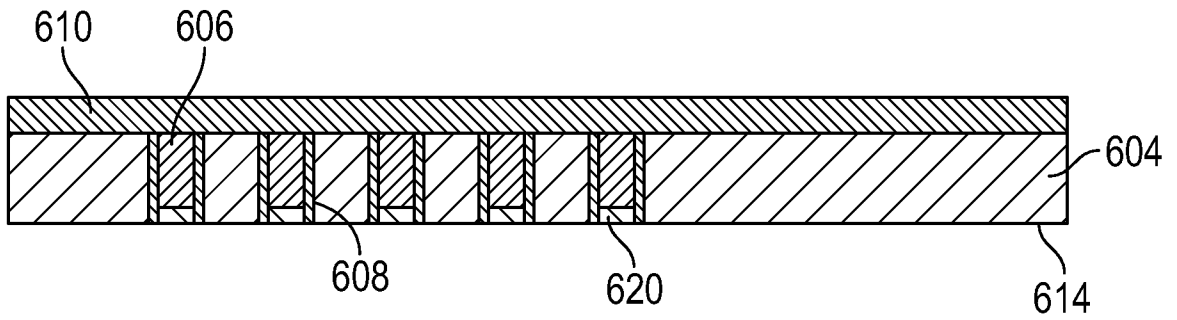


FIG. 6E

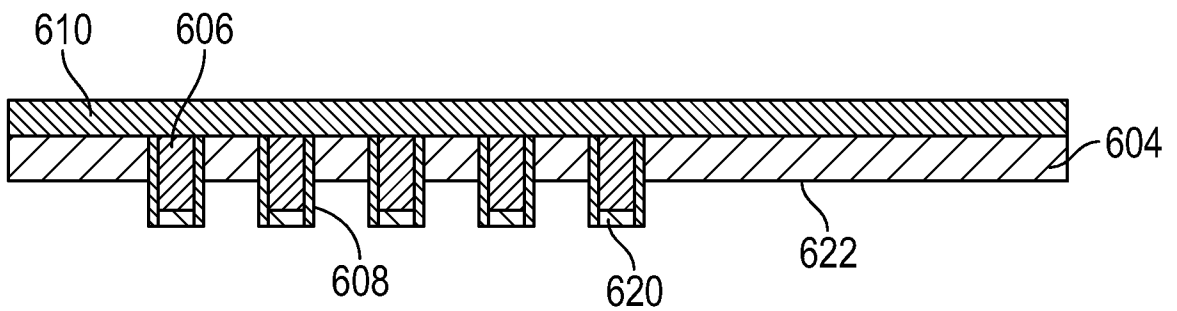


FIG. 6F

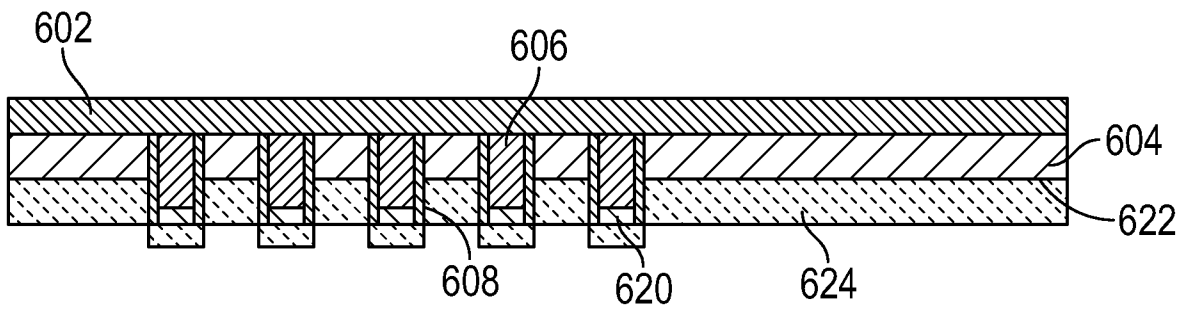


FIG. 6G

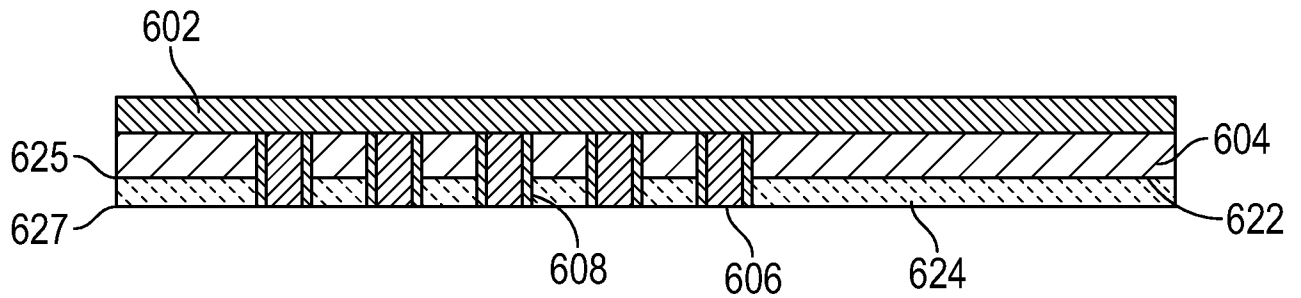


FIG. 6H

## INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2021/073122

<b>A. CLASSIFICATION OF SUBJECT MATTER</b>		
H01L 21/768(2006.01)i; H01L 23/48(2006.01)i; H01L 25/065(2006.01)i		
According to International Patent Classification (IPC) or to both national classification and IPC		
<b>B. FIELDS SEARCHED</b>		
Minimum documentation searched (classification system followed by classification symbols) H01L 21/768(2006.01); H01L 23/00(2006.01); H01L 23/48(2006.01); H01L 23/498(2006.01); H01L 23/532(2006.01)		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Korean utility models and applications for utility models Japanese utility models and applications for utility models		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) eKOMPASS(KIPO internal) & Keywords: via, bulk semiconductor portion, barrier layer, recess, fill		
<b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2013-0119543 A1 (HONG YU et al.) 16 May 2013 (2013-05-16) paragraphs [0020]-[0037] and figures 1A-2C	1-2,42-43,60-61
Y		3-5,18-22,32-36,72-73
A		44-48,54-59, 62-71,74-85
Y	US 2019-0385935 A1 (INVENSAS BONDING TECHNOLOGIES, INC.) 19 December 2019 (2019-12-19) paragraphs [0041]-[0044] and figure 3A-5	3-4,21-22,72-73
Y	US 2013-0119547 A1 (SU-KYOUNG KIM et al.) 16 May 2013 (2013-05-16) paragraphs [0056]-[0097] and figures 1D-3E	5,18-22,32-36
<input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C. <input checked="" type="checkbox"/> See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "D" document cited by the applicant in the international application "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search <b>21 April 2022</b>		Date of mailing of the international search report <b>21 April 2022</b>
Name and mailing address of the ISA/KR <b>Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon 35208, Republic of Korea</b> Facsimile No. +82-42-481-8578		Authorized officer <b>PARK, Hye Lyun</b> Telephone No. +82-42-481-3463

## INTERNATIONAL SEARCH REPORT

International application No.

**PCT/US2021/073122**

<b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2019-0385966 A1 (INVENSAS BONDING TECHNOLOGIES, INC.) 19 December 2019 (2019-12-19) paragraphs [0068]-[0076] and figures 9-12	1-5,18-22,32-36,42-48,54-85
A	US 2015-0028476 A1 (MICRON TECHNOLOGY, INC.) 29 January 2015 (2015-01-29) paragraphs [0013]-[0027] and figures 1-14	1-5,18-22,32-36,42-48,54-85

**Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)**

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1.  Claims Nos.:  
because they relate to subject matter not required to be searched by this Authority, namely:
  
2.  Claims Nos.: **7, 9-11, 15, 24, 26-27, 30, 40, 50-51, 53**  
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:  
  
Claims 7, 9-11, 15, 24, 26-27, 30, 40, 50-51, 53 are unclear, because these claims refer to the multiple dependent claims which do not comply with PCT Rule 6.4(a).
  
3.  Claims Nos.: **6, 8, 12-14, 16-17, 23, 25, 28-29, 31, 37-39, 41, 49, 52**  
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

**INTERNATIONAL SEARCH REPORT**  
**Information on patent family members**

International application No.

**PCT/US2021/073122**

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
US	2013-0119543	A1	16 May 2013	None			
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				CN	112534574	A	19 March 2021
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				WO	2014-062602	A1	24 April 2014