(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 3 200 089 A1

(12) EUROPEAN PATENT APPLICATION
published in accordance with Art. 153(4) EPC

(43) Date of publication:
02.08.2017 Bulletin 2017/31

(21) Application number: **15850035.5**

(22) Date of filing: **14.04.2015**

(51) Int Cl.:
G06F 13/42 *(2006.01)*

(86) International application number:
PCT/CN2015/076547

(87) International publication number:
WO 2016/058344 (21.04.2016 Gazette 2016/16)

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA ME
Designated Validation States:
MA

(30) Priority: **14.10.2014 CN 201410542155**

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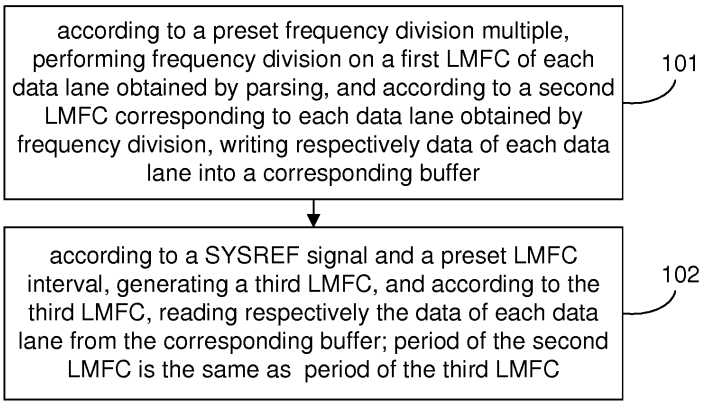
(54) METHOD, APPARATUS, COMMUNICATION EQUIPMENT AND STORAGE MEDIA FOR DETERMINING LINK DELAY

(57) The disclosure provides a method for determining link delay. The method includes: according to a preset frequency division multiple, performing frequency division on a first Local Multi Frame Clock (LMFC) of each data lane obtained by parsing to obtain a second LMFC corresponding to each data lane, and, according to the second LMFC, writing respectively the data of each data lane into a corresponding buffer; and according to a SYSREF signal and a preset LMFC interval, generating a third LMFC, and, according to the third LMFC, reading respectively the data of each data lane from the corresponding buffer. The period of the second LMFC is the same as the period of the third LMFC. The disclosure also provides an apparatus, a communication device and a storage medium for implementing the method.

Fig. 1



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Description

TECHNICAL FIELD

[0001] The disclosure relates to JESD204B interface technologies in the field of wireless communications, and in particular to a method, an apparatus, a communication device and a storage medium for determining link delay based on JESD204B interface.

BACKGROUND

[0002] At present, the requirement of the increasing base station data throughput causes increases in both component cost and power consumption of wireless communication units and makes related printed circuit boards and interfaces more complex, and meanwhile puts more emphasis on the requirement of signal integrity.

[0003] Thus, traditional concurrent Low-Voltage Differential Signalling (LVDS) I/O interfaces are no longer suitable for the demands on cost reduction, system reliability enhancement, integration improvement, shortening of the time to market, design complexity reduction and so on; therefore, Solid State Technology Association (JEDEC) publishes a JESD204B interface standard applicable to the universal interface of Analogue Digital Conversion (ADC)/Digital Analogue Conversion (DAC).

[0004] As the proposal of the JESD204B interface standard, how to realize the alignment of a plurality of data lanes at the receiving side and how to guarantee the determined delay of link become problems needed to be resolved urgently for the adoption of the JESD204B interface standard. However, the JESD204B interface protocol puts forward a limit that the processing delay from a data transmitting end to a data receiving data cannot exceed the length of one Local Multi Frame Clock (LMFC) (or called a local multi frame head) at most and that the delay difference between each lane cannot exceed the length of one LMFC too. However, the length of the LMFC may have a minimum of 17 bytes. Since the delay is shorter if the board level wiring is shorter, the limit of the above protocol has a high demand on hardware processing and board level wiring, so that the complexity of the design implementation is greatly increased.

SUMMARY

[0005] In order to solve the technical problem in existing technologies, embodiments of the disclosure provide a method, an apparatus, a communication device and a storage medium for determining link delay.

[0006] An embodiment of the disclosure provides a method for determining link delay, including:

according to a preset frequency division multiple, performing frequency division on a first LMFC of each data lane obtained by parsing to obtain a second LMFC corresponding to each data lane, and according to the second LMFC, writing respectively data of each data lane into a corresponding buffer; and

according to a system reference (SYSREF) signal and a preset LMFC interval, generating a third LMFC, and, according to the third LMFC, reading respectively the data of each data lane from the corresponding buffer.

[0007] The period of the second LMFC is the same as the period of the third LMFC.

[0008] Here, the period of the second LMFC corresponding to each data lane obtained after the frequency division is greater than a data transmission delay difference corresponding to the data lane having the maximum data transmission delay in all the data lanes before the frequency division.

[0009] Here, according to a preset frequency division multiple, performing frequency division on a first LMFC of each data lane obtained by parsing includes:

parsing the received data of each data lane, and according to the Initial Lane Alignment (ILA) information already existing in the data of each data lane, parsing to obtain the first LMFC; and, according to the preset frequency division multiple, performing frequency division on the first LMFC obtained by parsing to obtain a second LMFC.

[0010] Here, according to the second LMFC, writing the data of each data lane into a buffer includes:

for each data lane, resetting the data write address of the buffer according to the first valid signal of the second LMFC, and then writing the data of each data lane into the buffer in sequence.

[0011] Here, in each data lane, the data transmission delay difference is: (N-1)*T_LMFC;
where N is the preset frequency division multiple, and T_LMFC is the length of a standard LMFC.

[0012] Here, according to the third LMFC, reading the data of each data lane from the buffer includes:

for each data lane, resetting the read address of the buffer according to the first valid signal of the third LMFC, and then reading the data of each data lane from the buffer in sequence.

[0013] An embodiment of the disclosure further provides a storage medium, including a set of instructions, which, when executed, causes at least one processor to execute the operation described above.

[0014] An embodiment of the disclosure further provides an apparatus for determining link delay, including: a frequency division and write control unit, a buffer and read control unit.

[0015] The frequency division and write control unit is configured to: according to a preset frequency division multiple, perform frequency division on a first LMFC of each data lane obtained by parsing to obtain a second LMFC of each data lane, and, according to the second LMFC, write respectively the data of each data lane into a corresponding buffer.

[0016] The read control unit is configured to: according to a SYSREF signal and a preset LMFC interval, generate a third LMFC, and, according to the third LMFC, read respectively the data of each data lane from the corresponding buffer.

[0017] Here the period of the second LMFC is the same as the period of the third LMFC.

[0018] Here, the frequency division and write control unit includes: a frequency division module and a write module, and

the frequency division module is configured to: according to the preset frequency division multiple, perform frequency division on the first LMFC of each data lane obtained by parsing to obtain the second LMFC corresponding to each data lane; and

the write module is configured to: according to the second LMFC generated by the frequency division module, write the data of each data lane into the corresponding buffer.

[0019] Here, the read control unit includes: an LMFC generation module and a read module.

[0020] The LMFC generation module is configured to: according to the SYSREF signal and the preset LMFC interval, generate the third LMFC;

the read module is configured to: according to the third LMFC generated by the LMFC generation module, read respectively the data of each data lane from the corresponding buffer.

[0021] An embodiment of the disclosure further provides a communication device for determining link delay, including the apparatus described above.

[0022] The method, apparatus, communication device and storage medium for determining link delay provided by embodiments of the disclosure perform frequency division, according to a preset frequency division multiple, on a first LMFC of each data lane obtained by parsing to obtain a second LMFC corresponding to each data lane, and write respectively the data of each data lane into a corresponding buffer according to the second LMFC, generate a third LMFC according to a SYSREF signal and a preset LMFC interval, and read respectively the data of each data lane from the corresponding buffer according to the third LMFC. The period of the second LMFC is the same as the period of the third LMFC. Thus, the embodiment of the disclosure eases the restriction to the delay processing of existing links, may reduce the complexity of clock (the processing lock for JESD204B interface for receiving data) frequency and link processing. In addition, the setting of the buffer may support different delay differences of different data lanes before data alignment. Since the delay may be greater than the length of a standard LMFC, the number of periods of the lane transmission processing clock is increased. Therefore, the design requirements for board level wiring may be reduced correspondingly, and the complexity of design may be reduced.

[0023] In addition, as the change of application scenes, embodiments of the disclosure only need to change the configuration of the lengths of the second LMFC and the third LMFC, that is, change the preset frequency division multiple and the LMFC interval according to the change of application scenes, and change the size of the buffer correspondingly. Such changes have high flexibility.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] In drawings (which are not necessarily drawn according to proportion), similar drawing references may be used to describe similar parts in different views. Similar drawing references with different letter suffixes may indicate different examples of similar parts. The drawings generally illustrate each embodiment discussed herein by way of examples rather than limit.

Fig. 1 is an implementation flowchart of a method for determining link delay according to an embodiment of the disclosure;

Fig. 2 is schematic diagram of determining link delay according to an embodiment of the disclosure;

Fig. 3 is a structure diagram of an apparatus for determining link delay according to an embodiment of the disclosure;

Fig. 4 is a structure diagram of a frequency division and write control unit according to an embodiment of the disclosure; and

Fig. 5 is a structure diagram of a read control unit according to an embodiment of the disclosure.

DETAILED DESCRIPTION

[0025] In the embodiment of the disclosure, according to a preset frequency division multiple, frequency division is performed on a first LMFC of each data lane obtained by parsing to obtain a second LMFC corresponding to each data lane, and, according to the second LMFC, data of each data lane is respectively written into a corresponding buffer; and according to a SYSREF signal and a preset LMFC interval, a third LMFC is generated, and according to the third LMFC, the data of each data lane is respectively read from the corresponding buffer. The period of the second LMFC is the same as the period of the third LMFC.

[0026] Here, the method described in the embodiment of the disclosure is implemented at the receiving side. The corresponding receiving process is a process of transmitting data from ADC to a JESD204B interface data

lane.

[0027] It should be noted that: since the method of the embodiment of the disclosure is based on the JESD204B interface, the method is widely applicable to the requirements of existing ADC devices.

[0028] The disclosure is described below in further detail in conjunction with the drawings and specific embodiments.

[0029] Fig. 1 is an implementation flowchart of a method for determining link delay according to an embodiment of the disclosure. As shown in Fig. 1, the method includes:

Step 101: according to a preset frequency division multiple, performing frequency division on a first LMFC of each data lane obtained by parsing to obtain a second LMFC corresponding to each data lane, and according to the second LMFC, writing respectively the data of each data lane into a corresponding buffer.

[0030] Specifically, the received data of each data lane is parsed. According to the Initial Lane Alignment (ILA) information already existing in the data of each data lane, parsing is performed to obtain the first LMFC, that is, a lane associated LMFC . The reason why the first LMFC is called the lane associated LMFC is that the LMFC is obtained by parsing the transmitted data of the lane but is not locally recovered, and moreover, the first LMFC of each data lane obtained by parsing is not the same, that is, the first LMFC of each data lane is not aligned. According to the preset frequency division multiple, frequency division is performed on the first LMFC of each data lane obtained by parsing to obtain the second LMFC corresponding to each data lane, that is, a new and extended lane associated LMFC. According to the second LMFC, the data of each data lane is respectively written into a respective buffer corresponding to each data lane. Specifically, for each data lane, the data write address of the buffer is reset according to the first valid signal of the second LMFC, and then the data of each data lane is written into the buffer in sequence.

[0031] Of course, here the data write address also may be reset according to the second valid signal of the second LMFC. However, it must guarantee that, under one frequency division configuration, only one reset is allowed, and continuous resets are not allowed.

[0032] In addition, since different data lanes have different delays in transmitting data, the moment when the data is written into the buffer probably is not the same.

[0033] Here, following points need to be considered when configuring the frequency division multiple:

(1) For the condition of a single data lane, it is needed to consider the delay difference of the data of the single data lane on the entire transmission link from the opposite end JESD204B interface framing to the local JESD204B interface deframing, that is, the delay difference of the data transmission of the single data lane; then, the LMFC period after the frequency division needs to be greater than the transmission delay difference before the frequency division.

(2) For the condition of multiple data lanes, it is needed to consider the delay difference of the data of the multiple data lanes on the entire transmission link from the opposite end JESD204B interface framing to the local JESD204B interface deframing, that is, the delay difference of the data transmission of each data lane; then, the LMFC period after the frequency division needs to be greater than the transmission delay difference of the lane having the maximum transmission delay before the frequency division.

[0034] Therefore, for the data transmission of the multiple data lanes in the embodiment of the disclosure, the period of the second LMFC obtained after the frequency division is greater than a data transmission delay difference corresponding to the data lane having the maximum data transmission delay in all the data lanes before the frequency division.

[0035] In addition, the preset frequency division multiples for different data lanes in the embodiment of the disclosure must be kept consistent; therefore, only one frequency division multiple needs to be configured.

[0036] In the embodiment of the disclosure, in order to ensure that there is no other data in the buffer before storing the data of each data lane, during actual operations it is needed to first clear the write address in the buffer using the second LMFC. The specific operation is described as the above mentioned.

[0037] Step 102: according to a SYSREF signal and a preset LMFC interval, generating a third LMFC, and according to the third LMFC, reading respectively data of each data lane from the corresponding buffer. The period of the second LMFC is the same as the period of the third LMFC.

[0038] Here, the SYSREF signal is an existing signal in the JESD204B interface protocol. The transmitting side determines the start point of data transmission according to the SYSREF signal, and generates, according to the SYSREF signal, a protocol standard LMFC, that is, the first LMFC mentioned above. As shown in Fig. 2, in the JESD204B interface protocol, the transmitting side starts transmitting data from the second LMFC.

[0039] In Step 102, a new uniform LMFC is generated according to the SYSREF signal and the preset LMFC interval, that is, the third LMFC is generated. The interval between adjacent two third LMFCs is the same as the interval between adjacent two second LMFCs, that is, the period of the third LMFC is the same as the period of the second LMFC; the data of each data lane is read from the buffer at the boundary of the third LMFC. Specifically, for each data lane, the read address of the buffer is reset according to the first valid signal of the generated new uniform third LMFC, and then the data of each data lane is read from the buffer in sequence. Of course, here

the data read address also may be reset according to the second valid signal of the third LMFC, but it must guarantee that, under one frequency division configuration, only one reset is allowed, continuous resets are not allowed.

[0040] Here, in order to ensure that no other data is read when reading the data of each data lane. During actual operations it is needed to first clear the read address of the buffer using the third LMFC.

[0041] In the embodiment of the disclosure, the frequency division basis of the third LMFC is the same as the frequency division basis of the second LMFC, as described above. The second LMFC controls the data of data lanes to be written into the buffer. Since each data lane has a different delay difference, the first LMFC of each data lane is not aligned, and the second LMFC obtained by frequency division is not aligned. Therefore, the write of the data of each data lane can only be controlled by the second LMFC of the corresponding lane. However, in order to guarantee the alignment among multiple data lanes when reading data, a uniform LMFC, that is, the third LMFC, is needed to perform the control. The third LMFC can only be generated according to the SYSREF signal, and cannot be obtained by frequency division according to the first LMFC of a certain data lane.

[0042] To sum up, the embodiment of the disclosure may ensure that the data of each data lane is read starting from one same moment after being buffered. In this way, the data output of each data lane is aligned, and moreover the data delay (from the transmitting side to the receiving side) of each data lane is the same.

[0043] In the embodiment of the disclosure, a corresponding buffer is set corresponding to each data lane so as to realize the buffer of the data of each data lane. Although the data of each data lane is transmitted uniformly at the transmitting side, due to the board delay, the moment of arriving at the receiving side probably is different. Thus the buffer is needed to delay the data of each data lane, so as to guarantee that the data of each data lane is output at the same moment and that the data of each data lane is aligned.

[0044] Thus, the embodiment of the disclosure eases the restriction to the delay processing of existing links, and it may reduce the complexity of clock (the processing lock for JESD204B interface for receiving data) frequency and link processing. In addition, the setting of the buffer may support different delay differences of different data lanes before data alignment. Since the delay may be greater than the length of a standard LMFC, the number of periods of the lane transmission processing clock is increased. Therefore, the design requirements for board level wiring may be reduced correspondingly, and the complexity of design may be reduced.

[0045] The selection of the above processing lock for JESD204B interface for receiving data is associated to the processing delay of the whole data lane. The higher the processing clock is, the higher is the number of the clock periods of the transmission delay of the whole data lane. The lower the processing clock is, the lower is the number of the clock periods of the transmission delay of the whole data lane. By using the LMFC frequency division method of the embodiment of the disclosure, the processing clock may be selected lower, so as to correspondingly increase the number of the clock periods of the transmission delay.

[0046] In addition, as the change of application scenes, the embodiment of the disclosure only needs to change the configuration of the lengths of the second LMFC and the third LMFC, that is, change the preset frequency division multiple and the LMFC interval according to the change of application scenes, and change the size of the buffer correspondingly. Such changes have high flexibility.

[0047] The embodiment of the disclosure further provides a storage medium, including a set of instructions, which, when executed, causes at least one processor to execute the operation described above.

[0048] Fig. 2 is schematic diagram of determining link delay according to an embodiment of the disclosure. As shown in Fig. 2, the transmitting side (TX) generates a standard LMFC, that is, the first LMFC, according to a SYSREF signal, and the receiving side (RX) also generates an extended LMFC, that is, the third LMFC, according to the SYSREF signal. The extended LMFC and the standard LMFC are aligned. The starting point of each data lane transmitting data is at the location of the LMFC (the second LMFC valid signal) . Due to the board wiring delay, the data of different data lanes arrives at the receiving side at different time. The receiving side uses the buffer, and uniformly reads the data of each data lane from the buffer at the boundary of the extended LMFC. Thus, through the extension of the standard LMFC, the delay of the data of the data lane may exceed the length of a standard LMFC.

[0049] As shown in Fig. 2, the delay difference between each data lane also may exceed the length of a standard LMFC. The link determined delay difference of all data lanes is (N-1)*T_LMFC, where N is an extended multiple of the standard LMFC, that is, the preset frequency division multiple mentioned above, and T_LMFC is the length of a standard LMFC.

[0050] The embodiment of the disclosure further provides an apparatus for determining link delay. As shown in Fig. 3, the apparatus includes: a frequency division and write control unit 301, a buffer 302 and a read control unit 303. In the embodiment of the disclosure, the buffer 302 and the read control unit 303 may be correspondingly set for each data lane respectively, in which,

the frequency division and write control unit 301 is configured to: according to a preset frequency division multiple, perform frequency division on a first LMFC of each data lane obtained by parsing to obtain a second LMFC corresponding to each data lane, and according to the second LMFC, write respectively the data of each data lane into the corresponding buffer 302.

[0051] Specifically, the frequency division and write

control unit 301 parses the received data of each data lane, parses according to the ILA information already existing in the data of each data lane to obtain the first LMFC, that is, a lane associated LMFC, performs frequency division, according to the preset frequency division multiple, on the first LMFC obtained by parsing to obtain a second LMFC, that is, a new extended lane associated LMFC, and, writes the data of each data lane into the buffer according to the second LMFC. Specifically, the frequency division and write control unit 301 may reset the data write address according to the first valid signal of the second LMFC and then write the data of the data lane into the buffer in sequence.

[0052] Of course, here the data write address also may be reset according to the second valid signal of the second LMFC, but it must guarantee that, under one frequency division configuration, only one reset is allowed, continuous resets are not allowed.

[0053] In the above content, the period of the second LMFC corresponding to each data lane obtained after the frequency division is greater than a data transmission delay difference corresponding to the data lane having the maximum data transmission delay in all the data lanes before the frequency division.

[0054] Here, following points need to be considered when configuring the frequency division multiple:

(1) The delay difference of the data of a single data lane on the entire transmission link from the opposite end JESD204B interface framing to the local JESD204B interface deframing, correspondingly, the LMFC period after the frequency division needs to be greater than the transmission delay difference.

(2) The delay difference of the data of multiple data lanes on the entire transmission link from the opposite end JESD204B interface framing to the local JESD204B interface deframing, correspondingly, the LMFC period after the frequency division needs to be greater than the delay difference of the lane having the maximum transmission delay.

[0055] In addition, the preset frequency division multiples for different data lanes in the embodiment of the disclosure must be kept consistent. Therefore, only one frequency division multiple needs to be configured.

the read control unit 303 is configured to: according to a SYSREF signal and a preset LMFC interval, generate a third LMFC, and according to the third LMFC, read respectively the data of each data lane from the corresponding buffer 302. The read process specifically may include resetting the read address according to the first valid signal of the third LMFC, and then reading the data of each data lane from the buffer in sequence. Of course, here the data read address also may be reset according to the second valid signal of the third LMFC, but it must guarantee that, under one frequency division configuration, only one reset is allowed, continuous resets are not allowed.

[0056] Here, the interval between adjacent two second LMFCs is the same as the interval between adjacent two third LMFCs, that is, the period of the third LMFC is the same as the period of the second LMFC.

[0057] During actual applications, the frequency division and write control unit 301 and the read control unit 303 may be implemented through a Central Processing Unit (CPU), a Digital Signal Processor (DSP) or a Field-Programmable Gate Array (FPGA).

[0058] Here, the SYSREF signal is an existing signal in the JESD204B interface protocol. The transmitting side determines the start point of data transmission according to the SYSREF signal, and generates, according to the SYSREF signal, a protocol standard LMFC, that is, the first LMFC mentioned above. As shown in Fig. 2, in the JESD204B interface protocol, the transmitting side starts transmitting data from the second LMFC.

[0059] In this step, a new LMFC is generated according to the SYSREF signal and the preset LMFC interval, that is, the third LMFC is generated. The interval between adjacent two third LMFCs is the same as the interval between adjacent two second LMFCs, that is, the period of the third LMFC is the same as the period of the second LMFC. The data of each data lane is read from the buffer at the boundary of the third LMFC. Here, in order to ensure that no other data is read when reading the data of each data lane, during actual operations it is needed to first clear the read address of the buffer using the third LMFC.

[0060] In the embodiment of the disclosure, the corresponding buffer 302 is set corresponding to each data lane so as to realize the buffer of the data of each data lane. Although the data of each data lane is transmitted uniformly at the transmitting side, due to the board delay, the moment of arriving at the receiving side probably is different. Thus the buffer 302 is needed to delay the data of each data lane, so as to guarantee that the data of each data lane is output at the same moment and that the data of each data lane is aligned.

[0061] Thus, the embodiment of the disclosure eases the restriction to the delay processing of existing links, and it may reduce the complexity of clock (the processing lock for JESD204B interface for receiving data) frequency and link processing. In addition, the setting of the buffer may support different delay differences of different data lanes before data alignment. Since the delay may be greater than the length of a standard LMFC, the number of periods of the lane transmission processing clock is increased. Therefore, the design requirements for board level wiring may be reduced correspondingly, and the complexity of design may be reduced.

[0062] In addition, as the change of application scenes, the embodiment of the disclosure only needs to change the configuration of the lengths of the second LMFC and the third LMFC, that is, change the preset frequency division multiple and the LMFC interval according to the change of application scenes, and change the size of the

buffer correspondingly. Such changes have high flexibility.

[0063] In an embodiment of the disclosure, as shown in Fig. 4, the frequency division and write control unit 301 includes: a frequency division module 3011 and a write module 3012.

[0064] Here, the frequency division module 3011 is configured to: according to the preset frequency division multiple, perform frequency division on the first LMFC of each data lane obtained by parsing to obtain the second LMFC corresponding to each data lane; and
the write module 3012 is configured to: according to the second LMFC generated by the frequency division module 3011, write the data of each data lane into the corresponding buffer 302.

[0065] The frequency division module 3011 and the write module 3012 may be implemented through a CPU, DSP or FPGA.

[0066] In an embodiment of the disclosure, the read control unit 303 includes: an LMFC generation module 3031 and a read module 3032.

[0067] Here, the LMFC generation module 3031 is configured to: according to the SYSREF signal and the preset LMFC interval, generate the third LMFC; and
the read module 3032 is configured to: according to the third LMFC generated by the LMFC generation module 3031, read respectively the data of each data lane from the corresponding buffer 302.

[0068] The LMFC generation module 3031 and read module 3032 may be implemented through a CPU, DSP or FPGA.

[0069] The embodiment of the disclosure further provides a communication device for determining link delay, including the apparatus described above. For example, the communication device may be a device in a wireless base station and the like.

[0070] Those skilled in the art should understand that the embodiments of the disclosure can provide a method, a system or a computer program product. Thus, forms of hardware embodiments, software embodiments or embodiments integrating software and hardware can be adopted in the disclosure. Moreover, a form of the computer program product implemented on one or more computer available storage media (including, but not limited to, a disk memory, an optical memory and the like) containing computer available program codes can be adopted in the disclosure.

[0071] The disclosure is described with reference to flowcharts and/or block diagrams of the method, the device (system) and the computer program product according to the embodiments of the disclosure. It should be understood that each flow and/or block in the flowcharts and/or the block diagrams and a combination of the flows and/or the blocks in the flowcharts and/or the block diagrams can be realized by computer program instructions. These computer program instructions can be provided for a general computer, a dedicated computer, an embedded processor or processors of other programmable data processing devices to generate a machine, so that an apparatus for realizing functions assigned in one or more flows of the flowcharts and/or one or more blocks of the block diagrams is generated via instructions executed by the computers or the processors of the other programmable data processing devices.

[0072] These computer program instructions can also be stored in a computer readable memory capable of guiding the computers or the other programmable data processing devices to work in a specific mode, so that a manufactured product including an instruction apparatus is generated via the instructions stored in the computer readable memory, and the instruction apparatus realizes the functions assigned in one or more flows of the flowcharts and/or one or more blocks of the block diagrams.

[0073] These computer program instructions can also be loaded to the computers or the other programmable data processing devices, so that processing realized by the computers is generated by executing a series of operation steps on the computers or the other programmable devices, and therefore the instructions executed on the computers or the other programmable devices provide a step of realizing the functions assigned in one or more flows of the flowcharts and/or one or more blocks of the block diagrams.

[0074] The above are merely the preferred embodiments of the disclosure, but not to limit the protection scope of the disclosure.

Claims

1. A method for determining link delay, comprising:

   according to a preset frequency division multiple, performing frequency division on a first Local Multi Frame Clock (LMFC) of each data lane obtained by parsing to obtain a second LMFC corresponding to each data lane, and according to the second LMFC, writing respectively data of each data lane into a corresponding buffer; and
   according to a system reference (SYSREF) signal and a preset LMFC interval, generating a third LMFC, and according to the third LMFC, reading respectively the data of each data lane from the corresponding buffer, wherein
   period of the second LMFC is the same as period of the third LMFC.

2. The method according to claim 1, wherein the period of the second LMFC corresponding to each data lane obtained after the frequency division is greater than a data transmission delay difference corresponding to the data lane having the maximum data transmission delay in all the data lanes before the frequency division.

3. The method according to claim 1 or 2, wherein, according to a preset frequency division multiple, performing frequency division on a first LMFC of each data lane obtained by parsing comprises:

   parsing the received data of each data lane, and according to the Initial Lane Alignment (ILA) information already existing in the data of each data lane, parsing to obtain the first LMFC; and according to the preset frequency division multiple, performing frequency division on the first LMFC obtained by parsing to obtain a second LMFC.

4. The method according to claim 1, wherein, according to the second LMFC, writing the data of each data lane into a buffer comprises:

   for each data lane, resetting the data write address of the buffer according to the first valid signal of the second LMFC, and then writing the data of each data lane into the buffer in sequence.

5. The method according to claim 1, wherein, in each data lane, the data transmission delay difference is: (N-1)*T_LMFC;
   where N is the preset frequency division multiple, and T_LMFC is the length of a standard LMFC.

6. The method according to claim 1, wherein, according to the third LMFC, reading the data of each data lane from the buffer comprises:

   for each data lane, resetting the read address of the buffer according to the first valid signal of the third LMFC, and then reading the data of each data lane from the buffer in sequence.

7. An apparatus for determining link delay, comprising: a frequency division and write control unit, a buffer and read control unit, wherein
   the frequency division and write control unit is configured to: according to a preset frequency division multiple, perform frequency division on a first Local Multi Frame Clock (LMFC) of each data lane obtained by parsing to obtain a second LMFC corresponding to each data lane, and according to the second LMFC, write respectively data of each data lane into the corresponding buffer; and
   the read control unit is configured to: according to a SYSREF signal and a preset LMFC interval, generate a third LMFC, and according to the third LMFC, read respectively the data of each data lane from the corresponding buffer, wherein
   period of the second LMFC is the same as period of the third LMFC.

8. The apparatus according to claim 7, wherein the frequency division and write control unit comprises: a frequency division module and a write module, wherein
   the frequency division module is configured to: according to the preset frequency division multiple, perform frequency division on the first LMFC of each data lane obtained by parsing to obtain the second LMFC corresponding to each data lane; and
   the write module is configured to: according to the second LMFC generated by the frequency division module, write the data of each data lane into the corresponding buffer.

9. The apparatus according to claim 7, wherein, the read control unit comprises: an LMFC generation module and a read module, wherein
   the LMFC generation module is configured to: according to the SYSREF signal and the preset LMFC interval, generate the third LMFC;
   the read module is configured to: according to the third LMFC generated by the LMFC generation module, read respectively the data of each data lane from the corresponding buffer.

10. A communication device for determining link delay, comprising the apparatus according to any one of claims 7 to 9.

11. A storage medium, comprising a set of instructions, which, when executed, causes at least one processor to execute the operation according to any one of claims 1 to 6.

Fig. 1

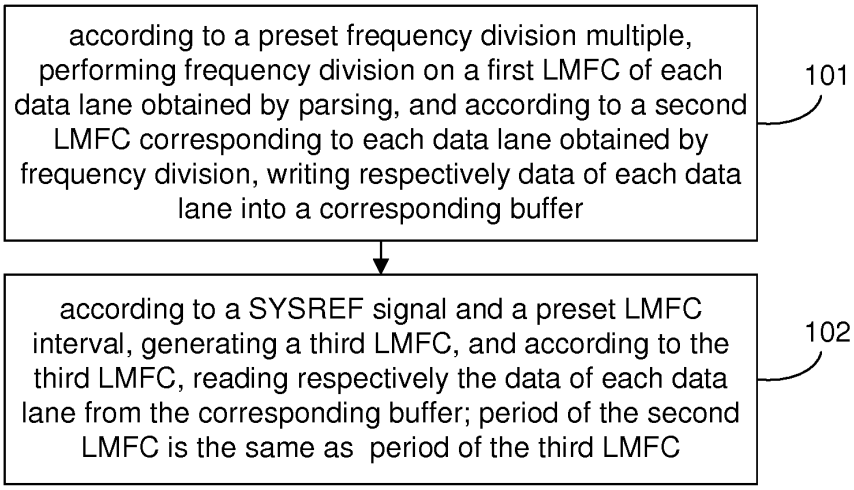

according to a preset frequency division multiple, performing frequency division on a first LMFC of each data lane obtained by parsing, and according to a second LMFC corresponding to each data lane obtained by frequency division, writing respectively data of each data lane into a corresponding buffer
101
according to a SYSREF signal and a preset LMFC interval, generating a third LMFC, and according to the third LMFC, reading respectively the data of each data lane from the corresponding buffer; period of the second LMFC is the same as period of the third LMFC
102

Fig. 2

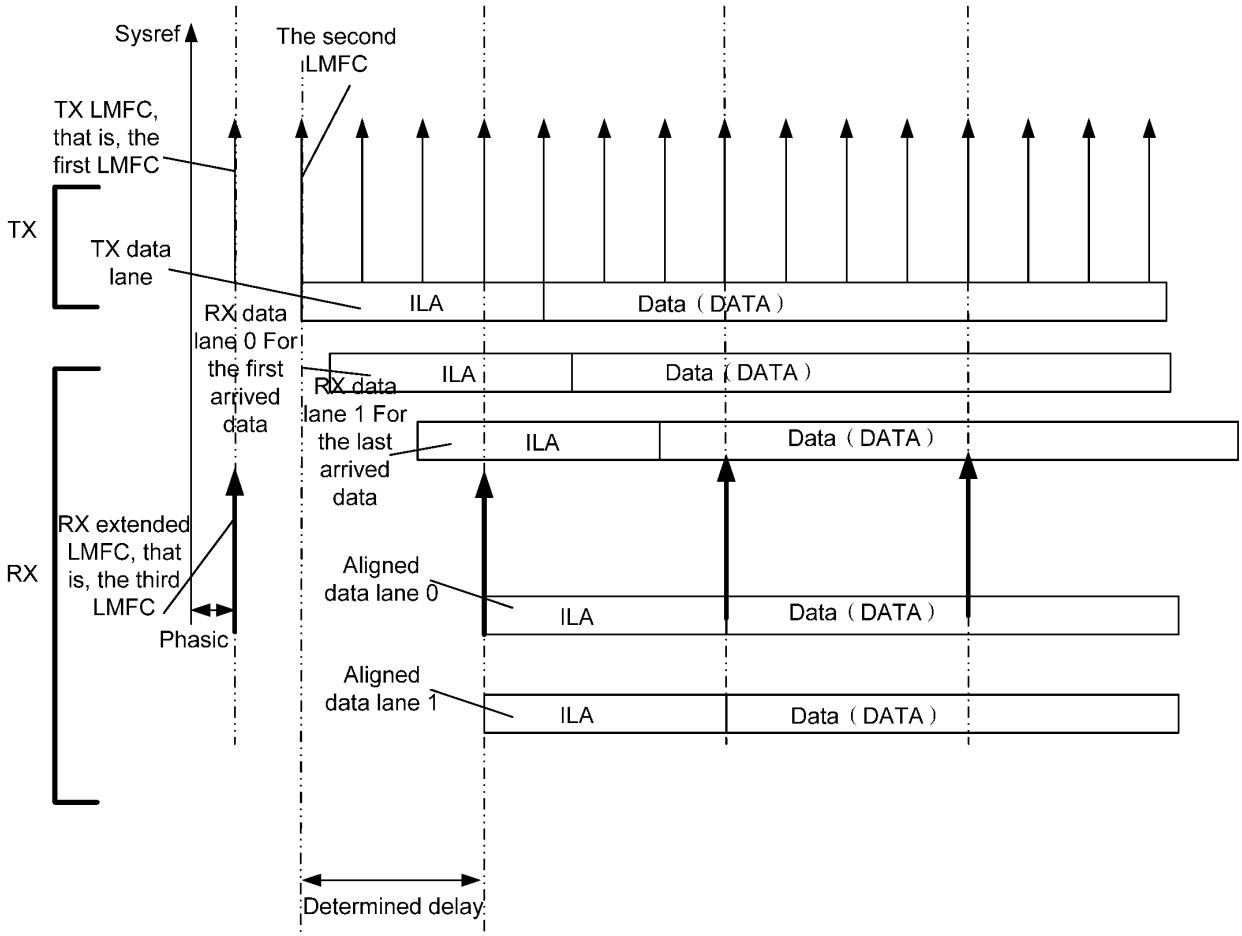

Sysref
The second LMFC
TX LMFC, that is, the first LMFC
TX
TX data lane
ILA
Data（DATA）
RX data lane 0 For the first arrived data
RX data lane 1 For the last arrived data
RX
RX extended LMFC, that is, the third LMFC
Phasic
Aligned data lane 0
Aligned data lane 1
Determined delay

Fig. 3

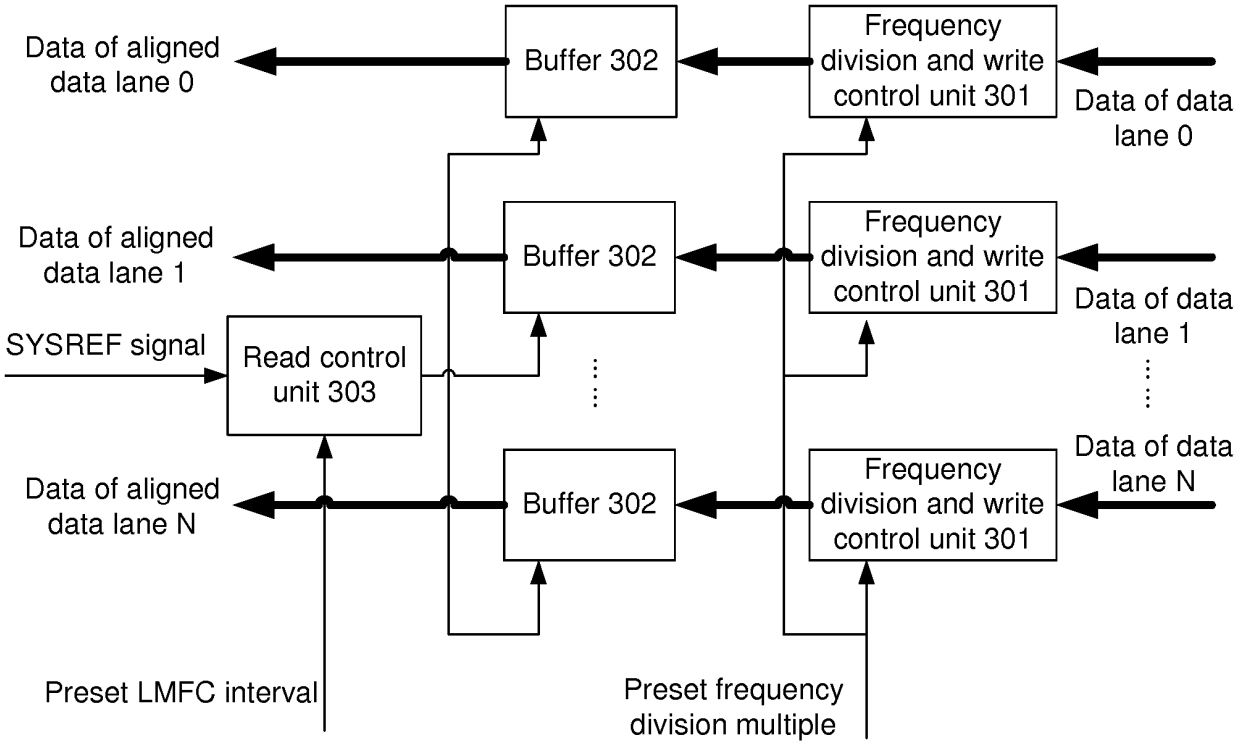

Data of aligned data lane 0
Buffer 302
Frequency division and write control unit 301
Data of data lane 0
Data of aligned data lane 1
Buffer 302
Frequency division and write control unit 301
Data of data lane 1
SYSREF signal
Read control unit 303
Data of aligned data lane N
Buffer 302
Frequency division and write control unit 301
Data of data lane N
Preset LMFC interval
Preset frequency division multiple

Fig. 4

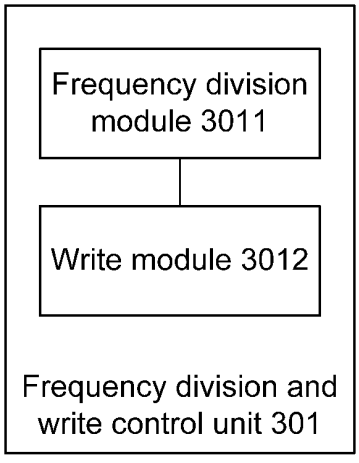
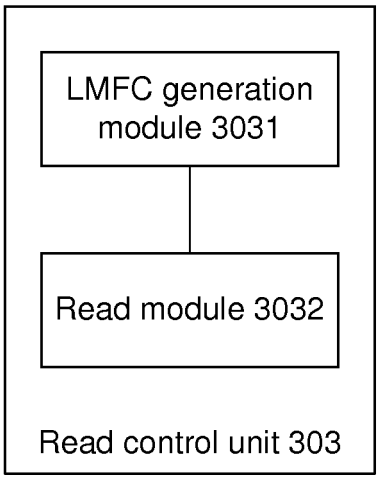

Frequency division module 3011
Write module 3012
Frequency division and write control unit 301

Fig. 5


LMFC generation module 3031
Read module 3032
Read control unit 303

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2015/076547

A. CLASSIFICATION OF SUBJECT MATTER

G06F 13/42 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F; H04L; H04Q

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, CNKI, EPODOC, WPI: analog to digital conversion, local multifrequency clock, frequency division, low voltage differential signal, system reference signal, LMFC, divide, frequency, ADC, lvds, JESD204B, SYSREF

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN 104050135 A (ANALOG DEVICES, INC.), 17 September 2014 (17.09.2014), description, paragraphs [0021]-[0026]	1-11
A	CN 101366181 A (ANALOG DEVICES INC.), 11 February 2009 (11.02.2009), the whole document	1-11
A	US 2014105101 A1 (FREESCALE SEMICONDUCTOR, INC.), 17 April 2014 (17.04.2014), the whole document	1-11
A	US 2009284401 A1 (SAMPLIFY SYSTEMS, INC.), 19 November 2009 (19.11.2009), the whole document	1-11

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
01 June 2015 (01.06.2015)	**29 June 2015 (29.06.2015)**
Name and mailing address of the ISA/CN: State Intellectual Property Office of the P. R. China No. 6, Xitucheng Road, Jimenqiao Haidian District, Beijing 100088, China Facsimile No.: (86-10) 62019451	Authorized officer **ZHANG, Hangsu** Telephone No.: (86-10) **62413857**

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2015/076547

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
CN 104050135 A	17 September 2014	EP 2778942 A1	17 September 2014
		US 2014281654 A1	18 September 2014
CN 101366181 A	11 February 2009	EP 1925086 A1	28 May 2008
		WO 2007035260 A1	29 March 2007
		US 2007057835 A1	15 March 2007
US 2014105101 A1	17 April 2014	None	
US 2009284401 A1	19 November 2009	US 2010103011 A1	29 April 2010
		WO 2009140336 A2	19 November 2009

Form PCT/ISA/210 (patent family annex) (July 2009)