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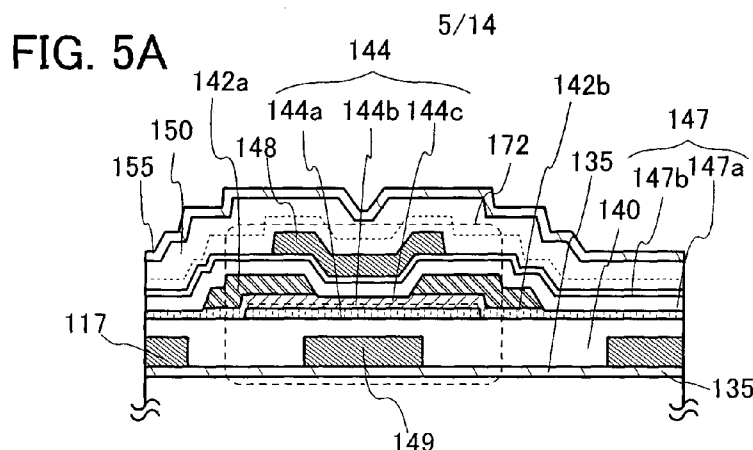
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(57) Abstract: To provide a highly reliable semiconductor device exhibiting stable electrical characteristics. To fabricate a highly reliable semiconductor device. Included are an oxide semiconductor stack in which a first oxide semiconductor layer, a second oxide semiconductor layer, and a third oxide semiconductor layer are stacked, a source and a drain electrode layers contacting the oxide semiconductor stack, a gate electrode layer overlapping with the oxide semiconductor layer with a gate insulating layer provided therebetween, and a first and a second oxide insulating layers between which the oxide semiconductor stack is sandwiched. The first to the third oxide semiconductor layers each contain indium, gallium, and zinc. The proportion of indium in the second oxide semiconductor layer is higher than that in each of the first and the third oxide semiconductor layers. The first oxide semiconductor layer is amorphous. The second and the third oxide semiconductor layers each have a crystalline structure.

## DESCRIPTION

**SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME**

## 5 TECHNICAL FIELD

[0001]

The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.

[0002]

- 10 Note that a semiconductor device in this specification refers to all devices which can function by utilizing semiconductor characteristics, and electro-optical devices, semiconductor circuits, and electronic devices are all semiconductor devices.

## BACKGROUND ART

15 [0003]

- Attention has been focused on a technique for forming a transistor including a semiconductor thin film formed over a substrate having an insulating surface (also referred to as a thin film transistor). The transistor is applied to a wide range of electronic devices such as an integrated circuit (IC) or an image display device (display device). A silicon-based semiconductor material is widely known as a material for a semiconductor thin film applicable to a transistor. As another material, an oxide semiconductor has been attracting attention.

[0004]

- For example, a transistor including an oxide semiconductor containing indium (In), gallium (Ga), and zinc (Zn) is disclosed in Patent Document 1.

[0005]

- An oxide semiconductor film can be formed by a technique for forming a thin film, such as a sputtering method. Further, the oxide semiconductor film can be formed at a relatively low temperature compared to a silicon semiconductor or the like.
- 30 Hence, the oxide semiconductor film can be formed to overlap with another transistor. For example, Patent Document 2 discloses a semiconductor device in which a cell area is reduced by providing, over a transistor including silicon, a transistor including an

oxide semiconductor layer serving as a channel formation region.

[Reference]

[0006]

[Patent Document 1] Japanese Published Patent Application No. 2006-165528

5 [Patent Document 2] Japanese Published Patent Application No. 2012-15500

## DISCLOSURE OF INVENTION

[0007]

10 In a transistor including an oxide semiconductor layer serving as a channel formation region, an oxygen vacancy (an oxygen defect) is generated by release of oxygen from the oxide semiconductor layer, and a carrier is generated due to the oxygen vacancy. Further, entry of an impurity such as hydrogen into the oxide semiconductor layer causes generation of a carrier.

[0008]

15 The carrier generated in the oxide semiconductor layer increases the off-state current of the transistor and a variation in threshold voltage. Thus, a shift in electrical characteristics of the transistor occurs, leading to a reduction in reliability of a semiconductor device.

[0009]

20 In view of the foregoing problem, an object of one embodiment of the present invention is to provide a highly reliable semiconductor device exhibiting stable electrical characteristics. Another object of one embodiment of the present invention is to fabricate a highly reliable semiconductor device.

[0010]

25 A semiconductor device of one embodiment of the present invention includes an oxide semiconductor stack in which a first oxide semiconductor layer, a second oxide semiconductor layer, and a third oxide semiconductor layer are stacked, and a first oxide insulating layer and a second oxide insulating layer between which the oxide semiconductor stack is provided. In the semiconductor device, the first oxide  
30 semiconductor layer, the second oxide semiconductor layer, and the third oxide semiconductor layer each contain at least indium, the proportion of indium in the second oxide semiconductor layer is higher than that in each of the first oxide

semiconductor layer and the third oxide semiconductor layer, the first oxide semiconductor layer is amorphous, and the second oxide semiconductor layer and the third oxide semiconductor layer each have a crystalline structure.

[0011]

5            Since the proportion of indium in the second oxide semiconductor layer is higher than that in each of the first oxide semiconductor layer and the third oxide semiconductor layer, the second oxide semiconductor layer has high carrier mobility and serves as a carrier path. Hence, a carrier flows in a region apart from the oxide insulating layers provided under and over the oxide semiconductor stack. Thus, an  
10 effect of impurities or the like entering from the oxide insulating layers can be reduced.

[0012]

Materials of the oxide semiconductor stack are selected as appropriate so that a well-shaped structure (also referred to as a well structure) is formed in which the bottom of the conduction band of the second oxide semiconductor layer is at the deepest energy  
15 level. Specifically, materials may be selected as appropriate so that the bottom of the conduction band of the second oxide semiconductor layer is deeper from the vacuum level than the bottoms of the conduction bands of the first and the third oxide semiconductor layers.

[0013]

20            Further, when silicon or carbon which is one of Group 14 elements is contained as an impurity in the oxide semiconductor layer, it can work as a donor and form an n-type region. Thus, the concentration of silicon contained in the oxide semiconductor layer is made lower than or equal to  $3 \times 10^{18}$  atoms/cm<sup>3</sup>, preferably lower than or equal to  $3 \times 10^{17}$  atoms/cm<sup>3</sup>. Further, the concentration of carbon in the oxide  
25 semiconductor layer is made lower than or equal to  $3 \times 10^{18}$  atoms/cm<sup>3</sup>, preferably lower than or equal to  $3 \times 10^{17}$  atoms/cm<sup>3</sup>. It is particularly preferable to employ a structure where the first and the third oxide semiconductor layers sandwich or surround the second oxide semiconductor layer serving as a carrier path so that a large number of Group 14 elements do not enter the second oxide semiconductor layer. That is to say,  
30 the first and the third oxide semiconductor layer can also be called barrier layers which prevent Group 14 elements such as silicon from entering the second oxide

semiconductor layer.

[0014]

When hydrogen or moisture is contained as an impurity in the oxide semiconductor stack, it can work as a donor and form an n-type region. Therefore, in terms of achieving the well-shaped structure, it is advantageous to provide a protective film (e.g., a silicon nitride film) that prevents entry of hydrogen or moisture from outside, under or over the oxide semiconductor stack.

[0015]

With the oxide semiconductor layers having the above stacked-layer structure, a region where a channel is formed can have an absorption coefficient due to the localized states measured by a constant photocurrent method (CPM) which is lower than or equal to  $3 \times 10^{-3}/\text{cm}$  (lower than or equal to  $3 \times 10^{13}/\text{cm}^3$  when converted into density of states).

[0016]

A semiconductor device of one embodiment of the present invention includes a first oxide insulating layer formed over a semiconductor substrate, an oxide semiconductor stack in which a first oxide semiconductor layer, a second oxide semiconductor layer, and a third oxide semiconductor layer are stacked over the first oxide insulating layer, a second oxide insulating layer over the oxide semiconductor stack, and a first gate electrode layer overlapping with the oxide semiconductor stack with the second oxide insulating layer provided therebetween. In the semiconductor device, the first to the third oxide semiconductor layers each contain at least indium, the proportion of indium in the second oxide semiconductor layer is higher than the proportion of indium in each of the first oxide semiconductor layer and the third oxide semiconductor layer, the second oxide semiconductor layer and the third oxide semiconductor layer each have a crystalline structure, and the first oxide semiconductor layer is amorphous.

[0017]

In addition to the above-described structure, a first nitride insulating layer may be provided under the first oxide semiconductor layer, and a second nitride insulating layer may be provided over the second oxide insulating layer. The first and the second nitride insulating layers prevent entry of hydrogen, moisture, or the like into the oxide

semiconductor stack.

[0018]

The first oxide insulating layer and the second oxide insulating layer may contain oxygen in excess of the stoichiometric composition. When oxygen is thus  
5 contained in excess of the stoichiometric composition, oxygen can be supplied to the oxide semiconductor stack, so that an oxygen vacancy can be filled with oxygen.

[0019]

In the first oxide semiconductor layer and the third oxide semiconductor layer, the concentration of at least indium may be higher than or equal to  $1 \times 10^{19}$  atoms/cm<sup>3</sup>.

10 Further, in the oxide semiconductor stack, the absorption coefficient due to localized states may be lower than or equal to  $3 \times 10^{-3}$  /cm.

[0020]

The semiconductor device may include a second gate electrode layer overlapping with the oxide semiconductor stack with the first oxide insulating layer  
15 provided therebetween.

[0021]

The second oxide semiconductor layer and the third oxide semiconductor layer may each include a crystal whose c-axis is aligned in a direction approximately perpendicular to a surface.

20 [0022]

The first oxide semiconductor layer, the second oxide semiconductor layer, and the third oxide semiconductor layer may each contain indium, zinc, and gallium. In particular, when the first oxide semiconductor layer, the second oxide semiconductor layer, and the third oxide semiconductor layer are formed using the same elements,  
25 scatterings at the interface between the first and the second oxide semiconductor layers and the interface between the second and the third oxide semiconductor layers can be reduced.

[0023]

The concentration of silicon in each of the first oxide semiconductor layer and  
30 the third oxide semiconductor layer may be lower than or equal to  $3 \times 10^{18}$  atoms/cm<sup>3</sup>. The concentration of carbon in each of the first oxide semiconductor layer and the third

oxide semiconductor layer may be lower than or equal to  $3 \times 10^{18}$  atoms/cm<sup>3</sup>.

[0024]

Another embodiment of the present invention is a method for fabricating a semiconductor device, including the following steps: forming a first oxide insulating layer over a semiconductor substrate; over the first oxide insulating layer, forming a first oxide semiconductor layer being amorphous and a second oxide semiconductor layer having a crystalline structure; performing first heat treatment in an atmosphere of oxygen and nitrogen; forming a third oxide semiconductor layer having a crystalline structure over the second oxide semiconductor layer; forming a second oxide insulating layer over the third oxide semiconductor layer; and performing second heat treatment in an atmosphere of oxygen and nitrogen.

[0025]

Another embodiment of the present invention is a method for fabricating a semiconductor device, including the following steps: forming a first oxide insulating layer over a semiconductor substrate; over the first oxide insulating layer, stacking a first oxide semiconductor layer being amorphous and a second oxide semiconductor layer having a crystalline structure; and forming a third oxide semiconductor layer over the second oxide semiconductor layer. Crystal growth of the third oxide semiconductor layer using a crystal in the second oxide semiconductor layer as a seed occurs.

[0026]

Note that a semiconductor substrate provided with a transistor may be used as the semiconductor substrate.

[0027]

According to one embodiment of the present invention, it is possible to provide a highly reliable semiconductor device that includes an oxide semiconductor and exhibits stable electrical characteristics. It is possible to fabricate a highly reliable semiconductor device.

## 30 BRIEF DESCRIPTION OF DRAWINGS

[0028]

FIG. 1 is a cross-sectional view illustrating a semiconductor device according

to one embodiment of the present invention.

FIGS. 2A and 2B are views illustrating a method for fabricating a semiconductor device, according to one embodiment of the present invention.

FIGS. 3A and 3B are views illustrating a method for fabricating a semiconductor device, according to one embodiment of the present invention.

FIGS. 4A and 4B are cross-sectional views each illustrating a semiconductor device according to one embodiment of the present invention.

FIGS. 5A to 5C are cross-sectional views each illustrating a semiconductor device according to one embodiment of the present invention.

FIGS. 6A and 6B are circuit diagrams each illustrating a semiconductor device according to one embodiment of the present invention.

FIGS. 7A to 7C are circuit diagrams and a conceptual diagram of a semiconductor device according to one embodiment of the present invention.

FIG. 8 is a block diagram of a semiconductor device according to one embodiment of the present invention.

FIG. 9 is a block diagram of a semiconductor device according to one embodiment of the present invention.

FIG. 10 is a block diagram of a semiconductor device according to one embodiment of the present invention.

FIGS. 11A and 11B illustrate an electronic device in which a semiconductor device according to one embodiment of the present invention can be used.

FIG. 12A is a view illustrating an oxide semiconductor stack included in a semiconductor device according to one embodiment of the present invention, FIG. 12B is a band diagram of the oxide semiconductor stack, and FIG. 12C is a band diagram of an oxide semiconductor stack included in a semiconductor device according to another embodiment of the present invention.

FIG. 13 is a top view illustrating an example of an apparatus for fabricating a semiconductor device.

FIG. 14A shows energy from a vacuum level to a bottom of a conduction band of an oxide semiconductor stack, and FIG. 14B is a band diagram thereof.

## BEST MODE FOR CARRYING OUT THE INVENTION



[0029]

Hereinafter, embodiments of the present invention will be described in detail with reference to the accompanying drawings. However, the present invention is not limited to the description below, and it is easily understood by those skilled in the art that modes and details thereof can be modified in various ways. Therefore, the present invention is not construed as being limited to description of the embodiments.

[0030]

Further, in embodiments hereinafter described, the same parts are denoted with the same reference numerals throughout the drawings. Note that the thickness, width, relative positional relation, and the like of components, i.e., a layer, a region, and the like, which are illustrated in the drawings are exaggerated for clarification of descriptions of the embodiments in some cases.

[0031]

Note that the term such as “over” in this specification and the like does not necessarily mean that a component is placed “directly on” another component. For example, the expression “a gate electrode layer over an insulating layer” does not exclude the case where there is an additional component between the insulating layer and the gate electrode layer. The same applies to the term “below”.

[0032]

In this specification and the like, the term “electrode layer” or “wiring layer” does not limit the function of components. For example, an “electrode layer” can be used as part of a “wiring layer”, and the “wiring layer” can be used as part of the “electrode layer”. In addition, the term “electrode layer” or “wiring layer” can also mean a combination of a plurality of “electrode layers” and “wiring layers”, for example.

[0033]

Functions of a “source” and a “drain” are sometimes replaced with each other when a transistor of opposite polarity is used or when the direction of current flowing is changed in circuit operation, for example. Therefore, the terms “source” and “drain” can be replaced with each other in this specification.

[0034]

Note that in this specification and the like, the term “electrically connected”

includes the case where components are connected through an object having any electric function. There is no particular limitation on an object having any electric function as long as electric signals can be transmitted and received between components that are connected through the object.

5 [0035]

Examples of an “object having any electric function” are an electrode and a wiring.

[0036]

(Embodiment 1)

10 In this embodiment, a semiconductor device according to one embodiment of the present invention is described in detail with reference to drawings. FIG. 1 illustrates a semiconductor device of one embodiment of the present invention.

[0037]

The semiconductor device includes a transistor 160 including a first  
15 semiconductor material, and a transistor 162 including a second semiconductor material formed over the transistor 160.

[0038]

Here, the semiconductor materials included in the transistor 160 and the transistor 162 preferably have different band gaps. For example, a silicon-based  
20 semiconductor (single crystal silicon, polycrystalline silicon, or the like) can be used for the first semiconductor material, and an oxide semiconductor can be used for the second semiconductor material. A transistor including a silicon-based semiconductor can easily operate at high speed. A transistor including an oxide semiconductor, on the other hand, has low off-state current owing to its characteristics.

25 [0039]

The transistor 160 illustrated in FIG. 1 includes a gate insulating layer 108 over the substrate 100 and a gate electrode layer 110 over the gate insulating layer 108. Note that the substrate 100 is provided with a channel formation region, a source region, and a drain region. An element isolation insulating layer 102 is provided to surround  
30 the transistor 160. A wiring layer 112 that is electrically connected to the transistor 160 is provided over the element isolation insulating layer 102.

[0040]

Note that a sidewall insulating layer may be provided in contact with the side surface of the gate electrode layer 110 of the transistor 160. When the sidewall insulating layer is not provided as illustrated in FIG. 1, high integration can be achieved.  
[0041]

5           An insulating layer 104 is formed over the transistor 160, the element isolation insulating layer 102, and the wiring layer 112. An opening reaching the wiring layer 112 is formed in the insulating layer 104. A wiring layer 114 is formed in the opening. The wiring layer 114 can be formed in such a way that, after the opening is formed in the insulating layer 104, a conductive film is formed in the opening, and the insulating  
10   layer 104 and the conductive film are planarized by chemical mechanical polishing (CMP) or the like.  
[0042]

          A wiring layer 115 is formed over the insulating layer 104. The wiring layer 115 has a stacked-layer structure of a wiring layer 115a, a wiring layer 115b, and a  
15   wiring layer 115c. However, the wiring layer 115 is not limited to this structure and may be provided in accordance with needed characteristics. An insulating layer 120 is provided over the wiring layer 115. The top surface of the insulating layer 120 is flat; thus, unevenness due to the transistor 160 and the wiring layer 115 is reduced.  
[0043]

20           An insulating layer 135 is provided over the insulating layer 120. The insulating layer 135 is formed using a film having a blocking property in order to inhibit the degradation in the characteristics of the transistor 160 which is caused by the release of hydrogen or the like from the transistor 162 and to prevent impurities due to the transistor 160 from entering the transistor 162. Here, examples of the impurities that  
25   enter the transistor 162 include hydrogen, moisture, and nitrogen. Thus, a film that does not transmit these impurities is preferably used for the insulating layer 135.  
[0044]

          In an opening formed in the insulating layer 135 and the insulating layer 120, a wiring layer 116 is formed in contact with the wiring layer 115. A wiring layer 117  
30   being in contact with the wiring layer 116 is formed over the insulating layer 135. An insulating layer 140 is formed over the wiring layer 117.  
[0045]

The insulating layer 140 may be a film which contains oxygen in excess of the stoichiometric composition. With the use of the insulating layer 140 containing oxygen in excess of in the stoichiometric composition, oxygen can be supplied to an oxide semiconductor stack 144 that is in contact with the insulating layer 140. Thus, oxygen vacancies of the oxide semiconductor stack 144 can be reduced.

[0046]

The top surface of the insulating layer 140 is subjected to planarization treatment by chemical mechanical polishing or the like, so that unevenness due to the transistor 160, the wiring layer 115, the wiring layer 117, and the like is reduced. By the improvement in planarity of the top surface of the insulating layer 140, the oxide semiconductor stack 144 can be made uniform in thickness distribution and the characteristics of the transistor 162 can be improved.

[0047]

The transistor 162 is formed over the insulating layer 140. The transistor 162 includes the oxide semiconductor stack 144, a source electrode layer 142a and a drain electrode layer 142b that are in contact with the oxide semiconductor stack 144, a gate insulating layer 147 over the oxide semiconductor stack 144, the source electrode layer 142a, and the drain electrode layer 142b, a gate electrode layer 148 over the gate insulating layer 147, an insulating layer 150 over the gate electrode layer 148, and an insulating layer 155.

[0048]

In the oxide semiconductor stack 144, a first oxide semiconductor layer 144a, a second oxide semiconductor layer 144b, and a third oxide semiconductor layer 144c are stacked. The second oxide semiconductor layer 144b is formed using an oxide semiconductor having higher carrier density than the first oxide semiconductor layer 144a and the third oxide semiconductor layer 144c. Thus, a channel is formed in the second oxide semiconductor layer 144b having high carrier density, and the region where the channel is formed can be apart from the interface between the oxide semiconductor stack 144 and the insulating layer.

[0049]

Further, the first oxide semiconductor layer 144a is amorphous, and the second oxide semiconductor layer 144b and the third oxide semiconductor layer 144c each have

a crystalline structure. A semiconductor film having a crystalline structure is used for the second oxide semiconductor layer 144b, whereby the effect of oxygen vacancies in the channel formation region can be reduced.

[0050]

5           Crystal growth of the third oxide semiconductor layer 144c occurs using a crystal in the second oxide semiconductor layer 144b as a seed. Thus, in some cases, a region of the third oxide semiconductor layer 144c which overlaps with the second oxide semiconductor layer 144b has a crystalline structure and a region of the third oxide semiconductor layer 144c which does not overlap with the second oxide semiconductor layer 144b (a region being in contact with the insulating layer 140 and the side surfaces of the first oxide semiconductor layer 144a) has an amorphous structure. Hence, in drawings, the hatch patterns of the region of the third oxide semiconductor layer 144c which overlaps with the second oxide semiconductor layer 144b and the other region of the third oxide semiconductor layer 144c are different from each other.

[0051]

          Note that the second oxide semiconductor layer 144b and the third oxide semiconductor layer 144c each have a crystalline structure and the interface between the second oxide semiconductor layer 144b and the third oxide semiconductor layer 144c is not clearly observed in some cases. Hence, the interface between the second oxide semiconductor layer 144b and the third oxide semiconductor layer 144c is indicated by a dotted line in drawings.

[0052]

25           Next, a method for fabricating the semiconductor device of one embodiment of the present invention is described. First, an insulating film which is to be the gate insulating layer 108 is formed over the substrate 100.

[0053]

30           A single crystal semiconductor substrate or a polycrystalline semiconductor substrate of silicon, silicon carbide, or the like or a compound semiconductor substrate of silicon germanium or the like may be used as the substrate 100. Alternatively, an SOI substrate, a semiconductor substrate over which a semiconductor element is provided, or the like can be used.

[0054]

Further alternatively, a glass substrate of barium borosilicate glass, aluminoborosilicate glass, or the like, a ceramic substrate, a quartz substrate, a sapphire substrate, or the like over which a semiconductor layer is formed by a sputtering method, a vapor phase growth method such as a plasma CVD method, or the like may be used. As the semiconductor layer, any of the following can be used: amorphous silicon; polycrystalline silicon obtained by crystallization of amorphous silicon by laser annealing or the like; single crystal silicon obtained in such a manner that a surface portion of a single crystal silicon wafer is separated after implantation of hydrogen ions or the like into the silicon wafer; and the like. Any of these semiconductor layers may be processed into an island-like shape by a photolithography step.

[0055]

A protective layer which is to be a mask for forming the element isolation insulating layer is formed, and etching is performed with the use of the protective layer as a mask, whereby a part of the substrate 100 which is not covered with the protective layer is removed. Thus, a plurality of isolated semiconductor regions is formed in an upper portion of the substrate 100. After an insulating layer is formed to cover the isolated semiconductor regions, the insulating layer which overlaps with the semiconductor regions is selectively removed. In this manner, the element isolation insulating layer 102 is formed.

[0056]

Next, the gate insulating layer 108 and the gate electrode layer 110 are stacked. The gate electrode layer 108 can be formed by a sputtering method, a molecular beam epitaxy (MBE) method, a chemical vapor deposition (CVD) method, a pulsed laser deposition (PLD) method, an atomic layer deposition (ALD) method, or the like, as appropriate. When the gate electrode layer 108 is formed by a sputtering method, an impurity element such as hydrogen can be reduced.

[0057]

The gate insulating layer 108 can be formed using an inorganic insulating film. It is preferable to use, for example, a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, an aluminum oxynitride film, a hafnium oxide film, a gallium oxide film, a silicon nitride film, an aluminum nitride film, a silicon nitride oxide film,

or an aluminum nitride oxide film. Further, the gate insulating layer 108 can be formed with a single-layer structure or a stacked-layer structure including two or more layers with the use of these compounds.

[0058]

5           The gate electrode layer 110 (and the wiring layer 112 formed using the same conductive film as the gate electrode layer 110, and the like) may be formed using a metal material such as molybdenum, titanium, tantalum, tungsten, aluminum, copper, chromium, neodymium, or scandium, or an alloy material containing any of these materials as its main component by a plasma CVD method, a sputtering method, or the  
10   like. The gate electrode layer 110 may also be formed using a semiconductor film typified by a polycrystalline silicon film doped with an impurity element such as phosphorus, or a silicide film of nickel silicide or the like. Further, the gate electrode layer 110 may also be formed using a conductive material such as indium tin oxide, indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide,  
15   indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, indium zinc oxide, or indium tin oxide to which silicon oxide is added. It is also possible that the gate electrode layer 110 has a stacked-layer structure of the above conductive material and the above metal material.

[0059]

20           Here, with the use of the gate electrode layer 110 as a mask, an impurity element imparting n-type conductivity or an impurity element imparting p-type conductivity is introduced to the substrate 100. Thus, a source region and a drain region are formed. As the method for introducing the impurity element, an ion implantation method, an ion doping method, a plasma immersion ion implantation  
25   method, or the like can be used.

[0060]

          Phosphorus, boron, nitrogen, arsenic, argon, aluminum, a molecular ion containing any of these elements, or the like can be used as the impurity element to be introduced. The dosage of such an element is preferably  $1 \times 10^{13}$  ions/cm<sup>2</sup> to  $5 \times 10^{16}$   
30   ions/cm<sup>2</sup>. When phosphorus is introduced as the impurity element, the acceleration voltage is preferably 0.5 kV to 80 kV.

[0061]

Note that the treatment for introducing the impurity element may be performed plural times. In the case where the treatment for introducing the impurity element is performed plural times, the kind of impurity element may be the same in the plural treatments or different in every treatment.

5 [0062]

By the above process, the transistor 160 can be fabricated.

[0063]

Next, the insulating layer 104 is formed to cover the gate electrode layer 110, the gate insulating layer 108, the element isolation insulating layer 102, and the wiring layer 112. The insulating layer 104 can be formed using a material and a method which are similar to those of the gate insulating layer 108.

[0064]

Further, an opening is formed in the insulating layer 104, and the wiring layer 114 is formed in the opening (see FIG. 2A). The wiring layer 114 can be formed using a material and a method which are similar to those of the wiring layer 112.

[0065]

Next, the wiring layer 115 is formed over the insulating layer 104. The wiring layer 115 can be formed using a material and a method which are similar to those of the wiring layer 112.

20 [0066]

Here, in order to reduce the resistance of the wiring layer 115 and allow the wiring layer 115 to have heat resistance, the wiring layer 115 has a three-layer structure. In the three-layer structure, an aluminum film having low resistivity is used as the wiring layer 115b, and titanium films each having a high melting point are formed as the wiring layer 115a and the wiring layer 115c over and under the aluminum film.

[0067]

Note that after conductive films to be the wiring layer 115 are formed, the conductive films are etched. In the step of etching the conductive films, the insulating layer 104 is also etched concurrently and is reduced in thickness in some cases. Hence, a region of the insulating layer 104 which overlaps with the wiring layer 115 has a larger thickness than the other region in some cases. Thus, a surface of the insulating layer 104 sometimes has unevenness.



[0068]

Next, the insulating layer 120 is formed over the insulating layer 104 and the wiring layer 115. The insulating layer 120 can be formed using an inorganic material which is similar to that of the gate insulating layer 108 or an organic material such as a polyimide resin, an acrylic resin, or a benzocyclobutene-based resin so that unevenness due to the transistor 160, the insulating layer 104, and the wiring layer 115 is reduced. Other than such organic materials, it is also possible to use a low dielectric constant material (low-k material) or the like. Alternatively, the insulating layer 120 may be formed by stacking a plurality of insulating films formed using any of these materials.

10 [0069]

Next, the insulating layer 135 is formed over the insulating layer 120.

[0070]

The insulating layer 135 is preferably formed using a film having a blocking property so that impurities due to the transistor 160 do not enter the transistor 162. For example, the insulating layer 135 may be formed using a film containing silicon nitride, aluminum oxide, aluminum oxynitride, gallium oxide, gallium oxynitride, yttrium oxide, yttrium oxynitride, hafnium oxide, hafnium oxynitride, or the like.

[0071]

Further, in the case where the insulating layer 135 includes a portion having low density or a portion where a film is not formed (hereinafter these portions are also collectively referred to as "cavity"), impurities enter the transistor through the cavity in some cases.

[0072]

The planarity of the insulating layer 120 may be improved in advance so that the cavity is not formed in the insulating layer 135. For example, planarization treatment such as chemical mechanical polishing treatment or plasma treatment may be performed on a surface of the insulating layer 120 before the insulating layer 135 is formed.

[0073]

After the insulating layer 135 is formed, an opening reaching the wiring layer 115 is formed in the insulating layer 135 and the insulating layer 120. The wiring layer 116 is formed in the opening. Over the insulating layer 135, the wiring layer 117

is formed in contact with the wiring layer 116. The wiring layers 116 and 117 can be formed using a material and a method which are similar to those of the gate electrode layer 110.

[0074]

5           Next, the insulating layer 140 is formed over the wiring layer 117 (see FIG. 2B). The insulating layer 140 may be formed using an oxide insulating layer containing nitrogen or an oxide insulating layer such as a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, an aluminum oxynitride film, a hafnium oxide film, or a gallium oxide film. Further, the insulating layer 140 can be formed with a single-layer  
10           structure or a stacked-layer structure including two or more layers with the use of these compounds. A film containing oxygen in excess of the stoichiometric composition may be used for the insulating layer 140 so as to supply oxygen to the oxide semiconductor stack 144 to be formed later.

[0075]

15           Further, the insulating layer 140 may be planarized by chemical mechanical polishing treatment or the like so that the oxide semiconductor stack 144 to be formed later is made uniform in film thickness distribution and is improved in crystallinity.

[0076]

            Next, the oxide semiconductor stack 144 is formed over the insulating layer  
20           140.

[0077]

            Each of the first to the third oxide semiconductor layers 144a to 144c is formed using a sputtering target which contains at least indium (In) and which allows film formation to be performed by an AC sputtering method or a DC sputtering method.

25           By containing indium, the sputtering target can have increased conductivity. With the use of such a sputtering target, film formation by an AC sputtering method or a DC sputtering method is performed more easily. The target may be such that a film formed with the use of the target contains indium at a concentration higher than or equal to  $1 \times 10^{19}$  atoms/cm<sup>3</sup> at least after the film is formed. The first oxide semiconductor  
30           layer 144a and the third oxide semiconductor layer 144c are each formed using a material that can be represented by  $\text{InM}_1\text{XZn}_Y\text{O}_Z$  ( $X \geq 1$ ,  $Y > 1$ ,  $Z > 0$ , and M1 is Ga, Hf,

or the like). Note that in the case where the first oxide semiconductor layer 144a and the third oxide semiconductor layer 144c are each formed using a material containing Ga, a material containing a high proportion of Ga, or more specifically, a material that can be represented by  $\text{InM}_1\text{Zn}_Y\text{O}_Z$  where  $X$  is larger than 10 is not suitable because, in that case, dust might be generated at the time of film formation and it is difficult to perform film formation by an AC sputtering method or a DC sputtering method.

[0078]

The second oxide semiconductor layer 144b is formed using a material that can be represented by  $\text{InM}_2\text{Zn}_Y\text{O}_Z$  ( $X \geq 1$ ,  $Y \geq X$ ,  $Z > 0$ ,  $\text{M}_2 = \text{Ga}, \text{Sn}, \text{or the like}$ ).

[0079]

In particular, in the case where the second oxide semiconductor layer 144b is In-M2-Zn oxide (M2 is Ga, Sn, or the like) and a target having the atomic ratio of metal elements of  $\text{In}:\text{M}_2:\text{Zn} = x_1:y_1:z_1$  is used for forming the second oxide semiconductor layer 144b,  $x_1/y_1$  is preferably greater than or equal to 1/3 and less than or equal to 6, further preferably greater than or equal to 1 and less than or equal to 6, and  $z_1/y_1$  is preferably greater than or equal to 1/3 and less than or equal to 6, further preferably greater than or equal to 1 and less than or equal to 6. Note that when  $z_1/y_1$  is greater than or equal to 1 and less than or equal to 6, a CAAC-OS film to be described later as the second oxide semiconductor layer 144b is easily formed. Typical examples of the atomic ratio of the metal elements of the target are  $\text{In}:\text{M}_2:\text{Zn} = 1:1:1$  and  $\text{In}:\text{M}_2:\text{Zn} = 3:1:2$ .

[0080]

Further, particularly in the case where each of the first oxide semiconductor layer 144a and the third oxide semiconductor layer 144c is In-M1-Zn oxide (M1 is Ga, Hf, or the like) and a target having the atomic ratio of the metal elements of  $\text{In}:\text{M}_1:\text{Zn} = x_2:y_2:z_2$  is used for forming each of the first oxide semiconductor layer 144a and the third oxide semiconductor layer 144c, it is preferable that  $x_2/y_2 < x_1/y_1$  and that  $z_2/y_2$  is greater than or equal to 1/3 and less than or equal to 6, further preferably greater than or equal to 1 and less than or equal to 6. Note that when  $z_2/y_2$  is greater than or equal to 1 and less than or equal to 6, CAAC-OS films to be described later are easily formed as the first oxide semiconductor layer 144a and the third oxide semiconductor layer 144c.

Typical examples of the atomic ratio of the metal elements of the target are In:M1:Zn = 1:3:2, In:M1:Zn = 1:3:4, In:M1:Zn = 1:3:6, In:M1:Zn = 1:3:8, and the like.

[0081]

As the first to the third oxide semiconductor layers 144a to 144c, oxide having  
5 the atomic ratio of In:Ga:Zn = 1:1:1 ( $=1/3:1/3:1/3$ ), In:Ga:Zn = 2:2:1 ( $=2/5:2/5:1/5$ ),  
In:Ga:Zn = 3:1:2 ( $=1/2:1/6:1/3$ ), In:Ga:Zn = 1:3:2 ( $=1/6:1/2:1/3$ ), In:Ga:Zn = 1:4:3  
( $=1/8:1/2:3/8$ ), In:Ga:Zn = 1:5:4 ( $=1/10:1/2:2/5$ ), or In:Ga:Zn = 1:6:6 ( $=1/13:6/13:6/13$ ),  
or the like may be used. Note that the first and the third oxide semiconductor layers  
144a and 144c may be formed using hafnium instead of gallium. Further, the second  
10 oxide semiconductor layer 144b may be formed using tin instead of gallium.

[0082]

Materials of the first to the third oxide semiconductor layers are selected as  
appropriate so that a well-shaped structure is formed in which the bottom of the  
conduction band of the second oxide semiconductor layer 144b is deeper from the  
15 vacuum level than the bottoms of the conduction bands of the first and the third oxide  
semiconductor layers 144a and 144c. The depth of a bottom of a conduction band  
from a vacuum level (such depth can also be expressed as electron affinity) can be  
obtained by subtracting a difference in energy between the bottom of the conduction  
band and a top of a valence band (what is called a band gap) from a difference in energy  
20 between the vacuum level and the top of the valence band (what is called an ionization  
potential).

[0083]

Note that the ionization potential of an oxide semiconductor which is used for  
obtaining electron affinity can be measured by ultraviolet photoelectron spectroscopy  
25 (UPS) or the like. As a typical measurement device of UPS, VersaProbe  
(manufactured by ULVAC-PHI, Inc) is used. The electron affinity refers to a  
difference in energy between the vacuum level ( $E_{\infty}$ ) and an end of the conduction band  
( $E_c$ ). Further, energy band gap ( $E_g$ ) can be measured by a full automatic spectroscopic  
ellipsometer UT-300. The energy of the bottom of the conduction band is obtained by  
30 subtracting the energy band gap from the value of the ionization potential, and thus, the  
band structure of a single layer or stacked layers can be formed. By using this method,

it can be confirmed whether a buried channel is formed with the use of the stacked-layer structure disclosed in this specification. FIGS. 14A and 14B each illustrate an example thereof.

[0084]

5           FIG. 14A shows data of energy from the vacuum level to the bottom of the conduction band. FIG. 14B shows the band structure formed on the basis of the data. To obtain the data, a sample with a stacked-layer structure is formed in such a manner that, after a 10 nm thick film is formed using an In-Ga-Zn oxide sputtering target having a composition of In:Ga:Zn = 1:1:1 [atomic ratio] under an atmosphere where the  
10           proportion of oxygen is 100 %, a 10 nm thick film is formed using an In-Ga-Zn oxide sputtering target having a composition of In:Ga:Zn = 3:1:2 [atomic ratio] under an atmosphere where the proportion of argon is 100 %, and then, a 10 nm thick film is formed using an In-Ga-Zn oxide sputtering target having a composition of In:Ga:Zn =  
1:1:1 [atomic ratio] under an atmosphere where the proportion of oxygen is 100 %.  
15           With the use of the sample, an ionization potential is measured, and an energy band gap is measured by a full automatic spectroscopic ellipsometer UT-300. The energy from the vacuum level to the bottom of the conduction band is obtained by subtracting the energy band gap from the ionization potential. It is found from FIG. 14B that a well-shaped structure is formed in which the bottom of the conduction band of the  
20           second oxide semiconductor layer is deeper from the vacuum level than the bottoms of the conduction bands of the first and the third oxide semiconductor layers.

[0085]

          Further, in the case where the first to the third oxide semiconductor layers 144a to 144c are formed using an In-Ga-Zn oxide, the constituent elements of the first to the  
25           third oxide semiconductor layers 144a to 144c are the same. Hence, the number of trap levels at the interface between the first oxide semiconductor layer 144a and the second oxide semiconductor layer 144b and the interface between the second oxide semiconductor layer 144b and the third oxide semiconductor layer 144c is small. Thus, it is possible to reduce a change of a transistor over time and a change in threshold  
30           voltage due to stress test.

[0086]

In Ga, the formation energy of oxygen vacancies is larger and thus oxygen vacancies are less likely to occur, than in In; therefore, the oxide having a composition in which the proportion of In is equal to or lower than that of Ga has more stable characteristics than the oxide having a composition in which the proportion of In is higher than that of Ga. Hence, the interface between the first oxide semiconductor layer 144a and a silicon insulating layer and the interface between the third oxide semiconductor layer 144c and a silicon insulating layer can be stable. Thus, a highly reliable semiconductor device can be obtained.

[0087]

In an oxide semiconductor, the s orbital of heavy metal mainly contributes to carrier transfer, and when the proportion of In in the oxide semiconductor is increased, overlap of the s orbital is likely to be increased. Therefore, oxide having a composition in which the proportion of In is higher than that of Ga has higher mobility than oxide having a composition in which the proportion of In is equal to or lower than that of Ga. Hence, when a carrier is formed in the second oxide semiconductor layer 144b containing a high proportion of indium, high mobility can be achieved.

[0088]

A material of the second oxide semiconductor layer 144b is selected as appropriate so that the bottom of the conduction band of the second oxide semiconductor layer 144b forms a well-shaped structure. An example of the well-shaped structure is illustrated in FIG. 12B. FIG. 12B is an energy band diagram along Y1-Y2 in a transistor illustrated in FIG. 12A. Note that the transistor illustrated in FIG. 12A has a structure similar to that of a transistor 163 illustrated in FIG. 4A; therefore, a detailed description thereof is omitted.

[0089]

Here, when silicon or carbon which is one of Group 14 elements is contained as an impurity in the oxide semiconductor layer, it can work as a donor and form an n-type region. Thus, the concentration of silicon in each oxide semiconductor layer is less than or equal to  $3 \times 10^{18}$  atoms/cm<sup>3</sup>, preferably less than or equal to  $3 \times 10^{17}$  atoms/cm<sup>3</sup>. Further, the concentration of carbon is less than or equal to  $3 \times 10^{18}$  atoms/cm<sup>3</sup>, preferably less than or equal to  $3 \times 10^{17}$  atoms/cm<sup>3</sup>. In particular, it is

preferable to use a structure in which the first oxide semiconductor layer 144a and the third oxide semiconductor layer 144c sandwich or surround the second oxide semiconductor layer 144b to be a carrier path so that Group 14 elements are prevented from being contained at a high proportion in the second oxide semiconductor layer 144b.

- 5 That is to say, the first and the third oxide semiconductor layer 144a and 144c can also be called barrier layers which prevent Group 14 elements such as silicon from entering the second oxide semiconductor layer 144b.

[0090]

- Hydrogen contained in the oxide semiconductor stack 144 reacts with oxygen  
10 bonded to metal to produce water, and a defect is formed in a lattice from which oxygen is released (or a portion from which oxygen is removed). In addition, a bond of a part of hydrogen and oxygen causes generation of electrons serving as carriers. Thus, the impurities containing hydrogen are reduced as much as possible in the step of forming the oxide semiconductor stack 144, whereby the hydrogen concentration in the oxide  
15 semiconductor stack 144 can be reduced. When the oxide semiconductor stack 144 which is highly purified by removing hydrogen as much as possible is used as a channel formation region, a shift of the threshold voltage in the negative direction can be reduced, and the leakage current between a source and a drain of the transistor (typically, the off-state current or the like) can be decreased to several yoctoamperes per  
20 micrometer to several zeptoamperes per micrometer. As a result, electric characteristics of the transistor can be improved.

[0091]

- When the oxide semiconductor films to be semiconductor layers of the transistor have the above-described stacked-layer structure, in a region where a channel  
25 is formed, an absorption coefficient due to the localized states measured by a constant photocurrent method (CPM) can be lower than or equal to  $3 \times 10^{-3}/\text{cm}$  (lower than or equal to  $3 \times 10^{13}/\text{cm}^3$  when converted into density of states).

[0092]

- The above-described stacked-layer structure is an example in which one  
30 well-shaped structure is formed using the first to the third oxide semiconductor layers; however, the present invention is not limited to the above-described stacked layer

structure. A plurality of well-shaped structures may be formed using the second oxide semiconductor layer with a multilayer structure. FIG. 12C illustrates an example thereof.

[0093]

5 As a sputtering gas, a rare gas (typically argon) atmosphere, an oxygen atmosphere, or a mixed gas of a rare gas and oxygen is used as appropriate. In the case of using the mixed gas of a rare gas and oxygen, the proportion of oxygen is preferably higher than that of a rare gas.

[0094]

10 The target for forming the oxide semiconductor layer may be selected as appropriate in accordance with the composition of the oxide semiconductor layer to be formed.

[0095]

As an example of the target, an In-Ga-Zn oxide target is described below.

15 [0096]

The In-Ga-Zn oxide target, which is polycrystalline, is made by mixing  $\text{InO}_X$  powder,  $\text{GaO}_Y$  powder, and  $\text{ZnO}_Z$  powder in a predetermined molar ratio, applying pressure, and performing heat treatment at a temperature higher than or equal to 1000 °C and lower than or equal to 1500 °C. Note that  $X$ ,  $Y$ , and  $Z$  are each a given positive number. Here, the predetermined molar ratio of  $\text{InO}_X$  powder to  $\text{GaO}_Y$  powder and  $\text{ZnO}_Z$  powder is, for example, 2:2:1, 8:4:3, 3:1:1, 1:1:1, 4:2:3, or 3:1:2. The kinds of powder and the molar ratio for mixing powder may be determined as appropriate depending on the desired target.

[0097]

25 The second oxide semiconductor layer 144b and the third oxide semiconductor layer 144c may have different crystallinities. That is, any of a single crystal oxide semiconductor film, a polycrystalline oxide semiconductor film, a microcrystalline oxide semiconductor film, and a CAAC-OS film may be combined as appropriate.

[0098]

30 Here, the details of the CAAC-OS film are described. The CAAC-OS film is one of oxide semiconductor films having a plurality of c-axis aligned crystal parts. In an image obtained with a transmission electron microscope (TEM), a grain boundary in



the CAAC-OS film cannot be found. Thus, in the CAAC-OS film, a reduction in electron mobility due to the grain boundary is less likely to occur.

[0099]

In this specification, a term “parallel” indicates that the angle formed between two straight lines is greater than or equal to  $-10^\circ$  and less than or equal to  $10^\circ$ , and accordingly also includes the case where the angle is greater than or equal to  $-5^\circ$  and less than or equal to  $5^\circ$ . In addition, a term “perpendicular” indicates that the angle formed between two straight lines is greater than or equal to  $80^\circ$  and less than or equal to  $100^\circ$ , and accordingly includes the case where the angle is greater than or equal to  $85^\circ$  and less than or equal to  $95^\circ$ .

[0100]

In this specification, the trigonal and rhombohedral crystal systems are included in the hexagonal crystal system.

[0101]

According to the TEM image of the CAAC-OS film observed in a direction substantially parallel to a sample surface (cross-sectional TEM image), metal atoms are arranged in a layered manner in the crystal parts. Each metal atom layer has a morphology reflected by a surface over which the CAAC-OS film is formed (hereinafter, a surface over which the CAAC-OS film is formed is referred to as a formation surface) or a top surface of the CAAC-OS film, and is arranged in parallel to the formation surface or the top surface of the CAAC-OS film.

[0102]

On the other hand, according to the TEM image of the CAAC-OS film observed in a direction substantially perpendicular to the sample surface (plan TEM image), metal atoms are arranged in a triangular or hexagonal configuration in the crystal parts. However, there is no regularity of arrangement of metal atoms between different crystal parts.

[0103]

From the results of the cross-sectional TEM image and the plan TEM image, alignment is found in the crystal parts in the CAAC-OS film.

[0104]

Most of the crystal parts included in the CAAC-OS film each fit inside a cube whose one side is less than 100 nm. Thus, there is a case where a crystal part included in the CAAC-OS film fits a cube whose one side is less than 10 nm, less than 5 nm, or less than 3 nm. Note that when a plurality of crystal parts included in the CAAC-OS film are connected to each other, one large crystal region is formed in some cases. For example, a crystal region with an area of 2500 nm<sup>2</sup> or more, 5 μm<sup>2</sup> or more, or 1000 μm<sup>2</sup> or more is observed in some cases in the plan TEM image.

[0105]

A CAAC-OS film is subjected to structural analysis with an X-ray diffraction (XRD) apparatus. For example, when the CAAC-OS film including an InGaZnO<sub>4</sub> crystal is analyzed by an out-of-plane method, a peak appears frequently when the diffraction angle ( $2\theta$ ) is around 31°. This peak is derived from the (009) plane of the InGaZnO<sub>4</sub> crystal, which indicates that crystals in the CAAC-OS film have c-axis alignment, and that the c-axes are aligned in a direction substantially perpendicular to the formation surface or the top surface of the CAAC-OS film.

[0106]

On the other hand, when the CAAC-OS film is analyzed by an in-plane method in which an X-ray enters a sample in a direction substantially perpendicular to the c-axis, a peak appears frequently when  $2\theta$  is around 56°. This peak is derived from the (110) plane of the InGaZnO<sub>4</sub> crystal. Here, analysis ( $\phi$  scan) is performed under conditions where the sample is rotated around a normal vector of a sample surface as an axis ( $\phi$  axis) with  $2\theta$  fixed at around 56°. In the case where the sample is a single-crystal oxide semiconductor film of InGaZnO<sub>4</sub>, six peaks appear. The six peaks are derived from crystal planes equivalent to the (110) plane. On the other hand, in the case of a CAAC-OS film, a peak is not clearly observed even when  $\phi$  scan is performed with  $2\theta$  fixed at around 56°.

[0107]

According to the above results, in the CAAC-OS film having c-axis alignment, while the directions of a-axes and b-axes are different between crystal parts, the c-axes are aligned in a direction parallel to a normal vector of a formation surface or a normal vector of a top surface. Thus, each metal atom layer arranged in a layered manner

observed in the cross-sectional TEM image corresponds to a plane parallel to the a-b plane of the crystal.

[0108]

Note that the crystal part is formed concurrently with deposition of the CAAC-OS film or is formed through crystallization treatment such as heat treatment. As described above, the c-axis of the crystal is aligned in a direction parallel to a normal vector of a formation surface or a normal vector of a top surface. Thus, for example, in the case where a shape of the CAAC-OS film is changed by etching or the like, the c-axis might not be necessarily parallel to a normal vector of a formation surface or a normal vector of a top surface of the CAAC-OS film.

[0109]

Further, distribution of c-axis aligned crystal parts in the CAAC-OS film is not necessarily uniform. For example, in the case where crystal growth leading to the crystal parts of the CAAC-OS film occurs from the vicinity of the top surface of the film, the proportion of the c-axis aligned crystal parts in the vicinity of the top surface is higher than that in the vicinity of the formation surface in some cases. Further, when an impurity is added to the CAAC-OS film, a region to which the impurity is added is altered, and the proportion of the c-axis aligned crystal parts in the CAAC-OS film varies depending on regions, in some cases.

[0110]

Note that when the CAAC-OS film with an  $\text{InGaZnO}_4$  crystal is analyzed by an out-of-plane method, a peak of  $2\theta$  may also be observed at around  $36^\circ$ , in addition to the peak of  $2\theta$  at around  $31^\circ$ . The peak of  $2\theta$  at around  $36^\circ$  indicates that a crystal having no c-axis alignment is included in part of the CAAC-OS film. It is preferable that in the CAAC-OS film, a peak of  $2\theta$  appear at around  $31^\circ$  and a peak of  $2\theta$  do not appear at around  $36^\circ$ .

[0111]

The CAAC-OS film is an oxide semiconductor film having low impurity concentration. The impurity is an element other than the main components of the oxide semiconductor film, such as hydrogen, carbon, silicon, or a transition metal element. In particular, an element that has higher bonding strength to oxygen than a

metal element included in the oxide semiconductor film, such as silicon, disturbs the atomic arrangement of the oxide semiconductor film by depriving the oxide semiconductor film of oxygen and causes a decrease in crystallinity. Further, a heavy metal such as iron or nickel, argon, carbon dioxide, or the like has a large atomic radius (molecular radius), and thus disturbs the atomic arrangement of the oxide semiconductor film and causes a decrease in crystallinity when it is contained in the oxide semiconductor film. Note that the impurity contained in the oxide semiconductor film might serve as a carrier trap or a carrier generation source.

[0112]

10 The CAAC-OS film is an oxide semiconductor film having a low density of defect states. In some cases, oxygen vacancies in the oxide semiconductor film serve as carrier traps or serve as carrier generation sources when hydrogen is captured therein.

[0113]

The state in which impurity concentration is low and density of defect states is low (the number of oxygen vacancies is small) is referred to as a “highly purified intrinsic” or “substantially highly purified intrinsic” state. A highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor film has few carrier generation sources, and thus can have a low carrier density. Thus, a transistor including the oxide semiconductor film rarely has negative threshold voltage (is rarely normally on). The highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor film has few carrier traps. Accordingly, the transistor including the oxide semiconductor film has little variation in electrical characteristics and high reliability. Electric charge trapped by the carrier traps in the oxide semiconductor film takes a long time to be released, and might behave like fixed electric charge. Thus, the transistor which includes the oxide semiconductor film having high impurity concentration and a high density of defect states has unstable electrical characteristics in some cases.

[0114]

30 With the use of the CAAC-OS film in a transistor, variation in the electrical characteristics of the transistor due to irradiation with visible light or ultraviolet light is small.

[0115]

In an oxide semiconductor having a crystal part as the CAAC-OS film, defects in the bulk can be further reduced and when the surface flatness of the oxide semiconductor is improved, mobility higher than that of an oxide semiconductor in an amorphous state can be obtained. In order to improve the surface planarity, the oxide semiconductor is preferably formed over a flat surface.

[0116]

When a CAAC-OS film is formed, for example, the CAAC-OS film is formed by a sputtering method using a polycrystalline oxide semiconductor sputtering target. By collision of ions with the target, a crystal region included in the target may be separated from the target along an a-b plane; in other words, a sputtered particle having a plane parallel to an a-b plane (flat-plate-like sputtered particle or pellet-like sputtered particle) may flake off from the target. In that case, the flat-plate-like sputtered particle reaches a substrate while maintaining their crystal state, whereby the CAAC-OS film can be formed.

[0117]

For the deposition of the CAAC-OS film, the following conditions are preferably used.

[0118]

By reducing the amount of impurities entering the CAAC-OS film during the deposition, the crystal state can be prevented from being broken by the impurities. For example, the concentration of impurities (e.g., hydrogen, water, carbon dioxide, or nitrogen) which exist in the deposition chamber may be reduced. Furthermore, the concentration of impurities in a deposition gas may be reduced. Specifically, a deposition gas whose dew point is  $-80^{\circ}\text{C}$  or lower, preferably  $-100^{\circ}\text{C}$  or lower is used.

[0119]

By increasing the substrate heating temperature during the deposition, migration of a sputtered particle is likely to occur after the sputtered particle reaches a substrate surface. Specifically, the substrate heating temperature during the deposition is higher than or equal to  $100^{\circ}\text{C}$  and lower than or equal to  $740^{\circ}\text{C}$ , preferably higher than or equal to  $200^{\circ}\text{C}$  and lower than or equal to  $500^{\circ}\text{C}$ . By increasing the substrate

heating temperature during the deposition, when the flat-plate-like sputtered particle reaches the substrate, migration occurs on the substrate surface, so that a flat plane of the flat-plate-like sputtered particle is attached to the substrate.

[0120]

5 Furthermore, it is preferable that the proportion of oxygen in the deposition gas be increased and the power be optimized in order to reduce plasma damage at the deposition. The proportion of oxygen in the deposition gas is 30 vol% or higher, preferably 100 vol%.

[0121]

10 Next, a microcrystalline oxide semiconductor film will be described.

[0122]

In an image obtained with the TEM, crystal parts cannot be found clearly in the microcrystalline oxide semiconductor in some cases. In most cases, a crystal part in the microcrystalline oxide semiconductor is greater than or equal to 1 nm and less than  
15 or equal to 100 nm, or greater than or equal to 1 nm and less than or equal to 10 nm. A microcrystal with a size greater than or equal to 1 nm and less than or equal to 10 nm, or a size greater than or equal to 1 nm and less than or equal to 3 nm is specifically referred to as nanocrystal (nc). An oxide semiconductor film including nanocrystal is referred to as an nc-OS (nanocrystalline oxide semiconductor) film. In an image  
20 obtained with TEM, a crystal grain cannot be found clearly in the nc-OS film in some cases.

[0123]

In the nc-OS film, a microscopic region (for example, a region with a size greater than or equal to 1 nm and less than or equal to 10 nm, in particular, a region with  
25 a size greater than or equal to 1 nm and less than or equal to 3 nm) has a periodic atomic order. Further, there is no regularity of crystal orientation between different crystal parts in the nc-OS film; thus, the orientation of the whole film is not observed. Accordingly, in some cases, the nc-OS film cannot be distinguished from an amorphous oxide semiconductor film depending on an analysis method. For example, when the  
30 nc-OS film is subjected to structural analysis by an out-of-plane method with an XRD apparatus using an X-ray having a beam diameter larger than that of a crystal part, a

peak which shows a crystal plane does not appear. Further, a halo-like pattern is shown in a selected-area electron diffraction pattern of the nc-OS film obtained by using an electron beam having a probe diameter (e.g., larger than or equal to 50 nm) larger than that of a crystal part. Meanwhile, spots are shown in a nanobeam electron diffraction pattern of the nc-OS film obtained by using an electron beam having a probe diameter (e.g., larger than or equal to 1 nm and smaller than or equal to 30 nm) close to, or smaller than that of a crystal part. Further, in a nanobeam electron diffraction pattern of the nc-OS film, regions with high luminance in a circular (ring) pattern are shown in some cases. Also in a nanobeam electron diffraction pattern of the nc-OS film, a plurality of spots is shown in a ring-like region in some cases.

[0124]

Since the nc-OS film is an oxide semiconductor film having more regularity than the amorphous oxide semiconductor film, the nc-OS film has a lower density of defect states than the amorphous oxide semiconductor film. However, there is no regularity of crystal orientation between different crystal parts in the nc-OS film; hence, the nc-OS film has a higher density of defect states than the CAAC-OS film.

[0125]

Note that an oxide semiconductor film may be a stacked film including two or more films of an amorphous oxide semiconductor film, a microcrystalline oxide semiconductor film, and a CAAC-OS film, for example.

[0126]

Here, by the above-described method, the first oxide semiconductor layer 144a and the second oxide semiconductor layer 144b are stacked, and then, heat treatment is performed, and selective etching is performed with the use of a mask.

[0127]

In this embodiment, the first oxide semiconductor layer 144a having an amorphous structure is formed under the condition where the substrate temperature is set to room temperature and a target having an atomic ratio of In:Ga:Zn = 1:3:2 is used. The thickness of the first oxide semiconductor layer 144a having an amorphous structure is set to be greater than or equal to 10 nm and less than or equal to 40 nm, preferably greater than or equal to 20 nm and less than or equal to 30 nm. The first oxide semiconductor layer 144a having an amorphous structure has such a large film

thickness; thus, the diffusion of silicon from a base film (an insulating film containing silicon) can be prevented. Further, the second oxide semiconductor layer 144b having a crystalline structure is formed under the condition where the substrate temperature is set to 400 °C and a target having an atomic ratio of In:Ga:Zn = 1:1:1 is used. The second oxide semiconductor layer 144b is a film containing a crystal whose c-axis is aligned in a direction approximately perpendicular to a surface, preferably a CAAC-OS film. The second oxide semiconductor layer 144b has a thickness greater than or equal to 5 nm and less than or equal to 10 nm.

[0128]

The second oxide semiconductor layer 144b having a crystalline structure is stacked over the first oxide semiconductor layer 144a having an amorphous structure. Hence, the stack can be also referred to as a heterostructure.

[0129]

The film formation temperature of the second oxide semiconductor layer 144b is higher than or equal to 400 °C and lower than or equal to 550 °C, preferably higher than or equal to 450 °C and lower than or equal to 500 °C. Note that the film formation is performed at temperatures that the wiring layers already formed can withstand.

[0130]

The heat treatment after the film formation is performed under reduced pressure in an atmosphere of nitrogen, oxygen, or nitrogen and oxygen at a temperature higher than or equal to 150 °C and lower than the strain point of the substrate, preferably higher than or equal to 300 °C and lower than or equal to 500 °C, further preferably higher than or equal to 350 °C and lower than or equal to 450 °C. By the heat treatment, excess hydrogen (including water or a hydroxyl group) in the oxide semiconductor layer is removed (dehydration or dehydrogenation). Further, a high-purity oxygen gas or ultra dry air (the moisture amount is less than or equal to 20 ppm (−55 °C by conversion into a dew point), preferably less than or equal to 1 ppm, further preferably less than or equal to 10 ppb, in the measurement with use of a dew point meter of a cavity ring down laser spectroscopy (CRDS) system) may be introduced into the same furnace while the heating temperature after the termination of



the heat treatment is maintained or slow cooling is performed to lower the temperature from the heating temperature. By the effect of the oxygen gas, oxygen which is a main component of the oxide semiconductor and which has been reduced at the same time as the step for removing impurities by dehydration or dehydrogenation is supplied.

5 [0131]

The heat treatment is performed after the second oxide semiconductor layer 144b is formed, whereby the hydrogen concentration in the second oxide semiconductor layer 144b can be lower than  $5 \times 10^{18}$  atoms/cm<sup>3</sup>, preferably lower than or equal to  $1 \times 10^{18}$  atoms/cm<sup>3</sup>, further preferably lower than or equal to  $5 \times 10^{17}$  atoms/cm<sup>3</sup>, still  
10 further preferably lower than or equal to  $1 \times 10^{16}$  atoms/cm<sup>3</sup>.

[0132]

The heat treatment is performed under an inert gas atmosphere containing nitrogen or a rare gas such as helium, neon, argon, xenon, or krypton. Further, the heat treatment may be performed under an inert gas atmosphere first, and then under an  
15 oxygen atmosphere. It is preferable that the above inert gas atmosphere and the above oxygen atmosphere do not contain hydrogen, water, and the like. The treatment time is 3 minutes to 24 hours. The number of times of the heat treatment performed on the oxide semiconductor layer is not limited, and the timing of the heat treatment is not limited.

20 [0133]

Note that heating may be performed with the oxide insulating layer provided over and/or under the oxide semiconductor stack 144, in which case oxygen is supplied from the oxide insulating layer to the oxide semiconductor stack 144 to reduce oxygen defects in the oxide semiconductor stack 144. The reduction of the oxygen defects in  
25 the oxide semiconductor stack 144 leads to favorable semiconductor characteristics.

[0134]

Next, the third oxide semiconductor layer 144c is formed to cover the top surface and the side surfaces of the second oxide semiconductor layer 144b and the side surfaces of the first oxide semiconductor layer 144a (see FIG. 3A). The heat treatment  
30 for dehydration or dehydrogenation of the oxide semiconductor may be performed also after the third oxide semiconductor layer 144c is formed.

[0135]

The third oxide semiconductor layer 144c is formed using a target having an atomic ratio of In:Ga:Zn = 1:3:2 at a substrate temperature of 400 °C. The third oxide semiconductor layer 144c is formed over the second oxide semiconductor layer 144b having a crystalline structure, whereby crystal growth of the third oxide semiconductor layer 144c occurs using a crystal in the second oxide semiconductor layer as a seed. Thus, the third oxide semiconductor layer 144c easily becomes a film having a crystalline structure. Accordingly, the boundary between the second oxide semiconductor layer 144b and the third oxide semiconductor layer 144c is difficult to determine in a cross-sectional TEM image in some cases. In drawings, the interface between the second oxide semiconductor layer 144b and the third oxide semiconductor layer 144c is indicated by a dotted line.

[0136]

A part of the third oxide semiconductor layer 144c, i.e. a region of the third oxide semiconductor layer 144c which is in contact with the insulating layer 140 and does not overlap with the second oxide semiconductor layer 144b easily has an amorphous structure. The thickness of the third oxide semiconductor layer 144c is greater than or equal to 10 nm and less than or equal to 40 nm, preferably greater than or equal to 20 nm and less than or equal to 30 nm. Further, in the third oxide semiconductor layer 144c, a region which overlaps with the second oxide semiconductor layer 144b has a crystalline structure, and the other region has an amorphous structure. In order to illustrate this clearly in drawings, the hatch patterns of the region of the third oxide semiconductor layer 144c which overlaps with the second oxide semiconductor layer 144b and the other region of the third oxide semiconductor layer 144c are different from each other.

[0137]

Note that the third oxide semiconductor layer 144c has lower crystallinity than the second oxide semiconductor layer 144b. Hence, it can be said that the boundary can be determined by the degree of crystallinity. Further, in the case where an oxide semiconductor layer having a crystalline structure is provided as the third oxide semiconductor layer 144c over the second oxide semiconductor layer 144b and the third oxide semiconductor layer 144c has a different composition from the second oxide

semiconductor layer 144b, the stack can be also referred to as a heterostructure having different compositions.

[0138]

Crystal growth of the third oxide semiconductor layer 144c occurs under the influence of crystallinity of the second oxide semiconductor layer 144b, so that the third oxide semiconductor layer 144c has a crystalline structure similar to that of the second oxide semiconductor layer 144b. Hence, defects and states at the interface between the second oxide semiconductor layer 144b and the third oxide semiconductor layer 144c are reduced, and thus, a highly reliable semiconductor device can be obtained.

10 [0139]

A state at the interface between the second oxide semiconductor layer 144b and the third oxide semiconductor layer 144c may be mixed (or alloyed) state. The mixed state at the interface reduces damage due to stress difference between the second oxide semiconductor layer 144b and the third oxide semiconductor layer 144c, leading to a reduction of interface scattering.

[0140]

Similarly, the interface between the first oxide semiconductor layer 144a and the second oxide semiconductor layer 144b may be alloyed.

[0141]

20 Next, a conductive film to be the source electrode layer 142a and the drain electrode layer 142b is formed over the oxide semiconductor stack 144. The conductive film can be formed using a material and a method which are similar to those of the gate electrode layer 110.

[0142]

25 Note that in etching at the time of forming the source electrode layer 142a and the drain electrode layer 142b, a region of the oxide semiconductor stack 144 which is located between the source electrode layer 142a and the drain electrode layer 142b is also etched concurrently and is reduced in thickness in some cases. Thus, a region of the oxide semiconductor stack 144 which does not overlap with the source electrode layer 142a and the drain electrode layer 142b has a smaller thickness than a region overlapping with the source electrode layer 142a and the drain electrode layer 142b in some cases.

30

[0143]

In the oxide semiconductor stack 144, the second oxide semiconductor layer 144b to be the channel formation region is sandwiched between the first oxide semiconductor layer 144a and the third oxide semiconductor layer 144c. Hence, even when the oxide semiconductor stack 144 is etched concurrently with the etching of the source electrode layer 142a and the drain electrode layer 142b, the second oxide semiconductor layer 144b to be the channel formation region is hardly affected by the etching, and there is little possibility that the channel formation region is etched and reduced in thickness. Thus, stable characteristics can be exhibited.

[0144]

Next, the oxide insulating layer to be used for the gate insulating layer 147 is formed over the source electrode layer 142a and the drain electrode layer 142b. Here, the gate insulating layer 147 has a two-layer structure in which a gate insulating layer 147a including the oxide insulating layer and a gate insulating layer 147b including a nitride insulating layer are stacked.

[0145]

The oxide insulating layer to be used for the gate insulating layer 147a can be formed using a material and a method which are similar to those of the insulating layer 140. In particular, a film formation condition causing less plasma damage may be used for forming the gate insulating layer 147a in order to reduce plasma damage to the oxide semiconductor stack 144. Further, since the gate insulating layer 147a is in contact with the oxide semiconductor stack 144, the gate insulating layer 147a may be formed using a film which contains oxygen in excess of the stoichiometric composition and from which oxygen is easily released by heat treatment so that oxygen can be supplied to the oxide semiconductor stack 144.

[0146]

An insulating film which can be used for the gate insulating layer 147b may be formed using a silicon film containing oxygen and nitrogen such as a silicon nitride oxide silicon film or a silicon oxynitride film.

[0147]

Next, the gate electrode layer 148 is formed over the gate insulating layer 147. The gate electrode layer 148 can be formed using a material and a method which are

similar to those of the gate electrode layer 110.

[0148]

The insulating layer 150 is formed over the gate electrode layer 148. The insulating layer 150 can be formed using a material and a method which are similar to those of the insulating layer 140. The insulating layer 150 preferably contains oxygen in excess of the stoichiometric composition so that oxygen can be supplied to the oxide semiconductor stack 144.

[0149]

Oxygen may be added to the insulating layer 150 by an ion implantation method, an ion doping method, a plasma immersion ion implantation method, or the like. By the addition of oxygen, excess oxygen can be contained in the insulating layer 150 and oxygen can be supplied from the insulating layer 150 to the oxide semiconductor stack 144. Note that, in drawings, a dotted line is drawn in the insulating layer 150 to illustrate clearly that oxygen is added to the insulating layer 150 and an oxygen concentration has a peak in the insulating layer 150.

[0150]

After the insulating layer 150 is formed, heat treatment is performed. The oxide semiconductor stack 144 includes oxygen vacancies formed by damage due to plasma or etching which is performed after the oxide semiconductor stack 144 is formed. Hence, in order to repair the damage caused after the oxide semiconductor stack is formed, the heat treatment is performed to supply oxygen, whereby oxygen vacancies are reduced. The temperature of the heat treatment is typically higher than or equal to 200 °C and lower than or equal to 450 °C. By the heat treatment, nitrogen in the oxide insulating layer containing nitrogen can be released. Note that by the heat treatment, water, hydrogen, or the like can be released from the oxide insulating layer containing nitrogen.

[0151]

For example, heat treatment is performed in a mixed atmosphere of nitrogen and oxygen at 350 °C for one hour. By the heat treatment, hydrogen atoms and oxygen atoms in the oxide semiconductor stack 144 are released from the oxide semiconductor stack 144 or the interface between the oxide semiconductor stack 144

and each of the insulating layers (the insulating layer 140 and the gate insulating layer 147). In the oxide semiconductor stack 144, sites from which oxygen atoms are released become oxygen vacancies. However, oxygen atoms contained in the oxide insulating layer, which are in excess of the stoichiometric composition, move to the sites  
5 of the oxygen vacancies, and the oxygen vacancies are filled with the oxygen atoms.

[0152]

In this manner, nitrogen, hydrogen, or water is released from the oxide semiconductor film by the heat treatment performed after the insulating layer 150 is formed, whereby the proportion of nitrogen, hydrogen, or water in the film can be  
10 reduced to about a tenth.

[0153]

The insulating layer 155 is formed over the insulating layer 150. The insulating layer 155 can be formed using a material and a method which are similar to those of the insulating layer 135. The insulating layer 155 can inhibit entry of an  
15 impurity from the top of the semiconductor device into the oxide semiconductor stack 144 or can inhibit release of oxygen in the oxide semiconductor stack 144 and the insulating layer 150 to the outside from the top of the semiconductor device.

[0154]

By the aforementioned process, the semiconductor device can be fabricated  
20 (see FIG. 3B).

[0155]

In the semiconductor device described in this embodiment, the second oxide semiconductor layer 144b to be the channel formation region is sandwiched between the first oxide semiconductor layer 144a and the third oxide semiconductor layer 144c.  
25 Thus, the channel formation region can be apart from a surface of the oxide semiconductor stack 144, which leads to a reduction in the effect of surface scattering.

[0156]

Further, the insulating layers containing oxygen in excess of the stoichiometric composition is formed so that the oxide semiconductor stack 144 is sandwiched  
30 therebetween. Hence, oxygen is supplied to the oxide semiconductor stack 144 and an oxygen vacancy in the oxide semiconductor stack 144 is filled with the oxygen. Thus, a highly reliable semiconductor device can be obtained.

[0157]

In addition, the nitride insulating films each having a property of blocking hydrogen or oxygen are formed so that the insulating layers containing excess oxygen are sandwiched therebetween. Hence, it is possible to inhibit entry of an impurity such as hydrogen or moisture into the oxide semiconductor stack 144 or inhibit release of oxygen from the oxide semiconductor layers and the insulating layers containing excess oxygen.

[0158]

Note that the above-described structure is not necessarily used for a second transistor of the semiconductor device described in this embodiment. For example, another mode of the semiconductor device of one embodiment of the present invention is illustrated in each of FIGS. 4A and 4B and FIGS. 5A to 5C. Note that in FIGS. 4A and 4B and FIGS. 5A to 5C, only the second transistor is illustrated, and a first transistor, the wiring layer, and the like are omitted.

[0159]

The transistor 163 illustrated in FIG. 4A is different from the transistor 162 illustrated in FIG. 1 in that the third oxide semiconductor layer 144c does not cover the side surfaces of the second oxide semiconductor layer 144b and the side surfaces of the first oxide semiconductor layer 144a. The transistor 163 can be formed in such a manner that, after the first oxide semiconductor layer 144a, the second oxide semiconductor layer 144b, and the third oxide semiconductor layer 144c are successively formed without exposure to the air, etching is performed with the use of a mask such that the oxide semiconductor stack 144 has an island shape. Thus, a surface of the second oxide semiconductor layer 144b is not exposed to the air and is not subjected to etching treatment; hence, stable characteristics can be provided.

[0160]

Further, since the third oxide semiconductor layer 144c is etched, the gate insulating layer 147 (the gate insulating layer 147a) and the insulating layer 140 are in contact with each other, and thus, the oxide semiconductor stack 144 can be surrounded by the oxide insulating layers. Furthermore, with the oxide insulating layers which are in contact with each other, adhesion can be improved.

[0161]

In the case where the three oxide semiconductor layers are formed in succession without exposure to the air, a manufacturing apparatus a top view of which is illustrated in FIG. 13 may be employed.

[0162]

5           The manufacturing apparatus illustrated in FIG. 13 is single wafer multi-chamber equipment, which includes three sputtering devices 10a, 10b, and 10c, a substrate supply chamber 11 provided with three cassette ports 14 for holding a process substrate, load lock chambers 12a and 12b, a transfer chamber 13, substrate heating chambers 15 and 16, and the like. Note that a transfer robot for transferring a process  
10           substrate is provided in each of the substrate supply chamber 11 and the transfer chamber 13. Atmospheres of the sputtering devices 10a, 10b, and 10c, the transfer chamber 13, and the substrate heating chambers 15 and 16 are preferably controlled so as to hardly contain hydrogen or moisture (i.e., so as to be an inert atmosphere, a reduced pressure atmosphere, a dry air atmosphere, or the like). For example, a  
15           preferable atmosphere is a dry nitrogen atmosphere in which the dew point of moisture is -40 °C or lower, preferably -50 °C or lower. An example of a procedure of the manufacturing steps with use of the manufacturing apparatus illustrated in FIG. 13 is as follows. A process substrate is transferred from the substrate supply chamber 11 to the substrate heating chamber 15 through the load lock chamber 12a and the transfer  
20           chamber 13; moisture attached to the process substrate is removed by vacuum baking or the like in the substrate heating chamber 15; the process substrate is transferred to the sputtering device 10c through the transfer chamber 13; and the first oxide semiconductor layer 144a is formed in the sputtering device 10c. Then, the process substrate is transferred to the sputtering device 10a through the transfer chamber 13  
25           without exposure to the air, and the second oxide semiconductor layer 144b is formed in the sputtering device 10a. Then, the process substrate is transferred to the sputtering device 10b through the transfer chamber 13 without exposure to the air, and the third oxide semiconductor layer 144c is formed in the sputtering device 10b. If necessary, the process substrate is transferred to the substrate heating chamber 16 though the  
30           transfer chamber 13 without exposure to the air and subjected to heat treatment. As described above, with use of the manufacturing apparatus illustrated in FIG. 13, a manufacturing process can proceed without the process substrate being exposed to the



air. Further, with the use of the sputtering devices in the manufacturing apparatus in FIG. 13, a process performed without exposure to the air can be achieved by change of the sputtering target. As the sputtering devices in the manufacturing apparatus in FIG. 13, a parallel plate sputtering device, an ion beam sputtering device, a facing-target type sputtering device, or the like may be used. In a facing-target type sputtering device, an object surface is separated from plasma and thus damage in film formation is small; therefore, a CAAC-OS film having high crystallinity can be formed.

[0163]

A high-purity gas in which the concentration of impurities such as hydrogen, water, a hydroxyl group, or hydride is low is used as a deposition gas for forming the oxide semiconductor layers in the sputtering devices 10a, 10b, and 10c.

[0164]

The heating treatment may be performed in the substrate heating chamber 16 under reduced pressure, under a nitrogen atmosphere, under an oxygen atmosphere, in ultra dry air (air in which the moisture amount is less than or equal to 20 ppm (-55 °C by conversion into a dew point), preferably less than or equal to 1 ppm, further preferably less than or equal to 10 ppb, in the measurement with the use of a dew point meter in the cavity ring down laser spectroscopy (CRDS) system), or under a rare gas (argon, helium, or the like) atmosphere. It is preferable that water, hydrogen, and the like be not contained in the nitrogen atmosphere, in the oxygen atmosphere, in the ultra dry air, in the rare gas atmosphere, or the like. It is also preferable that the purity of nitrogen, oxygen, or the rare gas which is introduced into a heat treatment apparatus be set to be 6N (99.9999 %) or higher, preferably 7N (99.99999 %) or higher (that is, the impurity concentration is 1 ppm or lower, preferably 0.1 ppm or lower).

[0165]

A transistor 164 illustrated in FIG. 4B is similar to the transistor 162 in that the third oxide semiconductor layer 144c covers the top surface and the side surfaces of the second oxide semiconductor layer 144b and the side surfaces of the first oxide semiconductor layer 144a. However, the transistor 164 is different from the transistor 162 in that the third oxide semiconductor layer 144c is etched so that the edge portions of the third oxide semiconductor layer 144c overlap with the source electrode layer

142a and the drain electrode layer 142b. With such a structure, the side surfaces of the second oxide semiconductor layer 144b can be covered with the third oxide semiconductor layer 144c, and the insulating layer 140 can be in contact with the gate insulating layer 147.

5 [0166]

Further, the second transistor may have a structure including two gate electrode layers. Transistors each including two gate electrode layers are illustrated in FIGS. 5A to 5C.

[0167]

10 A transistor 172 illustrated in FIG. 5A has the structure in which a gate electrode layer 149 is added to the transistor 162 in FIG. 1. The gate electrode layer 149 can be formed using the same conductive film as the wiring layer 117. By application of different potentials to the gate electrode layer 148 and the gate electrode layer 149, the threshold voltage of the transistor 172 can be controlled, in a preferable  
15 manner, the negative shift in the threshold voltage can be suppressed. Alternatively, when the same potential is applied to the gate electrode layer 148 and the gate electrode layer 149, the on-state current of the transistor 172 can be increased.

[0168]

FIG. 5B similarly illustrates a transistor 173 having the structure in which the  
20 gate electrode layer 149 is added to the transistor 163. FIG. 5C illustrates a transistor 174 having the structure in which the gate electrode layer 149 is added to the transistor 164.

[0169]

The semiconductor device of this embodiment can be combined with any of the  
25 semiconductor devices of the other embodiments as appropriate.

[0170]

(Embodiment 2)

FIG. 6A illustrates an example of a circuit diagram of a NOR circuit, which is a logic circuit, as an example of the semiconductor device described in Embodiment 1.

30 FIG. 6B is a circuit diagram of a NAND circuit.

[0171]

In the NOR circuit illustrated in FIG. 6A, p-channel transistors 801 and 802

each have a structure similar to that of the transistor 160 in FIG. 1 in that a single crystal silicon substrate is used for a channel formation region, and n-channel transistors 803 and 804 each have a structure similar to structures of the transistor 162 illustrated in FIG. 1, the transistors 163 and 164 illustrated in FIGS. 4A and 4B, and the transistors 172 to 174 illustrated in FIGS. 5A to 5C in that an oxide semiconductor film is used for a channel formation region.

[0172]

In the NOR circuit illustrated in FIG. 6A, a conductive layer controlling electrical characteristics of the transistor may be provided to overlap with a gate electrode layer with an oxide semiconductor film provided therebetween in each of the transistors 803 and 804. By controlling the potential of the conductive layer to GND, for example, the threshold voltages of the transistors 803 and 804 are increased, so that the transistors can be normally off.

[0173]

In the NAND circuit illustrated in FIG. 6B, p-channel transistors 811 and 814 each have a structure similar to that of the transistor 160 in FIG. 1, and n-channel transistors 812 and 813 each have a structure similar to structures of the transistor 162 illustrated in FIG. 1, the transistors 163 and 164 illustrated in FIGS. 4A and 4B, and the transistors 172 to 174 illustrated in FIGS. 5A to 5C in that an oxide semiconductor film is used for a channel formation region.

[0174]

In the NAND circuit illustrated in FIG. 6B, a conductive layer controlling electrical characteristics of the transistor may be provided to overlap with a gate electrode layer with an oxide semiconductor film provided therebetween in each of the transistors 812 and 813. By controlling the potential of the conductive layer to GND, for example, the threshold voltages of the transistors 812 and 813 are increased, so that the transistors can be normally off.

[0175]

By using a transistor including an oxide semiconductor for a channel formation region and having extremely small off-state current for the semiconductor device in this embodiment, power consumption of the semiconductor device can be sufficiently reduced.

[0176]

A semiconductor device which is miniaturized, is highly integrated, and has stable and excellent electrical characteristics by stacking semiconductor elements including different semiconductor materials and a method for manufacturing the semiconductor device can be provided.

[0177]

By using the semiconductor device described in Embodiment 1, entry of impurities into the oxide semiconductor layer can be inhibited. In addition, by using the semiconductor device in which oxygen vacancies of the oxide semiconductor layer are reduced, a NOR circuit and a NAND circuit which are highly reliable and exhibit stable characteristics can be provided.

[0178]

The NOR circuit and the NAND circuit including the transistor described in Embodiment 1 are described as examples in this embodiment; however, the present invention is not limited to the circuits, and an AND circuit, an OR circuit, or the like can be formed using the transistor described in Embodiment 1.

[0179]

The semiconductor device of this embodiment can be combined with any of the semiconductor devices of the other embodiments as appropriate.

[0180]

(Embodiment 3)

In this embodiment, an example of a semiconductor device (memory device) which includes the semiconductor device described in Embodiment 1, which can hold stored data even when not powered, and which has an unlimited number of write cycles is described with reference to drawings.

[0181]

FIG. 7A is a circuit diagram illustrating the semiconductor device of this embodiment.

[0182]

A transistor 260 illustrated in FIG. 7A can have a structure similar to that of the transistor 160 illustrated in FIG. 1 and easily operates at high speed. Further, a transistor 262 can have a structure similar to structures of the transistor 162 illustrated

in FIG. 1, the transistors 163 and 164 illustrated in FIGS. 4A and 4B, and the transistors 172 to 174 illustrated in FIGS. 5A to 5C and enables charge to be held for a long time owing to its characteristics.

[0183]

5           Although all the transistors are n-channel transistors here, p-channel transistors can be used as the transistors used for the semiconductor device described in this embodiment.

[0184]

10           In FIG. 7A, a first wiring (a 1st Line) is electrically connected to a source electrode layer of the transistor 260, and a second wiring (a 2nd Line) is electrically connected to a drain electrode layer of the transistor 260. A third wiring (3rd Line) is electrically connected to one of a source electrode layer and a drain electrode layer of the transistor 262, and a fourth wiring (4th Line) is electrically connected to a gate electrode layer of the transistor 262. A gate electrode layer of the transistor 260 and  
15           the other of the source electrode layer and the drain electrode layer of the transistor 262 are electrically connected to one electrode of a capacitor 264. A fifth wiring (5th Line) and the other electrode of the capacitor 264 are electrically connected to each other.

[0185]

20           The semiconductor device illustrate in FIG. 7A utilizes a characteristic in which the potential of the gate electrode layer of the transistor 260 can be held, and thus enables data writing, holding, and reading as follows.

[0186]

25           Writing and holding of data will be described. First, the potential of the fourth wiring is set to a potential at which the transistor 262 is turned on, so that the transistor 262 is turned on. Accordingly, the potential of the third wiring is supplied to the gate electrode layer of the transistor 260 and to the capacitor 264. That is, predetermined charge is supplied to the gate electrode layer of the transistor 260 (writing). Here, charge for supplying either of two different potential levels (hereinafter referred to as low-level charge and high-level charge) is given. After that,  
30           the potential of the fourth wiring is set to a potential at which the transistor 262 is turned off, so that the transistor 262 is turned off. Thus, the charge given to the gate electrode layer of the transistor 260 is held (holding).

[0187]

Since the off-state current of the transistor 262 is extremely low, the charge of the gate electrode layer of the transistor 260 is held for a long time.

[0188]

5           Next, reading of data will be described. By supplying an appropriate potential (a reading potential) to the fifth wiring while supplying a predetermined potential (a constant potential) to the first wiring, the potential of the second wiring varies depending on the amount of charge held at the gate electrode layer of the transistor 260. This is because in general, when the transistor 260 is an n-channel transistor, an  
10           apparent threshold voltage  $V_{th\_H}$  in the case where the high-level charge is given to the gate electrode layer of the transistor 260 is lower than an apparent threshold voltage  $V_{th\_L}$  in the case where the low-level charge is given to the gate electrode layer of the transistor 260. Here, an apparent threshold voltage refers to the potential of the fifth line, which is needed to turn on the transistor 260. Thus, the potential of the fifth  
15           wiring is set to a potential  $V_0$  which is between  $V_{th\_H}$  and  $V_{th\_L}$ , whereby charge given to the gate electrode layer of the transistor 260 can be determined. For example, in the case where the high-level charge is given in writing, when the potential of the fifth wiring is set to  $V_0$  ( $> V_{th\_H}$ ), the transistor 260 is turned on. In the case where the low-level charge is given in writing, even when the potential of the fifth wiring is set to  
20            $V_0$  ( $< V_{th\_L}$ ), the transistor 260 remains in an off state. Therefore, the data held can be read by measuring the potential of the second wiring.

[0189]

Note that in the case where memory cells are arrayed to be used, only data of desired memory cells needs to be read. In the case where such reading is not  
25           performed, a potential at which the transistor 260 is turned off regardless of the state of the gate electrode layer of the transistor 260, that is, a potential smaller than  $V_{th\_H}$  may be given to the fifth wiring. Alternatively, a potential at which the transistor 260 is turned on regardless of the state of the gate electrode layer, that is, a potential higher than  $V_{th\_L}$  may be given to the fifth wiring.

30           [0190]

FIG. 7B illustrates another example of one embodiment of a structure of a

memory device. FIG. 7B illustrates an example of a circuit configuration of a semiconductor device, and FIG. 7C is a conceptual diagram illustrating an example of a semiconductor device. First, the semiconductor device illustrated in FIG. 7B will be described, and then, the semiconductor device illustrated in FIG. 7C will be described.

5 [0191]

In the semiconductor device illustrated in FIG. 7B, a bit line BL is electrically connected to one of the source electrode layer or the drain electrode layer of the transistor 262, a word line WL is electrically connected to the gate electrode layer of the transistor 262, and the other of the source electrode layer or the drain electrode layer of the transistor 262 is electrically connected to a first terminal of a capacitor 254.

[0192]

Here, the transistor 262 including an oxide semiconductor has extremely low off-state current. For that reason, a potential of the first terminal of the capacitor 254 (or a charge accumulated in the capacitor 254) can be held for an extremely long time by turning off the transistor 262.

15 [0193]

Next, writing and holding of data in the semiconductor device (a memory cell 250) illustrated in FIG. 7B will be described.

[0194]

20 First, the potential of the word line WL is set to a potential at which the transistor 262 is turned on, and the transistor 262 is turned on. Accordingly, the potential of the bit line BL is supplied to the first terminal of the capacitor 254 (writing). After that, the potential of the word line WL is set to a potential at which the transistor 262 is turned off, so that the transistor 262 is turned off. Thus, the potential of the first terminal of the capacitor 254 is held (holding).

25 [0195]

Because the off-state current of the transistor 262 is extremely small, the potential of the first terminal of the capacitor 254 (or a charge accumulated in the capacitor) can be held for an extremely long period.

30 [0196]

Next, reading of data will be described. When the transistor 262 is turned on, the bit line BL which is in a floating state and the capacitor 254 are electrically

connected to each other, and the charge is redistributed between the bit line BL and the capacitor 254. As a result, the potential of the bit line BL is changed. The amount of change in potential of the bit line BL varies depending on the potential of the first terminal of the capacitor 254 (or the charge accumulated in the capacitor 254).

5 [0197]

For example, the potential of the bit line BL after charge redistribution is represented by  $(C_B * V_{B0} + C * V) / (C_B + C)$ , where  $V$  is the potential of the first terminal of the capacitor 254,  $C$  is the capacitance of the capacitor 254,  $C_B$  is the capacitance of the bit line BL (hereinafter also referred to as bit line capacitance), and  $V_{B0}$  is the potential of the bit line BL before the charge redistribution. Therefore, it can be found that assuming that the memory cell 250 is in either of two states in which the potentials of the first terminal of the capacitor 254 are  $V_1$  and  $V_0$  ( $V_1 > V_0$ ), the potential of the bit line BL in the case of holding the potential  $V_1$  ( $= (C_B * V_{B0} + C * V_1) / (C_B + C)$ ) is higher than the potential of the bit line BL in the case of holding the potential  $V_0$  ( $= (C_B * V_{B0} + C * V_0) / (C_B + C)$ ).

15  $(= (C_B * V_{B0} + C * V_0) / (C_B + C))$ .

[0198]

Then, by comparing the potential of the bit line BL with a predetermined potential, data can be read.

[0199]

20 As described above, the semiconductor device illustrated in FIG. 7B can hold charge that is accumulated in the capacitor 254 for a long time because the amount of the off-state current of the transistor 262 is extremely small. In other words, power consumption can be adequately reduced because refresh operation becomes unnecessary or the frequency of refresh operation can be extremely low. Moreover, stored data can be held for a long time even when power is not supplied.

25

[0200]

Next, the semiconductor device illustrated in FIG. 7C will be described.

[0201]

The semiconductor device illustrated in FIG. 7C includes memory cell arrays 251a and 251b including a plurality of memory cells 250 illustrated in FIG. 7B as memory circuits in an upper portion, and a peripheral circuit 253 in a lower portion

30



which is necessary for operating a memory cell array 251 (the memory cell arrays 251a and 251b). Note that the peripheral circuit 253 is electrically connected to the memory cell array 251.

[0202]

5 In the structure illustrated in FIG. 7C, the peripheral circuit 253 can be provided directly under the memory cell array 251 (the memory cell arrays 251a and 251b). Thus, the size of the semiconductor device can be reduced.

[0203]

10 It is preferable that a semiconductor material of the transistor provided in the peripheral circuit 253 be different from that of the transistor 262. For example, silicon, germanium, silicon germanium, silicon carbide, gallium arsenide, or the like can be used, and a single crystal semiconductor is preferably used. Alternatively, an organic semiconductor material or the like may be used. A transistor including such a semiconductor material can operate at sufficiently high speed. Therefore, a variety of  
15 circuits (e.g., a logic circuit or a driver circuit) which need to operate at high speed can be favorably realized by the transistor.

[0204]

Note that FIG. 7C illustrates, as an example, the semiconductor device in which two memory cell arrays 251 (the memory cell arrays 251a and 251b) are stacked;  
20 however, the number of memory cell arrays to be stacked is not limited thereto. Three or more memory cell arrays may be stacked.

[0205]

When a transistor including an oxide semiconductor in a channel formation region is used as the transistor 262, stored data can be held for a long time. In other  
25 words, power consumption can be sufficiently reduced because a semiconductor memory device in which refresh operation is unnecessary or the frequency of refresh operation is extremely low can be provided.

[0206]

Further, the semiconductor device described in this embodiment is the  
30 semiconductor device described in Embodiment 1 in which the oxide semiconductor layers are stacked to form the oxide semiconductor stack and the second oxide semiconductor layer to be the channel formation region is apart from the surface of the

oxide semiconductor stack. Thus, a highly reliable semiconductor device that exhibits stable electrical characteristics can be obtained.

[0207]

(Embodiment 4)

5 In this embodiment, examples of application of the semiconductor device described in any of the above embodiments to electronic devices such as a mobile phone, a smartphone, or an electronic book will be described with reference to FIG. 8, FIG. 9, FIG. 10, and FIGS. 11A and 11B.

[0208]

10 FIG. 8 is a block diagram of an electronic device. An electronic device illustrated in FIG. 8 includes an RF circuit 901, an analog baseband circuit 902, a digital baseband circuit 903, a battery 904, a power supply circuit 905, an application processor 906, a flash memory 910, a display controller 911, a memory circuit 912, a display 913, a touch sensor 919, an audio circuit 917, a keyboard 918, and the like. The display  
15 913 includes a display portion 914, a source driver 915, and a gate driver 916. The application processor 906 includes a CPU 907, a DSP 908, and an interface (IF) 909. In general, the memory circuit 912 includes an SRAM or a DRAM; by employing any of the semiconductor devices described in the above embodiments for the memory circuit 912, writing and reading of data can be performed at high speed, data can be held  
20 for a long time, and power consumption can be sufficiently reduced.

[0209]

FIG. 9 illustrates an example in which any of the semiconductor devices described in the above embodiments is used for a memory circuit 950 in a display. The memory circuit 950 illustrated in FIG. 9 includes a memory 952, a memory 953, a  
25 switch 954, a switch 955, and a memory controller 951. Further, the memory circuit is connected to a display controller 956 which reads and controls image data input through a signal line (input image data) and data stored in the memories 952 and 953 (stored image data), and is also connected to a display 957 which displays an image based on a signal input from the display controller 956.

30 [0210]

First, image data (input image data A) is formed by an application processor (not illustrated). The input image data A is stored in the memory 952 though the

switch 954. The image data (stored image data A) stored in the memory 952 is transmitted to the display 957 through the switch 955 and the display controller 956, and is displayed on the display 957.

[0211]

5           In the case where the input image data A is not changed, the stored image data A is read from the memory 952 through the switch 955 by the display controller 956 normally at a frequency of approximately 30 Hz to 60 Hz.

[0212]

10           Next, for example, when a user performs an operation to rewrite a screen (i.e., when the input image data A is changed), the application processor produces new image data (input image data B). The input image data B is stored in the memory 953 through the switch 954. Also during this time, the stored image data A is regularly read from the memory 952 through the switch 955. After the completion of storing the new image data (stored image data B) in the memory 953, from the next frame for the display 957, the stored image data B starts to be read, is transmitted to the display 957 through the switch 955 and the display controller 956, and is displayed on the display 957. This reading operation continues until another new image data is stored in the memory 952.

[0213]

20           By alternately writing and reading image data to and from the memory 952 and the memory 953 as described above, images are displayed on the display 957. Note that the memory 952 and the memory 953 are not necessarily separate memories and a single memory may be divided and used. By employing any of the semiconductor devices described in the above embodiments for the memory 952 and the memory 953, data can be written and read at high speed and held for a long time, and power consumption can be sufficiently reduced. Further, a semiconductor device which is hardly affected by entry of water, moisture, and the like from the outside and has high reliability can be provided.

[0214]

30           FIG. 10 is a block diagram of an electronic book. The electronic book in FIG. 10 includes a battery 1001, a power supply circuit 1002, a microprocessor 1003, a flash memory 1004, an audio circuit 1005, a keyboard 1006, a memory circuit 1007, a touch

panel 1008, a display 1009, and a display controller 1010.

[0215]

Here, the semiconductor device described in any of the above embodiments can be used for the memory circuit 1007 in FIG. 10. The memory circuit 1007 has a function of temporarily storing the contents of a book. For example, when a user uses a highlight function, the memory circuit 1007 stores and holds data of a portion specified by the user. Note that the highlight function is used to make a difference between a specific portion and the other portions while reading an electronic book, by marking the specific portion, e.g., by changing the display color, underlining, making characters bold, changing the font of characters, or the like. In order to store the data for a short time, the data may be stored in the memory circuit 1007. In order to store the data for a long time, the data stored in the memory circuit 1007 may be copied to the flash memory 1004. Also in such a case, by employing the semiconductor devices described in any of the above embodiments, data can be written and read at high speed and held for a long time, and power consumption can be sufficiently reduced. Further, a semiconductor device which is hardly affected by entry of water, moisture, and the like from the outside and which has high reliability can be provided.

[0216]

FIGS. 11A and 11B illustrate a specific example of an electronic device. FIGS. 11A and 11B illustrate a foldable tablet terminal. The tablet terminal is opened in FIG. 11A. The tablet terminal includes a housing 9630, a display portion 9631a, a display portion 9631b, a display mode switch 9034, a power switch 9035, a power saver switch 9036, a clasp 9033, and an operation switch 9038.

[0217]

The semiconductor device described in Embodiment 1 can be used for the display portion 9631a and the display portion 9631b, so that the tablet terminal can have high reliability. In addition, the memory device described in the above embodiment may be applied to the semiconductor device of this embodiment.

[0218]

Part of the display portion 9631a can be a touch panel region 9632a and data can be input when a displayed operation key 9638 is touched. Although a structure in which a half region in the display portion 9631a has only a display function and the

other half region also has a touch panel function is shown as an example, the display portion 9631a is not limited to the structure. For example, the display portion 9631a can display keyboard buttons in the whole region to be a touch panel, and the display portion 9631b can be used as a display screen.

5 [0219]

As in the display portion 9631a, part of the display portion 9631b can be a touch panel region 9632b. When a keyboard display switching button 9639 displayed on the touch panel is touched with a finger, a stylus, or the like, a keyboard can be displayed on the display portion 9631b.

10 [0220]

Touch input can be performed in the touch panel region 9632a and the touch panel region 9632b at the same time.

[0221]

The display mode switch 9034 can switch the display between portrait mode, landscape mode, and the like, and between monochrome display and color display, for example. The power saver switch 9036 can control display luminance in accordance with the amount of external light in use of the tablet terminal detected by an optical sensor incorporated in the tablet terminal. In addition to the optical sensor, another detection device including a sensor for detecting inclination, such as a gyroscope or an acceleration sensor, may be incorporated in the tablet terminal.

20

[0222]

Although the display portion 9631a and the display portion 9631b have the same display area in FIG. 11A, one embodiment of the present invention is not limited to this structure. The display portion 9631a and the display portion 9631b may have different areas or different display quality. For example, one of them may be a display panel that can display higher-definition images than the other.

25

[0223]

The tablet terminal is closed in FIG. 11B. The tablet terminal includes the housing 9630, a solar cell 9633, a charge and discharge control circuit 9634, a battery 9635, and a DCDC converter 9636. In FIG. 11B, a structure including the battery 9635 and the DCDC converter 9636 is illustrated as an example of the charge and discharge control circuit 9634.

30

[0224]

Since the tablet terminal is foldable, the housing 9630 can be closed when the tablet terminal is not used. As a result, the display portion 9631a and the display portion 9631b can be protected; thus, a tablet terminal which has excellent durability and excellent reliability in terms of long-term use can be provided.

[0225]

In addition, the tablet terminal illustrated in FIGS. 11A and 11B can have a function of displaying a variety of kinds of data (e.g., a still image, a moving image, and a text image), a function of displaying a calendar, a date, the time, or the like on the display portion, a touch-input function of operating or editing the data displayed on the display portion by touch input, a function of controlling processing by a variety of kinds of software (programs), and the like.

[0226]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

#### EXPLANATION OF REFERENCE

[0227]

100: substrate, 102: element isolation insulating layer, 104: insulating layer, 108: gate insulating layer, 110: gate electrode layer, 112: wiring layer, 114: wiring layer, 115: wiring layer, 115a: wiring layer, 115b: wiring layer, 115c: wiring layer, 116: wiring layer, 117: wiring layer, 120: insulating layer, 135: insulating layer, 140: insulating layer, 142a: source electrode layer, 142b: drain electrode layer, 144: oxide semiconductor stack, 144a: oxide semiconductor layer, 144b: oxide semiconductor layer, 144c: oxide semiconductor layer, 147: gate insulating layer, 147a: gate insulating layer, 147b: gate insulating layer, 148: gate electrode layer, 149: gate electrode layer, 150: insulating layer, 155: insulating layer, 160: transistor, 162: transistor, 163: transistor, 164: transistor, 172: transistor, 173: transistor, 174: transistor, 250: memory cell, 251: memory cell array, 251a: memory cell array, 251b: memory cell array, 253: peripheral circuit, 254: capacitor, 260: transistor, 262: transistor, 264: capacitor, 801: transistor, 802: transistor, 803: transistor, 804: transistor, 811: transistor, 812: transistor, 813:

transistor, 814: transistor, 901: RF circuit, 902: analog baseband circuit, 903: digital baseband circuit, 904: battery, 905: power supply circuit, 906: application processor, 907: CPU, 908: DSP, 909: interface, 910: flash memory, 911: display controller, 912: memory circuit, 913: display, 914: display portion, 915: source driver, 916: gate driver, 5 917: audio circuit, 918: keyboard, 919: touch sensor, 950: memory circuit, 951: memory controller, 952: memory, 953: memory, 954: switch, 955: switch, 956: display controller, 957: display, 1001: battery, 1002: power supply circuit, 1003: microprocessor, 1004: flash memory, 1005: audio circuit, 1006: keyboard, 1007: memory circuit, 1008: touch panel, 1009: display, 1010: display controller, 9033: clasp, 9034: switch, 9035: power switch, 9036: switch, 9038: operation switch, 9630: housing, 9631a: display portion, 10 9631b: display portion, 9632a: region, 9632b: region, 9633: solar cell, 9634: charge and discharge control circuit, 9635: battery, 9636: DCDC converter, 9638: operation key, 9639: button

15           This application is based on Japanese Patent Application serial no. 2012-178634 filed with Japan Patent Office on August 10, 2012, the entire contents of which are hereby incorporated by reference.

## CLAIMS

1. A semiconductor device comprising:
  - a first oxide semiconductor layer over an insulating surface;
  - 5 a second oxide semiconductor layer over the first oxide semiconductor layer;
  - a third oxide semiconductor layer over the second oxide semiconductor layer;
  - a first insulating layer over the third oxide semiconductor layer; and
  - a first gate electrode over the first insulating layer, the first gate electrode overlapping with the first oxide semiconductor layer, the second oxide semiconductor
  - 10 layer, and the third oxide semiconductor layer,

wherein each of the second oxide semiconductor layer and the third oxide semiconductor layer has a crystalline structure.
2. The semiconductor device according to claim 1, further comprising:
  - 15 a source electrode and a drain electrode over and electrically connected to the first oxide semiconductor layer, the second oxide semiconductor layer, and the third oxide semiconductor layer.
3. The semiconductor device according to claim 1, further comprising:
  - 20 a second insulating layer having the insulating surface; and
  - a second gate electrode under the second insulating layer, the second gate electrode overlapping with the first oxide semiconductor layer, the second oxide semiconductor layer, and the third oxide semiconductor layer.
4. The semiconductor device according to claim 1, wherein the first oxide semiconductor layer has an amorphous structure.
5. The semiconductor device according to claim 1, wherein each of the first oxide semiconductor layer, the second oxide semiconductor layer, and the third oxide
- 30 semiconductor layer comprises at least one of indium, zinc, and gallium.
6. The semiconductor device according to claim 1,



wherein each of the first oxide semiconductor layer, the second oxide semiconductor layer, and the third oxide semiconductor layer comprises indium, and

wherein a proportion of indium in the second oxide semiconductor layer is higher than a proportion of indium in the first oxide semiconductor layer and a  
5 proportion of indium in the third oxide semiconductor layer.

7. The semiconductor device according to claim 1, wherein the first insulating layer contains oxygen in excess of a stoichiometric composition.

10 8. The semiconductor device according to claim 1, wherein a concentration of silicon or carbon in each of the first oxide semiconductor layer and the third oxide semiconductor layer is lower than or equal to  $3 \times 10^{18}$  atoms/cm<sup>3</sup>.

9. A semiconductor device comprising:

15 a first insulating layer over a substrate, the first insulating layer comprising aluminum and oxygen;

a first gate electrode over the first insulating layer;

a second insulating layer over the first gate electrode;

20 a first oxide semiconductor layer over the second insulating layer, the first oxide semiconductor layer overlapping with the first gate electrode;

a second oxide semiconductor layer over the first oxide semiconductor layer, the second oxide semiconductor layer overlapping with the first gate electrode;

a source electrode and a drain electrode over and electrically connected to the first oxide semiconductor layer and the second oxide semiconductor layer;

25 a third insulating layer over the second oxide semiconductor layer, the source electrode, and the drain electrode; and

a second gate electrode over the third insulating layer, the second gate electrode overlapping with the first oxide semiconductor layer and the second oxide semiconductor layer.

30

10. The semiconductor device according to claim 9, wherein each of the first oxide semiconductor layer and the second oxide semiconductor layer has a crystalline

structure.

11. The semiconductor device according to claim 9, wherein each of the first oxide semiconductor layer and the second oxide semiconductor layer comprises at least one of indium, zinc, and gallium.

12. The semiconductor device according to claim 9, wherein each of the first oxide semiconductor layer and the second oxide semiconductor layer comprises indium.

13. The semiconductor device according to claim 9, wherein the second insulating layer contains oxygen in excess of a stoichiometric composition.

14. The semiconductor device according to claim 9, wherein a concentration of silicon or carbon in the first oxide semiconductor layer is lower than or equal to  $3 \times 10^{18}$  atoms/cm<sup>3</sup>.

15. A semiconductor device comprising:

a first insulating layer over a substrate, the first insulating layer comprising aluminum and oxygen;

a first gate electrode over the first insulating layer;

a second insulating layer over the first gate electrode;

a first oxide semiconductor layer over the second insulating layer, the first oxide semiconductor layer overlapping with the first gate electrode;

a second oxide semiconductor layer over the first oxide semiconductor layer, the second oxide semiconductor layer overlapping with the first gate electrode;

a third oxide semiconductor layer over the second oxide semiconductor layer, the third oxide semiconductor layer overlapping with the first gate electrode;

a source electrode and a drain electrode over and electrically connected to the first oxide semiconductor layer, the second oxide semiconductor layer, and the third oxide semiconductor layer;

a third insulating layer over the third oxide semiconductor layer, the source electrode, and the drain electrode; and

a second gate electrode over the third insulating layer, the second gate electrode overlapping with the first oxide semiconductor layer, the second oxide semiconductor layer, and the third oxide semiconductor layer.

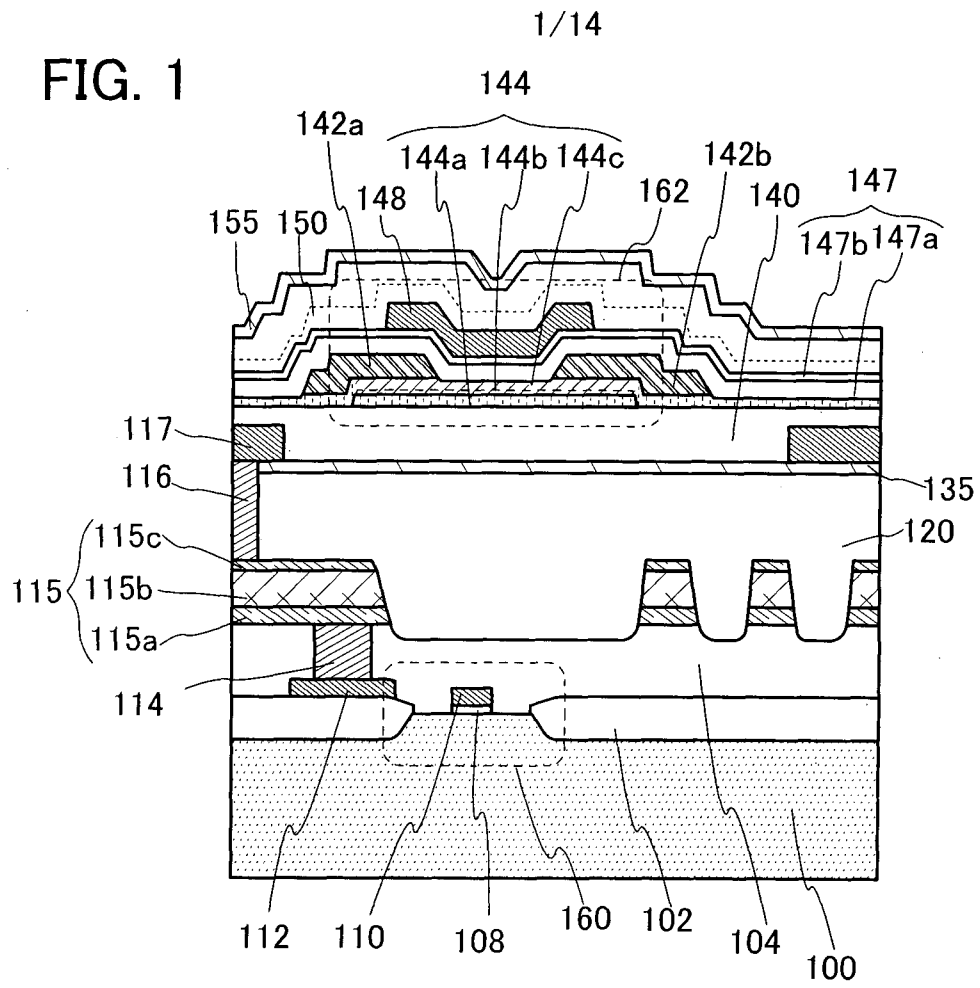
5           16. The semiconductor device according to claim 15,  
          wherein the first oxide semiconductor layer has an amorphous structure, and  
          wherein each of the second oxide semiconductor layer and the third oxide  
semiconductor layer has a crystalline structure.

10           17. The semiconductor device according to claim 15, wherein each of the first  
oxide semiconductor layer, the second oxide semiconductor layer, and the third oxide  
semiconductor layer comprises at least one of indium, zinc, and gallium.

          18. The semiconductor device according to claim 15,  
15           wherein each of the first oxide semiconductor layer, the second oxide  
semiconductor layer, and the third oxide semiconductor layer comprises indium, and  
          wherein a proportion of indium in the second oxide semiconductor layer is  
higher than a proportion of indium in the first oxide semiconductor layer and a  
proportion of indium in the third oxide semiconductor layer.

20           19. The semiconductor device according to claim 15, wherein the second  
insulating layer contains oxygen in excess of a stoichiometric composition.

25           20. The semiconductor device according to claim 15, wherein a concentration  
of silicon or carbon in each of the first oxide semiconductor layer and the third oxide  
semiconductor layer is lower than or equal to  $3 \times 10^{18}$  atoms/cm<sup>3</sup>.



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FIG. 2A

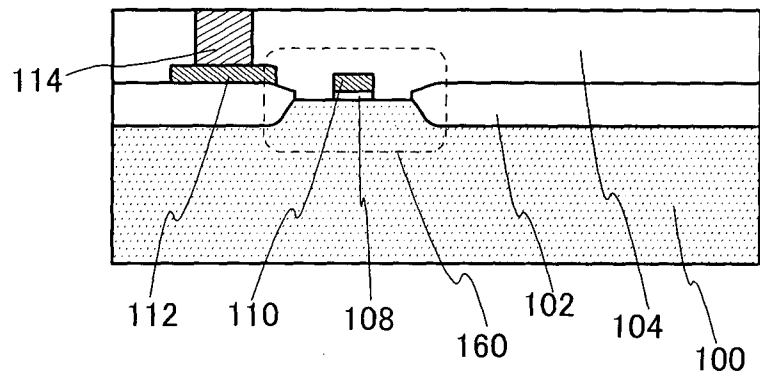


FIG. 2B

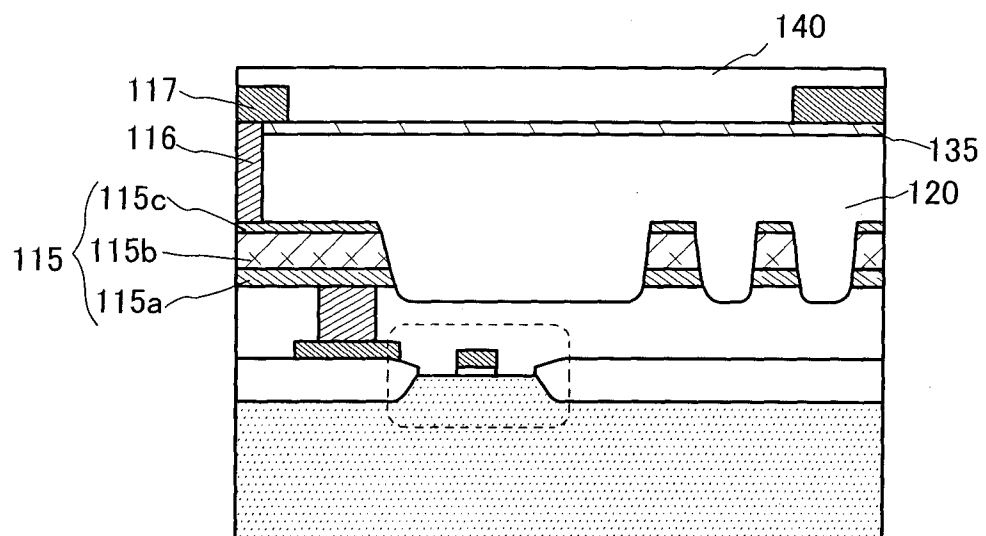


FIG. 3A

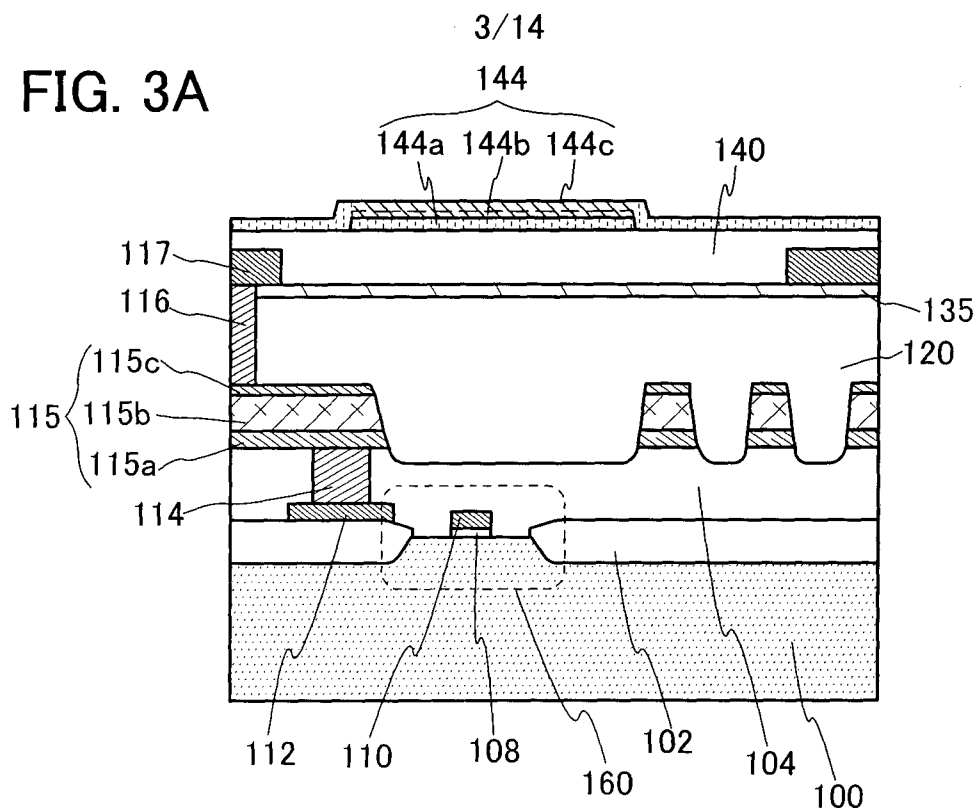
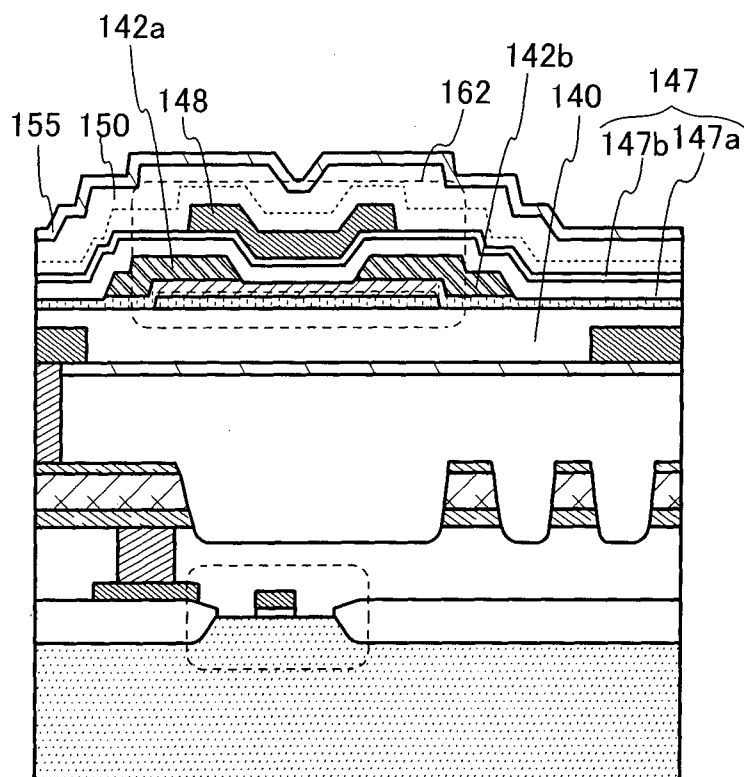


FIG. 3B



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FIG. 4A

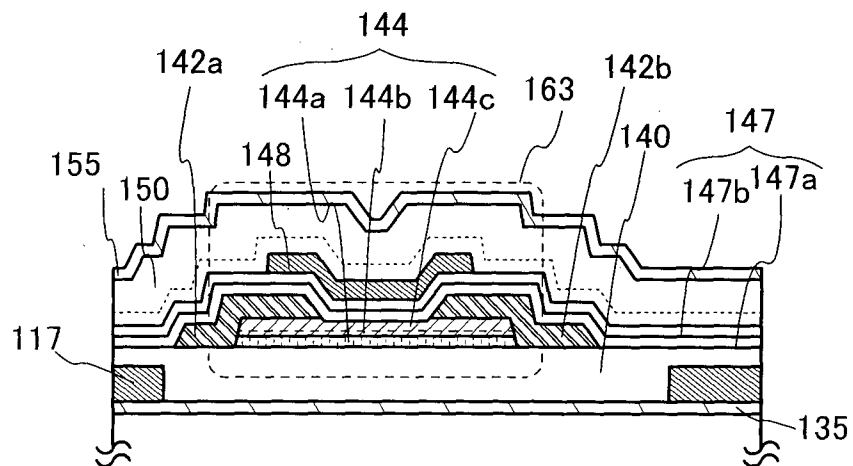
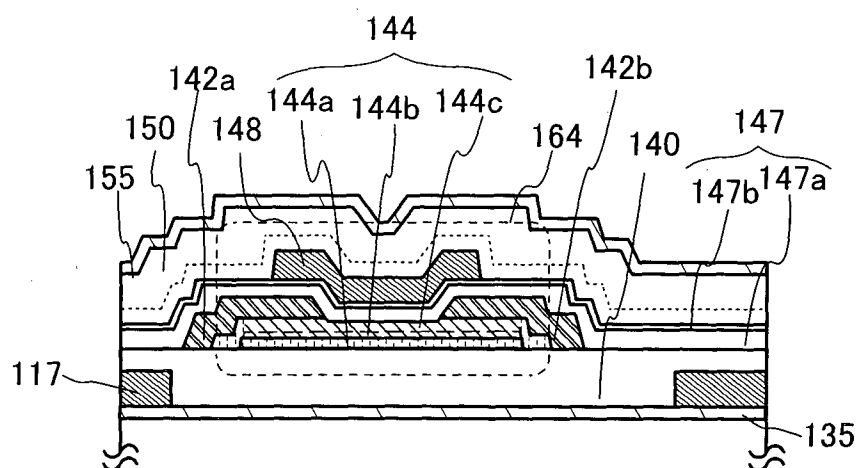
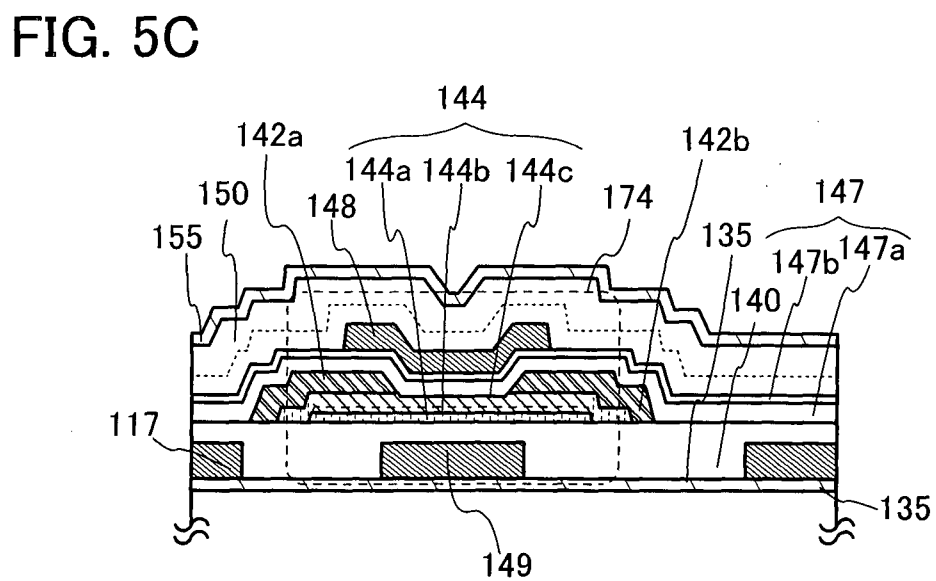
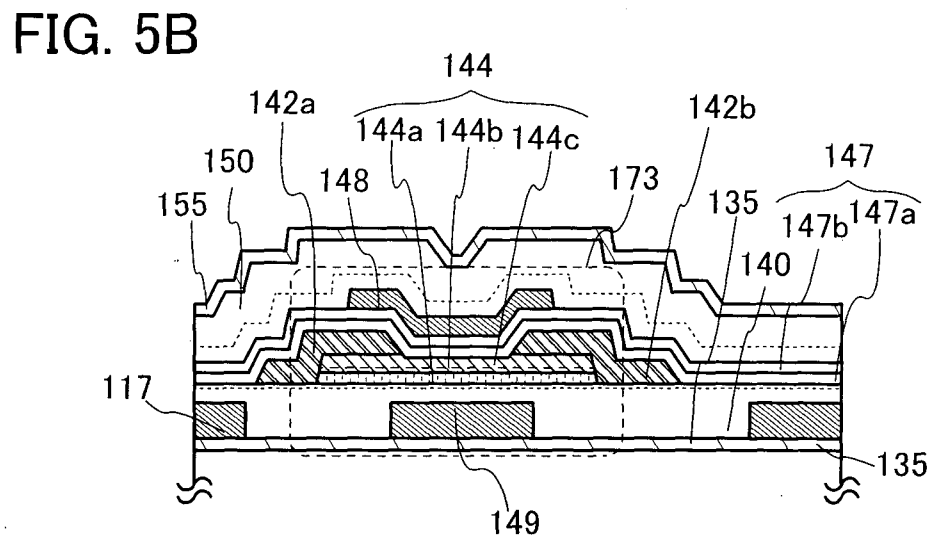
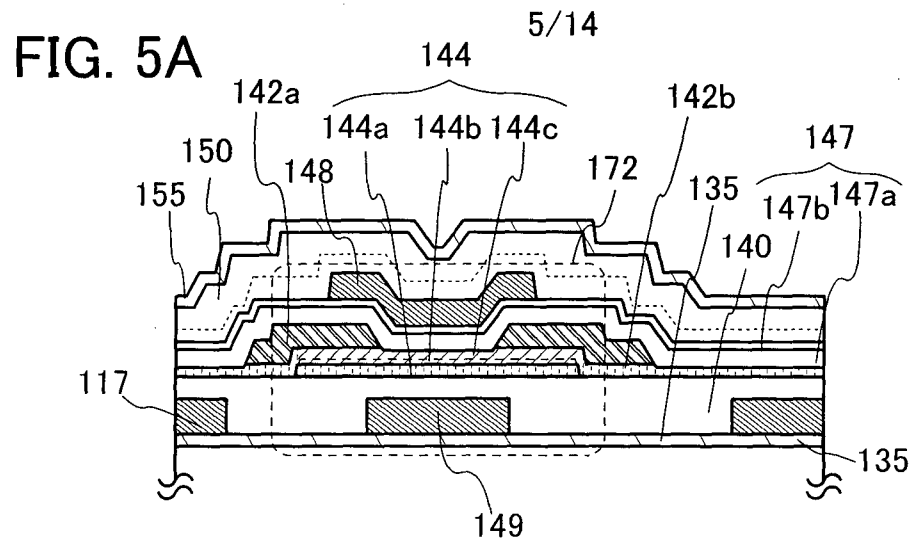


FIG. 4B







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FIG. 6A

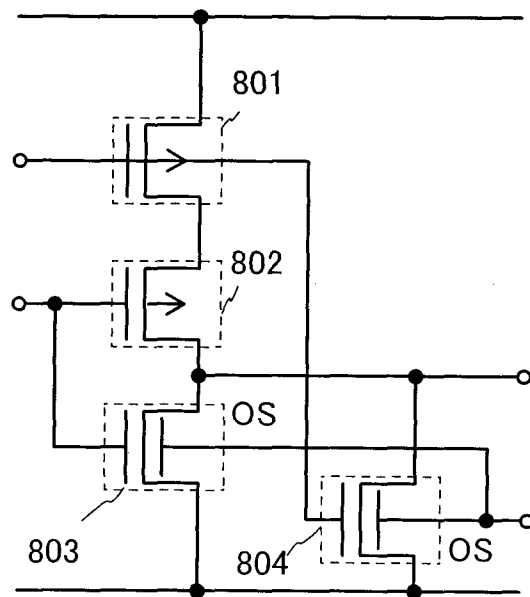
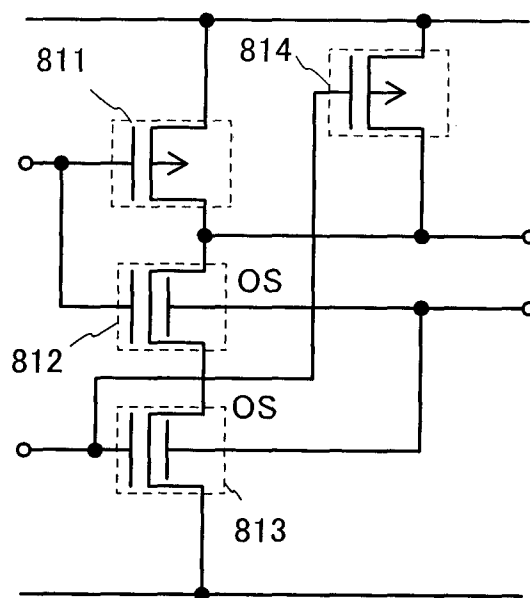


FIG. 6B



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FIG. 7A

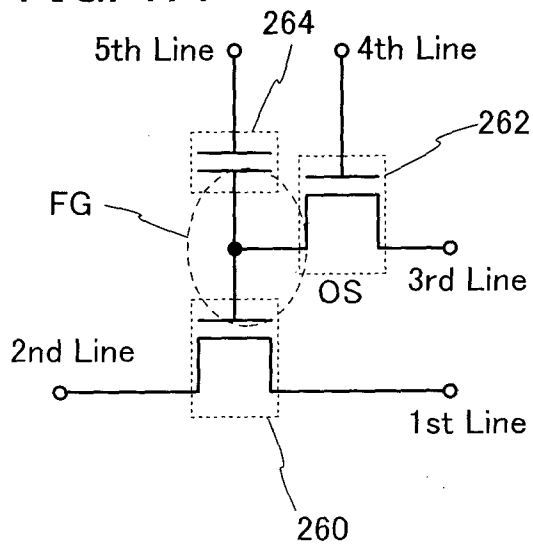


FIG. 7B

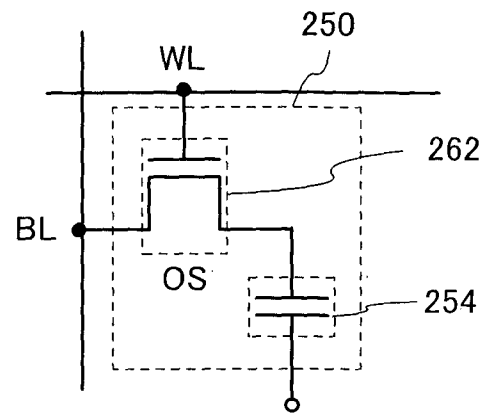


FIG. 7C

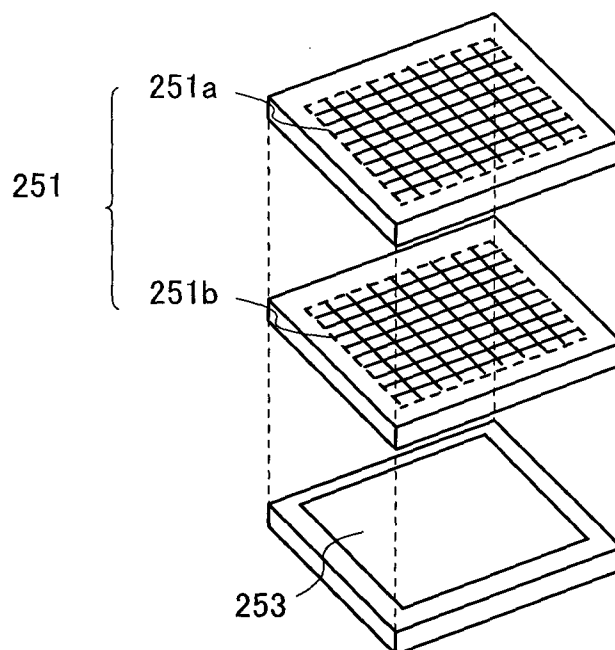


FIG. 8

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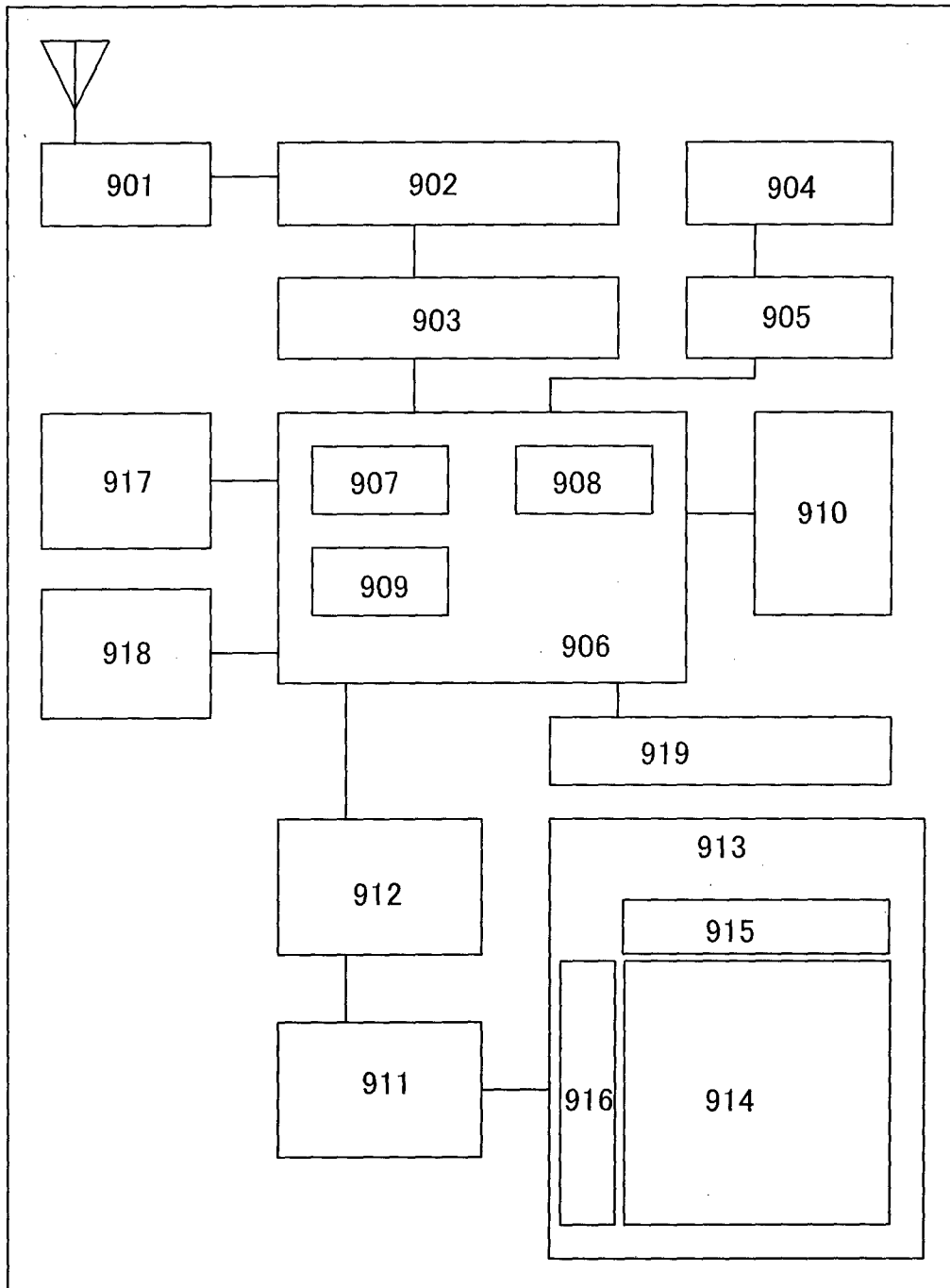
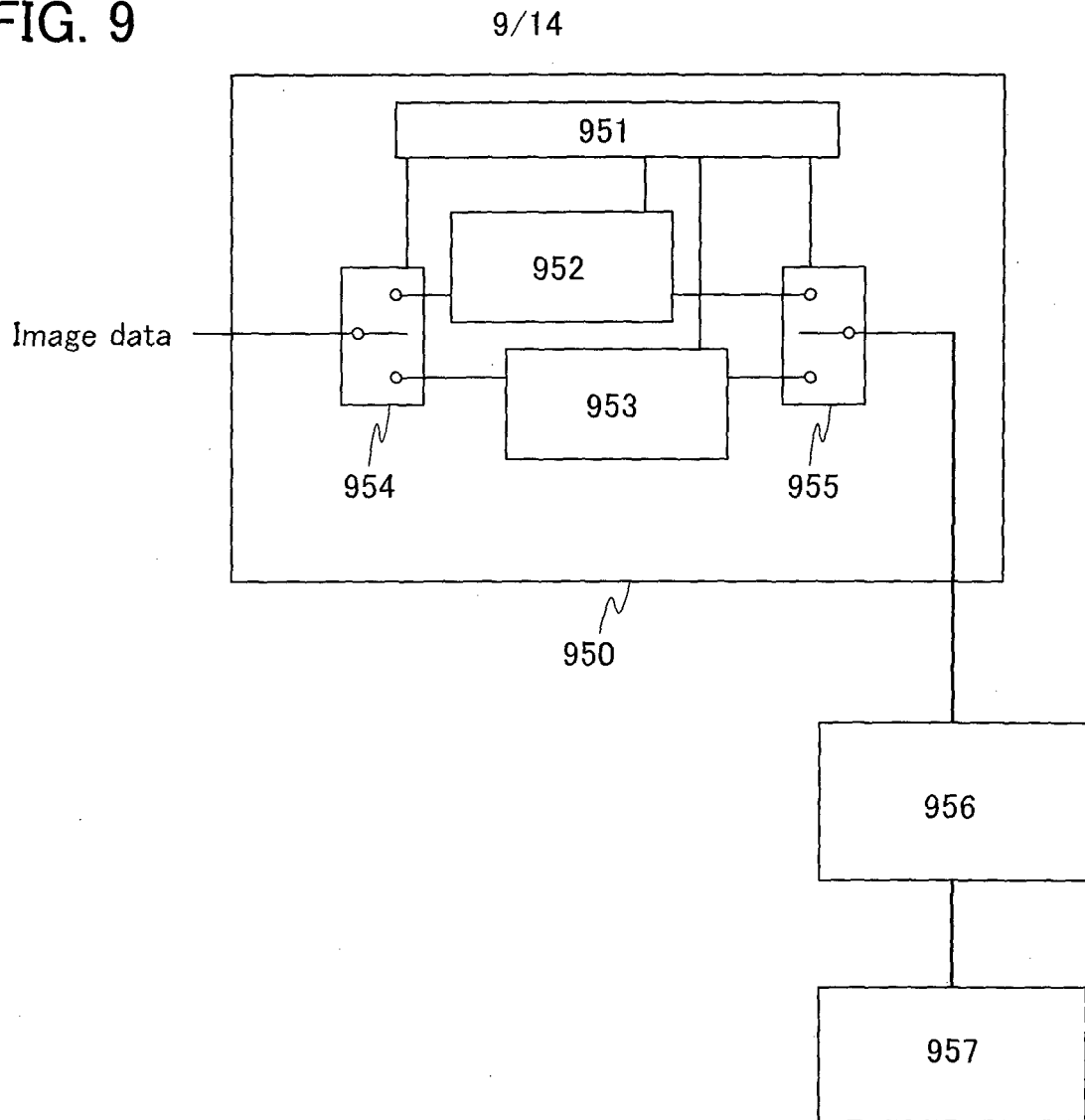


FIG. 9



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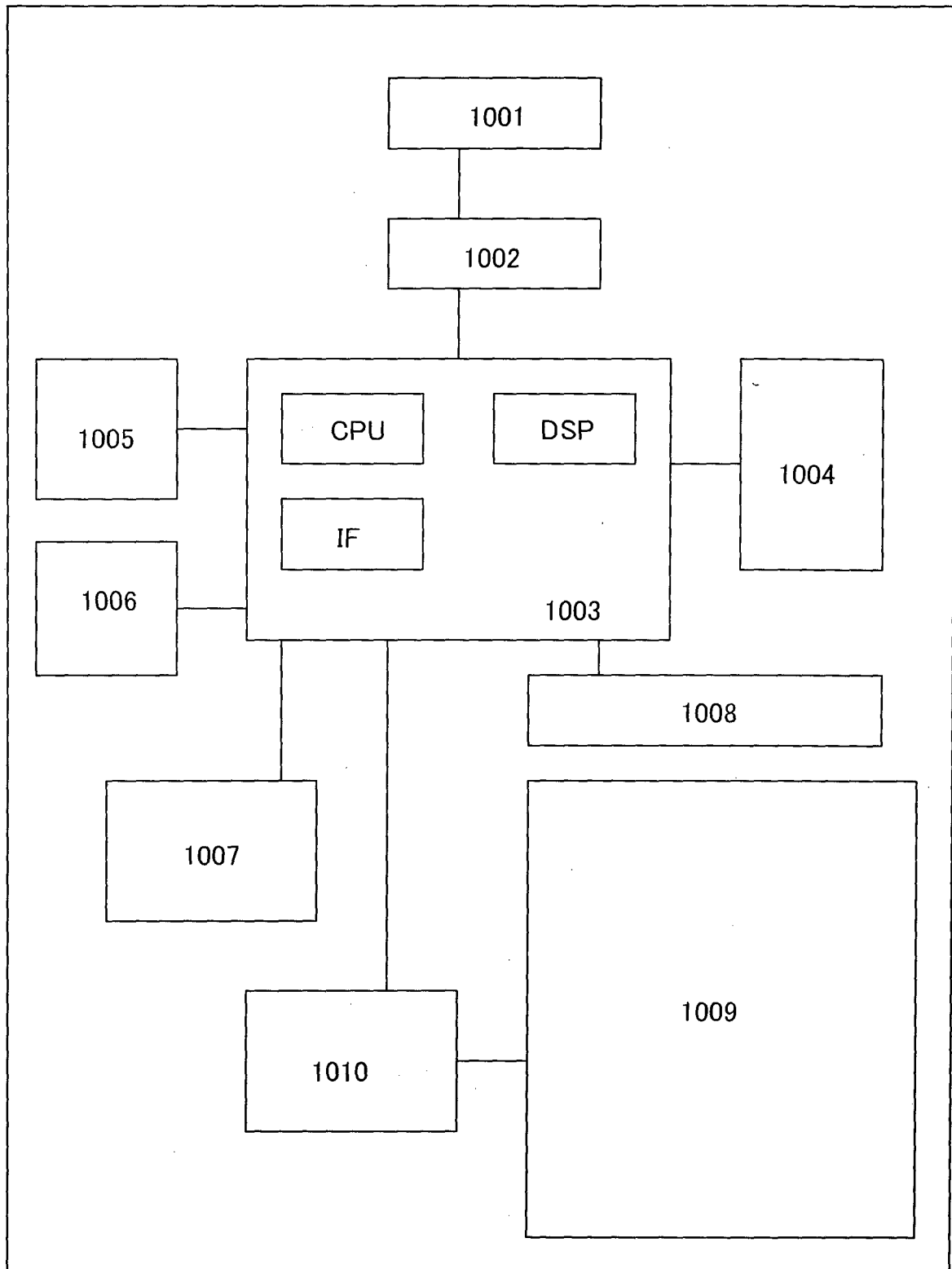


FIG. 10

FIG. 11A

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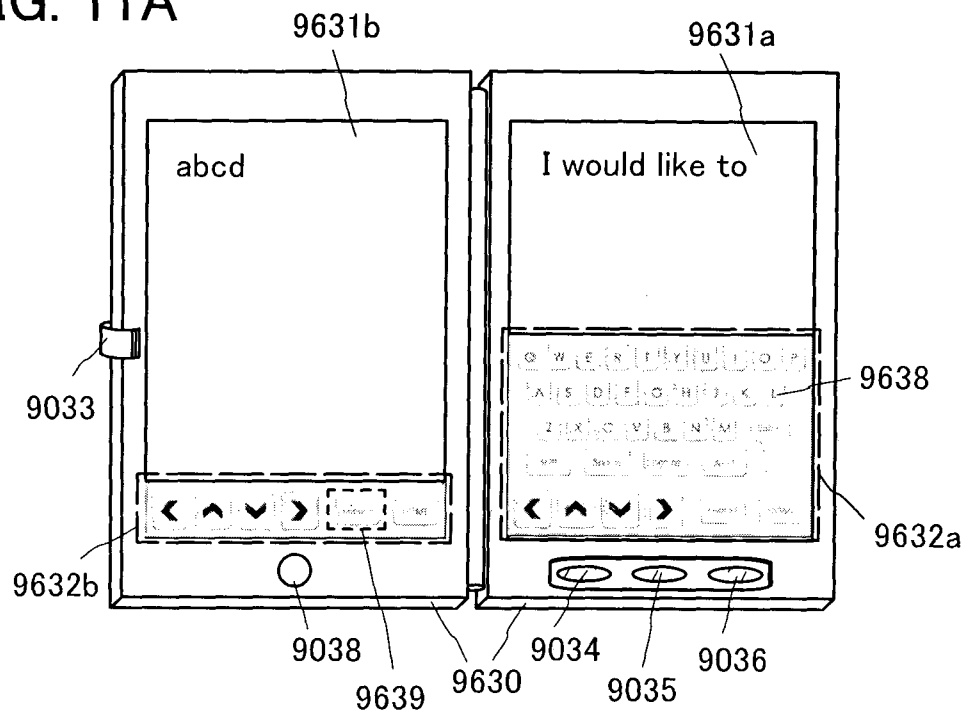


FIG. 11B

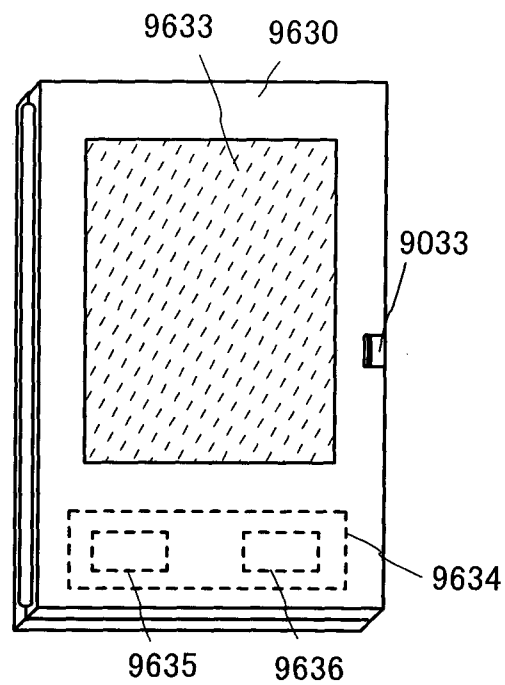


FIG. 12A

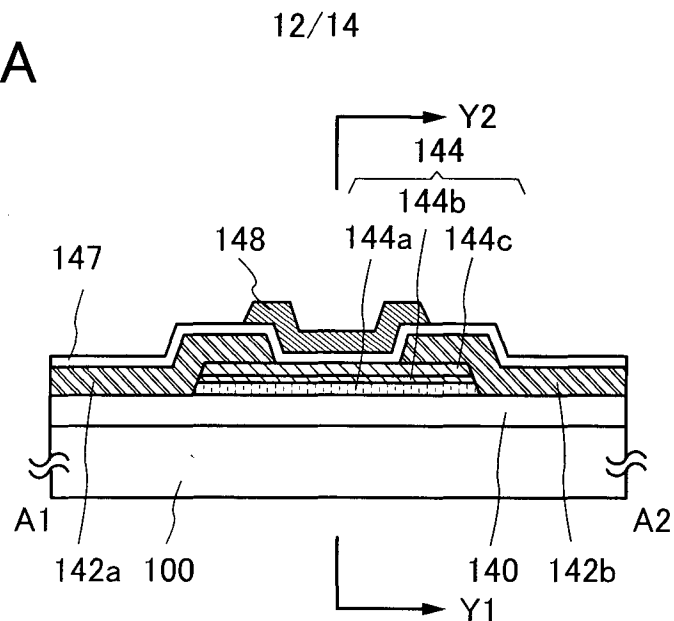


FIG. 12B

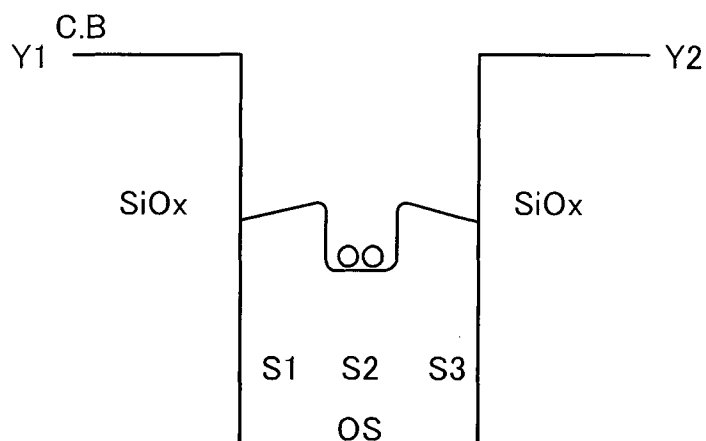


FIG. 12C

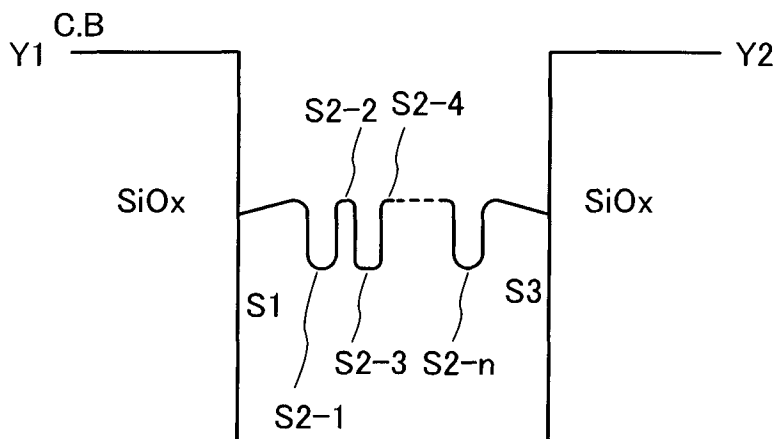
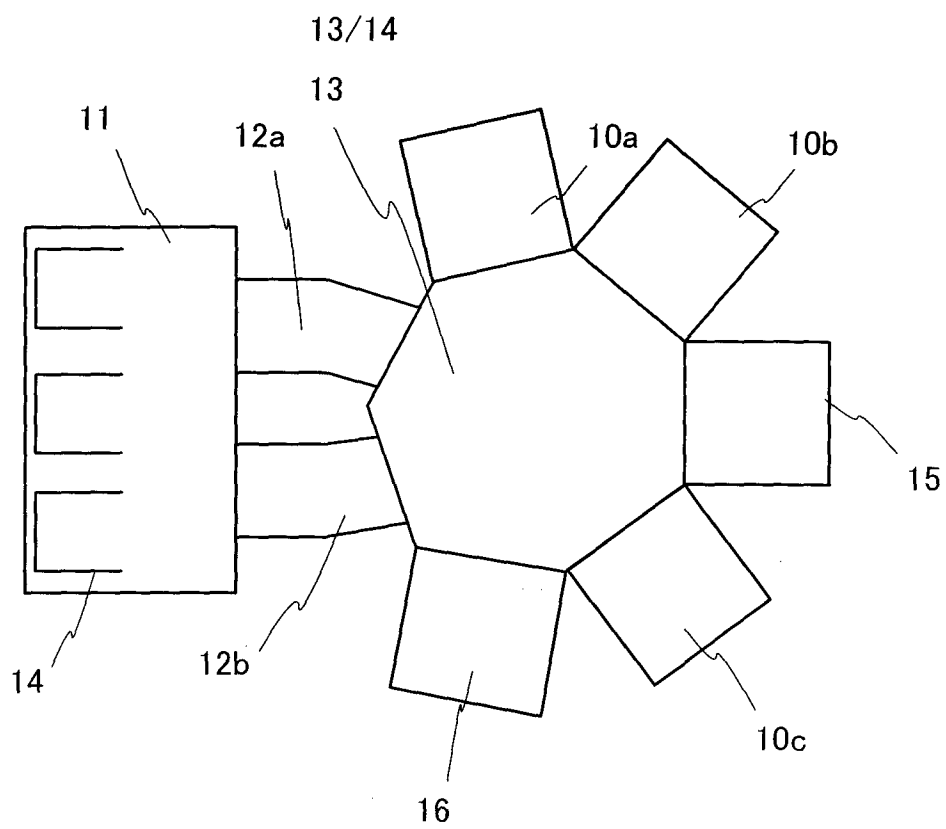


FIG. 13





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FIG. 14A

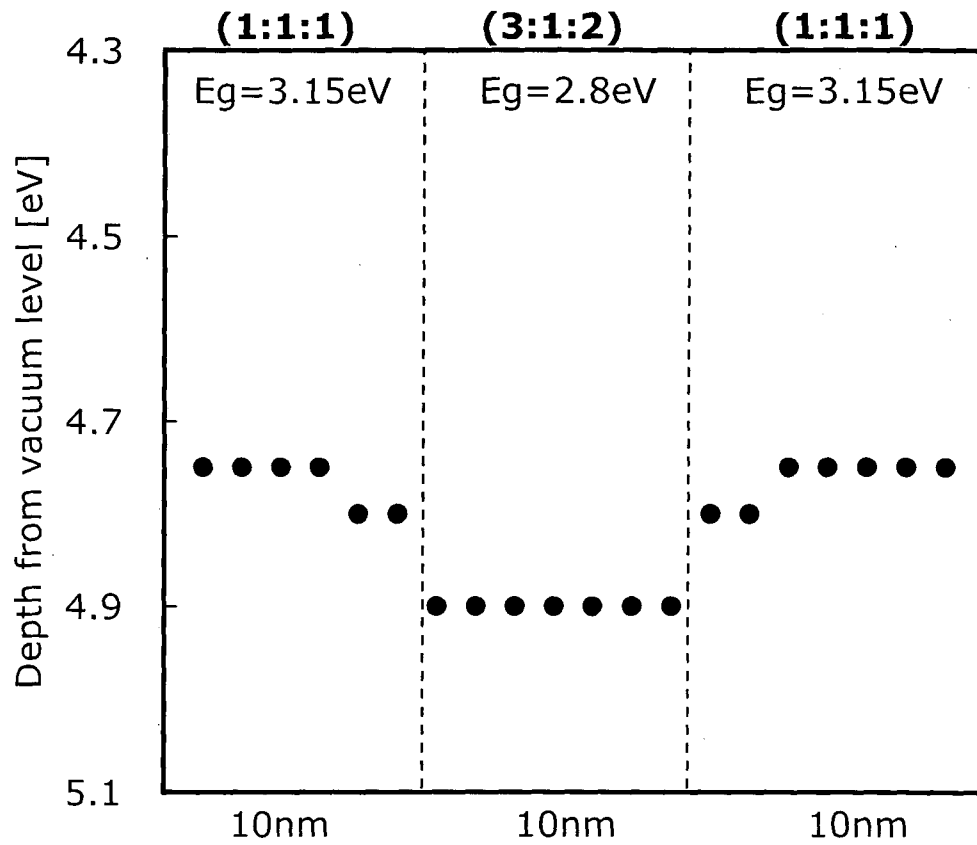
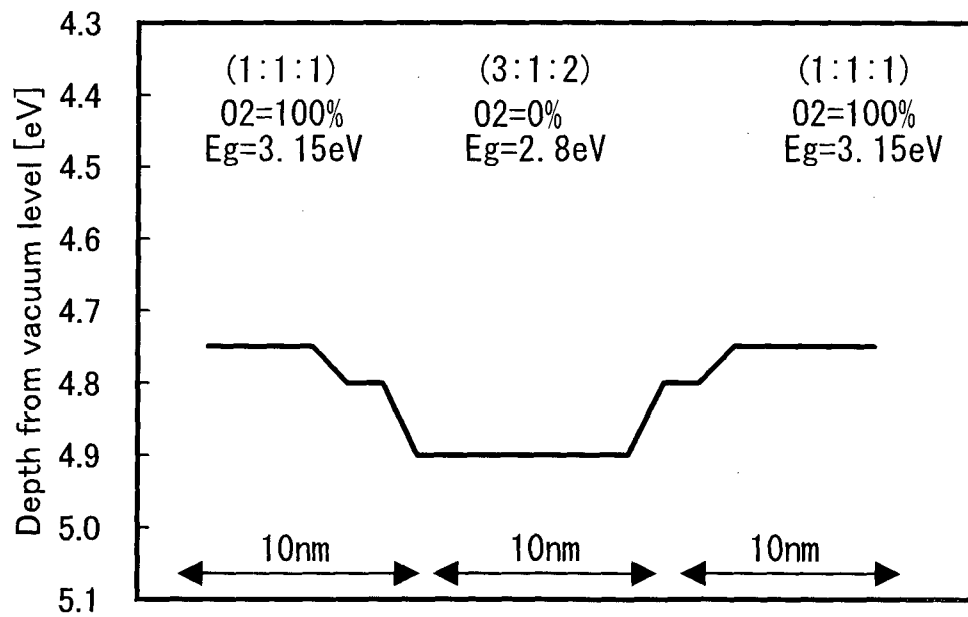


FIG. 14B



## INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2013/071578

## A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L29/786, H01L21/336, H01L21/363, H01L21/8234, H01L21/8242, H01L21/8247, H01L27/08, H01L27/088, H01L27/108, H01L27/115, H01L29/788, H01L29/792

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996  
 Published unexamined utility model applications of Japan 1971-2013  
 Registered utility model specifications of Japan 1996-2013  
 Published registered utility model applications of Japan 1994-2013

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2012-134467 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2012.07.12, paragraphs	1-3, 9-10, 15
Y	[0027]-[0124], [0148]-[0197], [0275]-[0283]; fig. 9, 17 & US 2012/0132903 A1 & WO 2012/073918 A1	4-8, 11-14, 16 -20
Y	JP 2011-187506 A (SONY CORPORATION) 2011.09.22, paragraphs [0023]-[0034], [0073]-[0077]; fig. 1, 8 & US 2011/0215328 A1 & CN 102194887 A & KR 10-2011-0100580 A	4-8, 11-14, 16 -20
Y	JP 2011-243745 A (FUJIFILM CORPORATION) 2011.12.01, paragraphs [0063]-[0067]; fig. 1 (No Family)	4-8, 11-14, 16 -20

☒ Further documents are listed in the continuation of Box C.
 ☐ See patent family annex.

\* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&amp;” document member of the same patent family

Date of the actual completion of the international search

22.08.2013

Date of mailing of the international search report

03.09.2013

Name and mailing address of the ISA/JP

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3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan

Authorized officer

**Yasuhiro TAKEGUCHI**

Telephone No. +81-3-3581-1101 Ext. 3559

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# INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2013/071578

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2012-9843 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2012.01.12, paragraphs [0052]-[0056]; fig. 1 & US 2011/0284848 A1	4-8, 11-14, 16-20
A	WO 2009/034953 A1 (IDEMITSU KOSAN CO., LTD.) 2009.03.19, paragraphs [0012]-[0031]; fig. 1 & TW 200915579 A	1-20

**INTERNATIONAL SEARCH REPORT**

International application No.

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CLASSIFICATION OF SUBJECT MATTER

H01L29/786(2006.01)i, H01L21/336(2006.01)i, H01L21/363(2006.01)i,  
H01L21/8234(2006.01)i, H01L21/8242(2006.01)i, H01L21/8247(2006.01)i,  
H01L27/08(2006.01)i, H01L27/088(2006.01)i, H01L27/108(2006.01)i,  
H01L27/115(2006.01)i, H01L29/788(2006.01)i, H01L29/792(2006.01)i