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- (54) Title:** STRUCTURE AND METHOD FOR FORMING POWER DEVICES WITH CARBON-CONTAINING REGION

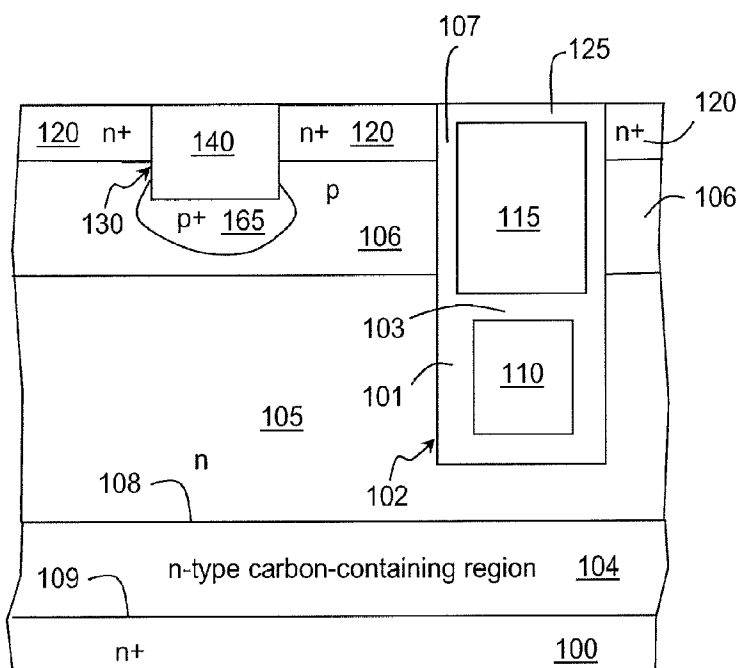


FIG. 1C

- (57) Abstract:** A field effect transistor (FET) includes body regions of a first conductivity type over a semiconductor region of a second conductivity type. The body regions form p-n junctions with the semiconductor region. Source regions of the second conductivity type extend over the body regions. The source regions form p-n junctions with the body regions. Gate electrodes extend adjacent to but are insulated from the body regions by a gate dielectric. A carbon-containing region extends in the semiconductor region below the body regions.



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STRUCTURE AND METHOD FOR FORMING POWER DEVICES WITH CARBON-CONTAINING REGION

CROSS-REFERENCES TO RELATED APPLICATIONS

- 5 [0001] This application claims the benefit of US Provisional Application No. 61/013,953, filed December 14, 2007, which is incorporated herein by reference in its entirety for all purposes.

BACKGROUND OF THE INVENTION

- 10 [0002] The present invention relates in general to semiconductor technology and more particularly to semiconductor power devices with carbon-doped region and method of forming the same.

[0003] Generally, an n-channel trench-gate power MOSFET includes an n-type substrate on which an n-type epitaxial layer is formed. The substrate embodies the drain of the MOSFET. A p-type body region extends into the epitaxial layer. Trenches extend through
15 the body region and into the portion of the epitaxial layer bounded by the body region and the substrate (commonly referred to as the drift region). A gate dielectric layer is formed on the sidewalls and bottom of each trench. Source regions flank the trenches. Heavy body regions are formed within the body region between adjacent source regions. Gate electrodes (e.g.,
20 from polysilicon) fill the trenches and embody the gate of the MOSFET. A dielectric cap covers the trenches and also partially extends over the source regions. A top-side metal layer electrically contacts the source regions and the heavy body regions. A bottom-side metal layer contacts the substrate

- [0004] In such conventional power devices, obtaining a higher breakdown voltage often
25 comes at the expense of higher on-resistance (R_{dson}). Thus, there is a need for techniques that improve breakdown voltage of power devices without adversely impacting other device characteristics.

[0005] In accordance with an embodiment of the invention, a field effect transistor (FET) includes body regions of a first conductivity type over a semiconductor region of a second conductivity type. The body regions form p-n junctions with the semiconductor region.

5 Source regions of the second conductivity type extend over the body regions. The source regions form p-n junctions with the body regions. Gate electrodes extend adjacent to but are insulated from the body regions by a gate dielectric. A carbon-containing region extends in the semiconductor region below the body regions.

[0006] In one embodiment, the semiconductor region further includes a substrate over
10 which the carbon-containing region extends, and a drift region of the second conductivity type that extends between the carbon-containing region and the body regions. The substrate has a doping concentration greater than that of the drift region.

[0007] In another embodiment, the carbon-containing region is in direct contact with the substrate and is spaced from the body regions.

15 [0008] In another embodiment, each gate electrode is disposed in a trench extending adjacent the body regions and terminating within the semiconductor region.

[0009] In another embodiment, each trench further includes a shield electrode disposed below the gate electrode. The gate and shield electrodes are insulated from one another by an inter-electrode dielectric layer.

20 [0010] In another embodiment, each trench includes a thick bottom dielectric extending along the bottom of the trench below the gate electrode.

[0011] In another embodiment, the gate electrodes extend laterally over the semiconductor and body regions and overlap the source regions.

[0012] In another embodiment, the entirety of carbon-containing region extends below the
25 trenches.

[0013] In another embodiment, the carbon-containing region abuts sidewalls of the trenches.

[0014] In another embodiment, the carbon-containing region is of the second conductivity type.

effect transistor (FET) includes forming a carbon-containing region over a substrate. An epitaxial layer is formed over the carbon-containing region. The epitaxial layer has a lower doping concentration than the substrate. A body region of a first conductivity type is formed in the epitaxial layer. The epitaxial layer is of a second conductivity type and forms a p-n junction with the body region. Gate electrodes are formed adjacent to but insulated from the body regions. Source regions of the second conductivity type are formed in the body regions. The source regions form p-n junctions with the body regions.

[0016] In one embodiment, the carbon-containing region is formed epitaxially.

10 [0017] In another embodiment, the carbon-containing region is in direct contact with the substrate.

[0018] In another embodiment, the carbon-containing region is of the second conductivity type.

15 [0019] In another embodiment, trenches extending into semiconductor regions are formed. The trenches house the gate electrodes.

[0020] In another embodiment, the entirety of carbon-containing region extends below the trenches.

[0021] In another embodiment, the trenches extend into the carbon-containing region.

20 BRIEF DESCRIPTION OF THE DRAWINGS

[0022] FIGS. 1A-1C are simplified cross-sectional views showing an exemplary method for forming a shielded gate trench power MOSFET in accordance with an embodiment of the present invention;

25 [0023] FIG. 1D is a schematic figure showing an exemplary carbon concentration profile within a carbon-containing layer in accordance with an embodiment of the present invention;

[0024] FIG. 2 is a simplified cross-sectional view showing an exemplary shielded gate trench power MOSFET in accordance with another embodiment of the present invention;

[0025] FIG. 3 is a simplified cross-sectional view showing an exemplary trench gate power MOSFET in accordance with an embodiment of the present invention;

accordance with an embodiment of the present invention; and

[0027] FIGS. 5A-5D are simplified cross-sectional views showing an exemplary method for forming a shielded gate trench power MOSFET in accordance with yet another

5 embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0028] According to the embodiments of the present invention, techniques directed to integrated circuits and their processing are disclosed. More particularly, the invention provides methods and devices for power field effect transistors (FETs) which include a carbon-containing layer. The carbon-containing layer is configured to provide a higher breakdown voltage and other advantageous features described more fully below. Merely by way of example, the invention has been described in the context of trench power MOSFETs, but it would be recognized that the invention has a much broader range of applicability. For example, the invention can be applied to planar power MOSFETs as well as to trench gate and planar gate IGBTs.

[0029] Depending on the embodiments, the carbon-containing layer may be formed in the drift region a trench gate FET. Alternatively, the carbon containing layer may abut sidewalls of trenches extending into the drift region. In some embodiments, the carbon-containing layer has a graded profile to allow for smooth transition from adjacent silicon regions. The above features may be in one or more of the embodiments described herein and their obvious variants. One of ordinary skill in the art would recognize many variations, modifications, and alternatives in view of this disclosure.

[0030] FIGS. 1A-1C are simplified cross-sectional views showing an exemplary method for forming a shielded gate trench power MOSFET in accordance with an embodiment of the present invention. In FIG. 1A, a carbon-containing layer 104 is formed over a substrate 100. Substrate 100 can be a silicon substrate, a III-V compound substrate, a silicon/germanium (SiGe) substrate, an epi-substrate, a silicon-on-insulator (SOI) substrate, a display substrate such as a liquid crystal display (LCD), a plasma display, an electro luminescence (EL) lamp display, or a light emitting diode (LED) substrate, for example. The embodiment shown is an n-channel MOSFET, and substrate 100 may include n-type dopants such as phosphorus, arsenic and/or other group V elements.

[0031] In some embodiments, carbon-containing layer 104 may be a carbon-containing

silicon epitaxial layer, a containing-carbon silicon-germanium epitaxial layer, or various combinations thereof. In some embodiments, carbon-containing layer 104 may be formed by an epitaxial process. The epitaxial process may use a silicon-containing precursor such as silane (SiH_4) and a carbon-containing precursor such as alkane (e.g., propane) to form carbon-containing layer 104. In some embodiments, the carbon-containing precursor may have a flow rate between about 1 standard cubic centimeter per minute (sccm) and about 1,000 sccm. In some embodiments, carbon containing layer 104 may have a carbon concentration between about 1×10^{18} and about 1×10^{21} . For the n-channel MOSFET embodiment shown, carbon-containing layer 104 may include n-type dopants such as phosphorus, arsenic and/or other group V dopants. In some embodiments, carbon-containing layer 104 may have a thickness between about 500 Å and about 5 μm. In other embodiments, carbon-containing layer 104 may have a thickness of about 1 μm.

[0032] In FIG. 1B, n-type epitaxial layer 105 is formed over carbon-containing layer 104.

In some embodiments, epitaxial layer 105 may be a silicon epitaxial layer, a silicon-germanium epitaxial layer, or a combination thereof. Epitaxial layer 105 may have n-type dopants such as phosphorus, arsenic and/or other group V dopant.

[0033] In some embodiments, carbon-containing layer 104 and epitaxial layer 105 are formed by different processes. In other embodiments, carbon-containing layer 104 and epitaxial layer 105 are formed in a single process. For example, during the formation of carbon-containing layer 104, the carbon-containing precursor, e.g., propane, is added within the processing chamber for interacting with the silicon precursor. After the formation of carbon-containing layer 104, the flow of the carbon-containing precursor is reduced and/or turned off, such that epitaxial layer 105 with little or no carbon therein is formed over carbon-containing layer 104.

[0034] In FIG. 1C, p-type body region 106 may be formed in or over epitaxial layer 105.

In some embodiments, body region 106 may be formed by implanting dopants in epitaxial layer 105. In other embodiments, body region 106 may be formed by an epitaxial process over epitaxial layer 105. Trenches 102 extending through body region 106 and terminating within a region of epitaxial layer 105 bounded by body region 106 and substrate 100 is formed using conventional techniques. The region of epitaxial layer 105 bounded by body region 106 and substrate 100 is commonly referred to as the drift region. Shield dielectric

layer 101 lining the bottom and the lower sidewalls of trenches 102 is formed using known processes.

[0035] Shield electrode 110 (e.g., comprising doped or undoped polysilicon) is formed in a bottom portion of each trenches 102 using conventional techniques. Inter-electrode dielectric 103 (e.g., comprising oxide) extending over shield electrode 110 is formed in each trench using conventional techniques. Gate dielectric layer 107 lining upper trench sidewalls is formed using known techniques. In some embodiments, gate dielectric layer 107 is thinner than shield dielectric layer 101. Gate electrode 115 is formed in an upper portion of each trench 102 using conventional methods. N-type source regions 120 are formed in body regions 106 adjacent the trenches, using known techniques.

[0036] Gate dielectric 107 may comprise, for example, oxide, nitride, oxynitride, dielectric material, high-k dielectric material or various combinations thereof. In some embodiments, the high-k dielectric can be one or more of aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), hafnium oxynitride (HfON), hafnium silicate (HfSiO_4), zirconium oxide (ZrO_2), zirconium oxynitride (ZrON), zirconium silicate (ZrSiO_4), yttrium oxide (Y_2O_3), lanthanum oxide (La_2O_3), cerium oxide (CeO_2), titanium oxide (TiO_2), tantalum oxide (Ta_2O_5), or combinations thereof. Gate dielectric 107 may be formed by, for example, a chemical vapor deposition (CVD) process, a physical vapor deposition (PVD) process or other known processes. Gate electrodes 115 may comprise, for example, polysilicon; amorphous silicon; metal-containing material such as Ru, Ti, Ta, W, Hf; metal nitride stacked gates; metal oxide gates such as RuO_2 or IrO_2 ; metal nitride gates such as MoN, WN, TiN, TaN, TaAlN; poly SiGe; gate silicide such as CoSi_2 or NiSi ; or various combinations thereof. Gate electrodes 115 may be formed by, for example, a CVD process, a PVD process, an electrochemical plating process, an electroless plating process or other known techniques.

[0037] In FIG. 1A, a dielectric layer 125 overlies gate electrodes 115. Dielectric layer 125 may comprise, for example, oxide, nitride, oxynitride, other dielectric material or various combinations thereof. In some embodiments, dielectric layer 125 may be a boron-phosphorus-silicate-glass (BPSG) layer which can be formed by, for example, a CVD process. While dielectric layer 125 is shown as having a flat top surface, in some embodiments, dielectric layer 125 has a dome shape and extends out of trench 102 and overlaps source regions 120.

[0038] Contact openings 130 are formed in a center portion of body region 106 between adjacent trenches. In some embodiments, contact openings 130 are formed using a patterned mask layer having a pattern corresponding to openings 130. The patterned mask may be, for example, a patterned photoresist layer or a patterned dielectric layer. P+ heavy body region 165 is formed in body region 106 along the bottom of each contact opening 130. Heavy body region 165 may be formed using conventional techniques such as implanting dopants in body region 106 through contact openings 130.

[0039] A top-side source interconnect layer (not completely shown) is formed over the structure, substantially filling contact opening 130. The Source interconnect layer makes direct contact with heavy body region 235 along the bottom of contact opening 230, and with source regions 120 at least along sidewalls of contact opening 130. The source interconnect layer may comprise, for example, copper, tungsten, aluminum, aluminum copper, titanium, tantalum, cobalt, nickel, platinum, polysilicon, or various combinations thereof. The source interconnect layer may be formed by a CVD process, a PVD process, an electrochemical planting process and/or an electroless plating process. A backside drain interconnect layer (not shown) may be formed on the backside of substrate 100. The drain interconnect layer may comprise similar material as the top-side source interconnect layer, and can be formed in a similar manner to the top-side source interconnect layer.

[0040] While the FIGS. 1A-1C show only one trench 102 and the structure appears asymmetric, it is to be understood that the design to which the cross section views shown and described herein correspond is a cell-based design where one cell is repeated many times to form the complete device.

[0041] In FIG. 1C, carbon-containing layer 104 may be directly under or within epitaxial layer 105. In some embodiments, a bottom surface 109 of carbon-containing layer 104 may be adjacent to by spaced from substrate 100. In other embodiments, bottom surface 109 may directly contact substrate 100. As shown in FIG. 1A, top surface 108 of carbon-containing layer 104 extends under trench 102.

[0042] FIG. 1D is a graph showing an exemplary carbon concentration profile within carbon-containing layer 104 in accordance with an embodiment of the present invention. In some embodiments, the carbon distribution within carbon-containing layer 104 may have a Gaussian distribution profile. In some embodiments, the carbon concentration near top surface 108 of carbon-containing layer 104 is about 1×10^{18} . In other embodiments, the

carbon concentration near bottom surface 109 of carbon-containing layer 104 is also about

1×10^{18} . In still other embodiments, the carbon concentration at the peak of the Gaussian

distribution profile of carbon-containing layer 104 is about 1×10^{21} . In yet other

embodiments, carbon-containing layer 104 has a graded carbon distribution profile to allow

for smooth transition from adjacent silicon regions. For example, the carbon concentration of

carbon-containing layer 104 is gradually increased from bottom surface 109 and top surface

108 of carbon-containing layer 104 to reach a peak concentration in a center region of layer

104.

[0043] Carbon-containing layer 104 advantageously has increased energy band gap such

that the avalanche breakdown voltage is desirably increased. Also, carbon-containing layer

104 desirably increases the thermal conductivity of the power MOSFET. Accordingly, heat

generated during operation of the power MOSFET may be dissipated through carbon-

containing layer 104 more rapidly.

[0044] While carbon-containing layer 104 is shown extending below trench 102, it can be

formed to extend higher up and abut sidewalls of trench 102. FIG. 2 shows such structure.

The structure in FIG. 2 is substantially similar to that in FIG. 1C except that carbon-

containing layer 104a is formed to extend up along the sidewalls of trench 102. As shown,

top surface 111 of carbon-containing layer 104a is adjacent to but is separated from body

region 125 by n-type drift region 105b. Materials and methods for forming carbon-

containing layer 104a are similar to those of carbon-containing layer 104 described above in

reference to FIG. 1C, except that carbon-containing layer 104a is thicker than carbon-

containing layer 104.

[0045] FIG. 3 is a simplified cross-sectional view of an exemplary trench gate MOSFET

according to another embodiment of the present invention. This embodiment is substantially

similar to the embodiment in FIG. 1C except that no shield electrode is formed under gate

electrode 145. Instead a dielectric layer which in some embodiments is thicker than gate

dielectric 107 (i.e., what is commonly known as thick bottom dielectric TBO) extends under

gate electrode 145 along the trench bottoms.

[0046] FIG. 4 is a simplified cross-sectional view of an exemplary planar MOSFET in

accordance with yet another embodiment of the invention. The structure in FIG. 4 is the

planar gate variation of the trench gate MOSFET shown in FIG. 3, and thus many of the same

layer of the various embodiments also apply to the structure in FIG. 4.

[0047] In FIG. 4, carbon-containing layer 205 extends over substrate 200. In some embodiments, the materials and methods for forming carbon-containing layer 205 and substrate 200 are similar to carbon-containing layer 104 and substrate 100 in FIG. 1C. N-type epitaxial layer 210 is formed over carbon-containing layer 205. In some embodiments, carbon-containing layer 205 is formed within epitaxial layer 210. Materials and methods for forming epitaxial layer 210 may be similar to epitaxial layer 105 in FIG. 1C.

[0048] The stacks of gate dielectric layer 215 and gate electrode 220 are formed over epitaxial layer 210 using known techniques. Body regions 225 are formed in epitaxial layer 210 using conventional techniques. Source regions 230 are formed in body regions 225 using conventional techniques. Heavy body contact openings are formed in body region 225 and later filled with contact material 240. Contact material 240 may form part of a top-side source interconnect layer (not shown) that extends over the structure but is insulated from gate electrodes 220.

[0049] FIGS. 5A-5D are simplified cross-sectional views showing an exemplary method for forming a shielded gate trench power MOSFET in accordance with another embodiment of the present invention. In FIG. 5A, epitaxial layer 304 may be formed over substrate 300. Materials and methods for forming substrate 300 may be similar to substrate 100 in FIG. 1A. Epitaxial layer 304 may be a doped or an undoped silicon epitaxial layer or silicon-germanium epitaxial layer. In some embodiments for forming an n-type MOSFET, epitaxial layer 304 may have dopants of phosphorus, arsenic or other group V dopant.

[0050] In FIG. 5B, a carbon implantation process 391 may be carried out to implant carbon into epitaxial layer 304 to form carbon-containing layer 304a. Carbon implantation process 391 can be designed to form carbon-containing layer 304a having a dopant profile similar to that of carbon-containing layer 104 in FIGS. 1A-1D.

[0051] In FIG. 5C, epitaxial layer 305 is formed over carbon-containing layer 304a. In some embodiments, materials and methods for forming the epitaxial layer 305 may be similar to epitaxial layer 105 in FIG. 1B. In FIG. 5D, the trench structure and the materials therein as well as body region 306, source regions 320, heavy body region 165 and contact opening 130 are all substantially similar to those in FIG. 1C and similar techniques to those described above may be used to form these regions and structures.

containing region is used, multiple such regions may be employed in the structures. Also, the techniques in accordance with the invention describe herein are not limited to any particular types of transistors and may be implemented in a variety of devices where incorporating a carbon-containing layer in the device is desired. For example, the process sequence depicted in FIGS. 1A-1C can be modified by those skilled in the art to form: p-channel shielded gate trench gate MOSFETs (i.e., a transistor similar in structure to that in FIG. 1C except that the conductivity type of all silicon regions is reversed); n-channel shielded gate trench IGBT (i.e., a transistor similar in structure to that in FIG. 1C except that a p-type substrate is used instead of the n-type substrate); p-channel shielded gate IGBT (i.e., a transistor similar in structure to that in FIG. 1C but with silicon regions of opposite conductivity except the substrate is kept n-type); p-channel variation of the trench gate MOSFET in FIG. 3; p-channel and n-channel IGBT variations of the trench gate MOSFET in FIG. 4; p-channel and n-channel IGBT variations of the planar gate MOSFET in FIG. 4; planar gate and trench gate synchronous FETs (i.e., integrated trench gate or shielded gate or planar gate MOSFET and Schottky rectifier); trench gate and planar gate variety of laterally conducting MOSFETs (i.e., a transistor where the drain contact is made on the top-side) and suprajunction variations of all the above devices (i.e., devices with columns of alternating conductivity type silicon).

[0053] Thus, while the above is a complete description of specific embodiments of the present invention, various modifications, variations, and alternatives may be employed. The scope of this invention should thus not be limited to the embodiments described herein, but is instead defined by the following claims.

- 1 1. A field effect transistor (FET), comprising:
2 body regions of a first conductivity type over a semiconductor region of a
3 second conductivity type, the body regions forming p-n junctions with the semiconductor
4 region;
5 source regions of the second conductivity type over the body regions, the
6 source regions forming p-n junctions with the body regions;
7 gate electrodes extending adjacent to but being insulated from the body
8 regions by a gate dielectric;
9 a carbon-containing region extending in the semiconductor region below the
10 body regions.
- 1 2. The FET of claim 1 wherein the semiconductor region further
2 comprises:
3 a substrate over which the carbon-containing region extends; and
4 a drift region of the second conductivity type extending between the carbon-
5 containing region and the body regions, wherein the substrate has a doping concentration
6 greater than that of the drift region.
- 1 3. The FET of claim 2 wherein the carbon-containing region is in direct
2 contact with the substrate and is spaced from the body regions.
- 1 4. The FET of claim 1, wherein each gate electrode is disposed in a
2 trench extending adjacent the body regions and terminating within the semiconductor region.
- 1 5. The FET of claim 4, wherein each trench further includes a shield
2 electrode disposed below the gate electrode, the gate and shield electrodes being insulated
3 from one another by an inter-electrode dielectric layer.
- 1 6. The FET of claim 4 wherein each trench includes a thick bottom
2 dielectric extending along the bottom of the trench below the gate electrode.
- 1 7. The FET of claim 1, wherein the gate electrodes extend laterally over
2 the semiconductor and body regions and overlap the source regions.

1 8. The FET of claim 4, wherein the entirety of carbon-containing region
2 extends below the trenches.

1 9. The FET of claim 4, wherein the carbon-containing region abuts
2 sidewalls of the trenches.

1 10. The FET of claim 1, wherein the carbon-containing region is of the
2 second conductivity type.

1 11. A method of forming a field effect transistor (FET), comprising:
2 forming a carbon-containing region over a substrate;
3 forming an epitaxial layer over the carbon-containing region, the epitaxial
4 layer having a lower doping concentration than the substrate;
5 forming a body region of a first conductivity type in the epitaxial layer, the
6 epitaxial layer being of a second conductivity type, the body region forming a p-n junction
7 with the epitaxial layer;
8 forming gate electrodes adjacent to but insulated from the body regions; and
9 forming source regions of the second conductivity type in the body regions,
10 the source regions forming p-n junctions with the body regions.

1 12. The method of claim 11 wherein the carbon-containing region is
2 formed epitaxially.

1 13. The method of claim 11 wherein the carbon-containing region is in
2 direct contact with the substrate.

1 14. The method of claim 11, wherein the carbon-containing region is of the
2 second conductivity type.

1 15. The method of claim 11 wherein the carbon in the carbon-containing
2 region has a Gaussian profile.

1 16. The method of claim 11, further comprising:
2 forming trenches extending into semiconductor regions, the trenches housing
3 the gate electrodes.

1 17. The method of claim 16 further comprising:
2 before forming the gate electrodes:
3 forming a shield dielectric layer lining lower sidewalls and bottom of
4 each trench;
5 forming a shield electrode in a lower portion of each trench; and
6 forming an inter-electrode dielectric layer in each trench over the
7 shield electrode.

1 18. The method of claim 16 further comprising:
2 before forming the gate electrode, forming a thick bottom dielectric extending
3 along the bottom of the trench.

1 19. The method of claim 11, wherein the gate electrodes extend laterally
2 over the semiconductor and body regions and overlap the source regions.

1 20. The method of claim 16 wherein the entirety of carbon-containing
2 region extends below the trenches.

1 21. The FET of claim 16, wherein the trenches extend into the carbon-
2 containing region.

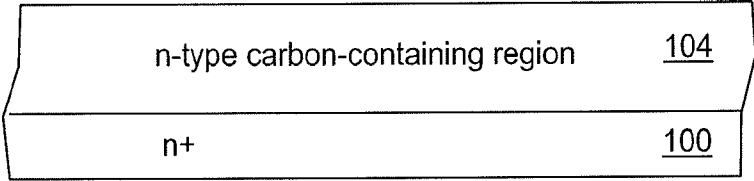


FIG. 1A

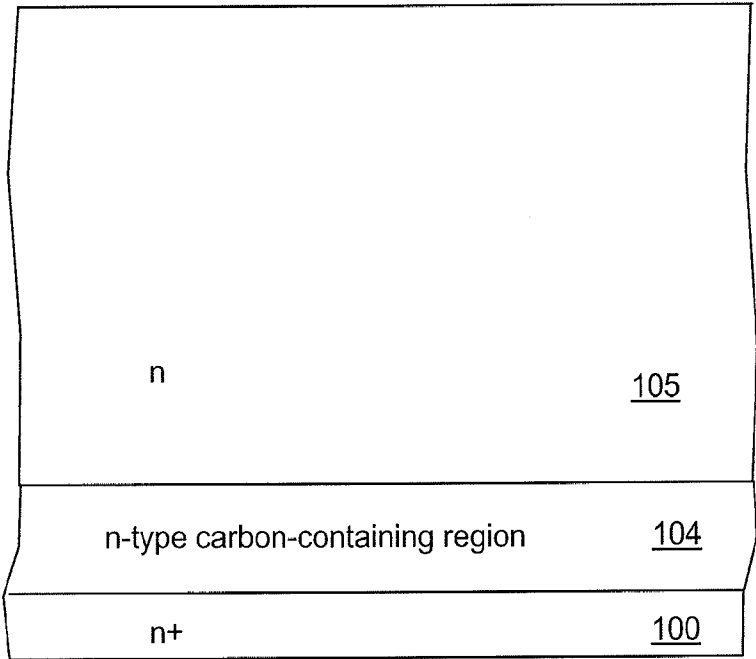


FIG. 1B

2/7

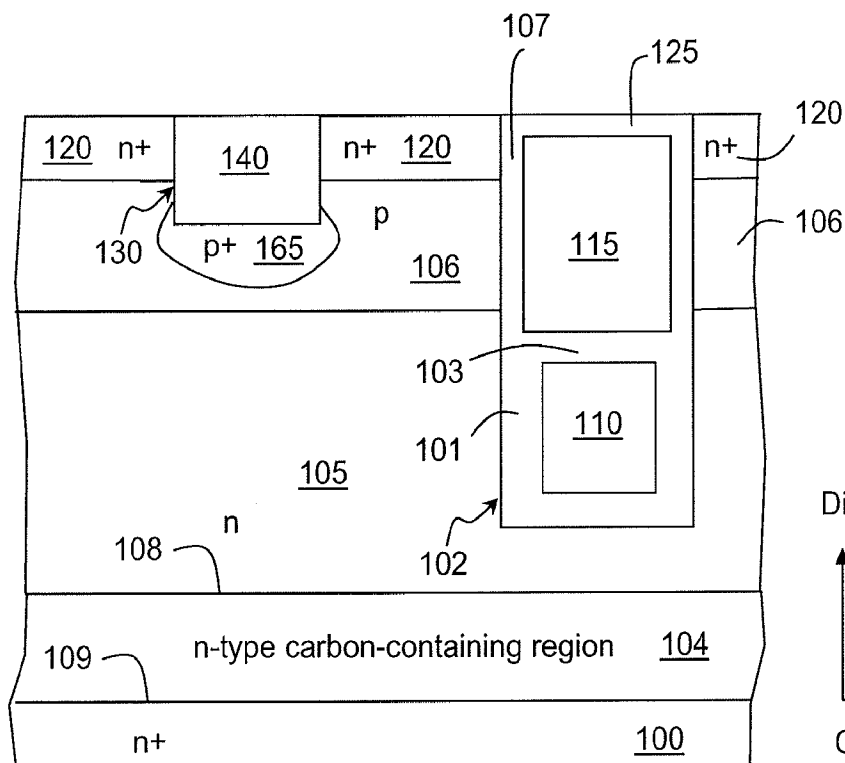


FIG. 1C

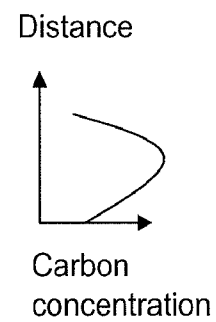


FIG. 1D

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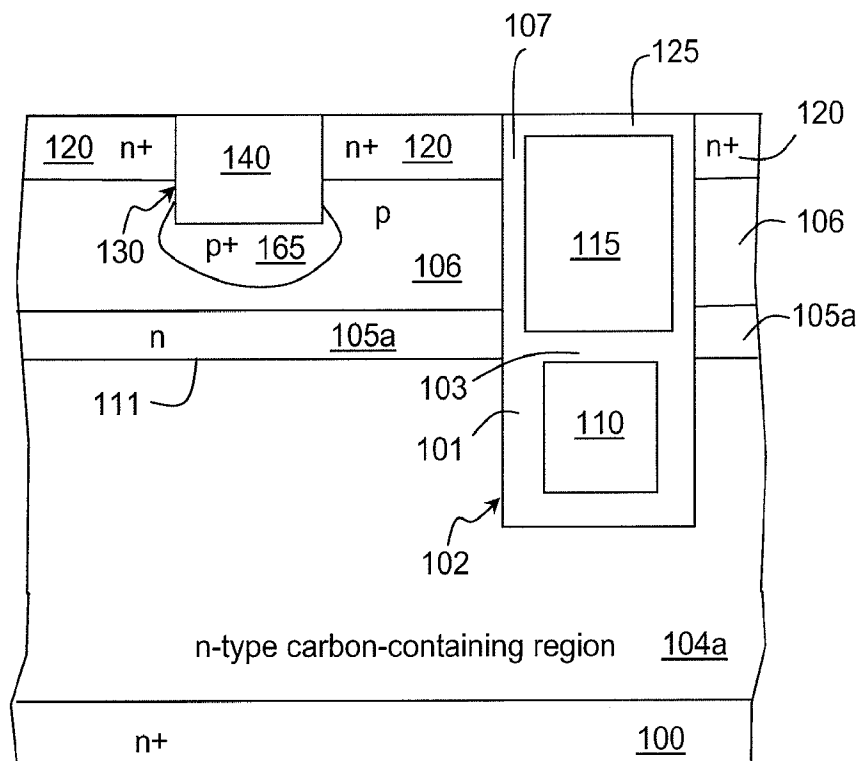


FIG. 2

4/7

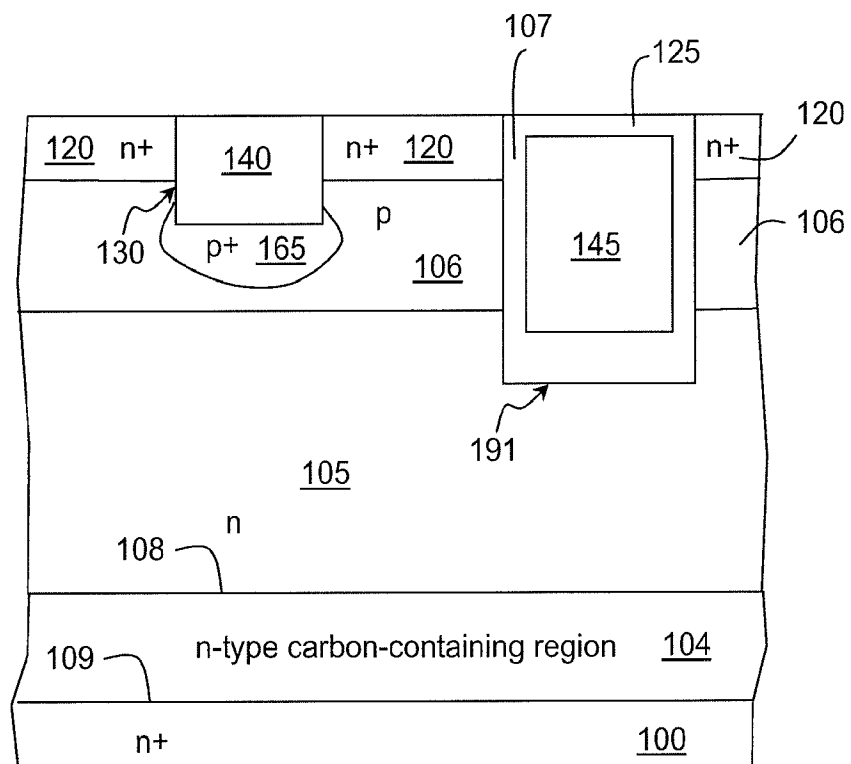


FIG. 3

5/7

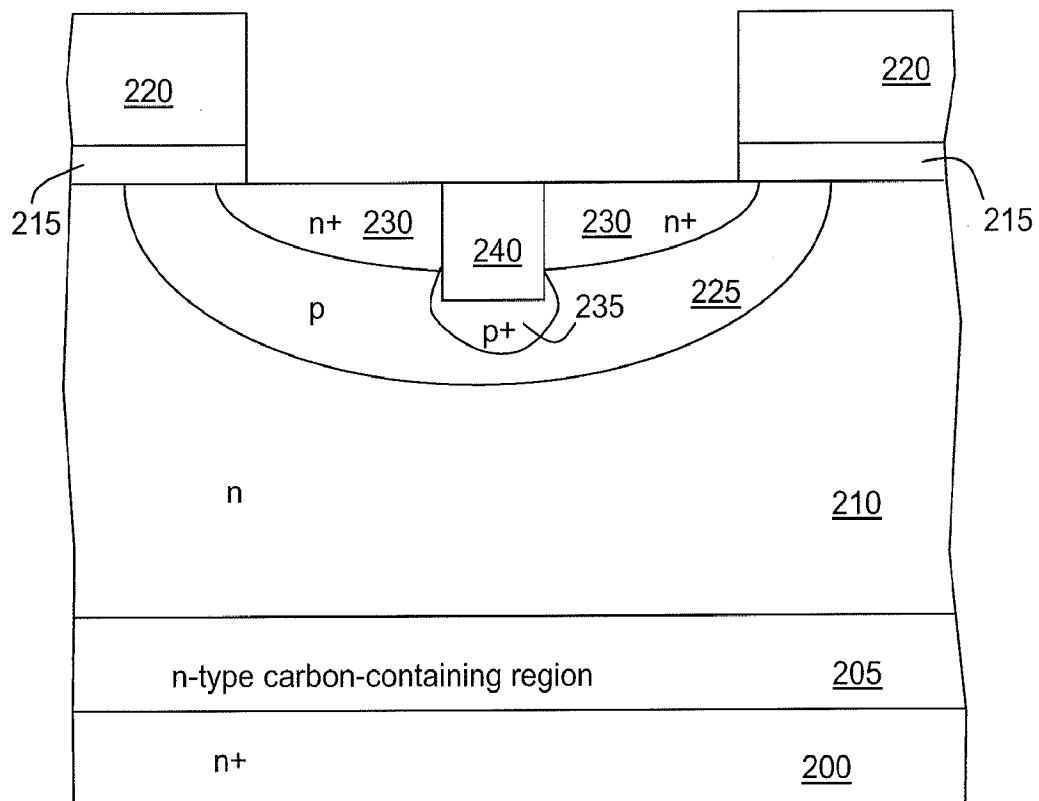


FIG. 4

6/7

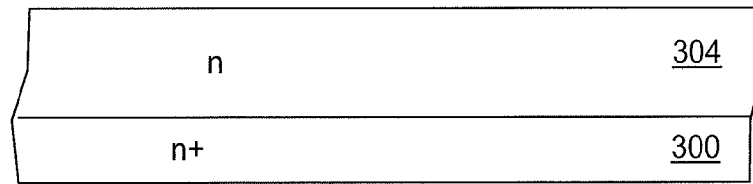


FIG. 5A

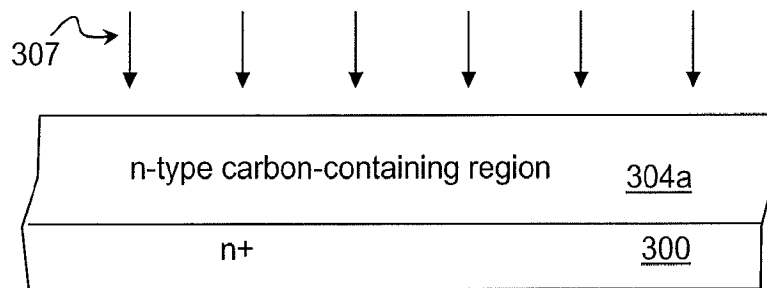


FIG. 5B

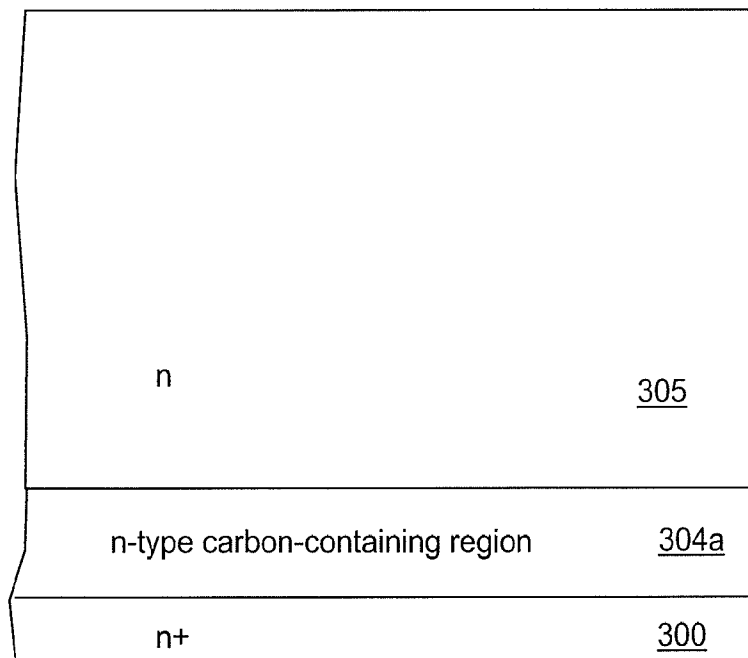


FIG. 5C

7/7

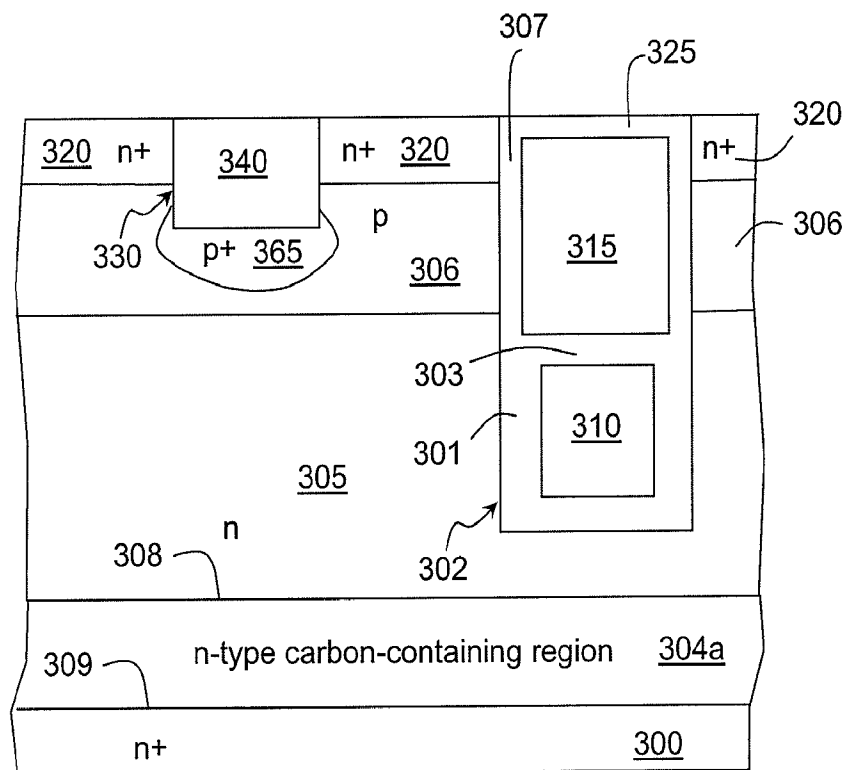


FIG. 5D

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 08/86841

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H01L 23/48 (2009.01)

USPC - 257/213

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

USPC: 257/213

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC: 257/213, 287, 322 keyword limited - see search terms below

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PubWest (PGPB,USPT,USOC,EPAB,JPAB), Google Scholar, Google Patent

Search terms: FET, field effect transistor, carbon, carbide, layer, region, semiconductor, trench, well, epitaxial, drift, shield, electrode, disposed, dielectric, insulator, gate, substrate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2004/0119076 A1 (RYU) 24 June 2004 (24.06.2004), para [0010]-[0011], [0013]-[0014], [0018], [0040], [0043], [0046], [0053]	1-21
Y	US 2006/0214222 A1 (CHALLA et al.) 28 September 2006 (28.09.2006), para [0109], [0115]-[0116], [0127], [0164], [0168]	1-21
Y	US 5,950,076 A (BALIGA) 07 September 1999 (07.09.1999), col 2, ln 65 to col 3, ln 2, col 3, ln 15-18	15
A	US 6,198,157 B1 (ISHIDA et al.) 06 March 2001 (06.03.2001), entire document	1-21

☐ Further documents are listed in the continuation of Box C.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

04 February 2009 (04.02.2009)

Date of mailing of the international search report

13 FEB 2009

Name and mailing address of the ISA/US

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