

[54] PROTECTIVE RELAY USING AN INDICATOR AND ALARM CIRCUIT

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[51] Int. Cl.G08b 7/00, G08b 21/00

[58] Field of Search.....340/256, 326, 327, 253, 322, 340/309.1, 213; 317/28, 29

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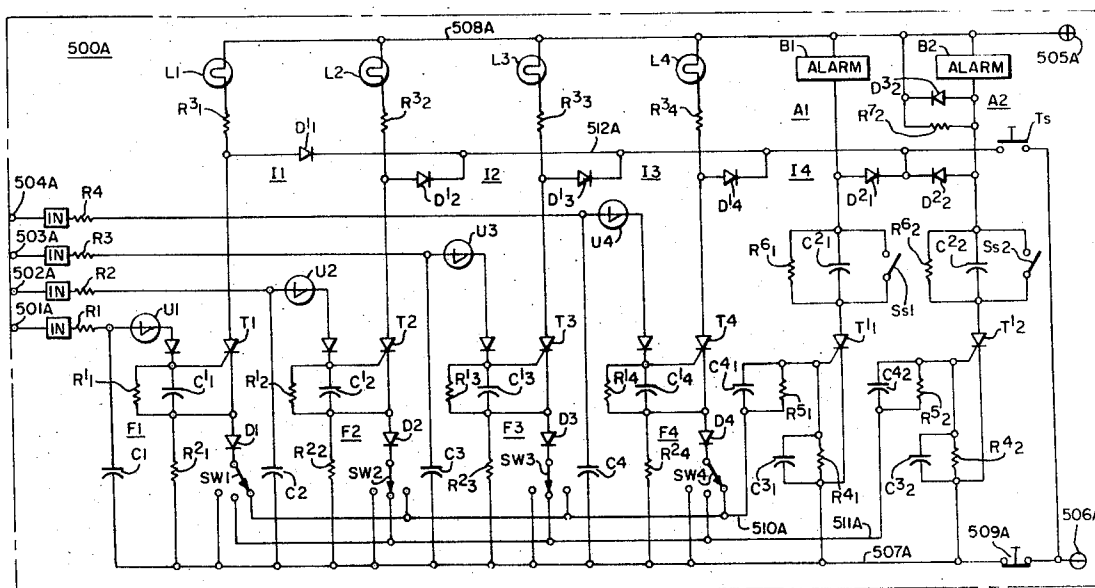
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[57] ABSTRACT

A protective relaying apparatus including an indicator and an alarm network to indicate, until reset, an indication whenever faulty operation has occurred and to provide an alarm which responds to each occurrence of any faulty operation and wherein the operation of the indicator is independent of the alarm.

18 Claims, 5 Drawing Figures



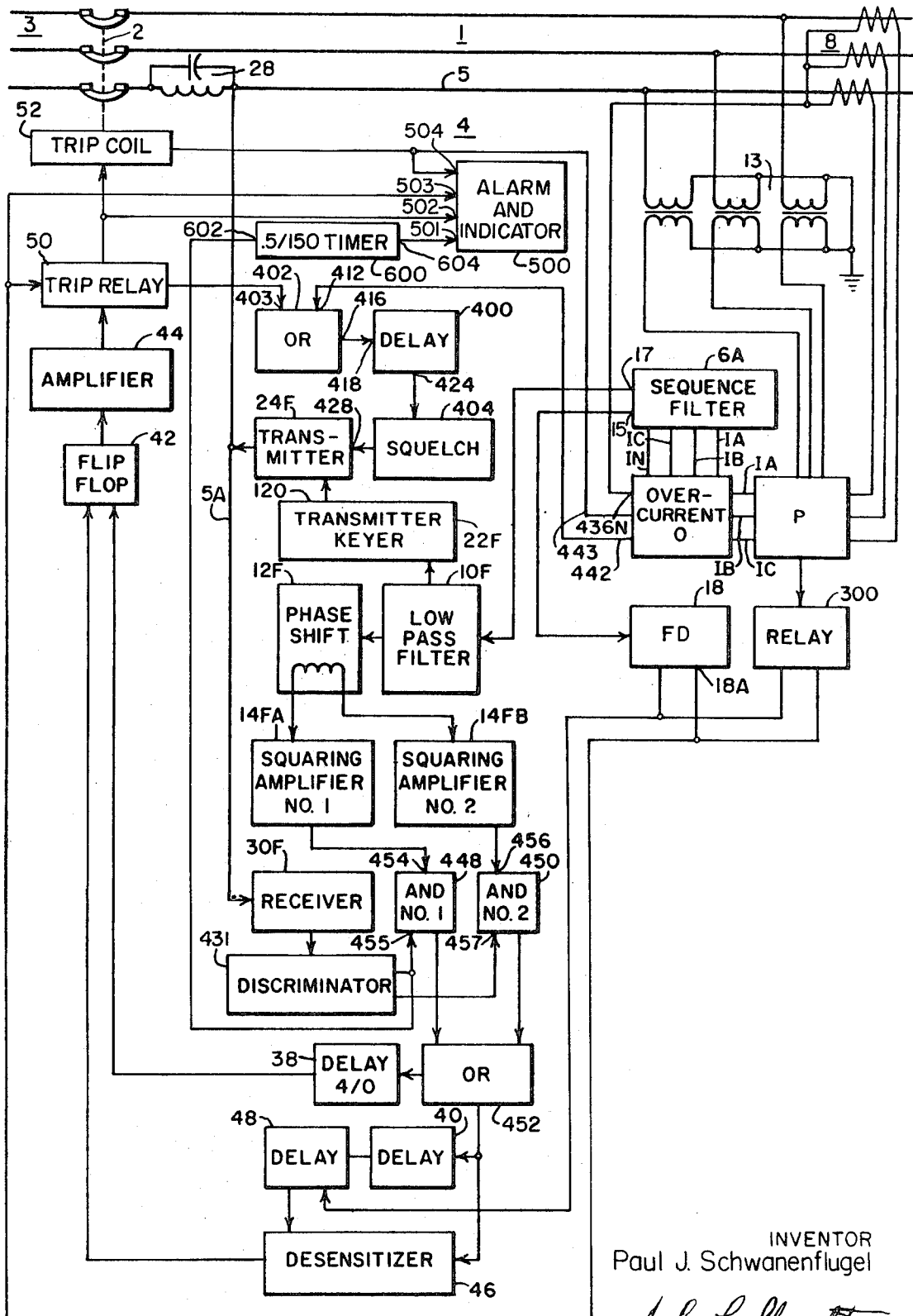


FIG. 1

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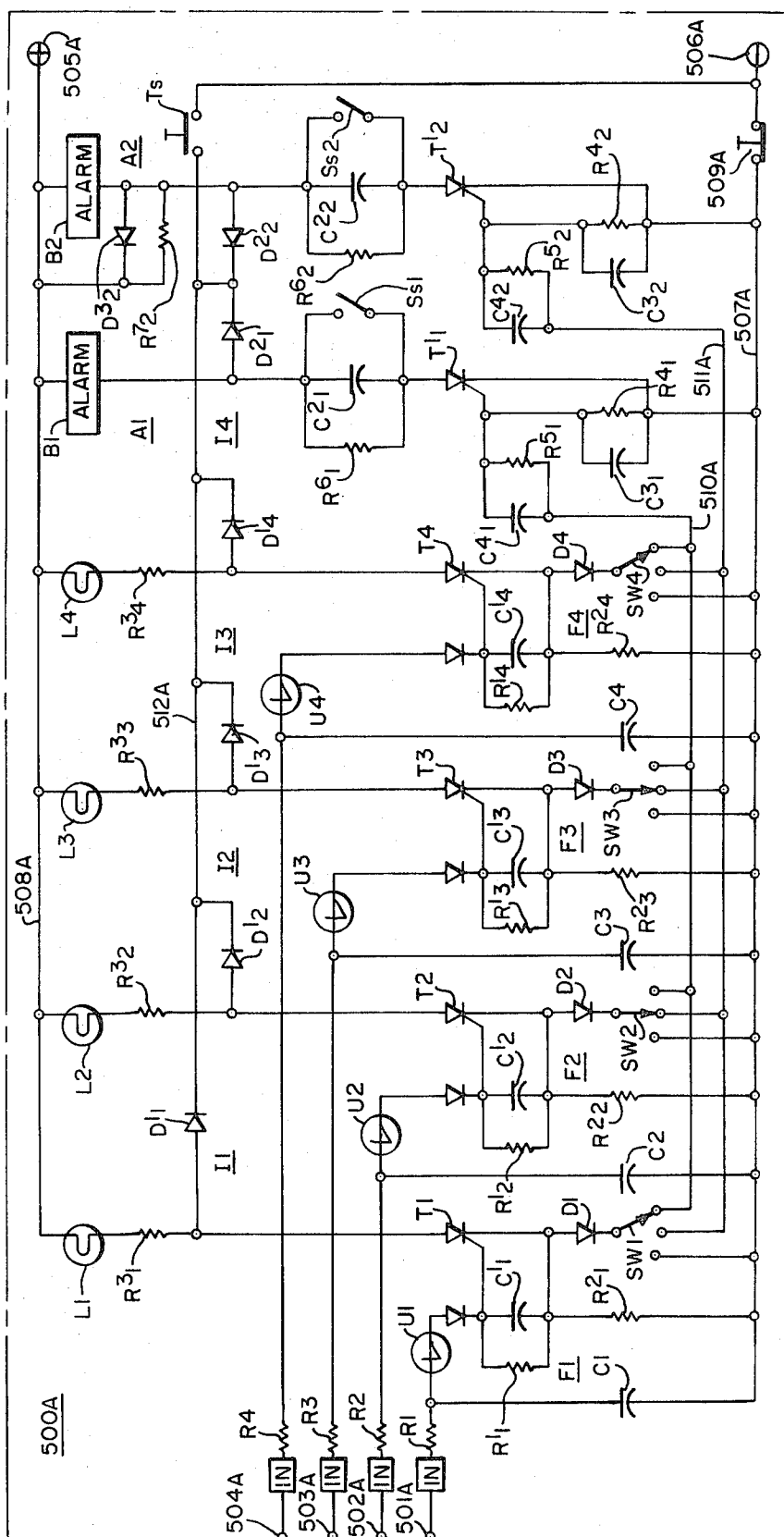


FIG. 2

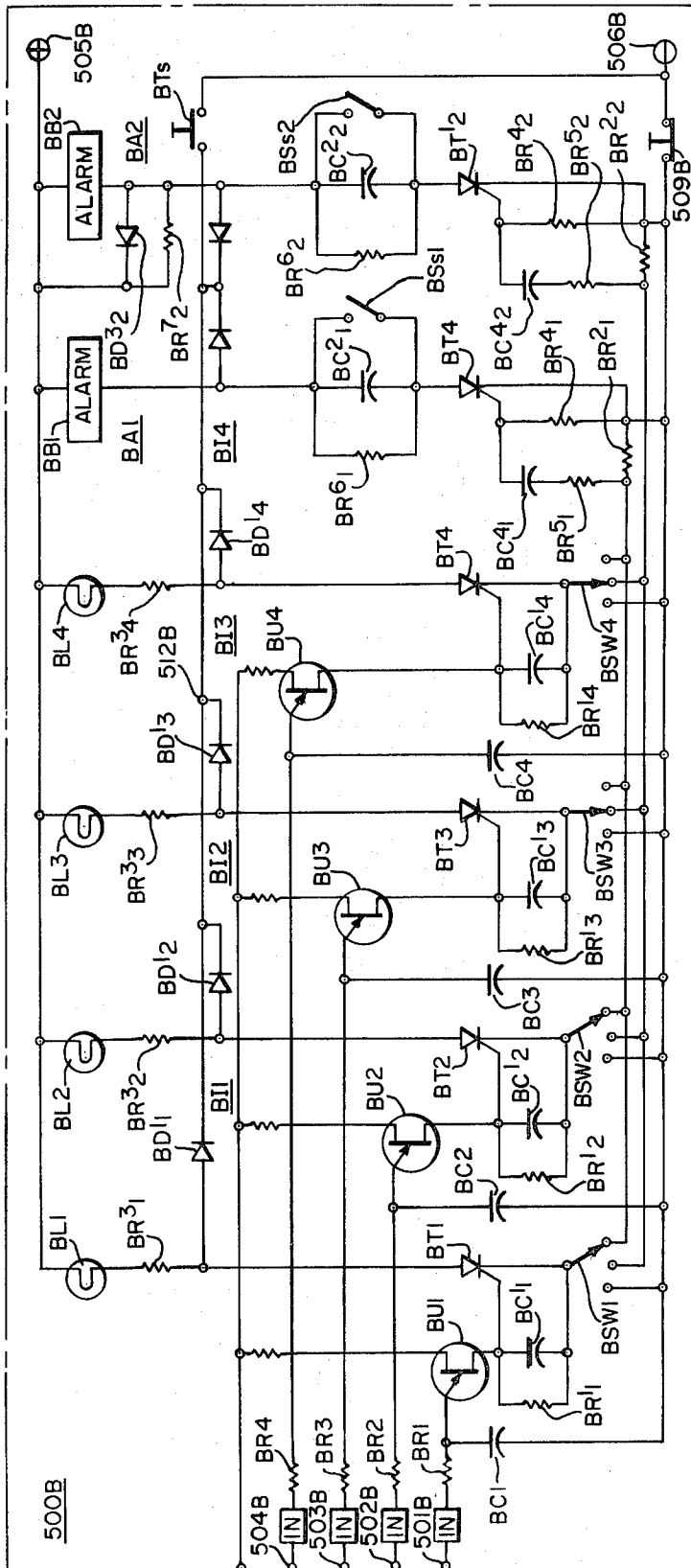


FIG. 5

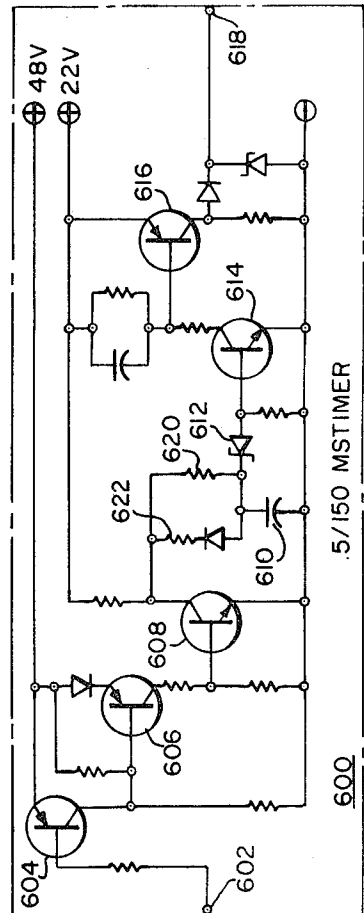


FIG. 4

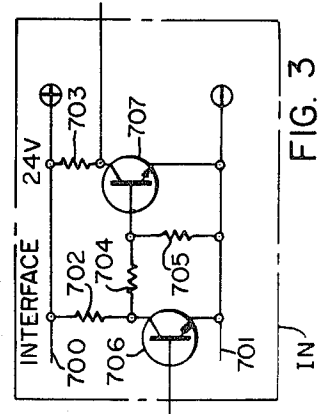


FIG. 3

PROTECTIVE RELAY USING AN INDICATOR AND ALARM CIRCUIT

CROSS REFERENCES TO RELATED APPLICATIONS

This invention is illustrated as being applied to the protective relaying system shown in copending application of George D. Rockefeller, Ser. No. 837,242, filed Jan. 27, 1969, now U.S. Pat. No. 3,590,324 dated June 29, 1971, for Phase Comparison Relaying Network and assigned to the same assignee as is this application.

SUMMARY OF THE INVENTION

This invention provides a protective relaying network for a transmission line including an alarm and indicator. The indicator is actuated in response to the occurrence of selected faults and remains in its indicated or actuated position until reset. The alarm provides a warning whenever the selected fault occurs and provides its warning independently of any actuation of the indicator. The alarm warning will exist solely for a predetermined interval even though the fault continues. The alarm is actuated each occurrence of the selected faults.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows, in block form, one terminal of a protective relaying network embodying the invention;

FIG. 2 is a schematic diagram showing the circuitry of the alarm and indicator network;

FIG. 3 is a schematic diagram showing an interface network for use in the networks of FIGS. 2 and 5;

FIG. 4 is a schematic diagram of the timer useful in the network of FIG. 1; and,

FIG. 5 is a schematic view of a modified form of circuitry for the alarm and indicator network.

This invention, as illustrated in FIG. 1, is embodied in a phase comparison relaying device similar to that set forth in the copending application of George D. Rockefeller, Jr., Ser. No. 837,242, filed June 27, 1969, now U.S. Pat. No. 3,590,324 dated June 29, 1971, entitled "Phase Comparison Relaying Network" and assigned to the same assignee as is this application. The said Rockefeller application is similar to Rockefeller U.S. Pat. No. 3,312,866 dated Apr. 4, 1967. Insofar as possible, the same reference characters as were used in the Rockefeller application are used herein. The details of much of the circuitry suitable for use in the blocks illustrated in this application, are the same as illustrated in the Rockefeller application and Rockefeller patent and since the details form no part of this invention, such details and much description found in the Rockefeller application and patent will not be repeated in this application but are embodied herein by reference.

Referring to the drawings by character of reference, the number 1 illustrates generally a protected section of a three-phase power transmission network having a first or local end connected by a local breaker 2 to local power busses 3 and a second or remote end connected by a remote breaker to remote power busses. The local breaker 2 is controlled by a local apparatus or device 4. The remote breaker is controlled by a similar remote apparatus. The apparatus 4 and the similar remote apparatus cooperate together to provide fault protection for the transmission line section 1.

The fault detectors P and O and the sequence filter 6A of the local relaying device 4 are actuated by current and/or voltage signals derived from the line section 1 by means of current and voltage transformer arrays 8 and 13. The sequence filter at its output terminal 17 provides a single phase alternating potential output quantity which is a quantity representing the weighted values of the positive, negative and zero sequence quantities of the current in the line section 1. This single phase alternating potential quantity after being filtered by the filter 10F is utilized to control the transmitter 24F to transmit "mark" and "space" signals to a receiver, in a remote apparatus similar to the apparatus 4 in response to the alternating potential of this single phase output quantity. The filtered quantity after being phase shifted by the phase shift network 12F is squared by squaring amplifiers 14FA and 14FB and supplied to the input terminals 454 and 456 of the AND networks 448 and 450 for comparison with the quantities supplied by the discriminator network 431 to the input terminals 455 and 457 as determined by the "mark" and "space" signals received by the local receiver 30F from the transmitter of the remote apparatus over the power line conductor 5. The signals from the remote transmitter are prevented from passing through the breaker 2 to the busses 3 by a network 28, which is tuned to pass power at the power frequency (which in the United States is usually 60 Hertz) but will not pass the "mark" and "space" signals of the local or of the remote transmitter.

The local sequence filter 6A and the similar remote sequence filter continually drive the respective transmitters whereby "mark" and "space" signals are always supplied to the opposite receivers. The discriminator 431 is arranged to provide a negative or ground output signal to the input terminal 455 and a positive output signal to the input terminal 457 when a "space" signal is being received by the receiver 30F. When a "mark" signal is being received the polarity of the output of the discriminator is reversed. In the absence of the reception of a signal by the receiver 30F, the discriminator 431 is arranged to provide continually the negative or ground output signal to both of the terminals 455 or 457. This will disable the "phase comparison" function but will not prevent the tripping of the breaker 2 in case of a fault.

The fault sensor P is illustrated as being a distance relay which may be of any desired type such as illustrated in the said Rockefeller patent. The fault sensor O is illustrated as being an overcurrent relay. The overcurrent relay O is, preferably, a fast-acting device set to operate at high values of line current indicative of a close-in fault. This current magnitude is substantially above the rated full load current of the transmission line 1. The sequence filter in addition to providing a single phase alternating potential quantity as above noted also provides a rectified quantity at its output terminal 15.

Under normal operating conditions of the transmission line 1, the receiver 30F will phase the discriminator 431 output with respect to the outputs of the squaring amplifiers 14FA and 14FB such that a positive signal always will be present at one or the other of the input terminals of each of the AND networks 448 and 450. With this sequence, the AND networks 448 and 450 will each supply a negative or a zero potential signal to the OR network 452.

If fault current flows in the line section 1, caused by an internal fault, the "mark" and "space" signals received by the receiver 30F will reverse their relationship with respect to the output signals of the squaring amplifiers 14FA and 14FB. This causes the negative or ground potential signals from the discriminator 431 to occur simultaneously at both input terminals of at least one of the AND networks 448 and 450. When this condition exists, the OR network 452 is actuated to initiate operation of the delay network 38 and the desensitizer 46. The actuation of the desensitizer 46 causes it to transfer control of the flip-flop 42 to the delay network 38. At the end of a 4 ms. delay time, the network 38 causes the flip-flop 42 to actuate the amplifier 44 to provide a signal to the trip relay 50.

Before the trip relay 50 can be actuated by the amplifier 44 it must previously have been "set" by an output signal from one of the fault detector 18 or relay 300. The fault detector 18 is actuated when the direct current output signal supplied thereto from the output 15 of the sequence filter 6A indicates the current to be of at least a predetermined minimum magnitude. For this purpose, the sequence filter 6A is constructed such that the DC potential supplied thereby is dependent upon the magnitude of the current derived from the current transformer array 8. When the magnitude of the current is above the predetermined minimum and indicates a fault current condition, the fault detector 18 provides the preliminary "setting" signal whereby the amplifier 44 will energize the trip relay 50.

In the case of an external fault (fault beyond the line section 1), the direction of the fault current at the remote and local terminals is such that the "space" and "mark" signals received by the receiver are arranged with respect to the signals supplied by the amplifiers 14FA and 14FB so that neither the AND network 448 nor the AND network 450 will actuate the OR network 452. Therefore, irrespective of the "setting" operation of the networks 18 and 300, the flip-flop 42 will not be actuated and trip relay 50 will not be energized to trip the breaker 2.

The networks 18 and 300 operate in response to either internal or external faults to initiate the timing out of the delay network 48. At the end of the timing interval of the network 48, (which is greater than the timing interval of the network 38) the desensitizer 46 is supplied with a signal to again desensitize the flip-flop 42 and place it in a condition such that it will not falsely actuate the breaker 2 in response to spurious signals.

If an interval fault should occur after the timing out of the delay network 48, the OR network 452 will initiate a timing interval of the time delay network 40. At the end of its delay interval, the network 40 will reset the delay network 48, whereupon the desensitizer 46 will sensitize the flip-flop 42 for flipping in response to the output signal of the delay network 38. The timing interval of the delay network 40 is longer than any expected transient or other spurious signal which the flip-flop 42 should not respond.

In the event of the occurrence of a close in fault, the magnitude of the fault current would be substantially greater than any load current and the overcurrent relay O will actuate the trip coil 52 independently of the phase comparison action as above described.

In order that the operating personnel may be aware of a malfunction in either the protective relaying net-

work itself or in the protected line section, there is provided an alarm and indicator 500, shown in box form in FIG. 1 and in schematic forms in FIGS. 2 and 4. Prior art protecting networks have been provided with means to indicate either by sound or light the fact that a malfunction has occurred. But such prior art means after having once been actuated remained actuated until externally reset. As such, the prior art means was ineffective to indicate a sequence of the same malfunction although it might indicate separately different kinds of malfunction.

Unlike the prior art, the alarm and indicator 500 will provide and maintain a first signal (illumination of a lamp) in response to the initial occurrence of a first selected malfunction and will provide a second signal (sounding of a sound-producing device) solely for a predetermined time interval irrespective of the continuance or discontinuance of the said first selected malfunction. Should the said first selected malfunction cease and thereafter reoccur, the second signal will again occur for the said predetermined time interval. Each signal can occur independently of the other. The present alarm and indicator 500 contemplates that a plural number of selected malfunctions may utilize a single said second signal (sound alarm). The species of alarm and indicator 500 (as shown in FIG. 1), 500A (shown in FIG. 2) and 500B (shown in FIG. 4) each are shown as responding to four different selected malfunctions. It should be clearly understood, however, that the particular number is not critical and may be increased or decreased as desired.

The alarm and indicator 500A is provided with four signal input terminals 501A, 502A, 503A and 504A and power input terminals 505A and 506A. Each of the signal input terminals is individually connected through an interface network IN through a timing circuit to the negative polarity potential bus 507A. The timing circuit comprises in series a resistor R and a capacitor C.

The interface network IN is shown in detail in FIG. 3. It comprises a positive bus 700, a negative bus 701, a plurality of resistors 702, 703, 704, 705 and a pair of transistors 706 and 707. The emitter of each of the transistors 706 and 707 is directly connected to the negative bus 701. The collector of the transistor 707 is connected to the 24 volt bus 700 through the resistor 703. The transistor 707 is normally maintained conducting by base current which flows from the bus 700 through resistors 702 and 704. A resistor 705 is connected between the base and emitter of the transistor 707.

When a positive signal is supplied to the base of the transistor 706, it conducts and causes the transistor 707 to become non-conductive whereby the collector thereof rises in potential from substantially that of the negative bus 701 to substantially that of the positive bus 700 to energize the firing circuit F with which it is associated. The firing circuits F for the indicator circuits I are connected individually in shunt with each capacitor C. These circuits F each includes a silicon unilateral switch U series connected with first and second resistors R¹ and R². A capacitor C¹ is connected in shunt with the resistor R¹.

Each of the indicator circuits I is connected between the negative and positive potential busses 507A and 508A and includes a suitable switch such as the anode-

cathode circuit of a thyristor T and the resistor R² and a current limiting resistor R₃. The gate and cathode of the thyristor T are connected across the parallelly connected resistor R¹ and capacitor C¹ combination whereby the thyristor T is rendered conducting, to illuminate the lamp L, as a consequence of the capacitor C charging to the critical breakover potential of the unilateral switch U. The resistor R³ limits the current through the lamp L to a value which will give satisfactory lamp life, but which current value is still sufficient to maintain the thyristor T conducting. Therefore, when the lamp L once becomes energized, it will stay illuminated until manually reset by opening the reset switch 509A.

As illustrated, the alarm and indicator 500A includes two alarm circuits A. Each alarm circuit is connected between the busses 507A and 508A and each includes a suitable audible alarm such as a bell B. The alarm circuit includes in series connection the bell B, a capacitor C² and a suitable switch such as the anode cathode circuit of a thyristor T¹. The thyristor T¹ is rendered conductive by energizing a firing circuit connected between its gate and cathode and including a resistor R⁴ shunted by a capacitor C³. The firing circuit for thyristor T¹, is connected between a bus 510A and the bus 507A and includes a resistor R⁵1 shunted by a capacitor C⁴1. Similarly the firing circuit for the thyristor T² is connected between a bus 511A and the bus 507A and includes a resistor R⁵2 shunted by a capacitor C⁴2. The resistor R⁵ serves as a discharge path for the capacitor C⁴ while the capacitor C³ acts to prevent false operation of the thyristor T¹ by spurious signals.

To permit flexibility in the interconnecting of the indicator circuits I with the alarm circuits A, the cathode end of the resistor R² of each of the indicating circuits is individually connected by means of a single pole triple throw switch SW to the busses 507A, 510A and 511A. A diode rectifier D is provided in series with each switch to prevent current flow from any of the busses 507A, 510A and 511A to any of the indicating circuits I.

In the event the bell B is sufficiently inductive to cause faulty operation of the alarm circuit A a suitable network may be connected in parallel with the bell B and in series with the thyristor T¹. Such a network is illustrated in connection with the alarm circuit A2 and includes in parallel connection with the bell B2 a diode D³2 and a resistor R⁷2. The diode D³2 will suppress the inductive transient voltages which may be generated by the alarm B2. The resistor R⁷2 provides starting current for the thyristor T¹2 in the event the inductance of the alarm B² prevents a rapid enough build up of the current during the interim that the gate of the thyristor T¹2 is energized. It will be appreciated that a similar network may be used in connection with the alarm circuit A1 if desired.

In the event that a continued energization of the bell B is desired the capacitors C² may be shunted by closure of the switch Ss.

The common connection of the resistor R³ and thyristor T of each indicator circuit I is connected through a diode rectifier D¹ to a test bus 512A which is connected to the negative terminal 506A through a test switch Ts. Similarly the common connection of the

alarm A and resistor R⁸ capacitor C² network of each alarm circuit A is connected to the test bus 512A through an individual diode D².

While the values of the circuit elements may vary widely depending upon the magnitudes of the potential supplied thereto suitable illustrative values for the circuit elements when an energizing potential of 24 volts is used are as follows:

Elements	Value
All R resistors	10K Ohms
All R ¹ and R ² resistors	27 Ohms
All R ³ resistors	1.2K Ohms
All R ⁴ resistors	1K Ohms
All R ⁵ resistors	100K Ohms
All R ⁶ resistors	150K Ohms
All C capacitors	0.082 Mfd
All C ¹ capacitors	0.01 Mfd
All C ² capacitors	25 Mfd
All C ³ capacitors	0.01 Mfd
All C ⁴ capacitors	0.56 Mfd
All Unilateral Switches	Style 2N4990
All Thyristors	Style K1149-13

One of the malfunctions which should be sensed is the "loss of signal" condition in which the local receiver 30F fails to receive "space" and "mark" signals from the remote transmitter whereby the discriminator 431 fails to periodically render the terminal 455 positive. When this occurs, the periodic resetting signal for the timer 600 is absent and the negative or ground signal is not periodic. Under this condition the timer will time out and provide a positive signal to the alarm and indicator terminal 501 to which it is connected. The timer is preferably adjusted to provide for energizing its output terminal 604 after the negative signal has existed for 150 milliseconds, a time greater than the time of a full period of the power in line section 1. The timer 600 preferably has a short resetting period which may be as low as 0.5 milliseconds so that it will not time out and will not energize terminal 604 during normal operation of the receiver 30F.

When a "mark" signal is being received, terminal 602 (FIG. 3) is positive and transistor 604 is prevented from conducting, transistors 606 and 608 conduct and capacitor 610 discharges or remains discharged depending upon the prior history of the transistor 608. With the charge in capacitor 610 below the breakover potential of the Zener diode 612, the transistors 614 and 616 remain non-conducting and the potential of the output terminal 618 is at negative or ground potential. When a "space" signal is being received, terminal 602 is negative and transistor 604 conducts. Transistors 606 and 608 become non-conducting and the capacitor 610 commences to charge through resistor 620. The time required to charge the capacitor 610 to the critical potential of the diode 612 is shown as being 150 ms. This time interval is greater than the time period of any normal "space" signal so that the transistors 614 and 616 will remain non-conducting for the duration of the normal "space" signal. During the ensuing "mark" signal, transistor 604 will block and transistors 606 and 608 will conduct. Capacitor 610 will discharge through resistor 622 in a time interval of 0.5 ms. which is considerably less than one-half a period of the power in line section 1. Therefore, during normal operation the

charge in the capacitor 610 cannot reach the critical potential necessary for the breakover of the Zener diode 612 and as long as "space" and "mark" signals are being provided, the output terminal 618 will remain at negative or ground potential.

In the event of the "loss of signal," the receiver 30F fails to receive the normal "mark" and "space" signals, the discriminator 431 causes the terminal 602 to remain at negative or ground potential with the result that transistors 606 and 608 remain non-conducting, capacitor 610 continues to charge until the critical potential required to break over the Zener diode 612 is reached, and transistors 614 and 616 conduct. The conduction of transistor 616 establishes a positive potential at the output terminal 618 and at the input terminal 501 of the network 500. It will now be appreciated that the specifics of the timer 600 as illustrated are not required for the operation of the invention. Other timers which will differentiate between a continuous signal and a pulsating signal representative of a malfunction and a normal function respectively may be utilized.

To illustrate the invention the indicator and alarm network 500 is shown as responding to the operation of the trip relay 50 by the phase comparison fault detecting operation (input terminal 502), to the operation of one or both of the fault detector 18 and relay 300, and to the energization of the trip coil 52 by the overcurrent fault detector O. As suggested herein other fault conditions could be used if desired.

Upon the occurrence of a first to occur of the selected malfunctions, one of the input terminals 501, 503, 503 and 504 eventually will be energized with a positive potential. The first malfunction to occur will be assumed to be that which energizes terminal 502A (FIG. 2) whereby the capacitor C² charges through its associated resistor R². At the end of this time period the capacitor C² will reach its critical charge and the silicon unilateral switch U² will conduct. The silicon unilateral switch U² when conducting provides a low impedance and the capacitor C² dumps its charge through the resistors R¹² and R²². The potential established across the resistor R¹² causes the thyristor T² to conduct and the Lamp L² will light up. The current flow through lamp L² is sufficient to maintain the thyristor T² conducting and the lamp L² will remain lighted and maintain an indication of the specific selected malfunction which occurred until reset by opening the switch 509A.

The potential established across the resistor R²² by the discharge current of the capacitor C² causes charging current to flow through the capacitor C⁴² and the resistor R⁴². The resulting energization of the network R⁴² provides a gate signal to the thyristor T¹² which thereupon conducts and the alarm A² becomes energized. The energization of the gate of the thyristor T¹² is short and is limited in duration by the dumping time of the capacitor C². When conductive, the voltage drop across the switch U² is less than 2 volts and that across the diode in series therewith is less than 1 volt. When the magnitudes of the resistors R¹ and R² each being low (27 ohms each) with respect to that of the resistor R (10,000 ohms) and disregarding the resistor 703 (which would still further reduce the current to the firing circuit, the current passed through the resistors R¹ and R² will not be greater than 2.5 milliamperes

whereby the voltage supplied to the thyristor T¹ is less than 65 millivolts which is considerably less than that required to turn on the thyristor T¹ even if the voltage drop across the diode D were ignored.

Current flow through the alarm B² charges the capacitor C²² until the charging current is reduced to an amount less than the holding current of the thyristor T¹² which thereupon terminates its conduction and the actuation of the alarm B² is terminated. The resistance of the resistor R²² is of sufficient magnitude whereby the current flow therethrough is below the maintaining current for the thyristor T¹² but it does serve to discharge the capacitor C²².

Should the said first malfunction terminate and the signal be removed from terminal 502A, the switch U² will reestablish an open circuit thereacross. If thereafter the said first malfunction reoccurred, the capacitor C² would recharge, the switch U² would reconduct to dump the charge in capacitor C² through the resistor R²² and charging current would again flow to the capacitor C⁴² and refire the thyristor T¹² to resound the alarm A².

Should the said first malfunction continue and a second of the selected malfunctions occur, as for example the malfunction which energizes U³ will conduct and capacitor C³ will dump through resistors R¹³ and R²³. The potential across resistor R¹³ causes the thyristor T³ to fire and energize lamp L³. The potential across R²³ due to the dumping of the capacitor C³ is higher than the existing potential across the resistor R²² and charging current will flow to capacitor C⁴² and refire thyristor T¹² to resound the alarm A². The diodes D prevent current flow from the bus 511A through any of the resistors R² and in this case the rise in potential in the bus 511A from raising the potential of the cathode of the conducting thyristor T² which might terminate the flow of lamp current therethrough thereby permitting the lamp L² to remain energized.

FIG. 4 illustrates another form of alarm and indicator 500B in which similar or equivalent parts to the four shown in FIG. 2 and designed by the same reference characters except for the suffix B instead of A in the case of numeral designations and the addition of a prefix B in the case of letter designations. The major difference between the network 500B and network 500A is the use of a unijunction transistor BU for the silicon unilateral switch U and the elimination of the diodes D and the use of the resistors BR² in place of the resistors R². In the network 500B the capacitors BC² are in series with the resistors BR⁴ as distinguished from the parallel arrangement of the capacitors C² with the resistors R⁴ in the network 500A. Capacitors C³ are omitted in the network 500B.

The network 500B operates in much the same manner as does the network 500A except that the impedance of the conducting unijunction transistors BU will not become as low as that of the unilateral switch U of FIG. 2.

What is claimed and is desired to be secured by United States Letters Patent is as follows:

1. An indicator and alarm control apparatus comprising a pair of input terminals adapted to be energized by an actuating signal, a signal indicating device, a signal alarm device, an indicating network including said indicating device, an alarm network including said

alarm, said indicating network including a pair of control terminals effective when in a first energized condition to render said indicating network effective to energize said indicating device and further indicating means maintaining said indicating device energized until it is deenergized by a reset device irrespective of the energization of the control terminals of said indicating network, said alarm network including a pair of control terminals and being effective on a consequence of the initial flowing of said contact terminals in a first energized condition to render said alarm network effective to energize said alarm device, said alarm network further including automatic control means effective to deenergize said alarm after said control terminals of said alarm network have been maintained in their said first energized condition for a predetermined time interval, said control means further being effective to maintain said alarm deenergized at least until the termination of said energized condition of said control terminals of said alarm network and means connecting said control terminals of each said network to said input terminals for placement of said contact terminals in their said first condition as a consequence of the energization of the input terminals with said actuation signal.

2. The combination of claim 1 in which there is provided a time delay apparatus, said time delay apparatus being connected intermediate said input terminals and said contact terminals of at least one of said networks, said control means of said alarm network being effective to maintain said alarm device energized for a time interval irrespective of the termination of said first energized condition of said contact terminals of said alarm network.

3. An indicator and an alarm control apparatus comprising a plurality of energizable networks, each said network including a control circuit connected to a pair of signal terminals, and a main circuit, each said control circuit including a switch which is rendered in a first state as a consequence of the applications of a start signal to the said signal terminals associated with its respective said control circuit to actuate the said main circuit which is associated therewith, each said switch being effective to maintain the said main circuit controlled thereby in its actuated condition irrespective of the continued application of said first signal to its said pair of start terminals, a first pair of input terminals adapted to be energized by an actuating signal, means connecting said signal terminals of a first and a second of said networks to said first pair of input terminals and effective upon the application of said actuating signal to said pair of input terminals to supply said start signals to said signal terminals of said first and second networks, said control circuit of said second network including means automatically terminating the application of said start signal to the said switch of said second network, said main circuit of said second network including means interrupting the actuation thereof independently of the operation of said switch associated therewith.

4. The combination of claim 3 in which said means for terminating said start signal includes a capacitor, connected in series in said control circuit of said second network intermediate its respective said signal terminals and its respective said switch, and there is an

impedance connected between said signal terminals of said second network.

5. The combination of claim 4 in which said means for interrupting the actuation of said main circuit of said second network includes a capacitor connected in series with said switch of said second network.

6. The combination of claim 3 in which there is provided a second pair of input terminals, said signal terminals of a third of said networks and of said second network being connected to said second pair of input terminals, first and second pulse producing circuits, means connecting said signal terminals of said second network to said first and second pairs of input terminals individually through said first and second pulse producing circuits respectively, each said pulse producing circuit being effective to produce a single pulse for each continued energization of the said pair of input terminals to which it is connected.

7. A protective relaying apparatus for an electrical transmission line comprising a plurality of operating circuits, each said circuit having a normal and an actuated operating condition, an alarm and indicator network, said network comprising a plurality of annunciator circuits, and at least one warning circuit, said warning circuits each having a set and a warning operation condition, each of said annunciator circuits having a first and a second operating condition, means individually connecting said plurality of operating circuits with said plurality of annunciator circuits for individual energization of said annunciator circuits from their said first to their said second conditions as a consequence of the change in the operating condition of the associated said operating circuits from its said normal condition to its said actuated condition, means connecting said warning circuit to at least one of said operating circuits for actuation of said warning circuit from its said set condition to its said warning condition each time said one operating circuit changes its state from its said normal condition to its said actuated condition, said network including timing means and a resetting means, said timing means being effective to return said warning circuit to its said set condition at the expiration of its timing interval, said network including means for maintaining each said annunciator circuit in its said second condition until reset by said resetting means.

8. The combination of claim 7 in which a first of said operating circuits includes first fault detecting apparatus and a second of said operating circuits includes a signal detecting apparatus, said signal detecting apparatus providing a first output when no signal is being received thereby, and said fault detecting apparatus providing a first output in response to the actuation thereby of a fault, said first operating circuit being changed from its said normal to its said actuated condition in response to the actuation thereof by said first output of said fault detecting apparatus and said second operating circuit being changed from its said normal to its said actuated condition in response to the actuation thereby of said first output of said signal detecting apparatus whereby said annunciator circuits will provide a continued indication of which undesired operation has occurred and said warning circuit will warn of each occurrence thereof.

9. The combination of claim 8 in which each of said individual connecting means includes an actuator having first and second portions connected for movement energization by each occurrence of the said first output from the associated said detecting apparatus and in which the associated said annunciator is actuated to its said second operating condition of the energization of said first portion of the associated said actuator and the associated said warning circuit is actuated to its said warning condition by the energization of said second portion of the associated said actuator.

10. The combination of claim 9 in which each of said individual connecting means includes a timing device whereby the associated said actuator is energized solely subsequent to a determined time period after the associated said operating circuit is placed in its said second operation condition.

11. The combination of claim 10 in which each of said timing devices comprise a resistor and a capacitor in series connection, each of said operating circuits when in its said second operating condition providing a potential output across said timing device of the respective said individual connecting means, each said actuator including a breakover device operable to provide a high impedance to current flow when the potential thereacross is below a critical value and to break over and conduct at a lower impedance when the potential thereacross reaches its said critical value, said first and second portions of each said actuator comprising first and second impedance elements, said first and second portions and said breakover device of each said actuator being connected in series with each other and in shunt with said capacitor of the associated said timing device, each of said annunciator circuits comprising an illuminable device and a first switch connected to the said first impedance element of the associated said actuator to energize its associated said illuminable device as a consequence of the energization of said associated said first impedance element, each of said first switches being of the type which is ineffective to interrupt circuit flow therethrough, said warning circuit comprising an audible device and an energization controlling means therefor, means connecting said energization controlling means to at least two of said second impedance elements, said energization controlling means being effective upon the energization of either of said two of said second impedance elements to actuate said audible device solely for a determined time irrespective of the continued energization of the said second impedance element which causes said energizing controlling means to actuate said audible device.

12. The combination of claim 11 in which said connecting means comprises a device and first and said energy level controlling devices, said second switch and said first storage device being connected in series circuit with said audible device whereby the change in energy storage in said first storage device from a first to a second energy level caused by the operation of said second switch actuates said audible device, means connecting said first energy level controlling device to said first storage device for changing the energy level thereof from said second to said first level, said means which connects said energizing controlling means to said two impedances including said second storage device, said second storage device being effective to

maintain said second switch operated for a determined interval as a consequence of a change in the energy level thereof from a first level to a second level, and means connecting said second energy level controlling device to said second storage device for changing the energy level thereof from its said second to its said first level.

13. The combination of claim 12 in which said first and second impedance elements are all resistors of the same resistance magnitude, said energization devices are capacitors, said energy level controlling devices are resistors, said resistors of each said actuator being connected in series with said resistor of its associated said timing device, the magnitude of the resistance of said resistor of each said timing network being so related to the magnitude of the potential supplied to such timing network from the associated said operating network in its said actuated condition, that the current flow therethrough is insufficient to maintain the associated second said impedance element effective to render its associated said second switch operated.

14. An alarm and indicator network comprising a pair of input terminals, a first timing resistor, a first timing capacitor, means connecting said resistor and capacitor in a first series circuit between said input terminals, said first series circuit being effective upon energization of said input terminal for not less than a minimum time interval to alter the changed condition of said capacitor to prevent a first potential thereacross, a first voltage sensitive switch, first indicator control resistor and a first alarm control resistor, means connecting said switch and said first control resistors in a second series circuit means connecting said second series circuit in shunt with said capacitor, said voltage sensitive switch being effective to conduct when the potential across said capacitor reaches said first potential, a first indicator controlling switch and a first alarm controlling switch, each of said indicator and said alarm switches having a main circuit and a contact circuit, said first switch being of the type that when one is transferred from its said first to its said second condition will not return to its said first condition, means connecting said control circuit of said first indicator switch to said control resistor, whereby a predetermined energization of said indicator control resistor will transfer said first indicator switch from its said first to its said second condition, a first indicator means connecting said indicator to said first indicator switch for actuation when said first indicator switch is in its said second condition, means for transferring said first indicator switch from its said second to its said first condition, an alarm network, said alarm network comprising an alarm and means including said first alarm switch for initiating the energization of said alarm, means connecting said alarm initiating means to said alarm control resistor whereby a predetermined energization of said alarm control resistor will transfer said first alarm switch from its said first to its said second condition, said alarm network being effective to energize said alarm when said alarm switch is transferred to its said second condition, and alarm interrupting means rendering said alarm network ineffective to maintain said alarm energized ineffective of the continued energization of said pair of input terminals.

15. The combination of claim 14 in which a first signal voltage source is selectably connected to said input terminals, the magnitude of said source voltage being relative to the magnitude of the resistance of said first timing resistor and of said alarm control resistor so as to reduce the energization of said alarm control resistor to a value below its said predetermined energization.

16. The combination of claim 15 in which said alarm switch is of the type that when once transferred to its said second condition will not return to its said first condition, and alarm interrupting means being effective to return said alarm switch to its said first condition at the expiration of a desired time interval.

17. The combination of claim 16 in which said second condition of said alarm switch is a current conducting condition said alarm network connects said alarm in series with said alarm switch, and said alarm interrupting means comprises a capacitor connected in series with said alarm, and discharge means associated with said last-named capacitor, said discharge means being effective to discharge said last-named capacitor when said alarm switch is in its said first operating condition.

18. The combination of claim 17 in which there is provided a second indicating means and a second indicator controlling switch and a second indicator and a second pair of input terminals and a second timing resistor and a second timing capacitor and a second indicator control resistor and a second alarm control resistor and a second voltage sensitive switch and a second signal voltage source, means connecting said second timing resistor and said second timing capacitor

in a third series circuit between said second pair of input terminals, means selectively connecting said second signal voltage means to said second pair of input terminals, means connecting said second control resistors and said second voltage sensitive switch in a fourth series circuit, means connecting said fourth series circuit in shunt with said second timing capacitor, means connecting said second indicator switch to said second indicator control resistor whereby a predetermined energization of said indicator control resistor will transfer said second indicator switch from its said first to its said second condition, a second indicator, means connecting said second indicator to said second indicator switch for actuation when said second indicator switch is in its said second condition, means connecting said alarm initiating means to said second alarm control resistor whereby a predetermined energization of said alarm control resistor will transfer said alarm switch from its said first to its said second condition, the magnitude of said second source voltage being related to the magnitude of the resistance of said second timing resistor and of said second alarm control resistor so as to reduce the energization of said second alarm control resistor to a value below its said predetermined energization, first and second asymmetric current flow devices, said first asymmetric device being connected in said means which connects said alarm initiating means to said first alarm control resistor, said second asymmetric device being connected in said means which connects said alarm initiating means to said second alarm control resistor.

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