(54) Title: A DIAGNOSTIC CIRCUIT FOR DIGITAL SYSTEMS
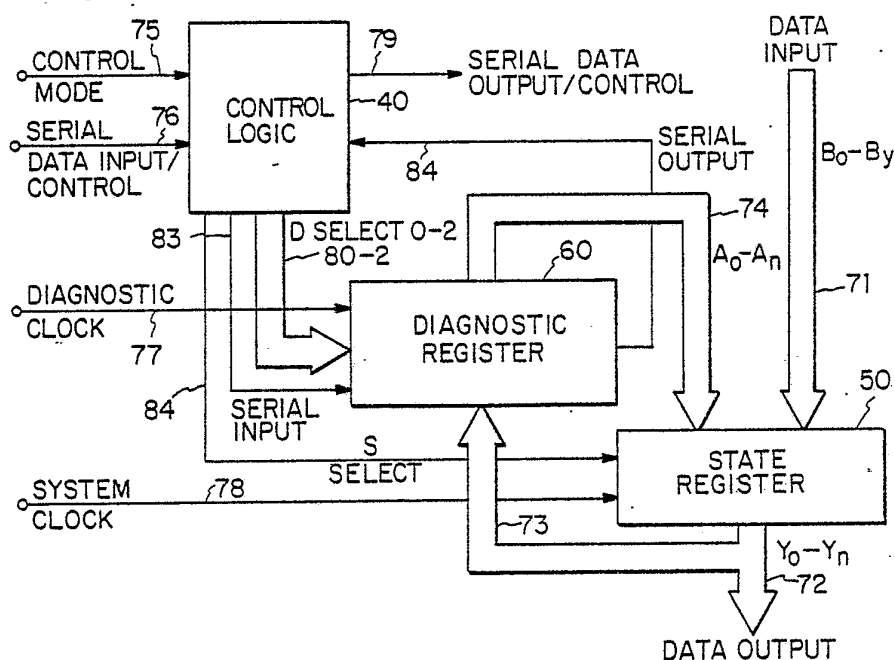
(57) Abstract

An improved circuit for serial scan diagnosis. A state register (50) in the signal path of the digital system under diagnosis is coupled to a diagnostic shift register (60). Test data is introduced and removed through the diagnostic shift register (60) through a serial input terminal (83) and serial output terminal (84). For certain operations the serial input terminal becomes a control terminal whereby a minimum number of control lines is required.

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A DIAGNOSTIC CIRCUIT FOR DIGITAL SYSTEMS

BACKGROUND OF THE INVENTION

Field of Invention

This invention relates to electrical circuits useful in diagnosing
faults in digital systems, and more particularly, for diagnosing faults by
serial scan techniques.

Description of the Prior Art

A digital system may often be generalized into a system of
logic blocks. The logic blocks, which may consist of a large number of
logic gates performing complicated functions, operate on sets of parallel
data and control signals. The signals enter a particular logic block, are
transformed, and leave the logic block for the next logic block. The data
travel through the logic blocks of the system until they exist as the desired
output data of the system.

Signal paths for the electrical control and data signals connect
the logic blocks. Registers are usually located in these signal paths to
temporarily hold the digital signals from one logic block and to release the
data to the next logic block at the proper time. The data may also be
released as feedback to logic blocks "upstream". Registers permit the
proper coordination of the data movement through the system.

In these sytems the testing and diagnosing of faults becomes a
problem. If a failure occurs at some point within the system and only the
input and output ports of the system are available for testing, then the
isolation of the failure becomes very difficult. For example, any test input
data must pass through logic blocks 1 and 2 before the data can be used to
test the logic in block 3. Any failure in these earlier logic blocks cause the
data to be unusable for testing later logic blocks. Even if logic "upstream"
from the failure functions correctly, the test output data may be ruined by
an intervening failure. The fault with this type of system organization is
that hardware failures may be detected but not located.

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Isolation of faults is possible if intermediate test points are
available and various designs have been proposed. One technique which is
used to provide these intermediate test points is the serial scan technique.
A generalized digital system, as discussed previously, is shown in FIG. 1.
5   The system is modified so that serial scan diagnosis is possible. As in a
generalized system, the data and control signals move from logic block to
logic block along signal path 11. Shift registers 12, 16, 20 maintain the
timing of signal movement. However, the registers are modified so that
they can operate in two modes. In the normal mode the registers pass
10 signals in parallel from one logic block to another. In the diagnostic mode
the registers operate as serial shift registers by which test data may be
shifted into the register. Then the registers in normal mode release the
test data into the logic blocks to be operated upon. The test data is then
read out by the registers receiving the test output data for examination of
15 faults. For example, logic block 2 in FIG. 1 may be examined by the serial
introduction of test data into the register 12, passing the data through
logic block 2 and serially removing the test data by the register 16.

A variation of the serial scan technique has the serial output
line connected to the serial input line of a succeeding register. A string of
20 test data is scanned into the registers, which are then set to operate in
normal mode. After the logic blocks operate on the test data from the
registers, the test data is scanned out in a string to determine whether
faults exist in the different logic blocks. Other variations of the serial
scan technique are possible. All of these variations reduce the number of
25 test-fix iterations necessary to repair or debug a system for a
corresponding reduction in cost.

However, the simple serial scan register circuit of FIG. 1 has
problems, one of which may occur when the register is in the control path
of the system, such as a microinstruction register of a processor. In such a
30 register, certain data combinations at certain bit positions may be
forbidden. This forbidden conditions may be violated as the data
information is scanned in or out of the serial shift register.

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For example, a typical field in a microinstruction register could include a series of enable bits to enable buffers onto a bus. If serial test data is shifted through this microinstruction register, a condition could result which is illegal in normal execution (a restriction is put on the

5   control flow such that only one bit can be low, or enabled, at a time). This illegal combination results in overstressing the devices and could seriously damage the associated circuitry.

Other problems result in latched systems and asynchronous systems. In an asynchronous system, if one of the outputs, or a logical

10 combinations of outputs, of the shift register is used to generate a signal to an asynchronous (unclocked) subsystem, such as a memory or input/output device, an unwanted access to the subsystem maybe be generated when the register is shifted for test operations. This could result in an unpredictable disruption of the system state, making fault isolation much more difficult.

15 In a latched system, the register used as a microinstruction register and having its bit outputs, or logical combinations thereof, setting, resetting or opening latches in the system causes problems also. Test data shifted through the register may disturb the system state. This type of problem is especially serious when the latch contents cannot be

20 re-established, making additional testing virtually impossible.

The present invention solves or substantially mitigates these problems and is a substantial advancement over the simple serial scan register. A circuit is provided by which data may be serially introduced into and removed from a signal path for the testing of the integrity of the

25 digital system. The circuit has a minimum number of control lines to achieve a savings in economy, yet retains ample control functions for flexibility.

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SUMMARY OF THE INVENTION

The present invention provides for a circuit for a digital signal path comprising control means; first means connected in the signal path and responsive to the control means for selectively holding the signals of
5. the path; and second means connected to the first means and responsive to the control means for selectively holding signals from the first means and releasing signals to the first means, the second means having input-output means for selectively accepting digital signals for selectivley sending digital signals, whereby digital signals may be inserted into the signal path
10 and removed from the signal path through the input-output means.

The present invention also provides for a circuit for the selective introduction and removal of digital signals into and from a digital signal path comprising a multiplexer, a first signal storage means connected to the multiplexer for holding digital signals from the
15 multiplexer, a second signal storage means connected to the multiplexer and first signal storage means for selectively holding digital signals from the first signal storage means and for providing digital signals to the multiplexer, the multiplexer controllably selecting signals from the digital signal path and from the second signal storage means, the shift register
20 further connected to serial input-output terminal means for the selective introduction and removal of digital signals.

The circuit is further designed so that the controllable selection of the digital signals by the multiplexer and the selection of holding and providing digital signals or introduction and removal of digital signals by
25 said second signal storage means is by means of a control signal on a single control line. Furthermore, the input-output terminal means may be first and second terminals wherein the first terminal is selectively an input terminal or a control terminal responsive to control signals on the control line.

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BRIEF DESCRIPTION OF THE DRAWINGS

A further understanding of the present invention may be attained by a perusal of the following Detailed Description in the specification and by reference to the following drawings.

5   FIG. 1 illustrates a generalized digital system having prior art serial scan registers for diagnosing errors in the system.

FIG. 2A is an illustration of the architecture of the present invention; FIG. 2B is a table of functional states for the system shown in FIG. 2A.

10   FIG. 3 is an illustration of the architecture of a specific embodiment of the present invention.

FIG. 4A illustrates in detail the control logic block used in FIG. 3; FIG. 4B is a table of states for the control logic block illustrated in FIG. 4A.

15   FIG. 5 is a detailed illustration of the state register block found in FIG. 3.

FIG. 6 is a detailed illustration of the diagnostic register block shown in FIG. 3.

DETAILED DESCRIPTION

20   The present invention has two registers, one is a state register which holds the signals of the data signal path in a digital system and the other is a diagnostic register which may be connected to external test equipment for loading and unloading test data. The two registers are coupled together so that a minimum number of control lines are used for

25   the proper coordination of the two registers. The signal contents may be transferred from one register to the other, and in the opposite direction. Furthermore, the signals may be serially introduced into and removed out of the diagnostic register. These functions are achieved with one full time control line, two clock lines, and two serial input and output lines.

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The provision of a state register and a diagnostic register prevents the problems associated with the simple serial scan register. Of course, the present invention is not restricted to registers. Other forms of signal storage circuits may be used, such as latches.

5   FIG. 2A illustrates the present invention. A register 24 temporarily holds the digital signals on the signal path 11 between logic blocks shown in FIG.1. The digital signal path 21 is illustrated by an arrow as input signals. The present invention provides for a separate shift register 26 which can hold the contents of the state register 24 by loading

10   its contents in parallel as shown by a branch of the signal path 25. The contents of the shift register 26 may be reloaded back into the state register 24 along the path 27. A multiplexer 22 by the control signals on the control mode line 28 selects whether the signals of the path 21 or of the path 27 are selected.

15   The shift register 26 can also load signal information serially through a serial input line 31 and can unload information serially by a serial output line 32. Both registers are controlled by clocks, the state register 24 by a system clock through a line 33 and the shift register 26 by a diagnostic clock through a line 29. Both registers 24 and 26 operate on the

20   rising edge of the clock pulse signals.

FIG. 2B illustrates the functional operation of the circuit shown in FIG. 2A. When the control mode signal on line 28 is "low", the circuit is in a "shift" mode so that with a rising clock pulse from the diagnostic clock on the line 29, the diagnostic register 26 accepts signal data along line 31

25   and shifts out its content along line 32 one rising clock pulse at a time. Thus the serial input in the table of FIG. 2B is shown as "I" as input and the serial output is shown as "O" as output. This is operation number 1. With the control mode still "low" and with the rising clock pulse of the system clock, the state register 24 loads the data signals of the system as

30   indicated by the data path 21 and 23. The multiplexer 22 with the control mode signal "L", or low, selects the signals of path 21.

When the control mode signal goes high, the "load" mode, the serial input line 31 becomes a control line. In operation 2 the serial input line is low and the shift register 26 is loaded in parallel with the contents

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of the state register 24 along the data path 25 upon a rising clock signal
from the diagnostic clock. With the same control signals and a rising
system clock signal, operation number 5 occurs. The state register 24 is
loaded with data contents of the diagnostic register 26 via the data path
27. The multiplexer 22 selects the path 27.

It should be noted that FIG. 2B indicates the timing of a
particular operation by an upward pointing arrow, the rising pulse of clock
signal. The other clock is always indicated as "___". This indicates that
the other clock has a stable signal, during the rising pulse of the first clock
so as to keep the timing of the circuit clear and orderly. Operations
number 3 and 6 in which the control mode signal is "H", or high, and the
serial input line 31 is also high, are optional operations and are indicated as
such. For example, in the embodiment shown in FIG. 3, operation 6 is
specifically selected to be a "hold" operation by which no operation occurs.
Despite the limited number of control lines, the circuit has more than
sufficient control states for the circuit to perform its function to permit
introduction and removal of data in digital signal paths.

Another feature of the circuit is that the serial output signal on
the line 32 follows the signal of the serial input on line 31 when that line is
being used as a control line. When the line 32 signal is high or low, the line
31 signal is high or low respectively. This is a useful feature. In many
cases it is useful to connect several of these diagnostic circuits so that the
serial output line 32 is connected to a serial input line 31 of another
diagnostic circuit which has its own serial output line 32 connected to the
input line 31 of a third diagnostic circuit and so forth. This permits
diagnostic data to be cycled into and out of the various diagnostic shift
registers 26, as discussed previously. When the control mode signal is high
to all of these circuits, input line 31 of the first diagnostic circuit controls
all of the other diagnostic circuits.

One detailed embodiment of the present invention is shown in
FIG. 3 and the individual component blocks are illustrated in FIGS. 4A, 5,
and 6. In FIG. 3 the state register 50 includes the multiplexer shown in
FIG. 2A. The state register 50 thus can accept the signals of the path 71
representing the data path of the digital system. The diagnostic register

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60 receives the contents of the state register along the path 73 and in turn
may load the state register 50 along the path 74. As shown in FIG. 3 these
parallel data paths are n+1 signal lines wide with the incoming system
signals designated as B_0-B_N, the output signals to the next logic block in
the digital system designated as Y_O-Y_N and the signals from the
diagnostic register 60 back into the state register designated as A_O-A_N.
This circuit functions in the same manner as discussed previously. The
control logic block 40 generates the internal control signals for performing
all of the required functions available of the circuit.

The control logic block 40 is illustrated in detail in FIG. 4A.
Control signals through input terminals for the control mode line 75 and
the serial data input/control line 76 generate control signals for the
S Select line 84, the serial input line 83, and the D Select lines 80-82.
Furthermore the block 40 receives the serial output signal from the
diagnostic register block 60 along the line 84.

FIG. 4B is a table of generated control signals for S select and
D select 0-2 generated by the control block 40. It should be noted from
the table that only one of the D Select lines is "H" or high at a time. D
Select O high indicates that the "shift" mode has been selected. D Select 1
high corresponds to the "load" mode and D Select 2 high to a "hold" mode in
which nothing changes. The serial input signal on line 83 is not included
since it is the same as signal D select O, the complement of the control
mode signal. Thus the inverters 41, 42 and AND gates 43, 44 generate the
control signals for the diagnostic register block 60 and the state register
block 50.

Responsive to control signals, the logic block 40 also selects
whether the serial output signal or the signal on the line 76 is to be sent on
line 79. When the line 75 is low so that the diagnostic circuit is in a "shift"
mode the AND gate 45 allows the signal on line 84 to enter the OR gate 47
to appear as an output signal on the serial data output line 79. When the
control mode signal is high the AND gate 45 no longer passes signals on the
line 84, instead, by the AND gate 46, signals on the line 76 are selected for

the OR gate to the serial data output line 79. In this fashion, when the line 76 is used as a control line, the line 76 input terminal signal passes through the line 79 output terminal.

A detailed illustration of the state register block 50 is shown in FIG. 5. The block 50 has multiplexing functions performed by the AND gates 51 and 52 and the OR gates 53. A low signal on the S select line 84, representing a high signal for the control mode, enables the AND gates 51 so that the signals A_O-A_N are selected. A high signal on the line 84 corresponding to a low signal for the control mode, selects signals B_O-B_N through the data path input terminals. The selected signals through the OR gate 53 enter the D flip flops 54. These D flip flops 54 are triggered by a positive rising clock pulse from the clock for the system through an input terminal of the line 78, the system clock line, and the signal is then registered. These registered values appear on the data output path 72 to the data path output terminals as values Y_O-Y_N.

FIG. 6 is detailed illustration of the diagnostic register block 60 which receives input signals along a diagnostic clock line 77, D Select lines 80-82, and a serial input line 83. As explained previously only one of the D Select lines can be high at one time. When D Select line 80 is high, corresponding to the "shift" mode, the AND gate 61 selects the serial input signal on the line 83, for the D flip flop 64 through the OR gate 66. This is true for the logic gates and flip flop for the 0th bit place. The gates and flip flops for bit places 1 to n select by the AND gates 61 the output signals of the preceding flip flops 64 on a feedback lines 65. A shift occurs when the rising edge of the diagnostic clock pulse occurs on the line 77. The signal A_n registered by the last flip flop 64 appears on the serial output line 84. With the rising clock pulse from a clock for the diagnostic circuit through an input terminal of the line 77 the flip flop 60 registers that value. A high signal on the D Select 1 line 81, selects the values Y_O-Y_N of the data path 72 as input signals to be latched by D flip flop 64. A high signal on the line 82 merely holds the value in the flip flop 64 since the AND gate 63 are enabled and the signals in the flip flops 64 are fed back along the feedback lines 65.

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Accordingly, while the invention has been particularly shown and described with reference to the preferred embodiments, it would be understood by those skilled in the art that changes in form and details may be made therein without departing from the spirit of the invention. It is

5   therefore intended that an exclusive right be granted to the invention as limited only by the metes and bounds of the appended claims.

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CLAIMS

1. A circuit for a digital signal path comprising control means,

first means connected in said signal path and responsive to said control means, for selectively holding signals of said path,

second means connected to said first means and responsive to said control means for selectively holding signals from said first means and releasing signals to said first means, said second means having input-output means for selectively accepting digital signals and for selectively sending digital signals,

whereby digital signals may be inserted into said signal path and removed from said signal path through said input-output means.

2. A circuit as in Claim 1 wherein said first means is connected to said second means in such a manner that signals are transferred in parallel between first means and second means and wherein signals are transferred serially through said input-output means.

3. A circuit as in Claim 2 wherein said control means comprises a first control terminal by which control signals determine the selected operations for said first means and said second means.

4. A circuit as in Claim 3 wherein said input-output means comprises an input terminal and an output terminal, said input terminal becoming a second control terminal by a predetermined control signal through said first control terminal, whereby the number of said circuit operations may be increased.

5. A circuit as in Claim 4 wherein by said predetermined control signal, said output terminal is coupled to said input terminal in such a manner that signals from said output terminal correspond to signals to said input terminal.

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6. A circuit for the selective introduction and removal of digital signals into and from a digital signal path comprising

multiplexer means,

first signal storage means connected to said multiplexer means

5   for holding digital signals from said multiplexer,

second signal storage means connected to said multiplexer means and said first signal storage means for selectively holding digital signals from said first register means and for providing digital signals to said multiplexer means, said multiplexer means controllably selecting

10   signals from said digital signal path and from said second signal storage means, said second signal storage means further connected to serial input-output terminal means for the selective introduction and removal of digital signals.

7. A circuit as in Claim 6 wherein the controllable selection of

15   digital signals by said multiplexer means, the selection of holding and providing digital or introduction and removal of digital signals by said second signal storage means is by means of a control signal on a single control line.

8. A circuit as in Claim 7 wherein said serial input-output

20   terminal means comprises an input terminal and an output terminal, said input terminal selectively an input terminal or a control terminal, responsive to control signals on said control line.

9. A circuit as in Claim 8 wherein, when said input terminal is selectively a control terminal, said output terminal is coupled to said input

25   terminal in such a manner that signals from said output terminal correspond to signals to said input terminal.

10. A circuit as in Claim 9 wherein said first signal storage means comprises a first register and said second signal storage means comprises a shift register.

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11.   A circuit as in Claim 10 wherein said first register is responsive to a first timing means and said shift register is responsive to a second timing means.

12.   A circuit for the introduction and removal of digital signals into and from a digital signal path having

a plurality of input terminals for accepting said path signals,

a plurality of output terminals for sending said path signals,

a serial input terminal for signals to be introduced into said signal path,

a serial output terminal for signals to be removed from said path,

a first control terminal responsive to a first signal for the movement of signals into said serial input terminal and from said serial output terminal, and to a second signal by which said serial input terminal becomes a second control terminal.

13.   A circuit as in Claim 12 wherein responsive to said second signal, said serial output terminal is coupled to said serial input terminal so that signals through said serial output terminal correspond to signals through said said serial input terminal.

14.   A circuit for the introduction and removal of signals into and from a digital signal path comprising:

first signal storage means coupled to said digital signal path,

second signal storage means coupled to said first signal storage means,

control logic means, having a control mode terminal, a serial input terminal, a serial output terminal, and coupled to said first and second signal storage means, whereby a first signal on said control mode terminal permits the introduction and removal of signals through said serial input and output terminals, and the transfer of signal path signals to said first signal storage means.
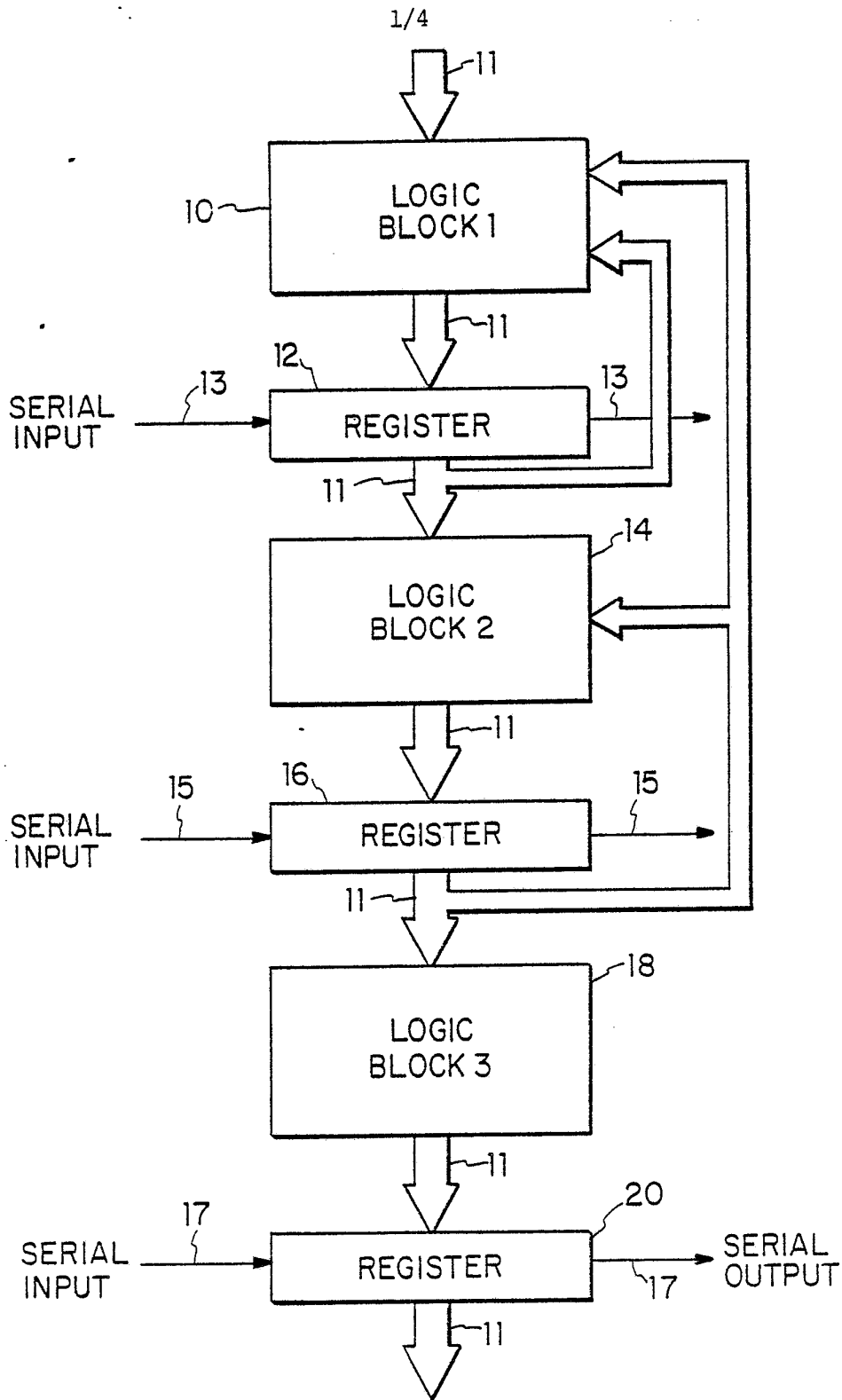
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15. A circuit as in Claim 14 wherein by a second signal on said control mode terminal, said serial input terminal operates as a control terminal, and a first signal on said serial input terminal permits signals to be transferred in parallel between said first and second signal storage means.

16. A circuit as in Claim 15 wherein, when said serial input terminal operates as a control terminal, said serial output terminal is coupled to said serial input terminal so that said serial output terminal signals correspond to said serial input terminal signals.

17. A circuit as in Claim 16 comprising a first clock terminal coupled to said first signal storage means so that signals are transferred from said second signal storage means to said first signal storage means, upon a first clock signal and a second clock terminal coupled to said second signal storage means so that signals are transferred from said first signal storage means to said second signal storage means upon a second clock signal.

18. A circuit as in Claim 17 wherein said first signal storage means comprises a register and said second signal storage means comprises a shift register.

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LOGIC
BLOCK 1

10

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SERIAL
INPUT

13

12

REGISTER

13

11

LOGIC
BLOCK 2

14

11

SERIAL
INPUT

15

16

REGISTER

15

11

LOGIC
BLOCK 3

18

11

SERIAL
INPUT

17

REGISTER

20

SERIAL
OUTPUT

17

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GENERALIZED DIGITAL SYSTEM WITH
PRIOR ART SERIAL SCAN

FIG.__1

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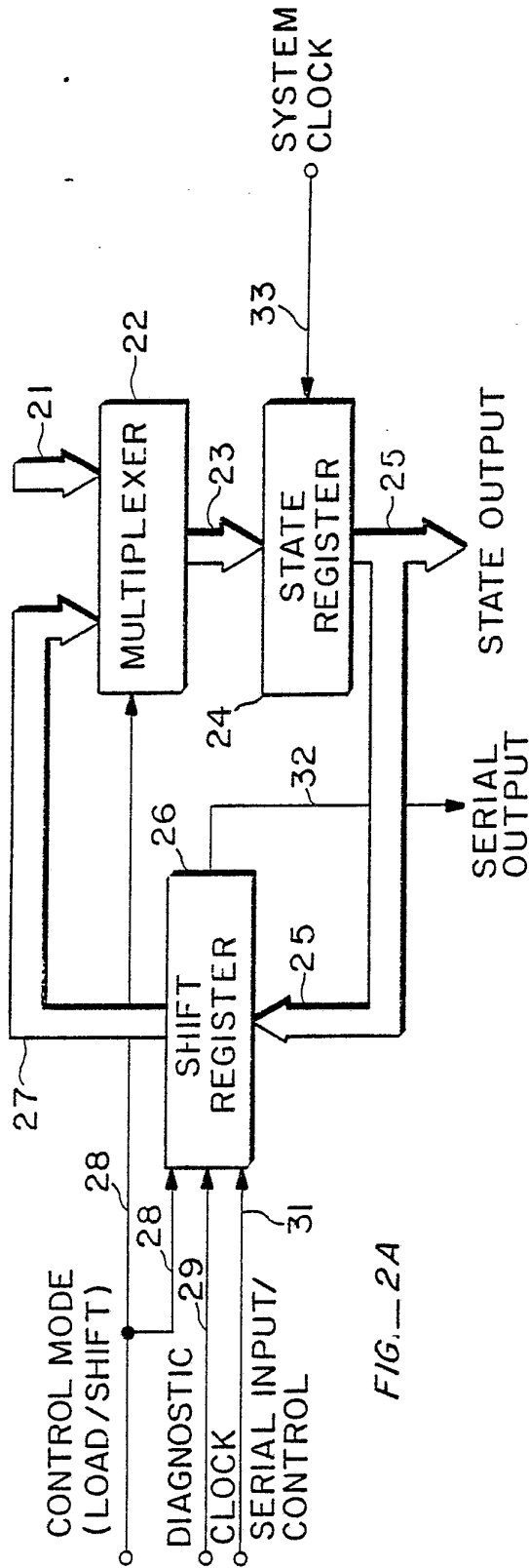
FIG._2A

OPERATION NUMBER	SERIAL INPUT	CONTROL MODE	DIAGNOSTIC CLOCK	SYSTEM CLOCK	SERIAL OUTPUT	OPERATION
1	H	L	←	—	O	SHIFT DIAGNOSTIC REGISTER
2	L	H	←	—	L	LOAD DIAGNOSTIC REGISTER FROM STATE REGISTER
3	H	H	←	—	H	OPTIONAL OPERATION
4	H	L	—	←	O	LOAD STATE REGISTER FROM SIGNAL PATH
5	L	H	—	←	L	LOAD STATE REGISTER FROM DIAGNOSTIC REGISTER
6	H	H	—	←	H	OPTIONAL OPERATION (HOLD)

FIG._2B
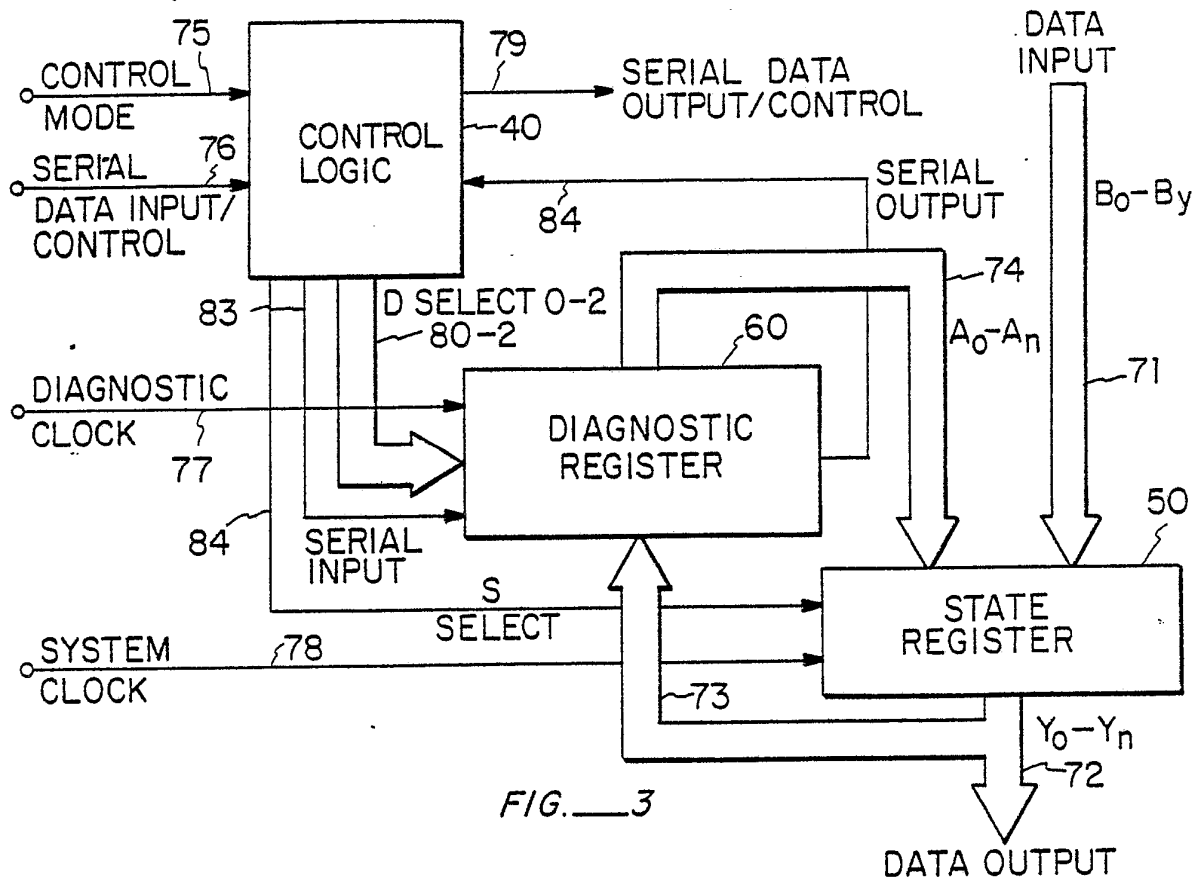
SUBSTITUTE SHEET

FIG.___3
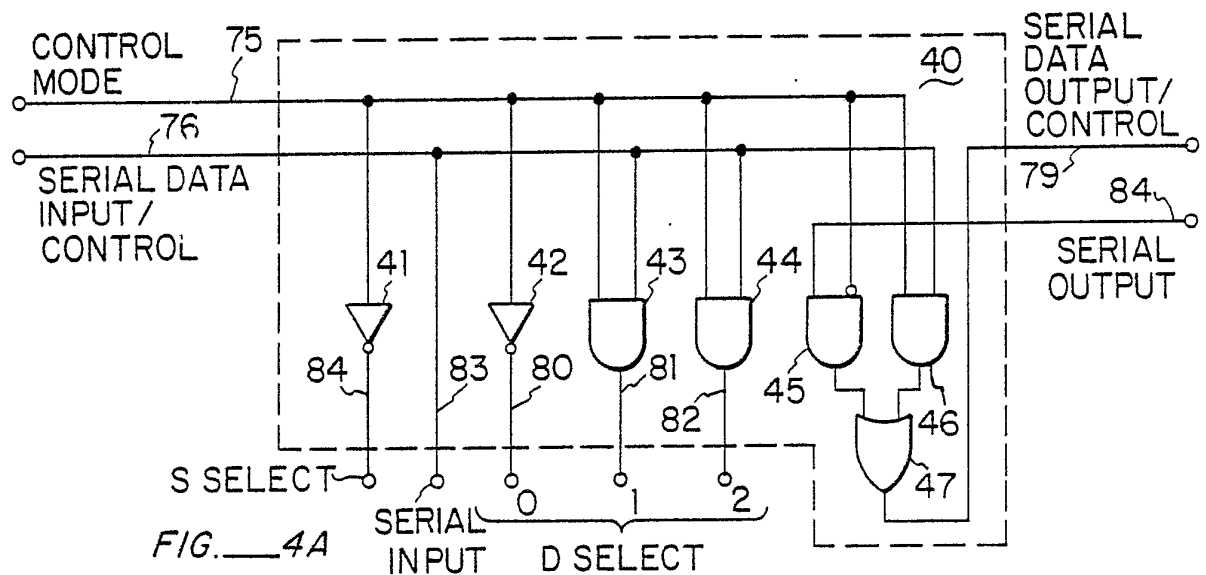
FIG.___4A

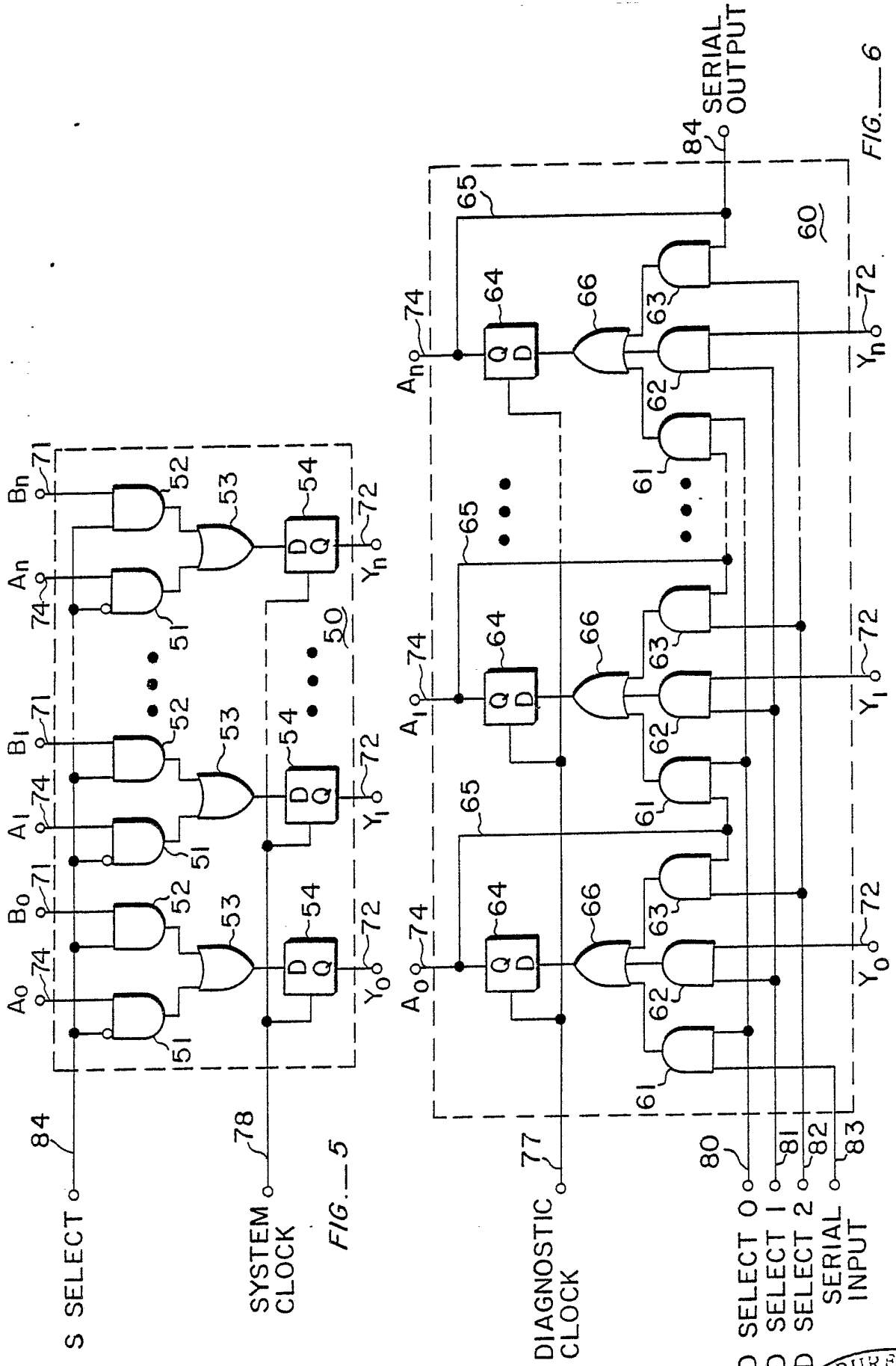| SERIAL DATA INPUT/CONTROL	CONTROL MODE	S SELECT	D SELECT 0	D SELECT 1	D SELECT 2
L	H	L	L	H	L
H	H	L	L	L	H
L	L	H	H	L	L
H	L	H	H	L	L

FIG.___4B

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FIG.—5

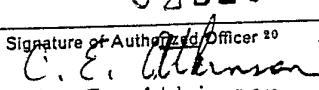
FIG.—6

INTERNATIONAL SEARCH REPORT

International Application No PCT/US83/01449

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT. CL. ^{3} G01R 31/28; H04B 17/00; H04L 1/00
U.S. CL. 364/900; 371/22, 25

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	364/900; 371/22, 25

Documentation Searched other than Minimum Documentation
to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category [*]	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X	US,A 3,657,699 (Rocher et al.) April 18, 1972	12, 13
A	US,A 3,761,695 (Eichelberger) September 25, 1972	1-18
A	US,A 4,042,794 (Lima et al.) August 16, 1977	1-18
A	US,A 4,241,307 (Hong) December 23, 1980	1-18
A	US,A 4,244,048 (Tsui) January 6, 1981	1-18
A	US,A 4,317,200 (Wakatsuki et al.) February 23, 1982	1-18

* Special categories of cited documents: [15]
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
17 November, 1983	02 DEC 1983
International Searching Authority [1]	Signature of Authorized Officer [20]
ISA/US	C. E. Atkinson

Form PCT/ISA/210 (second sheet) (October 1981)