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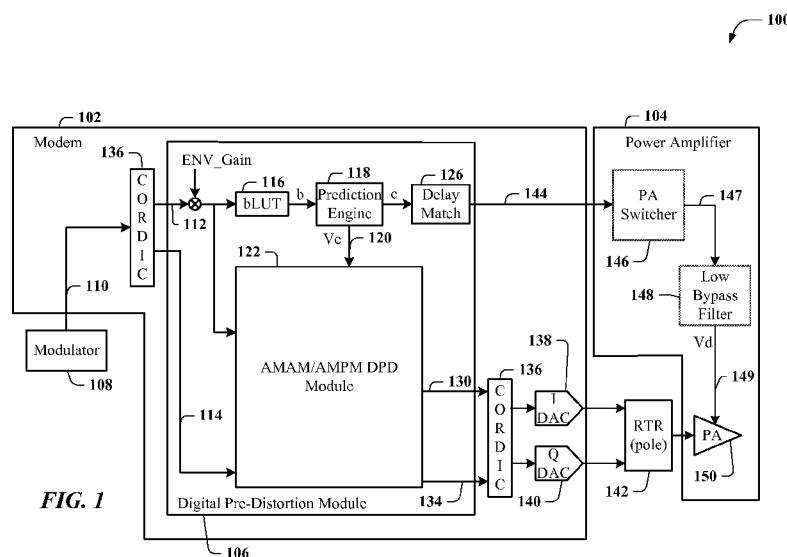


FIG. 1

(57) Abstract: Aspects disclosed herein relate to predicting one or more signal characteristics to improve efficiency for a power amplifier (150). A wireless communications device (100) may include a power amplifier (150) and a processor that is associated with a signal prediction module (118). In an aspect, the processor may be a modem (102), a RF chip, etc. In one example, the wireless communications device (100) may be configured to buffer one or more values associated with an input signal (110). The signal prediction module (118) may be configured to predict a system response to at least a portion of the one or more buffered values, and generate a switcher control signal (144) based on the system response. The signal prediction module (118) may also generate a predicted supply voltage (120) from the values associated with the input signal (110).

## **METHOD AND APPARATUS FOR PREDICTING SIGNAL CHARACTERISTICS FOR A NONLINEAR POWER AMPLIFIER**

### **BACKGROUND**

#### **Field**

**[0001]** The disclosed aspects relate generally to enabling communications using a power amplifier (PA) and specifically to methods and systems for predicting a control signal for a PA switcher and/or a predicted supply voltage for a digital pre-distortion module associated with the PA.

#### **Background**

**[0002]** Current PA control apparatuses and methods are generally configured to use one or more combination of four PA control schemes. First, a battery direct scheme directly connects the battery to the PA. This may be efficient at times when max power is needed, but at lower powers efficiency drops rapidly because it's not necessary to use full battery voltage. Second, an average power tracking (APT) scheme uses a third party switcher between the batter and PA and uses an algorithm to change voltage between power control groups. Compared to the battery direct scheme, at lower powers efficiency falls off more gradually since PA voltage is correspondingly decreased. Third, a super APT (SAPT) scheme uses an algorithm to change voltage per various power control groups and also uses predistortion and adaptiveness to squeeze voltage to limits. Fourth, envelope tracking (ET) uses a separate chipset to track the signal envelope at high speed and high precision. This scheme may require PAs optimized for ET usage and may require an ET digital to analog converter (DAC) on the mobile station modem (MSM).

**[0003]** Further, Power amplifiers typically do not behave in a linear manner. More particularly, power amplifier distortion may compress or may expand the output signal swing of the amplifier. Signal detectors receiving and decoding the amplified signals typically do not operate in such a non-linear fashion. Therefore, it is typically necessary to linearize the output of the amplifier. One approach to such linearization is digital predistortion. Digital predistorters may be used with power amplifiers to invert the power amplifier distortion characteristics by expanding the compression regions and compressing the expansion regions in the power amplifier characteristics curve.

[0004] Both PA control schemes and digital predistortion schemes would benefit from knowledge of future signal characteristics. As such, a system and apparatus that predicting a control signal for a PA switcher and/or a predicted supply voltage for a digital pre-distortion module associated with a PA may be desired.

## SUMMARY

[0005] The following presents a simplified summary of one or more aspects in order to provide a basic understanding of such aspects. This summary is not an extensive overview of all contemplated aspects, and is intended to neither identify key or critical elements of all aspects nor delineate the scope of any or all aspects. Its sole purpose is to present some concepts of one or more aspects in a simplified form as a prelude to the more detailed description that is presented later.

[0006] Various aspects are described in connection with predicting one or more signal characteristics to improve efficiency for a PA. A wireless communications device may include a power amplifier and a processor that is associated with a signal prediction module. In an aspect, the processor may be a modem, a RF chip, etc. In one example, the wireless communications device may be configured to buffer one or more values associated with an input signal. The signal prediction module may be configured to predict a system response to at least a portion of the one or more buffered values, and generate a switcher control signal based on the system response. The signal prediction module may also generate a predicted supply voltage from the values associated with the input signal.

[0007] According to related aspects, a method provides a mechanism for predicting one or more signal characteristics to improve efficiency for a PA. The method can include buffering one or more values associated with an input signal. Further, the method can include predicting a system response to at least a portion of the one or more buffered values. Moreover, the method can include generating a switcher control signal based on the system response.

[0008] Another aspect relates to a communications apparatus. The wireless communications apparatus can include means for buffering one or more values associated with an input signal. Further, the apparatus can include means for predicting a system response to at least a portion of the one or more buffered values. Moreover,

the apparatus can include means for generating a switcher control signal based on the system response.

[0009] Another aspect relates to a communications apparatus. The apparatus can include a buffer configured to store one or more values associated with an input signal, a reception module configured to provide the one or more values associated with the input signal to the buffer for storage, and a prediction module. The prediction module may be configured to predict a system response to at least a portion of the one or more buffered values. Further, the signal prediction module may be configured to generate a switcher control signal based on the system response.

[0010] Another aspect relates to a computer program product, which can have a computer-readable medium comprising code for buffering one or more values associated with an input signal. Further, the computer-readable medium can also include code for predicting a system response to at least a portion of the one or more buffered values. Moreover, the computer-readable medium can also include code for generating a switcher control signal based on the system response.

[0011] To the accomplishment of the foregoing and related ends, the one or more aspects comprise the features hereinafter fully described and particularly pointed out in the claims. The following description and the annexed drawings set forth in detail certain illustrative features of the one or more aspects. These features are indicative, however, of but a few of the various ways in which the principles of various aspects may be employed, and this description is intended to include all such aspects and their equivalents.

### **BRIEF DESCRIPTION OF THE DRAWINGS**

[0012] The disclosed aspects will hereinafter be described in conjunction with the appended drawings, provided to illustrate and not to limit the disclosed aspects, wherein like designations denote like elements, and in which:

[0013] FIG. 1 is a functional block diagram of an example transmitter including a modem and a power amplifier, according to an aspect;

[0014] FIG. 2 is an example schematic diagram of a signal prediction module, according to an aspect;

[0015] FIG. 3 is a graphical representation of a signal prediction module output, according to an aspect;

[0016] FIG. 4 is a flowchart diagram describing an example for predicting a control signal for a PA switcher and/or a predicted supply voltage for a digital pre-distortion module, according to an aspect;

[0017] FIG. 5 is a functional block diagram example architecture of a communications device, according to an aspect; and

[0018] FIG. 6 is a functional block diagram of an example communication system for predicting a control signal for a PA switcher and/or a predicted supply voltage for a digital pre-distortion module, according to an aspect.

### DETAILED DESCRIPTION

[0019] Various aspects are now described with reference to the drawings. In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of one or more aspects. It may be evident, however, that such aspect(s) may be practiced without these specific details.

[0020] A transmitter including a modem, a PA, and a PA switcher, coupled to the modem and PA, is described herein. The PA switcher may be configured to receive, from the modem, a switcher control signal on a control line, and switch among one or more voltage source paths and a ground voltage path to provide a supply voltage to low pass filter which may generate a smoothed supply voltage for the power amplifier. In an aspect, the switch control signal may indicate which path to use based on system response information. The transmitter may be used for various electronic devices such as wireless communication devices, cellular phones, personal digital assistants (PDAs), handheld devices, wireless modems, laptop computers, cordless phones, Bluetooth devices, consumer electronic devices, etc. For clarity, the use of the transmitter in a wireless communication device is described below.

[0021] **FIG. 1** illustrates a functional block diagram of an example transmitter 100 with modem 102 and PA component 104. Modem 102 may include a digital pre-distortion (DPD) module 106. PA component 104 may include PA switcher 146 that is configured to provide a supply voltage 147 to a low pass filter 148. Low pass filter 148 may process the supply voltage to generate a smoothed supply voltage 149 for PA 150.

[0022] Modem 102 may further include a coordinate rotation digital computer (CORDIC) component 136 that may be configured to receive a signal 110 from a modulator 108 and divide the signal 110 into an amplitude component 112 and a phase

component 114. DPD module 106 may process amplitude component 112 and phase component 114 to produce a pre-distorted amplitude component 130 and a pre-distorted phase component 134. The pre-distorted amplitude 130 and phase 134 components may be processed by CORDIC 136 and converted to amplitude and phase components of an analog signal using “I” digital to analog converter 138 (I DAC) and “Q” DAC 140, respectively. The analog signal components may be combined through a radio transceiver (RTR) 142 and provided to PA 150.

**[0023]** Within DPD module 106, the amplitude component 112 may be split, with a path (e.g., “b” path) leading to a prediction engine 118 and another path leading to an amplitude to amplitude (AMAM) / amplitude to phase (AMPM) DPD module 122.

**[0024]** In operation, the amplitude component 112 may be processed using AMAM/AMPM DPD module 122 to generate the pre-distorted amplitude component 130. In another aspect, the phase component 114 may be processed using AMAM/AMPM DPD module 122 to generate the pre-distorted phase component 134.

**[0025]** In another aspect, prior to being received by prediction engine 118, a gain associated with the amplitude component 112 (“b” path) may be modified using a LUT (e.g., bLUT) 116. Prediction engine 118 may then receive the modified amplitude component 112 and may determine an predicted voltage 120 for signal 110 and a control signal 144 for PA switcher 146. In an aspect, the received component 112 may include one or more state register values. In an aspect, prediction engine 118 may compare received component 112 (e.g.,  $V(k)$ ) and a bound value ( $b(k)$ ) at time ( $t$ ) and if any  $V(k)$  is within a tolerance ( $tol$ ) of  $b(k)$ , then prediction engine 118 may determine that a supply voltage control signal value 144 for time ( $t$ ) equals “1” (e.g., the control signal 144 prompts PA switcher 146 to use a path with a voltage supply). By contrast, where  $V(k)$  at time  $t$  does not fall within the tolerance for any  $b(k)$  value, then a supply voltage control signal value 144 for time ( $t$ ) may equal “0” (e.g., the control signal 144 prompts PA switcher 146 to use a path with a voltage ground). Further, in operation, the control signal 144 may pass through a delay match 126 (e.g., buffer) so as to match the arrival of the analog signal at the PA 150 with the smoothed supply voltage 14 from the low pass filter 148. In an aspect, a state register may be updated for a time ( $t$ ) plus a time increment ( $dt$ ) and the prediction engine 118 may predict a voltage ( $V_e$ ) value 120 for a future time ( $V(k)=V(k+1)-h(k)$ ,  $V_d=V(1)$  when  $V_s(t) = 0$ , and  $V(k)=V(k+1)-h(k)+h(k+1)$ ,  $V_d=V(1)+h(1)$  when  $V_s(t) = 1$ ).

[0026] FIG. 2 is a block diagram illustrating a signal prediction module 200, such as prediction engine 118, that is configured to generate projected supply voltage value(s) 212 and/or control signal(s) 222 for a predistortion module and/or power amplifier switcher associated with a nonlinear power amplifier.

[0027] Signal prediction module 200 may include an impulse function module 204, an input voltage sample module 208, a bound module 214, and a PA switcher control signal module 218. In an aspect, the impulse function module 204 may include one or more impulse functions 206 that may be applied (e.g., added and/or subtracted) to various input voltage samples 210. In such an aspect, signal prediction module 200 may predict a future supply voltage value 212 based on the application of the impulse functions 206 to the various input voltage samples 210. In an aspect, an impulse function 206 may provide a pre-calculated impulse response to a voltage supplied by a battery followed by ground voltage supply values (e.g.,  $V_s = [V_{bat}, 0, 0, \dots, 0]$ ). In one aspect, signal prediction module 200 may be configured to operate on “W” samples of a received input signal 202. In such an aspect, a modem, with which the signal prediction module 200 may be associated, may include a buffer (e.g., delay match 126) that may store “W” samples so as to allow signal prediction module 200 to generate a predicted supply voltage for a digital predistortion module (e.g., digital predistortion module 106). In an aspect, input voltage sample module 208 may be configured to receive at least a portion of an input signal 202. In such an aspect, input voltage sample module 208 may receive multiple samples 208 that may be modified by one or more impulse functions 206 to assist the signal prediction module 200 in generating a predicted voltage value 212. For example, impulse functions 206 may be used to modify each sample input signal value 210 to predict whether the signal, at a time associated with the signal sample 210, may be drop below and/or within a tolerance value 220 of a bound value 216. In another aspect, bound module 214 may include one or more bound values to be used in comparison with each of the input samples 210.

[0028] In operation, for a time “t” at least a portion of the “W” input voltage sample (e.g.,  $V(W-1), V(W-2) \dots V(1)$ ) may be modified through use of the various impulse functions “h” (e.g.,  $V(W)+h(W-1)$  results in  $(V(W-1)$ , etc.) and compared with a bound value “b” ( $b(W)$ ). For each of the W samples is compared, PA switcher control signal module 218 determines if any of the samples are within a tolerance value 220 of the corresponding bound value 216. If PA switcher control signal module 218 determines

any of the input voltage samples 210 are within a tolerance value 220 of their corresponding bound values 216, then a PA switcher control signal value 222 for time (t) may be set to “1” (e.g., the control signal prompts a switcher to use a path with a voltage supply). By contrast, if PA switcher control signal module 218 determines none of the input voltage samples 210 are within a tolerance value 220 of their corresponding bound values 216, then a PA switcher control signal value 222 for time (t) may be set to “0” (e.g., the control signal prompts a switcher to use a path with a voltage ground). Further, a state register associated with the input signal may be updated for a time (t) plus a time interment “dt” and signal prediction module 200 may project a supply voltage  $V_d$  value for a time “t” (e.g.,  $(V(k)=V(k+1)-h(k), V_d=V(1)$  when  $V_s(t) = 0$ , and  $V(k)=V(k+1)-h(k)+h(k+1), V_d=V(1)+h(1)$  when  $V_s(t) = 1$ )).

**[0029] FIG. 3** illustrates a graphical representation 300 of a signal prediction module output, according to an aspect.

**[0030]** Graphical representation 300 includes an x-axis 302 representing time in milliseconds. Graphical representation 300 further includes a y-axis 304 voltage values for a signal. In the depicted graph, the output voltages are represented in Volts. Example, curves for a real supply voltage ( $V_d$ ) 310, a  $V_d$  bound 306 are presented in graphical representation 300. In an operational aspect, a signal prediction module may use a  $V_d$  bound to calculate a supply voltage 308. Further, the calculated supply voltage 308 and/or the bound voltage value 310 may be used to generate a PA switcher control signal. This control signal may indicate times when the PA switcher is to use a path associated with a battery supply voltage. The “+” signs 312 indicates instances when a PA control signal would indicate to use the battery supply path.

**[0031]** As such, in an example aspect, a  $V_d$  bound 308, associated with a real supply voltage 310, may be used to assist in calculating an predicted supply voltage 308 and or a PA switcher control signal 312.

**[0032]** FIG. 4 illustrates methodologies in accordance with various aspects of the presented subject matter. While the methodologies are shown and described as a series of acts or sequence steps for the purposes of simplicity of explanation, it is to be understood and appreciated that the claimed subject matter is not limited by the order of acts, as some acts may occur in different orders and/or concurrently with other acts from that shown and described herein. For example, those skilled in the art will understand and appreciate that a methodology could alternatively be represented as a series of



interrelated states or events, such as in a state diagram. Moreover, not all illustrated acts may be required to implement a methodology in accordance with the claimed subject matter. Additionally, it should be further appreciated that the methodologies disclosed hereinafter and throughout this specification are capable of being stored on an article of manufacture to facilitate transporting and transferring such methodologies to computers. The term article of manufacture, as used herein, is intended to encompass a computer program accessible from any computer-readable device, carrier, or media.

**[0033] FIG. 4** illustrates a flowchart 400 describing a method for predicting a control signal for a PA switcher and/or a predicted supply voltage for a digital pre-distortion module.

**[0034]** At block 402, a signal prediction module may receive an input signal with amplitude and phase voltage components. In one aspect, the signal prediction module may store values (e.g., amplitude and/or phase) associated with the input signal in a buffer. As used herein, a state register values may be a voltage value at a time “t” ( $V(t)$ ) as a first state, and the derivative of the voltage at time “t” ( $V'(t)$ ) multiplied by a coefficient  $\frac{\sin \beta t}{\beta}$  as a second state. In such an aspect,  $\beta$  may be a component of an input signal with a state “s” root function characterized by  $s_{1,2} = \alpha \pm j\beta$ . In an aspect, one or more state register values may be associated with the input signal. In such an aspect, the state register values may include one or more coefficients that may assist with updating a state register for use during supply voltage predication. Further, the one or more coefficients may be further buffered to allow for online (e.g., real time) updating of the state register values.

**[0035]** At block 404, the signal prediction module may predict system response(s) to the received and buffered value(s). In an aspect, the signal prediction module may predict system response(s) by using an impulse function to generate projected supply voltage value(s). In an aspect, the signal prediction module may use different impulse functions with each of the first and second state functions. Further, as part of predicting the system response, the signal prediction module may compare each of the one or more projected supply voltage values with a corresponding bound value, and determine whether any projected supply voltage value of the one or more projected supply voltage values is within a tolerance threshold of the corresponding bound value.

**[0036]** At block 406, the signal prediction module may generate a switcher control signal based on the system response. In an aspect, the switcher control signal may

include a digital bit value prompting a power amplifier switcher to use one or more voltage source paths. In another aspect, the switcher control signal may include a digital bit value prompting a power amplifier switcher to use a ground voltage path. For example, the PA switcher control signal may include a first value (e.g., “1”) prompting the PA switcher to use a voltage source (e.g., battery) path when any of projected supply voltage values are within the tolerance threshold of their corresponding bound value, and/or a second value “0” prompting the switcher to use a ground source path when none of the projected supply voltage values are within the tolerance threshold of their corresponding bound value.

**[0037]** In an optional aspect, at block 408, the signal prediction module may provide the generated switcher control signal to a PA switcher.

**[0038]** In another optional aspect, at block 410, the signal prediction module may generate a predicted supply voltage from the one or more project supply voltage values. In such an aspect, the predicted supply voltage may be used by a predistortion module. In one aspect, the buffer may be large enough to allow W consecutive sample values to be stored. In such an aspect, the W consecutive sample values may be used to generate projected supply voltage value(s). In another aspect, the buffer may be large enough to allow N check-points associated with the input signal to generate the projected supply voltage value(s).

**[0039]** In such an optional aspect, at block 412, the signal prediction module may provide the generated predicted supply voltage to a predistortion module.

**[0040] FIG. 5** illustrates an example architecture of communications device 500. As depicted in FIG. 5, communications device 500 includes receiver 502 that receives a signal from, for instance, a receive antenna (not shown), performs typical actions on (e.g., filters, amplifies, downconverts, etc.) the received signal, and digitizes the conditioned signal to obtain samples. Receiver 502 can include a demodulator 504 that can demodulate received symbols and provide them to processor 506 for channel estimation. Processor 506 can be a processor dedicated to analyzing information received by receiver 502 and/or generating information for transmission by transmitter 520, a processor that controls one or more components of communications device 500, and/or a processor that both analyzes information received by receiver 502, generates information for transmission by transmitter 520, and controls one or more components of communications device 500. Further, signals may be prepared for transmission by

transmitter 520 through modulator 518 which may modulate the signals processed by processor 506.

**[0041]** Communications device 500 can additionally include memory 508 that is operatively coupled to processor 506 and that can store data to be transmitted, received data, information related to available channels, TCP flows, data associated with analyzed signal and/or interference strength, information related to an assigned channel, power, rate, or the like, and any other suitable information for estimating a channel and communicating *via* the channel. Communications device 500 can additionally include a power supply (e.g., battery 530, power supply interface, etc.).

**[0042]** Further, at least one of processor 506 or transmitter 520 can provide means for buffering one or more values associated with an input signal, means for predicting a system response to at least a portion of the one or more buffered values, and means for generating a switcher control signal based on the system response.

**[0043]** It will be appreciated that data store (e.g., memory 508) described herein can be either volatile memory or nonvolatile memory, or can include both volatile and nonvolatile memory. By way of illustration, and not limitation, nonvolatile memory can include read only memory (ROM), programmable ROM (PROM), electrically programmable ROM (EPROM), electrically erasable PROM (EEPROM), or flash memory. Volatile memory can include random access memory (RAM), which acts as external cache memory. By way of illustration and not limitation, RAM is available in many forms such as synchronous RAM (SRAM), dynamic RAM (DRAM), synchronous DRAM (SDRAM), double data rate SDRAM (DDR SDRAM), enhanced SDRAM (ESDRAM), Synchlink DRAM (SLDRAM), and direct Rambus RAM (DRRAM). Memory 508 of the subject systems and methods may comprise, without being limited to, these and any other suitable types of memory.

**[0044]** Communications device 500 transmitter 520 may include modem 522 and power amplifier 530. In an aspect, power amplifier 530 may include a PA switcher 532 that is configured to provide a supply voltage for power amplifier 530 from a ground source path or a battery 550 source path. In an aspect, the PA switcher may receive a PA switcher control signal 528 from the signal prediction module 524 prompting the PA switcher 532 to use either the battery 550 supply path or the ground supply path. In an aspect, modem 522 may include a signal prediction module 524 that may be configured predict various characteristics of an input signal to assist transmitter 520 with efficient

signal transmission through power amplifier 530. Signal prediction module 524 may further include impulse response function module 525 and bound module 527. In an aspect, impulse response function module 525 and bound module 527 may be used for modification of and/or comparison with one or more input signal samples. For example, input signal samples may be modified based on one or more impulse response functions to generate an predicted supply voltage 526. In another example, comparison of input signal sample values with one or more bound values may assist signal prediction module 524 in generating the PA switcher control signal 528.

**[0045]** In an operational aspect, signal prediction module 524 may process an input signal that can be characterized by a second order system, as shown in Equation (1) with roots shown in Equation (2).

$$LCs^2 + \frac{L}{R}s + V = 0 \quad (1)$$

$$s_{1,2} = \alpha \pm j\beta \quad (2)$$

**[0046]** With reference to the above equations L represents the system conductor value, C represents a system capacitance value, and R represents a system resistance value. A step response can be represented in Equation (3), where a voltage at time “t” can be treated as a state function.

$$\begin{bmatrix} V(t) \\ V'(t) \end{bmatrix} = \begin{bmatrix} (\cos \beta t - \frac{\alpha}{\beta} \sin \beta t)e^{\alpha t} & \frac{\sin \beta t}{\beta} e^{\alpha t} \\ -\frac{\alpha^2 + \beta^2}{\beta} \sin \beta t e^{\alpha t} & (\cos \beta t + \frac{\alpha}{\beta} \sin \beta t)e^{\alpha t} \end{bmatrix} \begin{bmatrix} V(0) \\ V'(0) \end{bmatrix} + \begin{bmatrix} 1 - (\cos \beta t - \frac{\alpha}{\beta} \sin \beta t)e^{\alpha t} \\ \frac{\alpha^2 + \beta^2}{\beta} \sin \beta t e^{\alpha t} \end{bmatrix} V_{bat} \quad (3)$$

**[0047]** Still further, different impulse functions (e.g., g(k) and/or h(k)) may be applied to equation (3) to provide updates to the state functions, as shown in equation (4).

$$\begin{bmatrix} s_1(t+dt) \\ s_2(t+dt) \end{bmatrix} = \begin{bmatrix} (\cos \beta dt - \frac{\alpha}{\beta} \sin \beta dt)e^{\alpha dt} & \frac{\sin \beta dt}{\beta} e^{\alpha dt} \\ -(\alpha^2 + \beta^2) \left( \frac{\sin \beta dt}{\beta} \right)^2 e^{\alpha dt} & (\cos \beta dt + \frac{\alpha}{\beta} \sin \beta dt)e^{\alpha dt} \end{bmatrix} \begin{bmatrix} s_1(t) - h(W) \\ s_2(t) - g(W) \end{bmatrix} \quad \text{if } V_s(t) = 0$$

$$\begin{bmatrix} s_1(t+dt) \\ s_2(t+dt) \end{bmatrix} = \begin{bmatrix} (\cos \beta dt - \frac{\alpha}{\beta} \sin \beta dt)e^{\alpha dt} & \frac{\sin \beta dt}{\beta} e^{\alpha dt} \\ -(\alpha^2 + \beta^2) \left( \frac{\sin \beta dt}{\beta} \right)^2 e^{\alpha dt} & (\cos \beta dt + \frac{\alpha}{\beta} \sin \beta dt)e^{\alpha dt} \end{bmatrix} \begin{bmatrix} s_1(t) - h(W) + h(W+1) \\ s_2(t) - g(W) + g(W+1) \end{bmatrix} \quad \text{if } V_s(t) = 1$$

$$+ \begin{bmatrix} 1 - (\cos \beta dt - \frac{\alpha}{\beta} \sin \beta dt)e^{\alpha dt} \\ (\alpha^2 + \beta^2) \left( \frac{\sin \beta dt}{\beta} \right)^2 e^{\alpha dt} \end{bmatrix} V_{bat} \quad (4)$$

[0048] In equation (4),  $g(k)$  is an impulse response function of  $\frac{\sin \beta t}{\beta}$  to  $V_s=[V_{bat},0,\dots,0]$ . While  $h(k)$  is an impulse response function of  $V(t)$  to  $V_s=[V_{bat}, 0, \dots, 0]$ . Further description of various interactions within modem 522 is provided above with reference to FIGs 1 and 2.

[0049] Additionally, communications device 500 may include user interface 540. User interface 540 may include input mechanisms 542 for generating inputs into communications device 500, and output mechanism 544 for generating information for consumption by the user of the communications device 500. For example, input mechanism 542 may include a mechanism such as a key or keyboard, a mouse, a touch-screen display, a microphone, etc. Further, for example, output mechanism 544 may include a display, an audio speaker, a haptic feedback mechanism, etc. In the illustrated aspects, the output mechanism 544 may include a display configured to present media content that is in image or video format or an audio speaker to present media content that is in an audio format.

[0050] Referring to **FIG. 6**, an apparatus 600 that predicts a control signal for a PA switcher and/or a predicted supply voltage for a digital pre-distortion module can reside at least partially within a transmitter. It is to be appreciated that apparatus 600 is represented as including functional blocks, which can represent functions implemented by a processor, software, or combination thereof (*e.g.*, firmware).

[0051] As such, apparatus 600 includes a logical grouping 602 of electrical components that can act in conjunction. For instance, logical grouping 602 can include means for buffering one or more values associated with an input signal (Block 604). In an aspect, the means for buffering 604 may be configured to receive one or more state register values associated with the input signal. In an aspect, the means for buffering 604 may be configured to receive two or more consecutive sample values of the input signal. In another aspect, the means for buffering 604 may be configured to receive a plurality of consecutive sample values sufficient to allow at least one dominant peak to one trough of the input signal to be stored in the buffer. For example, in an aspect, the means 604 can include modem 522 and memory 508 of communications device 500 and/or processor 506 of communications device 500.

[0052] Further, logical grouping 602 can include means for predicting a system response to at least a portion of the one or more buffered values (Block 606). In an aspect, the means for predicting 606 may be configured to use an impulse function to

generate one or more projected supply voltage values based at least in part on the buffered one or more values associated with the input signal, compare each of the one or more projected supply voltage values with a corresponding bound value, and determine whether any projected supply voltage value of the one or more projected supply voltage values is within a tolerance threshold of the corresponding bound value. For example, in an aspect, the means for using 606 can include modem 522, signal prediction module 524 and/or impulse response function module 525 of communications device 500 and/or processor 506 of communications device 500.

**[0053]** Further, logical grouping 602 can include means for generating a switcher control signal based on the system response (Block 608). In an aspect, the switcher control signal may include a digital bit value prompting a power amplifier switcher to use one or more voltage source paths. In another aspect, the switcher control signal may include a digital bit value prompting a power amplifier switcher to use a ground voltage path. In an aspect, the means for generating 608 may be further configured to generate a predicted supply voltage from the one or more values associated with the input signal. In an aspect, the means for generating 608 may be further configured to use using two or more consecutive sample values of the input signal to generate the predicted supply voltage. For example, in an aspect, the means for generating 608 can include modem 522 and/or signal prediction module 524 of communications device 500 and/or processor 506 of communications device 500.

**[0054]** In an optional aspect, logical grouping 602 can include means for providing one or more generated items to components associated with the processor (Block 610). In an aspect, the processor may be associated with a modem, a RF chip, etc. In an aspect, the means for providing 614 may include means for providing 614 providing the switcher control signal to the power amplifier switcher associated with a power amplifier. In another aspect, the means for providing 614 may include means for providing 614 providing the predicted supply voltage to a predistortion module. For example, in an aspect, the means for providing 614 can include modem 522 and/or signal prediction module 524 of communications device 500 and/or processor 506 of communications device 500.

**[0055]** Additionally, apparatus 600 can include a memory 612 that retains instructions for executing functions associated with electrical components 604, 606, 608, and 610. While shown as being external to memory 612, it is to be understood that one or more

of electrical components 604, 606, 608, and 610 can exist within memory 612. In an aspect, for example, memory 612 may be the same as or similar to memory 508 (FIG. 5).

**[0056]** As used in this application, the terms “component,” “module,” “system” and the like are intended to include a computer-related entity, such as but not limited to hardware, firmware, a combination of hardware and software, software, or software in execution. For example, a component may be, but is not limited to being, a process running on a processor, a processor, an object, an executable, a thread of execution, a program, and/or a computer. By way of illustration, both an application running on a computing device and the computing device can be a component. One or more components can reside within a process and/or thread of execution and a component may be localized on one computer and/or distributed between two or more computers. In addition, these components can execute from various computer readable media having various data structures stored thereon. The components may communicate by way of local and/or remote processes such as in accordance with a signal having one or more data packets, such as data from one component interacting with another component in a local system, distributed system, and/or across a network such as the Internet with other systems by way of the signal.

**[0057]** Furthermore, various aspects are described herein in connection with a terminal, which can be a wired terminal or a wireless terminal. A terminal can also be called a system, device, subscriber unit, subscriber station, mobile station, mobile, mobile device, remote station, remote terminal, access terminal, user terminal, terminal, communication device, user agent, user device, or user equipment (UE). A wireless terminal may be a cellular telephone, a satellite phone, a cordless telephone, a Session Initiation Protocol (SIP) phone, a wireless local loop (WLL) station, a personal digital assistant (PDA), a handheld device having wireless connection capability, a computing device, or other processing devices connected to a wireless modem. Moreover, various aspects are described herein in connection with a base station. A base station may be utilized for communicating with wireless terminal(s) and may also be referred to as an access point, a Node B, or some other terminology.

**[0058]** Moreover, the term “or” is intended to mean an inclusive “or” rather than an exclusive “or.” That is, unless specified otherwise, or clear from the context, the phrase “X employs A or B” is intended to mean any of the natural inclusive permutations.

That is, the phrase “X employs A or B” is satisfied by any of the following instances: X employs A; X employs B; or X employs both A and B. In addition, the articles “a” and “an” as used in this application and the appended claims should generally be construed to mean “one or more” unless specified otherwise or clear from the context to be directed to a singular form.

**[0059]** The techniques described herein may be used for various wireless communication systems such as CDMA, TDMA, FDMA, OFDMA, SC-FDMA and other systems. The terms “system” and “network” are often used interchangeably. A CDMA system may implement a radio technology such as Universal Terrestrial Radio Access (UTRA), cdma2000, etc. UTRA includes Wideband-CDMA (W-CDMA) and other variants of CDMA. Further, cdma2000 covers IS-2000, IS-95 and IS-856 standards. A TDMA system may implement a radio technology such as Global System for Mobile Communications (GSM). An OFDMA system may implement a radio technology such as Evolved UTRA (E-UTRA), Ultra Mobile Broadband (UMB), IEEE 802.11 (Wi-Fi), IEEE 802.16 (WiMAX), IEEE 802.20, Flash-OFDM, etc. UTRA and E-UTRA are part of Universal Mobile Telecommunication System (UMTS). 3GPP Long Term Evolution (LTE) is a release of UMTS that uses E-UTRA, which employs OFDMA on the downlink and SC-FDMA on the uplink. UTRA, E-UTRA, UMTS, LTE and GSM are described in documents from an organization named “3rd Generation Partnership Project” (3GPP). Additionally, cdma2000 and UMB are described in documents from an organization named “3rd Generation Partnership Project 2” (3GPP2). Further, such wireless communication systems may additionally include peer-to-peer (e.g., mobile-to-mobile) *ad hoc* network systems often using unpaired unlicensed spectrums, 802.xx wireless LAN, BLUETOOTH and any other short- or long- range, wireless communication techniques.

**[0060]** Various aspects or features will be presented in terms of systems that may include a number of devices, components, modules, and the like. It is to be understood and appreciated that the various systems may include additional devices, components, modules, etc. and/or may not include all of the devices, components, modules etc. discussed in connection with the figures. A combination of these approaches may also be used.

**[0061]** The various illustrative logics, logical blocks, modules, and circuits described in connection with the embodiments disclosed herein may be implemented or performed



with a general purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general-purpose processor may be a microprocessor, but, in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration. Additionally, at least one processor may comprise one or more modules operable to perform one or more of the steps and/or actions described above.

**[0062]** Further, the steps and/or actions of a method or algorithm described in connection with the aspects disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module may reside in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, a hard disk, a removable disk, a CD-ROM, or any other form of storage medium known in the art. An exemplary storage medium may be coupled to the processor, such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor. Further, in some aspects, the processor and the storage medium may reside in an ASIC. Additionally, the ASIC may reside in a user terminal. In the alternative, the processor and the storage medium may reside as discrete components in a user terminal. Additionally, in some aspects, the steps and/or actions of a method or algorithm may reside as one or any combination or set of codes and/or instructions on a machine readable medium and/or computer readable medium, which may be incorporated into a computer program product.

**[0063]** In one or more aspects, the functions described may be implemented in hardware, software, firmware, or any combination thereof. If implemented in software, the functions may be stored or transmitted as one or more instructions or code on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that facilitates transfer of a computer program from one place to another. A storage medium may be any available

media that can be accessed by a computer. By way of example, and not limitation, such computer-readable media can comprise RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that can be used to carry or store desired program code in the form of instructions or data structures and that can be accessed by a computer. Also, any connection may be termed a computer-readable medium. For example, if software is transmitted from a website, server, or other remote source using a coaxial cable, fiber optic cable, twisted pair, digital subscriber line (DSL), or wireless technologies such as infrared, radio, and microwave, then the coaxial cable, fiber optic cable, twisted pair, DSL, or wireless technologies such as infrared, radio, and microwave are included in the definition of medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk and blu-ray disc where disks usually reproduce data magnetically, while discs usually reproduce data optically with lasers. Combinations of the above should also be included within the scope of computer-readable media.

**[0064]** While the foregoing disclosure discusses illustrative aspects and/or embodiments, it should be noted that various changes and modifications could be made herein without departing from the scope of the described aspects and/or embodiments as defined by the appended claims. Furthermore, although elements of the described aspects and/or embodiments may be described or claimed in the singular, the plural is contemplated unless limitation to the singular is explicitly stated. Additionally, all or a portion of any aspect and/or embodiment may be utilized with all or a portion of any other aspect and/or embodiment, unless stated otherwise.

**WHAT IS CLAIMED IS:**

## CLAIMS

1. A method of communications, comprising:  
buffering one or more values associated with an input signal;  
predicting a system response to at least a portion of the one or more buffered values; and  
generating a switcher control signal based on the system response.
2. The method of claim 1, wherein the predicting the system response further comprises:  
using a response function based on a system configuration to generate one or more projected supply voltage values, wherein the system includes a low pass filter and a PA;  
comparing each of the one or more projected supply voltage values with a corresponding bound value based at least in part on the buffered one or more values associated with the input signal; and  
determining whether any projected supply voltage value of the one or more projected supply voltage values is within a tolerance threshold of the corresponding bound value.
3. The method of claim 2, wherein the generating further comprises generating the switcher control signal with a digital bit value prompting a power amplifier switcher to use a voltage source path upon a determination that any of the one or more projected supply voltage values is within the tolerance threshold of the corresponding bound value.
4. The method of claim 2, wherein the generating further comprises generating a switcher control signal with a value prompting the power amplifier switch to use a ground source path upon a determination that none of the one or more projected supply voltage values are within the tolerance threshold of the corresponding bound value.
5. The method of claim 1, further comprising:  
providing the switcher control signal to the power amplifier switcher.

6. The method of claim 1, further comprising tracking a system state through one or more state register values, wherein the system includes a low pass filter and a PA.
7. The method of claim 1, further comprising:
  - generating a predicted supply voltage from the one or more values associated with the input signal; and
  - providing the predicted supply voltage to a predistortion module.
8. The method of claim 7, further comprising receiving a plurality of consecutive sample values sufficient to allow at least one dominant peak to one trough of the input signal to be stored in the buffer.
9. An apparatus comprising:
  - a buffer configured to store one or more values associated with an input signal;
  - a reception module configured to buffer the one or more values associated with the input signal;
  - a prediction module configured to:
    - predict a system response to at least a portion of the one or more buffered values; and
    - generate a switcher control signal based on the system response.
10. The apparatus of claim 9, wherein the prediction module is further configured to:
  - use a response function based on a system configuration to generate one or more projected supply voltage values, wherein the system includes a low pass filter and a PA;
  - compare each of the one or more projected supply voltage values with a corresponding bound value based at least in part on the buffered one or more values associated with the input signal; and
  - determine whether any projected supply voltage value of the one or more projected supply voltage values is within a tolerance threshold of the corresponding bound value.

11. The apparatus of claim 10, wherein the prediction module is further configured to generate the switcher control signal with a digital bit value prompting a power amplifier switcher to use a voltage source path upon a determination that any of the one or more projected supply voltage values is within the tolerance threshold of the corresponding bound value.
12. The apparatus of claim 10, wherein the prediction module is further configured to generate a switcher control signal with a value prompting the power amplifier switcher to use a ground source path upon a determination that none of the one or more projected supply voltage values are within the tolerance threshold of the corresponding bound value.
13. The apparatus of claim 9, wherein the prediction module is further configured to: provide the switcher control signal to the power amplifier switcher.
14. The apparatus of claim 9, wherein the reception module is further configured to track a system state through one or more state register values, wherein the system includes a low pass filter and a PA.
15. The apparatus of claim 9, wherein the prediction module is further configured to: generate an predicted supply voltage from the one or more values associated with the input signal; and provide the predicted supply voltage to a predistortion module.
16. The apparatus of claim 15, wherein the reception module is further configured to buffer a plurality of consecutive sample values sufficient to allow at least one dominant peak to one trough of the input signal to be stored in the buffer.
17. An apparatus of communications, comprising:
  - means for buffering one or more values associated with an input signal;
  - means for predicting a system response to at least a portion of the one or more buffered values; and
  - means for generating a switcher control signal based on the system response.

18. The apparatus of claim 17, wherein the means for predicting the system response is configured to:

use a response function based on a system configuration to generate one or more projected supply voltage values, wherein the system includes a low pass filter and a PA;

compare each of the one or more projected supply voltage values with a corresponding bound value based at least in part on the buffered one or more values associated with the input signal; and

determine whether any projected supply voltage value of the one or more projected supply voltage values is within a tolerance threshold of the corresponding bound value.

19. The apparatus of claim 18, wherein the means for predicting the system response is configured to generate the switcher control signal with a digital bit value prompting a power amplifier switcher to use a voltage source path upon a determination that any of the one or more projected supply voltage values is within the tolerance threshold of the corresponding bound value.

20. The apparatus of claim 18, wherein the means for predicting the system response is configured to generate a switcher control signal with a value prompting the power amplifier switch to use a ground source path upon a determination that none of the one or more projected supply voltage values are within the tolerance threshold of the corresponding bound value.

21. The apparatus of claim 17, further comprising:  
means for providing the switcher control signal to the power amplifier switcher.

22. The apparatus of claim 17, wherein the means for buffering is further configured to track a system state through one or more state register values, wherein the system includes a low pass filter and a PA.

23. The apparatus of claim 17, wherein the means for predicting is further configured to:

generate a predicted supply voltage from the one or more values associated with the input signal; and

provide the predicted supply voltage to a predistortion module.

24. The apparatus of claim 23, wherein the means for buffering is further configured to receive a plurality of consecutive sample values sufficient to allow at least one dominant peak to one trough of the input signal to be stored in the buffer.

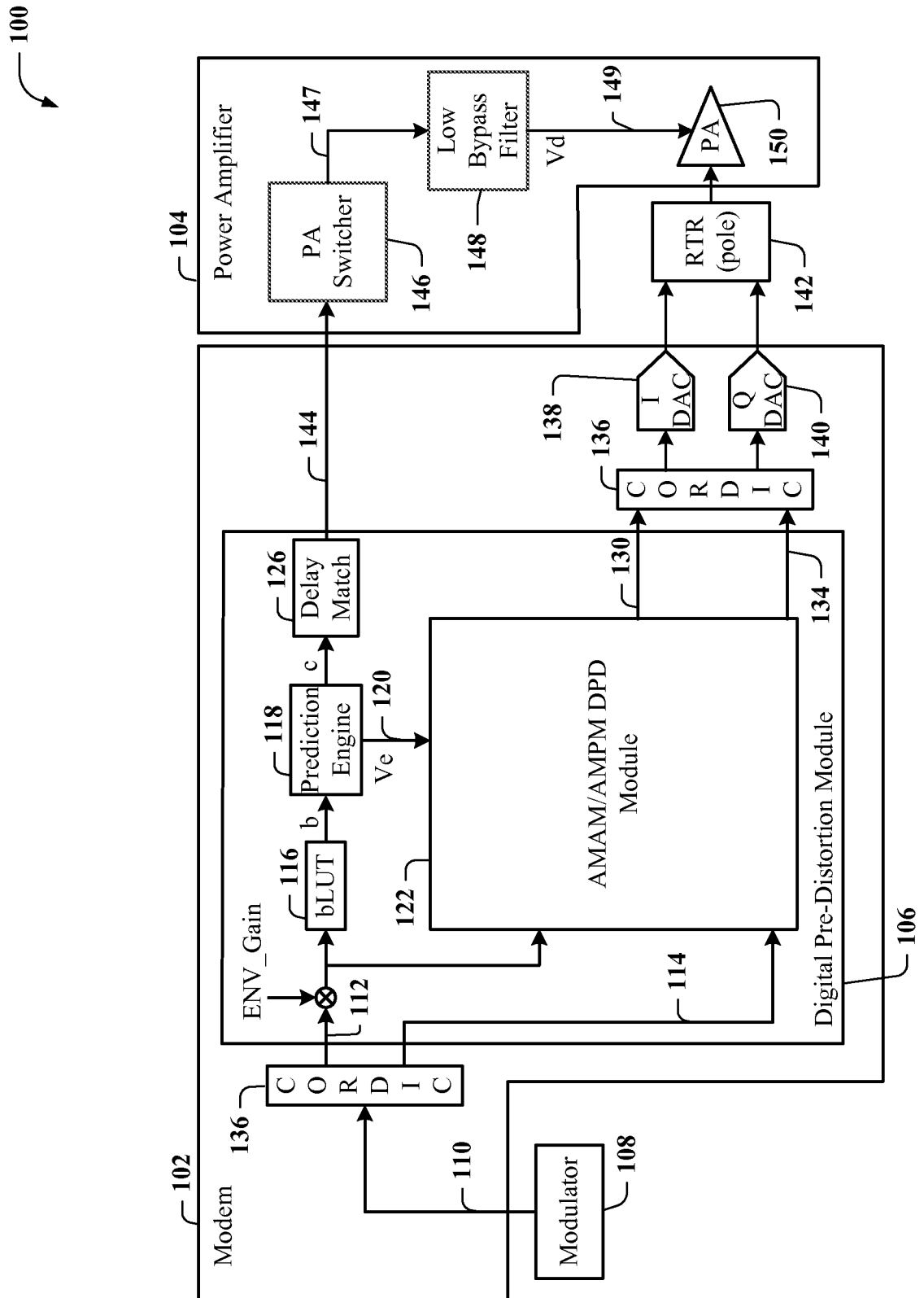
25. A computer program product comprising:

a computer-readable medium comprising code for:

receiving, into a buffer, one or more values associated with an input signal;

predicting a system response to at least a portion of the one or more buffered values; and

generating a switcher control signal based on the system response.



**FIG. 1**



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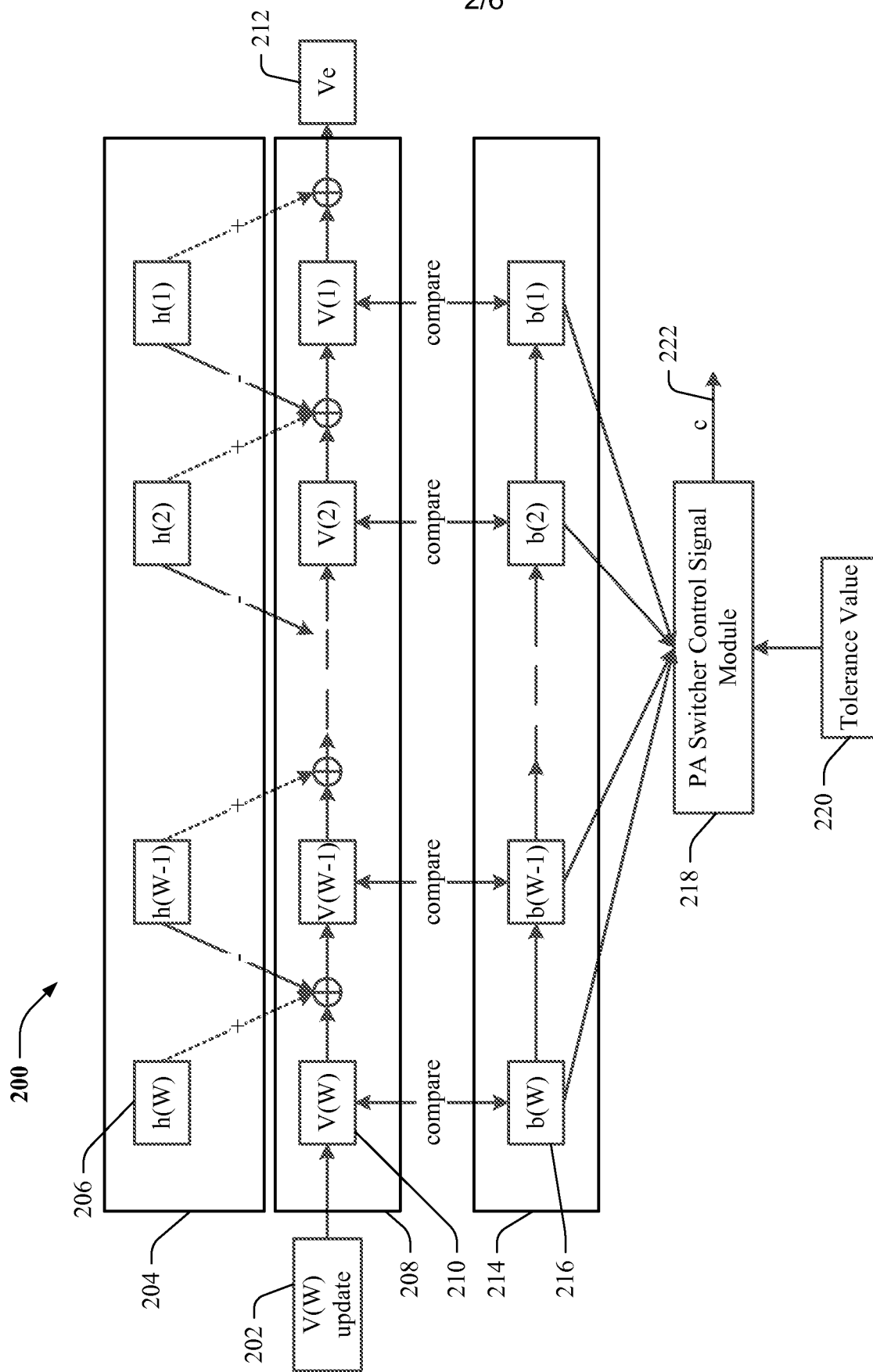


FIG. 2

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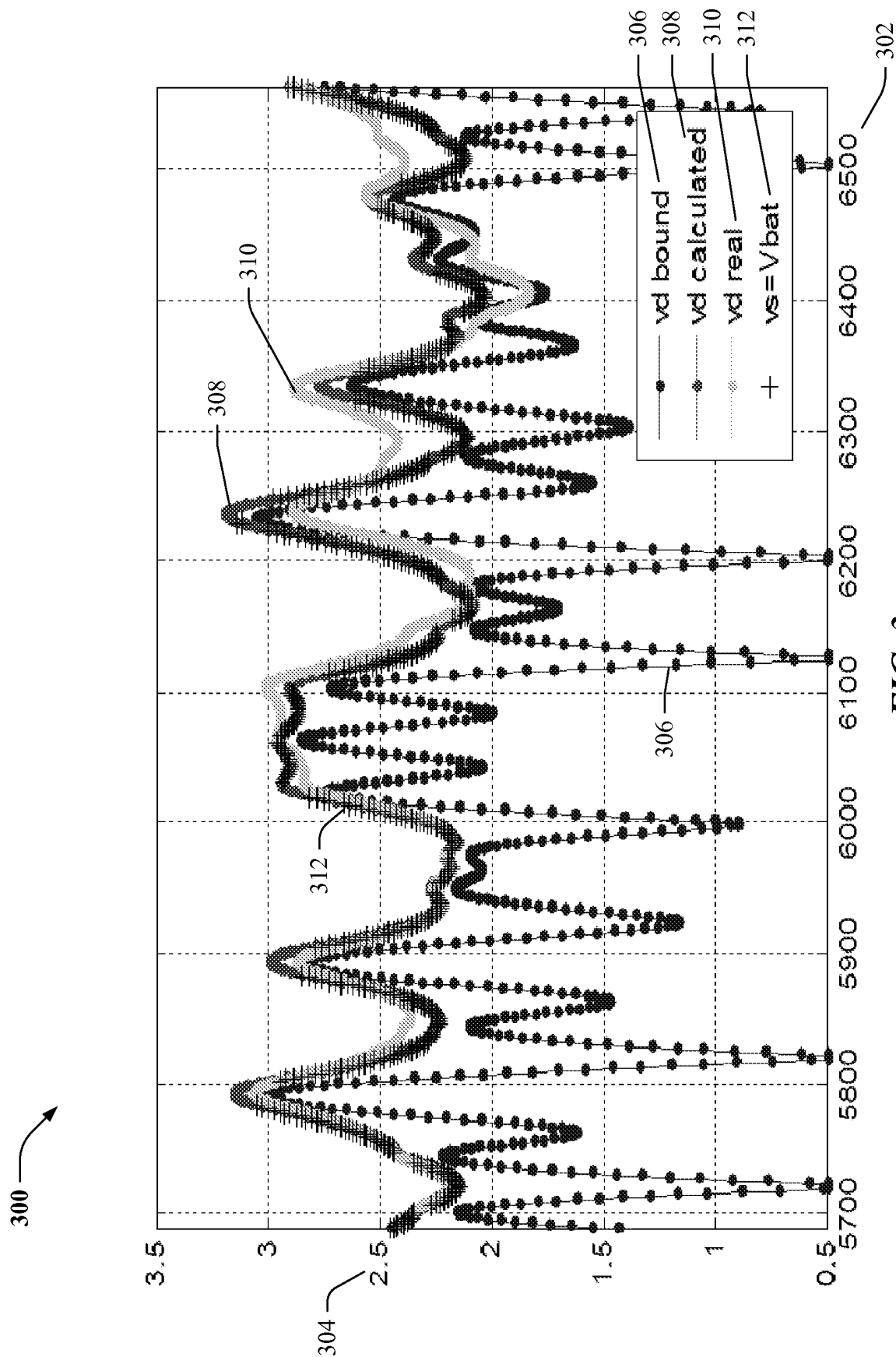
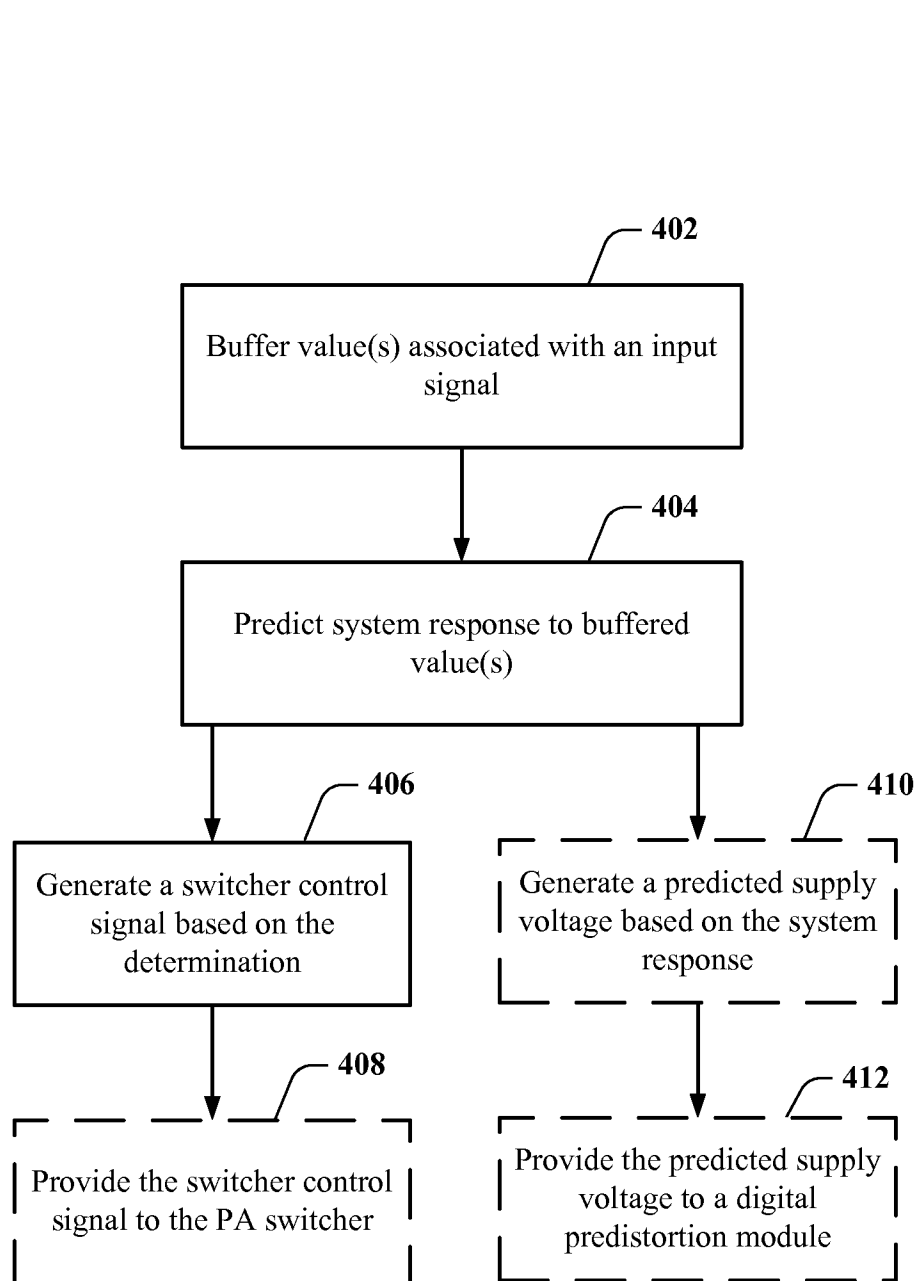
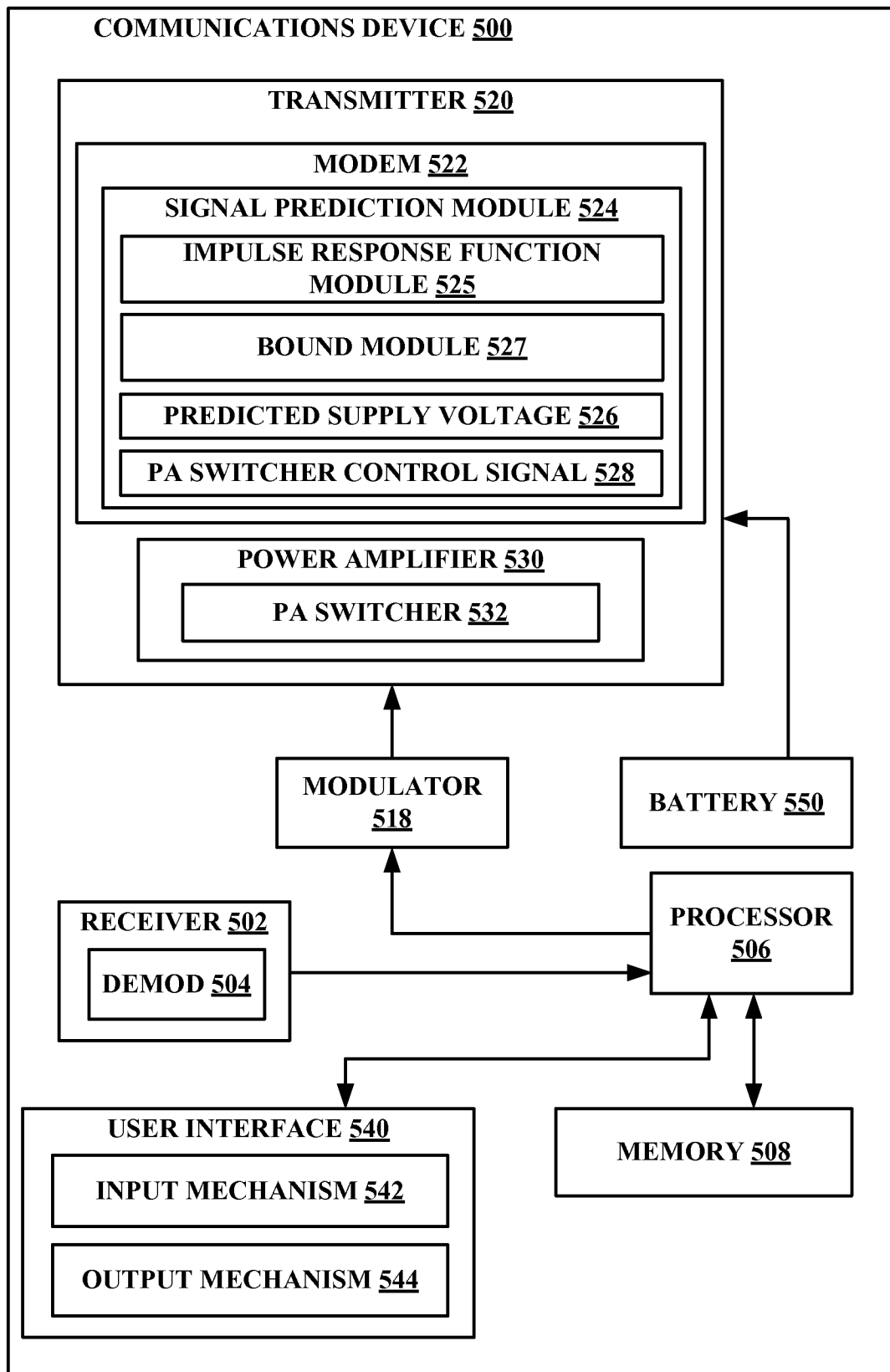


FIG. 3

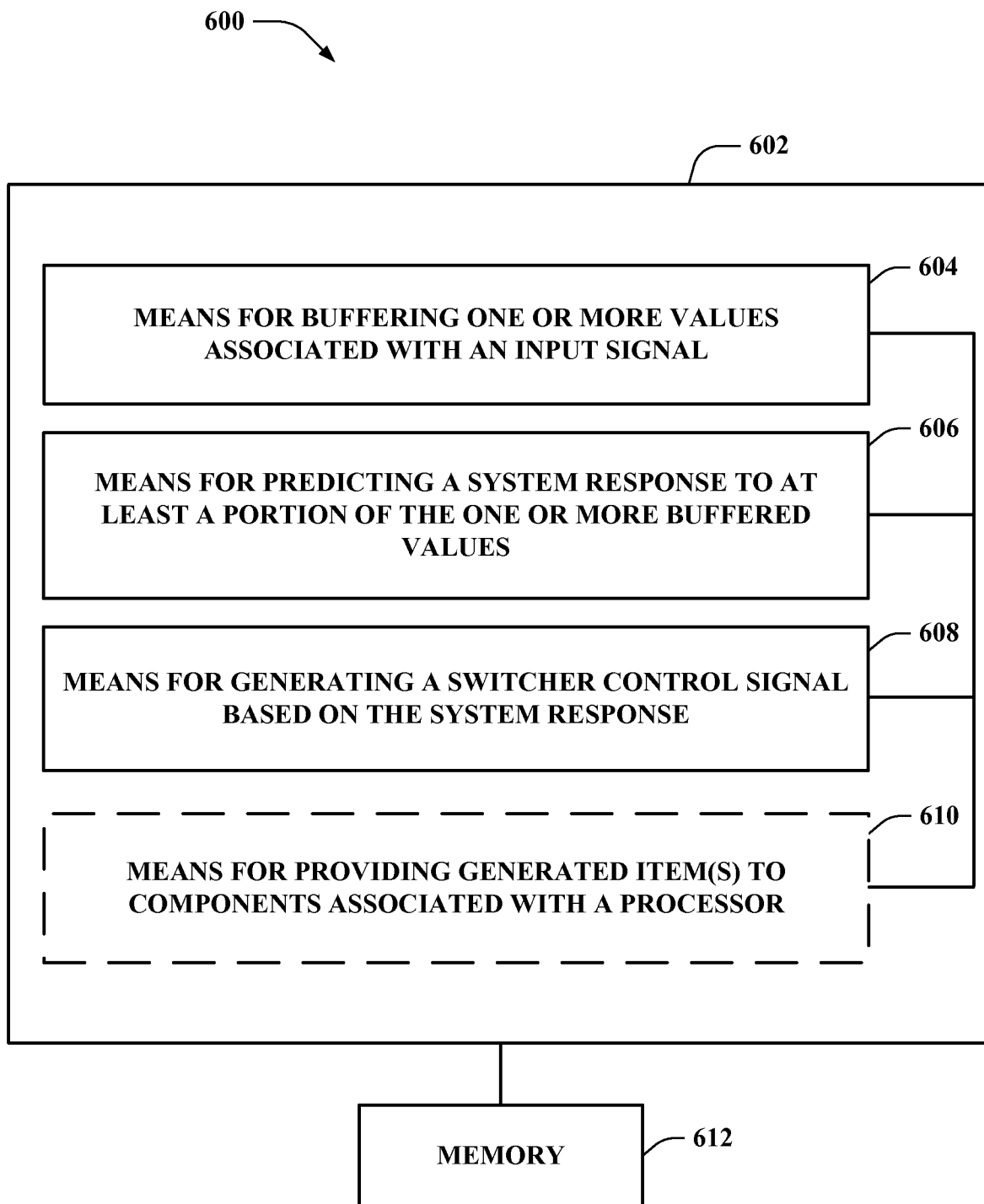
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**FIG. 4**

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**FIG. 5**

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**FIG. 6**

## INTERNATIONAL SEARCH REPORT

International application No  
PCT/US2013/064602

A. CLASSIFICATION OF SUBJECT MATTER  
INV. H03F1/02 H03F1/32 H04L27/36 H03F3/24  
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)  
H03F H04L H04B H03G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1 622 256 A1 (NORTEL NETWORKS LTD [CA]) 1 February 2006 (2006-02-01)	1,2, 5-10, 13-18, 21-25
A	paragraphs [0040] - [0117]; figures 1-10	3,4,11, 12,19,20
X	----- EP 1 811 651 A1 (FUJITSU LTD [JP]) 25 July 2007 (2007-07-25)	1,5-9, 13-17, 21-25
A	paragraphs [0015] - [0053]; figures 1,4,10,11	2-4, 10-12, 18-20
	----- -/-	



Further documents are listed in the continuation of Box C.



See patent family annex.

\* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

6 December 2013

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Name and mailing address of the ISA/

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Authorized officer

Fedi, Giulio

## INTERNATIONAL SEARCH REPORT

International application No

PCT/US2013/064602

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	paragraphs [0004] - [0056]; figures 1,2,3A,4A  -----	2-4,7,8, 10-12, 15,16, 18-20, 23,24

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Information on patent family members

International application No

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