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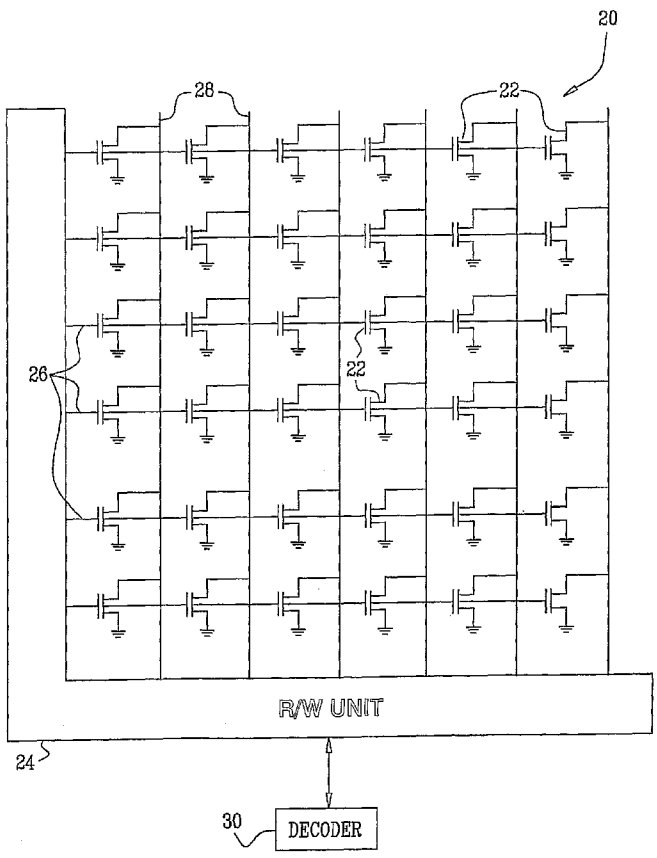
(54) Title: MEMORY CELL READOUT USING SUCCESSIVE APPROXIMATION



(57) Abstract: A method for operating a memory (20) includes storing analog values in an array of analog memory cells (22), so that each of the analog memory cells holds an analog value corresponding to at least first and second respective bits. A first indication of the analog value stored in a given analog memory cell is obtained using a first set of sampling parameters. A second indication of the analog value stored in the given analog memory cell is obtained using a second set of sampling parameters, which is dependent upon the first indication. The first and second respective bits are read out from the given analog memory cell responsively to the first and second indications.

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MEMORY CELL READOUT USING SUCCESSIVE APPROXIMATION

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the benefit of U.S. Provisional Patent Application 60/863,506, filed October 30, 2006, which is incorporated herein by reference.

FIELD OF THE INVENTION

The present invention relates generally to memory devices, and particularly to methods and systems for reading data from memory cells.

BACKGROUND OF THE INVENTION

Several types of memory devices, such as Flash memories, use arrays of analog memory cells for storing data. Each analog memory cell stores a quantity of an analog value, such as an electrical charge or voltage, which represents the information stored in the cell. In Flash memories, for example, each analog memory cell holds a certain amount of electrical charge. The range of possible analog values is typically divided into regions, each region corresponding to one or more data bit values. Data are written to an analog memory cell by writing a nominal analog value that corresponds to the desired bit or bits. The possible bit values that can be stored in an analog memory cell are also referred to as the memory states of the cell.

Some memory devices, commonly referred to as Single-Level Cell (SLC) devices, store a single bit of information in each memory cell, i.e., each memory cell can be programmed to assume one of two possible memory states. Higher-density devices, often referred to as Multi-Level Cell (MLC) devices, can be programmed to assume more than two possible memory states and thus store two or more bits per memory cell. Various methods are known in the art for reading out the multi-bit data that are stored in such cells.

For example, U.S. Patent 6,317,364, whose disclosure is incorporated herein by reference, describes a multi-state memory, which is said to use a flexible, self-consistent and self-adapting mode of detection, covering a wide dynamic range. In one embodiment, cells of the memory are read using a control gate in a binary search. The readout uses a sensing circuit consisting of a sense amplifier comparator, with one input lead that receives an input signal from the memory cell and another that receives a reference signal. The output of the comparator is used to update a Control Gate Register Element. The value stored in this element is used to provide the next control gate read voltage.

Takeuchi et al. suggest another cell readout technique in "A Multipage Cell Architecture for High-Speed Programming Multilevel NAND Flash Memories," *IEEE Journal of Solid-State Circuits* **33**:8 (1998), pages 1228-1238, which is incorporated herein by reference. The authors describe a cell that contains two "pages," meaning that the two bits in the cell are programmed in different operations. The cell is read using a four-level column latch circuit, which is shared by two bit lines. The read operation is composed of three phases, during which the word line control gate voltage is set to three different bias values. As a result of this operation, the first and second page data in the cell are read out on the cell bit line and latched in first and second latches, respectively, of the latch circuit.

SUMMARY OF THE INVENTION

An embodiment of the present invention provides a method for operating a memory, including:

storing analog values in an array of analog memory cells, so that each of the analog memory cells holds an analog value corresponding to at least first and second respective bits, the array including word lines and bit lines connected to the analog memory cells;

obtaining a first indication of the analog value stored in a given analog memory cell by precharging a bit line connected to the given analog memory cell to a first precharge voltage, and then sampling a first current on the bit line;

obtaining a second indication of the analog value stored in the given analog memory cell by precharging the bit line connected to the given analog memory cell to a second precharge voltage, which is dependent upon the first indication, and then sampling a second current on the bit line; and

reading out the first and second respective bits from the given analog memory cell responsively to the first and second indications.

Typically, the first indication is indicative of the first respective bit stored in the given analog memory cell, and the second indication is indicative of the second respective bit stored in the given analog memory cell. In disclosed embodiments, reading out the first and second respective bits includes reading out the first respective bit prior to sampling the second current. In one embodiment, the first respective bit belongs to a first page of data, and the second respective bit belongs to a second page of data, and the method includes using the first

respective bit read out from the given analog memory cell to decode the first page of the data while obtaining the second indication.

In some embodiments, sampling the first current includes comparing the first current to a predetermined threshold. Typically, precharging the bit line connected to the given analog memory cell to the second precharge voltage includes setting the second precharge voltage to a first level when the first current is below the predetermined threshold, and setting the second precharge voltage to a second level, greater than the first level, when the first current is above the predetermined threshold. In one embodiment, the predetermined threshold is a first threshold, and sampling the second current includes comparing the second current to a second threshold, which is different from the first threshold.

In a disclosed embodiment, obtaining a third indication of the analog value stored in the given analog memory cell by precharging the bit line connected to the given analog memory cell to a third precharge voltage, which is dependent upon at least the second indication, and then sampling a third current on the bit line, and reading out at least a third bit from the given analog memory cell responsively to the third indication.

Additionally or alternatively, the memory includes decoding data including at least one of the first and second respective bits that have been read out from the given analog memory cell, and upon occurrence of a failure in decoding the data, obtaining a third indication of the analog value stored in the given analog memory cell using a set of sampling parameters that is dependent upon at least the second indication, and then decoding the data using the third indication together with at least one of the first and second indications.

Typically, sampling the first current includes applying a predetermined control voltage to a word line connected to the given analog memory cell in order to cause the given analog memory cell to conduct the first current, and sampling the second current includes applying the same predetermined control voltage to the word line connected to the given analog memory cell in order to cause the given analog memory cell to conduct the second current.

Optionally, sampling the first current includes sampling the first current on the bit line after a first delay, and sampling the second current includes sampling the second current on the bit line after a second delay, which is dependent upon the first indication.

There is also provided, in accordance with an embodiment of the present invention, a method for operating a memory, including:

storing analog values in an array of analog memory cells, so that each of the analog memory cells holds an analog value corresponding to at least first and second respective bits, the array including word lines and bit lines connected to the analog memory cells;

obtaining a first indication of the analog value stored in a given analog memory cell by precharging a bit line connected to the given analog memory cell, and then sampling a first current on the bit line after a first delay;

obtaining a second indication of the analog value stored in the given analog memory cell by precharging the bit line connected to the given analog memory cell, and then sampling a second current on the bit line after a second delay, which is dependent upon the first indication; and

reading out the first and second respective bits from the given analog memory cell responsively to the first and second indications.

In a disclosed embodiment, sampling the first current includes comparing the first current to a predetermined threshold, and sampling the second current includes setting the second delay to a first delay time when the first current is below the predetermined threshold, and setting the second delay to a second delay time, greater than the first delay time, when the first current is above the predetermined threshold.

There is additionally provided, in accordance with an embodiment of the present invention, a method for operating a memory, including:

storing analog values in a group of analog memory cells, so that each of the analog memory cells holds an analog value corresponding to at least first and second respective bits belonging respectively to first and second pages of data;

obtaining a first indication of the analog value stored in a given analog memory cell by sampling the given analog memory cell using a first set of sampling parameters, wherein the first indication is indicative of the first respective bit stored in the given analog memory cell;

obtaining a second indication of the analog value stored in the given analog memory cell by sampling the given analog memory cell using a second set of sampling parameters, which is dependent upon the first indication, wherein the second indication is indicative of the second respective bit stored in the given analog memory cell; and

reading out the first bit from the given analog memory cell responsively to the first indication, and decoding the first page of the data using the first bit while obtaining the second indication.

In one embodiment, the method includes, upon occurrence of a failure in decoding one of the pages of the data, obtaining a third indication of the analog value stored in the given analog memory cell using a third set of sampling parameters that is dependent upon at least the second indication, and then decoding the one of the pages using the third indication together with at least one of the first and second indications.

There is further provided, in accordance with an embodiment of the present invention, memory apparatus, including:

an array of analog memory cells, which are configured to store analog values so that each of the analog memory cells holds an analog value corresponding to at least first and second respective bits, the array including word lines and bit lines connected to the analog memory cells; and

readout circuitry, which is connected to the word lines and the bit lines and is configured to obtain first and second indications of the analog value stored in the given memory cell by precharging a bit line connected to the given analog memory cell to a first precharge voltage and then sampling a first current on the bit line so as to obtain the first indication, and precharging the bit line connected to the given analog memory cell to a second precharge voltage, which is dependent upon the first indication, and then sampling a second current on the bit line so as to obtain the second indication, and which is configured to read out the first and second respective bits from the given analog memory cell responsively to the first and second indications.

There is moreover provided, in accordance with an embodiment of the present invention, memory apparatus, including:

an array of analog memory cells, which are configured to store analog values so that each of the analog memory cells holds an analog value corresponding to at least first and second respective bits, the array including word lines and bit lines connected to the analog memory cells; and

readout circuitry, which is connected to the word lines and the bit lines and is configured to obtain first and second indications of the analog value stored in the given

memory cell by precharging a bit line connected to the given analog memory cell and then sampling a first current on the bit line after a first delay so as to obtain the first indication, and precharging the bit line connected to the given analog memory cell and then sampling a second current on the bit line after a second delay, which is dependent upon the first indication, so as to obtain the second indication, and which is configured to read out the first and second respective bits from the given analog memory cell responsively to the first and second indications.

There is furthermore provided, in accordance with an embodiment of the present invention, memory apparatus, including:

a group of analog memory cells, which are configured to store analog values so that each of the analog memory cells holds an analog value corresponding to at least first and second respective bits belonging respectively to first and second pages of data;

readout circuitry, which is coupled to the analog memory cells and is configured to obtain a first indication of the analog value stored in a given analog memory cell by sampling the given analog memory cell using a first set of sampling parameters, wherein the first indication is indicative of the first respective bit stored in the given analog memory cell, and to obtain a second indication of the analog value stored in the given analog memory cell by sampling the given analog memory cell using a second set of sampling parameters, which is dependent upon the first indication, wherein the second indication is indicative of the second respective bit stored in the given analog memory cell; and

a decoder, which is coupled to receive the first bit from the readout circuitry and to decode the first page of the data using the first bit while the readout circuitry is obtaining the second indication.

The present invention will be more fully understood from the following detailed description of the embodiments thereof, taken together with the drawings in which:

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram that schematically illustrates a memory cell array, in accordance with an embodiment of the present invention;

Fig. 2 is a diagram that schematically illustrates memory states of the cells in the array of Fig. 1, in accordance with an embodiment of the present invention;

Fig. 3 is a block diagram that schematically shows details of a readout circuit for reading data from memory cells, in accordance with an embodiment of the present invention;

Fig. 4 is a timing diagram that schematically shows signals involved in reading out bits stored in a memory cell, in accordance with an embodiment of the present invention;

Fig. 5 is a timing diagram that schematically shows signals used in reading out bits from a memory cell using a method of successive approximation, in accordance with an embodiment of the present invention;

Fig. 6 is a timing diagram that schematically shows signals used in reading out bits from a memory cell using a method of successive approximation, in accordance with another embodiment of the present invention; and

Fig. 7 is a flow chart that schematically illustrates a method for parallel reading and decoding of data stored in a memory array, in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS

OVERVIEW

The embodiments of the present invention that are described hereinbelow provide improved methods and apparatus for reading data from analog memory cells, such as MLC Flash memory cells. These embodiments typically use a sequence of steps of successive approximation in order to determine the analog value stored in a given cell and thus read out the corresponding bits. The first step uses a certain set of sampling parameters to determine whether the analog value is in the upper or lower range of possible values. In the next step, one or more of the sampling parameters are modified, depending upon the results of the first step, in order to determine whether the analog value is in the upper or lower part of whichever range was identified in the first step. This process may be repeated until the actual analog value stored in the cell has been determined, and the bits in the cell have thus been read out.

In order to read the analog value stored in a given analog memory cell, the bit line that is connected to the cell is typically precharged to a certain precharge voltage, and the current that subsequently flows through the bit line is sampled. This sampled current is compared to a predetermined threshold in order to determine whether the analog value is in the upper or lower part of the range. A certain control voltage is applied to the word line that is connected to the given analog memory cell in order to cause the given analog memory cell to conduct the

current. The methods of controlling and varying the sampling parameters that are described hereinbelow, however, are not dependent on varying this control voltage (which is commonly referred to in Flash memories as the control gate voltage), and a constant control gate voltage may be used in all of the sampling steps.

In some of the disclosed embodiments, the precharge voltage that is applied to the bit line in the second and subsequent steps of the readout process depends upon the indication of the analog value that was obtained in the previous step. For example, if the first step of the process indicated that the analog value is in the upper part of the range, the precharge in the second step may then be set to a higher voltage than if the analog value had been indicated to be in the lower part of the range.

The current flowing through the bit line decays over time following application of the precharge and control gate voltage. (As a result, the choice of the threshold depends on the sampling delay, and *vice versa*.) The rate of decay of the bit line current depends on the analog value that is stored in the cell. Therefore, in some embodiments of the present invention, the sampling delay that is used in the second and subsequent steps of the readout process depends upon the indication of the analog value that was obtained in the previous step.

The techniques noted above for control of precharge and of sampling delay may be used individually, or they may alternatively be combined, with variation applied to both the precharge and the sampling delay depending on results of the previous step. Alternatively or additionally, other sampling parameters, such as the comparison threshold, may be varied from step to step along with the precharge and/or sampling delay.

Typically, the analog value that is stored in each cell corresponds to a set of two or more bits of data that are stored in the cell, and the indication of the analog value that is obtained in each of the successive approximation steps may be indicative of a different bit in the set. The data may be stored in the array so that each of the bits in a given cell belongs to a different page of data. In this case, each bit may be read out of a given cell prior to the sampling step that will yield the next bit, and may be used in decoding the page of data to which the bit belongs while the successive approximation of the succeeding bit or bits is still in progress.

MEMORY ARRAY STRUCTURE AND SYSTEM DESCRIPTION

Fig. 1 is a block diagram that schematically illustrates a MLC memory cell array 20, in accordance with an embodiment of the present invention. Although Fig. 1 refers to Flash memory cells that are connected in a particular array configuration, the principles of the present invention are applicable to other types of memory cells and other array configurations, as well.

Memory cells 22 of array 20 are arranged in a grid having multiple rows and columns. Each cell 22 comprises a floating gate Metal-Oxide Semiconductor (MOS) transistor. A certain amount of electrical charge (electrons or holes) can be stored in a particular cell by applying appropriate voltage levels to the transistor gate, source and drain. The amount of charge corresponds to the analog value that is stored in the cell, which is indicative of the data bits that are stored in the cell. In the exemplary configuration of Fig. 1, the gates of the transistors in each row are connected by word lines 26, while the sources of the transistors in each column are connected by bit lines 28. In some embodiments, such as in some NOR cell devices, the sources are connected to the bit lines directly. In alternative embodiments, such as in some NAND cell devices, the bit lines are connected to strings of floating-gate cells.

The source-drain resistance of each cell 22 depends on the amount of charge stored in the cell. This resistance may be estimated by applying a control voltage to the gate of the transistor and measuring the current flowing between the source and drain. For this purpose, a read/write (R/W) unit 24 precharges bit line 28 to which the cell is connected and then applies the control voltage to word line 26 of the cell. Unit 24 then samples the current flowing through the bit line in order to determine the analog value that is stored in the cell in a process of successive approximation, as explained in detail hereinbelow.

The memory cell array is typically divided into multiple pages, i.e., groups of memory cells that are programmed and read simultaneously. In some embodiments, each page comprises an entire row of the array. In other embodiments, each row (word line) can be divided into two or more pages. Typically, unit 24 reads a group of cells, such as an entire row, simultaneously. Alternatively, unit 24 may implement any other suitable read/write architecture. For the sake of convenience and clarity, however, the description that follows will relate generally to reading of individual cells, on the understanding that the techniques and circuits that are described hereinbelow may be extended in a straightforward manner to parallel readout of multiple cells.

Data stored in array 20 are read out by R/W unit 24 to a decoder 30. The decoder may be located either on the same integrated circuit chip as array 20 or in a separate processing and control device. The decoder may implement, *inter alia*, memory signal processing functions of the types described, for example, in PCT Patent Application PCT/IL2007/000580[DK1], filed May 10, 2007, which is assigned to the assignee of the present patent application and whose disclosure is incorporated herein by reference. These functions may include distortion estimation and application of error correcting codes to the values read out of array 20.

Fig. 2 is a diagram that schematically illustrates memory states 36 of cells 22 in array 20, in accordance with an embodiment of the present invention. In this example, it is assumed that array 20 stores three bits per cell, but the principles of the present invention may equally be applied to memories that store any other practical number of bits per cell. Each state 36 corresponds to a certain analog value, in the form of charge (or equivalently voltage levels) that is stored in the cell in question. In practice, the actual stored analog values in cells 22 that correspond to a given state 36 spread statistically over a range of values, as is illustrated by the curves corresponding to the states in Fig. 2. Read/write unit 24 reads the state of a given cell by determining whether the charge or voltage stored in the cell is above or below each of a set of successive thresholds, as described further hereinbelow.

Each state 36 represents a different set of bit values, which are marked as three-digit binary numbers on the respective states in Fig. 2. The top bit in each state will be referred to hereinbelow, for the sake of convenience, as the most significant bit (MSB), and bottom bit will be referred to as the least significant bit (LSB), with the middle bit in between. In many MLC memory devices, the MSB, middle bit, and LSB all belong to different pages of data, which are written in succession to a given row of cells. By convention, the LSB is written first, followed by the middle bit, and then finally by the MSB, and erased cells have the default value "111".

Various coding schemes may be used to assign the eight possible sets of bit values to states 36. In the scheme shown in Fig. 2, the four lower-voltage states have LSB=1, while the four upper-voltage states have LSB=0. Thus, the LSB determines whether the cell in question will have an analog value in one of two ranges, either above or below a central threshold ΔV. The middle bit then determines whether the cell will have an analog value in the upper or lower sub-range of the range associated with the LSB. In other words, the combination of the LSB

and middle bit defines four sub-ranges. Finally, the MSB determines whether the analog value of the cell will be in the upper state or the lower state of the two states contained in the sub-range defined by the middle bit. This scheme permits the LSB, middle bit, and MSB to be read out, in that order, by a process of successive approximation of the cell voltage that is explained hereinbelow.

READOUT CIRCUIT AND METHOD FOR SUCCESSIVE APPROXIMATION

Fig. 3 is a block diagram that schematically shows details of a readout circuit that may be used in R/W unit 24 for reading data from memory cells 22, in accordance with an embodiment of the present invention. Typically, the readout circuit (along with other components of the R/W unit) is fabricated on the same integrated circuit chip as the array of memory cells. Alternatively, certain elements of the readout circuit may be located on a separate memory controller chip. Although Fig. 3 shows the readout circuit as being connected only to a single memory cell, in practice the readout circuit typically serves an entire column of cells that are connected to a common bit line 28 (wherein word lines 26 are controlled to select the cell that is to be read out at any given time). Alternatively or additionally, the readout circuit may be time-multiplexed among multiple columns of cells in order to save space on the chip.

To read out the analog value stored in cell 22, a bit line voltage (V_{BL}) generator 40 precharges bit line 28 to a certain precharge voltage V1, which may be varied by a controller 48. For example, generator 40 may comprise a current generator, which applies a constant current for a certain period of time. The magnitude of the current and/or the length of the period of time is chosen by the controller in order to give the desired precharge voltage. R/W unit 24 applies a control gate voltage to word line 26, which causes a current to flow (and gradually decay) in bit line 28. A sense amplifier 44 compares the bit line current to a constant reference current (I_{REF}) provided by a current generator 42. (Alternatively, the sense amplifier may compare the bit line voltage to a reference voltage.) The output of amplifier 44 is recorded by a latch 46 at a sampling time that is specified by controller 48. If the bit line current is greater than I_{REF} at the specified sampling time, for example, the latch records a logical "0" and otherwise records a logical "1".

Fig. 4 is a timing diagram that schematically shows signals involved in reading out bits stored in cell 22 using the circuit of Fig. 3, in accordance with an embodiment of the present

invention. V_{BL} generator 40 outputs a precharge voltage pulse (VG) starting at time T_0, with an amplitude A that is determined by controller 48. The word line (WL) control gate voltage is applied to word line 26 at time T_1, after the precharge is complete. During the precharge pulse, the bit line current (BL) increases, and then it begins to decay upon application of the control gate voltage on the word line. (Although Fig. 4 shows bit line current, the bit line voltage behaves in the same manner.) The rate of decay depends, as noted above, on the source-drain resistance of cell 22, which in turn depends on the analog value stored in the cell.

Controller 48 applies a sampling pulse (SAMP) to latch 46 at time T_S following T_1, thus causing the latch to record a digital value LAT corresponding to the present output of sense amplifier 44. If the bit line current (which depends, of course, on the bit line voltage) is above the threshold value I_{TH} at T_S, the latch records a 0. In the example shown in Fig. 4, the bit line current has dropped below the threshold at T_S, and the latch will therefore record a 1. Each latched value corresponds to one of the bits stored in cell 22, which is then read out of array 20 for subsequent processing (possibly by decoder 30 – Fig. 1).

Controller 48 drives V_{BL} generator 40 and latch 46 to determine the analog value that is stored in cell 22 in a process of successive approximation. This process may take place both when data are to be read out of cells 22 and to verify that data have been written to the cells correctly, in a program-and-verify operation. In each step of the process, the controller may modify one or more sampling parameters, including the precharge voltage V1 or the sampling time SAMP, or both. In addition, the controller may optionally modify I_{TH} and may also control the word line voltage WL, although it is not necessary to control either I_{TH} or WL for the successive approximation method that is described herein.

In the first step of successive approximation of the analog value in a given cell 22, controller 48 typically has no information regarding the state of the cell, i.e., the cell could be in any one of states 36 (Fig. 2). Therefore, the controller uses preset values of V1 and SAMP, which are chosen so as to distinguish between the upper set of states (voltage above ΔV in Fig. 2) and the lower set (below ΔV). The resultant latch value, LAT1, indicates whether the cell voltage is in the upper or lower range, and thus whether the LSB stored in the cell is 0 or 1. The LSB may be output by R/W unit 24 (to decoder 30 or to a host processor – not shown) prior to or in parallel with the next steps of the successive approximation.

Based on LAT1, controller 48 selects the value of V1 and/or SAMP to be used in the next step. The rationale for and results of this selection are explained below with reference to Figs. 5 and 6. Typically, at least one of the sampling parameters (V1 and/or SAMP) is set to a different value in the next step from its value in the first step. Using this new parameter value, latch 46 records a new latch value, LAT2, which indicates whether the middle bit stored in the cell is 0 or 1. In the three-bit-per-cell example shown above, the controller finally uses the value LAT2, as well as LAT1, in setting the sampling parameter values for the third step of approximation, and thus latches and reads out the MSB. The middle bit may be read out prior to or in parallel with the approximation step that is used to find the MSB. Optionally, for purposes of error correction, the controller may drive a further step of even finer approximation, as described hereinbelow with reference to Fig. 7.

Controller 48 may comprise a hard-wired logic circuit, which selects and outputs the appropriate values of V1 and/or SAMP at each point in the process of successive approximation. Alternatively, the controller may comprise a programmable processing component, which may also perform other control and processing functions, or a combination of hard-wired and programmable elements. In one embodiment, the controller uses a look-up table (LUT) to determine the values of sampling parameters based on the previous latch values. The controller may be configured to drive and control a single readout circuit, as shown in Fig. 3, or it may alternatively control multiple readout circuits in parallel, thus serving multiple bit lines of array 20.

Fig. 5 is a timing diagram that schematically shows signals used in reading out bits stored in memory cell 22 using successive approximation with varying bit line precharge, in accordance with an embodiment of the present invention. This diagram assumes that the first successive approximation step has been completed and has yielded a certain latch value LAT1, corresponding to the LSB stored in the cell. Depending on LAT1, controller 48 sets the precharge voltage VG that is to be applied to bit line 28 in the next approximation step to one of two possible values: A1 if LAT1 = 1, or A2 if LAT1 = 0. Referring to Fig. 2, A1 is chosen to distinguish between the two sub-ranges below ΔV, while A2 is chosen to distinguish between the two sub-ranges above ΔV.

When LAT1 = 1 and precharge A1 is applied by V_{BL} generator 40, the bit line voltage will decay after time T1 roughly along a curve 50 if the middle bit of cell 22 has the value 1; or

roughly along a curve 52 if the middle bit has the value 0. At time T_S, when latch 46 is triggered, curve 50 is below the threshold I_{TH}, whereas curve 52 is above the threshold. Thus, decay along curve 50 will yield a new latch value LAT2 = 1, corresponding to the two lowest states (111 and 011 in Fig. 2) whereas curve 52 will yield LAT2 = 0, corresponding to the two upper states in the lower range (001 and 101). (In fact, each of the four states below ΔV will give its own decay curve, with the two curves due to states 111 and 011 below I_{TH} at T_S, and the other two curves above, but only curves 50 and 52 are shown in Fig. 5 for the sake of simplicity.)

On the other hand, when LAT1 = 0 and the greater precharge A2 is applied, the bit line voltage will decay roughly along a curve 54 if the middle bit has the value 0, and roughly along a curve 56 if the middle bit has the value 1. In other words, curve 54 will yield LAT2 = 1, corresponding to states 100 and 000, while curve 56 will yield LAT2 = 0, corresponding to states 010 and 110. (In this case, because of the coding scheme used in Fig. 2, the value of the middle bit is complementary to the latched value.)

The values of LAT1 and LAT2 are then used by controller 48 in a similar fashion to determine the precharge voltage levels that will be applied in approximating the MSB.

Fig. 6 is a timing diagram that schematically shows signals used in reading out bits stored in memory cell 22 using successive approximation with varying sampling delay, in accordance with another embodiment of the present invention. In this case, it is assumed that the precharge voltage VG (not shown in Fig. 6) is constant in successive steps of the approximation, and only the sampling time changes based on the previous latch value. Curves 60, 62, 64 and 66 correspond to the decay of bit line voltage in four different states (or groups of states) of cell 22. Thus, for example, curve 60 could correspond to the average decay of states 111 and 011 in Fig. 2, curve 62 to states 001 and 101, curve 64 to states 100 and 000, and curve 66 to states 010 and 110. In actuality, as explained above, there will be eight different curves, corresponding to the eight different states of the cell, which are resolved in three steps of successive approximation.

In the embodiment illustrated by Fig. 6, controller 48 initially sets the sampling time SAMP to a delay T_{S1}. At this sampling time, curves 60 and 62 are below I_{TH}, and thus will give LAT1 = 1, whereas curves 64 and 66 are above I_{TH}, and thus will give LAT1 = 0. Assuming LAT1 = 0, controller 48 increases the sampling time for the next step to T_{S2}. At

this greater sampling time, curve 64 will give LAT2 = 1, whereas curve 66 will give LAT2 = 0. On the other hand, if LAT1 = 0, controller 48 will decrease the sampling time in order to distinguish between curves 60 and 62.

SUCCESSIVE APPROXIMATION INTERLEAVED WITH DECODING

Fig. 7 is a flow chart that schematically illustrates a method for parallel reading and decoding of data stored in memory array 20, in accordance with an embodiment of the present invention. This method is again described on the assumption that cells 22 of array 20 each can store three bits, but the principles embodied in the method may similarly be applied to any suitable sort of MLC analog memory.

R/W unit 24 reads out the LSB from each of a group of cells 22, at a LSB reading step 70. In the case of Flash memory, the set of bits that is read out at step 70 may conveniently constitute a page of data. Unit 24 performs the readout using the method of successive approximation that is defined hereinabove, whereby the LSB is read out of each cell before the approximation of the middle bit has been completed. The R/W unit subsequently reads out the middle bit and the MSB of each cell, in middle bit reading and MSB reading steps 72 and 74, respectively.

Decoder 30 decodes the page (or other group) of LSB data, at a LSB decoding step 80. For example, if the page contains an error correcting code (ECC), the decoder may perform error correction to recover the actual data word encoded in the page, as described in the above-mentioned PCT Patent Application PCT/IL2007/000580. This decoding step may take place in parallel with reading step 72. Similarly, decoder 30 may decode the page of middle-bit data, at a middle bit decoding step 82, in parallel with reading step 74. The page of MSB data is decoded subsequently, at a MSB decoding step 84.

In some cases, the decoder may not be able to successfully decode one (or more) of the pages of data at step 80, 82 or 84. This sort of failure may occur, for example, when distortion causes the readout errors too severe for the ECC to correct. (In the example shown in Fig. 7, it is assumed that the failure occurred in decoding the MSB page, but the approach described below may be applied to any of the pages.) In such cases, controller 48 may invoke an additional approximation step 76. At this step the sampling parameters (such as the precharge voltage, sampling delay and/or threshold) may be adjusted to intermediate values, between the values that were used at step 74, and the sampling process described above may be repeated.

These intermediate values of the sampling parameters are not necessarily in the middle of the intervals between the previous values, but may rather be set at any point between the previous values. It may be advantageous, in fact, to choose intermediate values that are near certain previous values in order to give enhanced resolution in the vicinity of the boundaries between states 36 (Fig. 2).

The combined results of steps 74 and 76 effectively provide a readout of the analog value in cell 22 with enhanced resolution – sixteen resolution levels, rather than just eight. The high-resolution readout results of step 76 may then be used to determine the correct MSB data in a soft decoding process, at a soft decoding step 86. This sort of soft decoding is described, for example, in the above-mentioned PCT Patent Application PCT/IL2007/000580 or in another PCT patent application, filed on even date, entitled, "Reading Memory Cells Using Multiple Threshold[DK2]s," which is assigned to the assignee of the present patent application, and whose disclosure is incorporated herein by reference.

As noted earlier, although step 86 refers specifically to decoding of the MSB data, this same sort of high-resolution soft decoding may equally be applied to the LSB or middle bit data. As another alternative, multiple pages may be jointly coded with an ECC, and then jointly decoded using the high-resolution results provided by step 76.

Although array 20 is described above, for the sake of convenience and clarity, as comprising certain types of Flash memory cells 22, with associated circuits in a particular configuration, the principles of successive approximation that are embodied in array 20 may similarly be applied to memory devices and systems of other types. It will thus be appreciated that the embodiments described above are cited by way of example, and that the present invention is not limited to what has been particularly shown and described hereinabove. Rather, the scope of the present invention includes both combinations and subcombinations of the various features described hereinabove, as well as variations and modifications thereof which would occur to persons skilled in the art upon reading the foregoing description and which are not disclosed in the prior art.

CLAIMS

1. A method for operating a memory, comprising:

storing analog values in an array of analog memory cells, so that each of the analog memory cells holds an analog value corresponding to at least first and second respective bits, the array comprising word lines and bit lines connected to the analog memory cells;

obtaining a first indication of the analog value stored in a given analog memory cell by precharging a bit line connected to the given analog memory cell to a first precharge voltage, and then sampling a first current on the bit line;

obtaining a second indication of the analog value stored in the given analog memory cell by precharging the bit line connected to the given analog memory cell to a second precharge voltage, which is dependent upon the first indication, and then sampling a second current on the bit line; and

reading out the first and second respective bits from the given analog memory cell responsively to the first and second indications.

2. The method according to claim 1, wherein the first indication is indicative of the first respective bit stored in the given analog memory cell, and the second indication is indicative of the second respective bit stored in the given analog memory cell.

3. The method according to claim 2, wherein reading out the first and second respective bits comprises reading out the first respective bit prior to sampling the second current.

4. The method according to claim 3, wherein the first respective bit belongs to a first page of data, and the second respective bit belongs to a second page of data, and wherein the method comprises using the first respective bit read out from the given analog memory cell to decode the first page of the data while obtaining the second indication.

5. The method according to claim 1, wherein sampling the first current comprises comparing the first current to a predetermined threshold.

6. The method according to claim 5, wherein precharging the bit line connected to the given analog memory cell to the second precharge voltage comprises setting the second precharge voltage to a first level when the first current is below the predetermined threshold, and setting the second precharge voltage to a second level, greater than the first level, when the first current is above the predetermined threshold.

7. The method according to claim 5, wherein the predetermined threshold is a first threshold, and wherein sampling the second current comprises comparing the second current to a second threshold, which is different from the first threshold.

8. The method according to any of claims 1-7, and comprising obtaining a third indication of the analog value stored in the given analog memory cell by precharging the bit line connected to the given analog memory cell to a third precharge voltage, which is dependent upon at least the second indication, and then sampling a third current on the bit line, and reading out at least a third bit from the given analog memory cell responsively to the third indication.

9. The method according to any of claims 1-7, and comprising decoding data comprising at least one of the first and second respective bits that have been read out from the given analog memory cell, and upon occurrence of a failure in decoding the data, obtaining a third indication of the analog value stored in the given analog memory cell using a set of sampling parameters that is dependent upon at least the second indication, and then decoding the data using the third indication together with at least one of the first and second indications.

10. The method according to any of claims 1-7, wherein sampling the first current comprises applying a predetermined control voltage to a word line connected to the given analog memory cell in order to cause the given analog memory cell to conduct the first current, and wherein sampling the second current comprises applying the same predetermined control voltage to the word line connected to the given analog memory cell in order to cause the given analog memory cell to conduct the second current.

11. The method according to any of claims 1-7, wherein sampling the first current comprises sampling the first current on the bit line after a first delay, and wherein sampling the second current comprises sampling the second current on the bit line after a second delay, which is dependent upon the first indication.

12. A method for operating a memory, comprising:

storing analog values in an array of analog memory cells, so that each of the analog memory cells holds an analog value corresponding to at least first and second respective bits, the array comprising word lines and bit lines connected to the analog memory cells;

obtaining a first indication of the analog value stored in a given analog memory cell by precharging a bit line connected to the given analog memory cell, and then sampling a first current on the bit line after a first delay;

obtaining a second indication of the analog value stored in the given analog memory cell by precharging the bit line connected to the given analog memory cell, and then sampling a second current on the bit line after a second delay, which is dependent upon the first indication; and

reading out the first and second respective bits from the given analog memory cell responsively to the first and second indications.

13. The method according to claim 12, wherein the first indication is indicative of the first respective bit stored in the given analog memory cell, and the second indication is indicative of the second respective bit stored in the given analog memory cell.

14. The method according to claim 13, wherein reading out the first and second respective bits comprises reading out the first respective bit prior to sampling the second current.

15. The method according to claim 14, wherein the first respective bit belongs to a first page of data, and the second respective bit belongs to a second page of data, and wherein the method comprises using the first respective bit read out from the given analog memory cell to decode the first page of the data while obtaining the second indication.

16. The method according to claim 12, wherein sampling the first current comprises comparing the first current to a predetermined threshold.

17. The method according to claim 16, wherein sampling the second current comprises setting the second delay to a first delay time when the first current is below the predetermined threshold, and setting the second delay to a second delay time, greater than the first delay time, when the first current is above the predetermined threshold.

18. The method according to claim 16, wherein the predetermined threshold is a first threshold, and wherein sampling the second current comprises comparing the second current to a second threshold, which is different from the first threshold.

19. The method according to any of claims 12-18, and comprising obtaining a third indication of the analog value stored in the given analog memory cell by precharging the bit

line connected to the given analog memory cell, and then sampling a third current on the bit line after a third delay, which is dependent upon at least the second indication, and reading out at least a third bit from the given analog memory cell responsively to the third indication.

20. The method according to any of claims 12-18, and comprising decoding data comprising at least one of the first and second respective bits that have been read out from the given analog memory cell, and upon occurrence of a failure in decoding the data, obtaining a third indication of the analog value stored in the given analog memory cell using a set of sampling parameters that is dependent upon at least the second indication, and then decoding the data using the third indication together with at least one of the first and second indications.

21. The method according to any of claims 12-18, wherein sampling the first current comprises applying a predetermined control voltage to a word line connected to the given analog memory cell in order to cause the given analog memory cell to conduct the first current, and wherein sampling the second current comprises applying the same predetermined control voltage to the word line connected to the given analog memory cell in order to cause the given analog memory cell to conduct the second current.

22. A method for operating a memory, comprising:

storing analog values in a group of analog memory cells, so that each of the analog memory cells holds an analog value corresponding to at least first and second respective bits belonging respectively to first and second pages of data;

obtaining a first indication of the analog value stored in a given analog memory cell by sampling the given analog memory cell using a first set of sampling parameters, wherein the first indication is indicative of the first respective bit stored in the given analog memory cell;

obtaining a second indication of the analog value stored in the given analog memory cell by sampling the given analog memory cell using a second set of sampling parameters, which is dependent upon the first indication, wherein the second indication is indicative of the second respective bit stored in the given analog memory cell; and

reading out the first bit from the given analog memory cell responsively to the first indication, and decoding the first page of the data using the first bit while obtaining the second indication.

23. The method according to claim 22, and comprising, upon occurrence of a failure in decoding one of the pages of the data, obtaining a third indication of the analog value stored in the given analog memory cell using a third set of sampling parameters that is dependent upon at least the second indication, and then decoding the one of the pages using the third indication together with at least one of the first and second indications.

24. Memory apparatus, comprising:

an array of analog memory cells, which are configured to store analog values so that each of the analog memory cells holds an analog value corresponding to at least first and second respective bits, the array comprising word lines and bit lines connected to the analog memory cells; and

readout circuitry, which is connected to the word lines and the bit lines and is configured to obtain first and second indications of the analog value stored in the given memory cell by precharging a bit line connected to the given analog memory cell to a first precharge voltage and then sampling a first current on the bit line so as to obtain the first indication, and precharging the bit line connected to the given analog memory cell to a second precharge voltage, which is dependent upon the first indication, and then sampling a second current on the bit line so as to obtain the second indication, and which is configured to read out the first and second respective bits from the given analog memory cell responsively to the first and second indications.

25. The apparatus according to claim 24, wherein the first indication is indicative of the first respective bit stored in the given analog memory cell, and the second indication is indicative of the second respective bit stored in the given analog memory cell.

26. The apparatus according to claim 25, wherein the readout circuitry is configured to read out the first respective bit prior to sampling the second current.

27. The apparatus according to claim 26, wherein the first respective bit belongs to a first page of data, and the second respective bit belongs to a second page of data, and wherein the apparatus comprises a decoder, which is configured to decode the first page of the data using the first respective bit read out from the given analog memory cell while the readout circuitry is obtaining the second indication.

28. The apparatus according to claim 24, wherein the readout circuitry is configured to sample the first current by comparing the first current to a predetermined threshold.

29. The apparatus according to claim 28, wherein the readout circuitry is configured to set the second precharge voltage to a first level when the first current is below the predetermined threshold, and to set the second precharge voltage to a second level, greater than the first level, when the first current is above the predetermined threshold.

30. The apparatus according to claim 28, wherein the predetermined threshold is a first threshold, and wherein the readout circuitry is configured to compare the second current to a second threshold, which is different from the first threshold.

31. The apparatus according to any of claims 24-30, wherein the readout circuitry is configured to obtain a third indication of the analog value stored in the given analog memory cell by precharging the bit line connected to the given analog memory cell to a third precharge voltage, which is dependent upon at least the second indication, and then sampling a third current on the bit line, and reading out at least a third bit from the given analog memory cell responsively to the third indication.

32. The apparatus according to any of claims 24-30, and comprising a decoder, which is coupled to decode data comprising at least one of the first and second respective bits that have been read out from the given analog memory cell,

wherein upon occurrence of a failure in decoding the data, the readout circuitry is operative to obtain a third indication of the analog value stored in the given analog memory cell using a set of sampling parameters that is dependent upon at least the second indication, and the decoder is operative to decode the data using the third indication together with at least one of the first and second indications.

33. The apparatus according to any of claims 24-30, wherein the readout circuitry is configured to sample the first current by applying a predetermined control voltage to a word line connected to the given analog memory cell in order to cause the given analog memory cell to conduct the first current, and to apply the same predetermined control voltage to the word line connected to the given analog memory cell in order to cause the given analog memory cell to conduct the second current.

34. The apparatus according to any of claims 24-30, wherein the readout circuitry is configured to sample the first current on the bit line after a first delay, and to sample the second current on the bit line after a second delay, which is dependent upon the first indication.

35. Memory apparatus, comprising:

an array of analog memory cells, which are configured to store analog values so that each of the analog memory cells holds an analog value corresponding to at least first and second respective bits, the array comprising word lines and bit lines connected to the analog memory cells; and

readout circuitry, which is connected to the word lines and the bit lines and is configured to obtain first and second indications of the analog value stored in the given memory cell by precharging a bit line connected to the given analog memory cell and then sampling a first current on the bit line after a first delay so as to obtain the first indication, and precharging the bit line connected to the given analog memory cell and then sampling a second current on the bit line after a second delay, which is dependent upon the first indication, so as to obtain the second indication, and which is configured to read out the first and second respective bits from the given analog memory cell responsively to the first and second indications.

36. The apparatus according to claim 35, wherein the first indication is indicative of the first respective bit stored in the given analog memory cell, and the second indication is indicative of the second respective bit stored in the given analog memory cell.

37. The apparatus according to claim 36, wherein the readout circuitry is configured to read out the first respective bit prior to sampling the second current.

38. The apparatus according to claim 37, wherein the first respective bit belongs to a first page of data, and the second respective bit belongs to a second page of data, and wherein the apparatus comprises a decoder, which is configured to decode the first page of the data using the first respective bit read out from the given analog memory cell while the readout circuitry is obtaining the second indication.

39. The apparatus according to claim 35, wherein the readout circuitry is configured to sample the first current by comparing the first current to a predetermined threshold.

40. The apparatus according to claim 39, wherein the readout circuitry is configured to set the set the second delay to a first delay time when the first current is below the predetermined threshold, and to set the second delay to a second delay time, greater than the first delay time, when the first current is above the predetermined threshold.

41. The apparatus according to claim 39, wherein the predetermined threshold is a first threshold, and wherein the readout circuitry is configured to compare the second current to a second threshold, which is different from the first threshold.

42. The apparatus according to any of claims 35-41, wherein the readout circuitry is configured to obtain a third indication of the analog value stored in the given analog memory cell by precharging the bit line connected to the given analog memory cell to a third precharge voltage, which is dependent upon at least the second indication, and then sampling a third current on the bit line, and reading out at least a third bit from the given analog memory cell responsively to the third indication.

43. The apparatus according to any of claims 35-41, and comprising a decoder, which is coupled to decode data comprising at least one of the first and second respective bits that have been read out from the given analog memory cell,

wherein upon occurrence of a failure in decoding the data, the readout circuitry is operative to obtain a third indication of the analog value stored in the given analog memory cell using a set of sampling parameters that is dependent upon at least the second indication, and the decoder is operative to decode the data using the third indication together with at least one of the first and second indications.

44. The apparatus according to any of claims 35-41, wherein the readout circuitry is configured to sample the first current by applying a predetermined control voltage to a word line connected to the given analog memory cell in order to cause the given analog memory cell to conduct the first current, and to apply the same predetermined control voltage to the word line connected to the given analog memory cell in order to cause the given analog memory cell to conduct the second current.

45. Memory apparatus, comprising:

a group of analog memory cells, which are configured to store analog values so that each of the analog memory cells holds an analog value corresponding to at least first and second respective bits belonging respectively to first and second pages of data;

readout circuitry, which is coupled to the analog memory cells and is configured to obtain a first indication of the analog value stored in a given analog memory cell by sampling the given analog memory cell using a first set of sampling parameters, wherein the first indication is indicative of the first respective bit stored in the given analog memory cell, and to obtain a second indication of the analog value stored in the given analog memory cell by sampling the given analog memory cell using a second set of sampling parameters, which is dependent upon the first indication, wherein the second indication is indicative of the second respective bit stored in the given analog memory cell; and

a decoder, which is coupled to receive the first bit from the readout circuitry and to decode the first page of the data using the first bit while the readout circuitry is obtaining the second indication.

46. The apparatus according to claim 45, wherein upon occurrence of a failure in decoding one of the pages of the data, the readout circuit is operative to obtain a third indication of the analog value stored in the given analog memory cell using a third set of sampling parameters that is dependent upon at least the second indication, and the decoder is operative to decode the one of the pages using the third indication together with at least one of the first and second indications.

FIG. 1

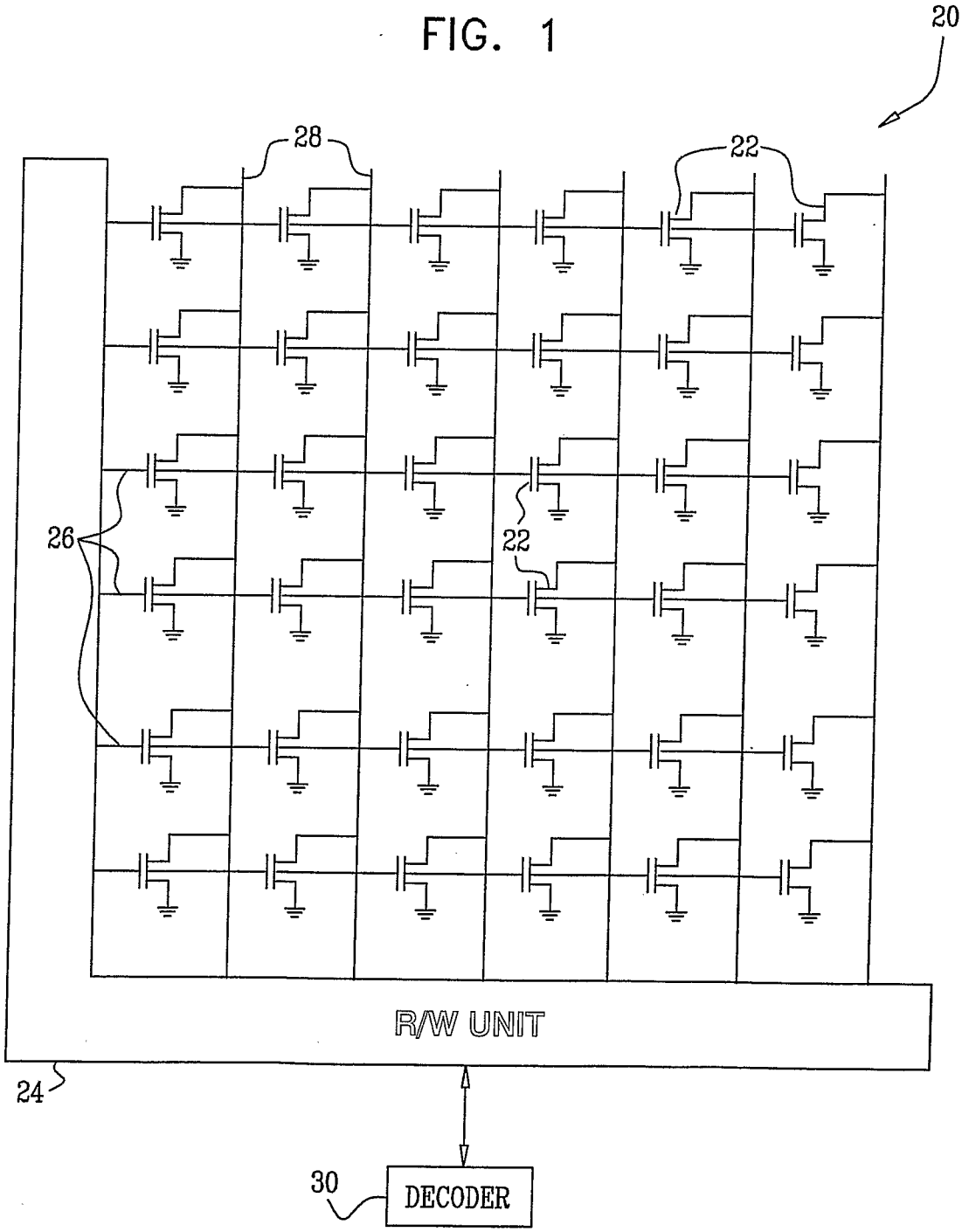


FIG. 2

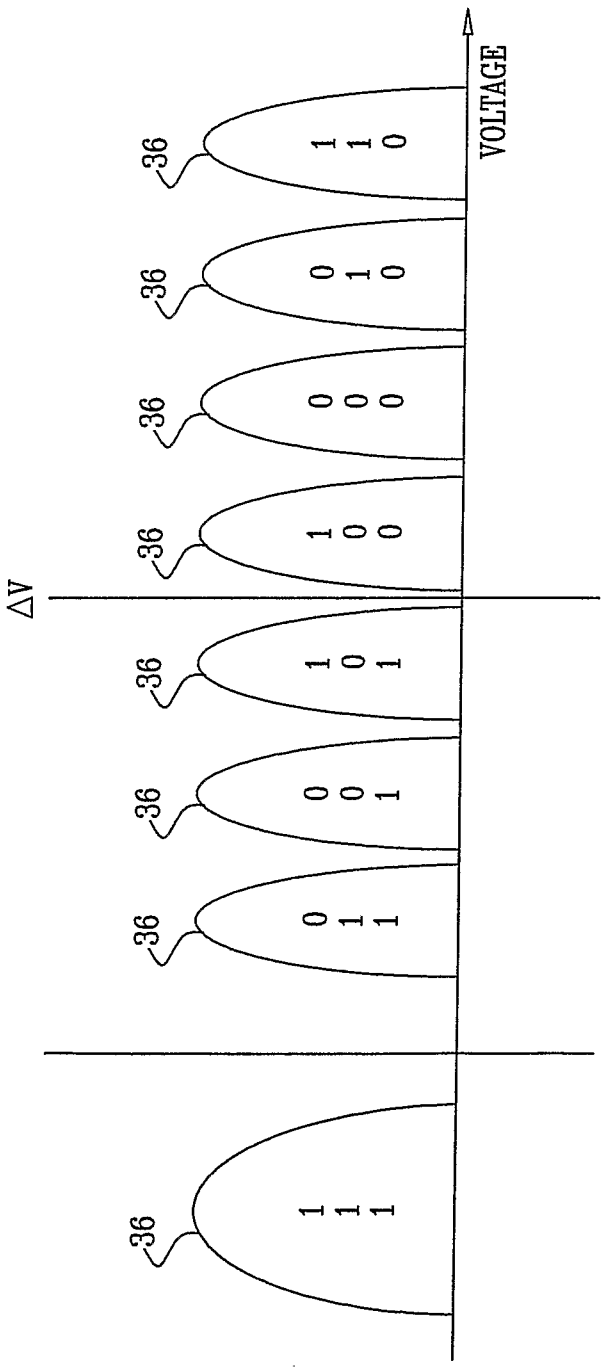
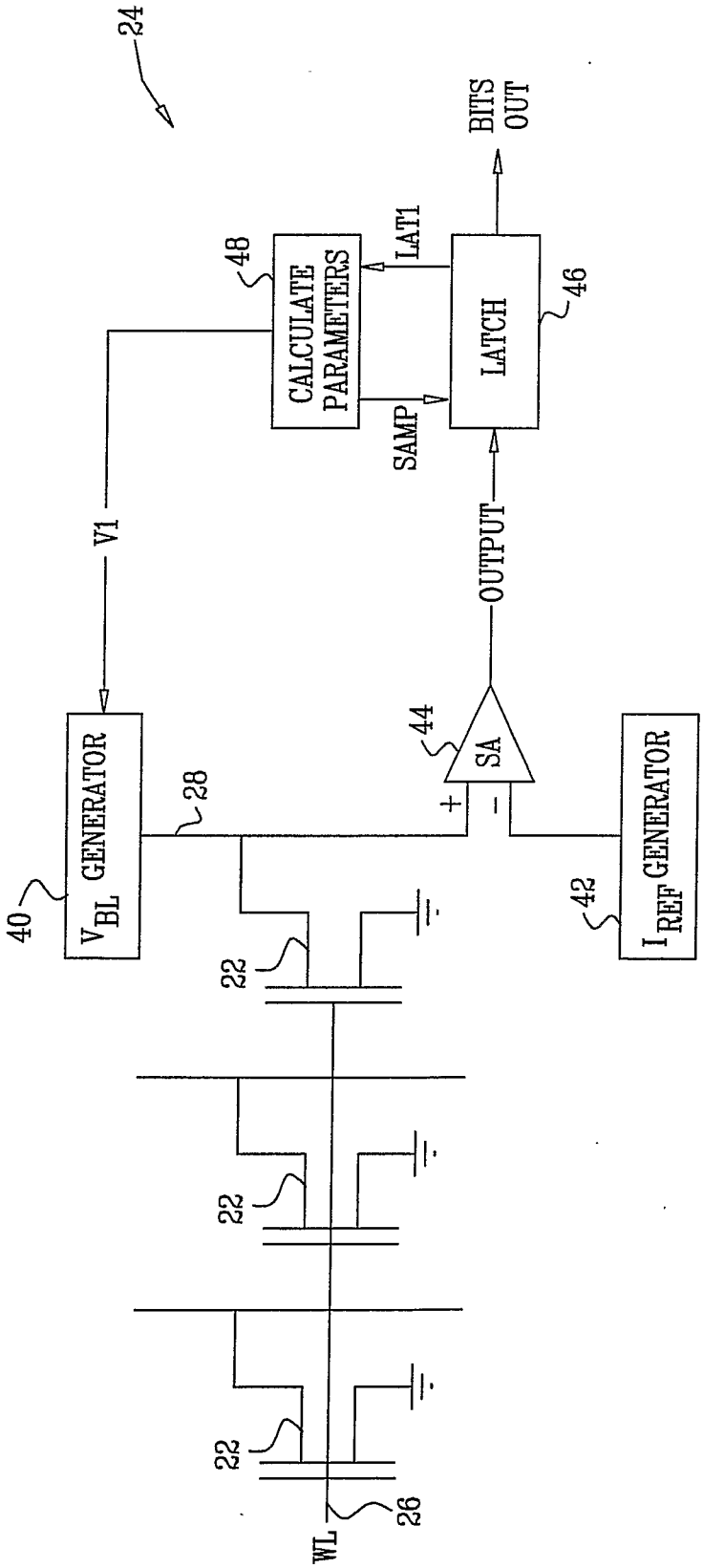


FIG. 3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LAT1
LATCH
46
SAMP
V1
OUTPUT
44
SA
+
−
40
V_{BL} GENERATOR
28
I_{REF} GENERATOR
42
22
22
22
26
WL

FIG. 4

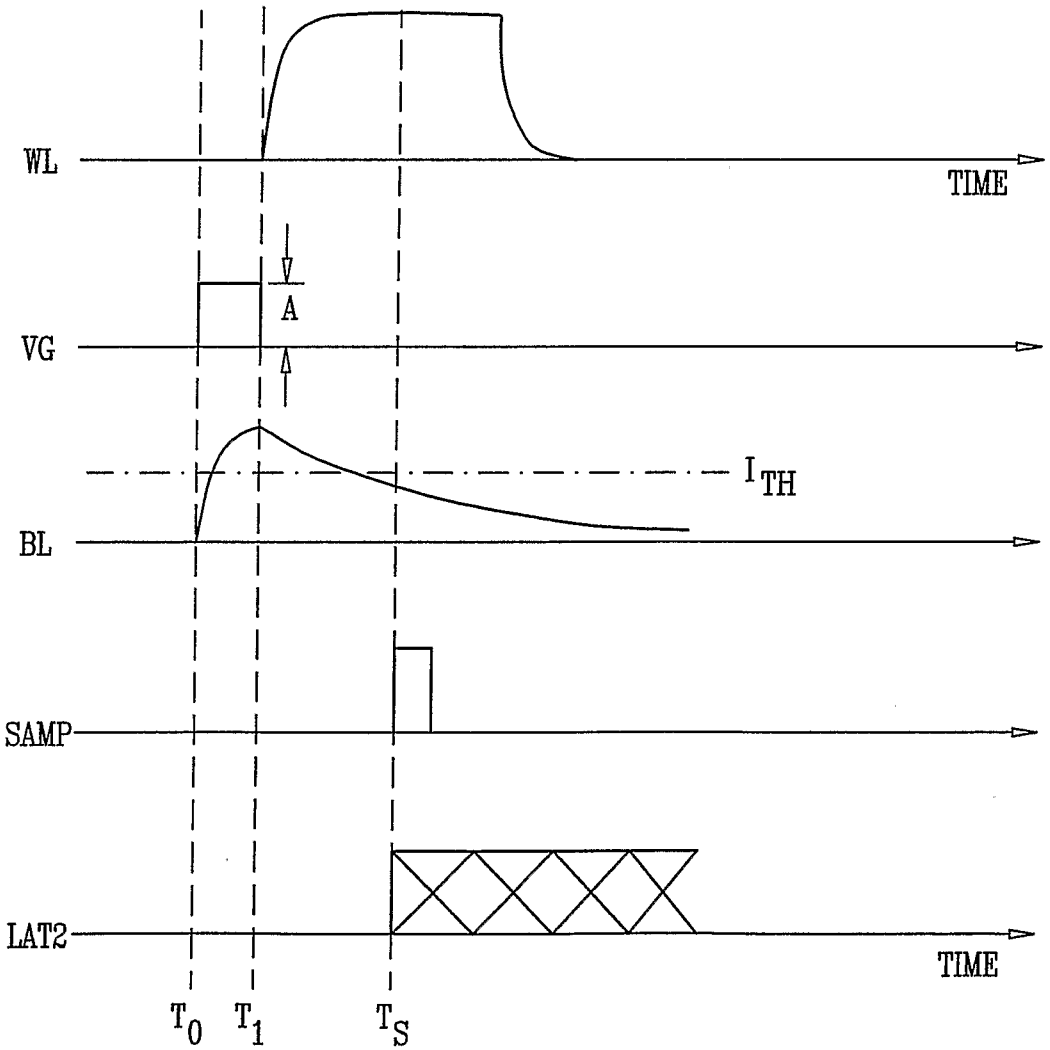
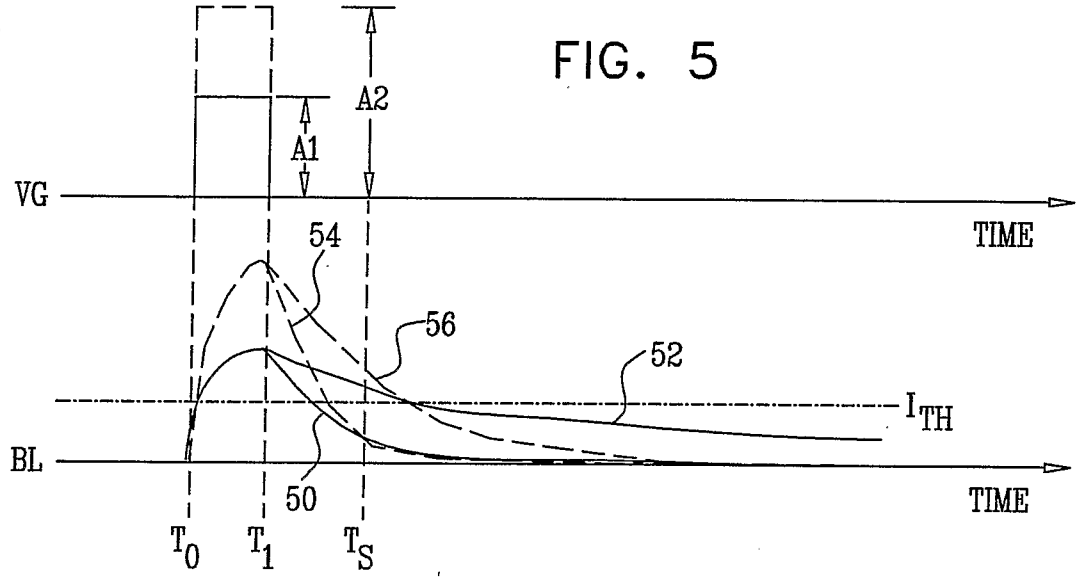


FIG. 5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A1
VG
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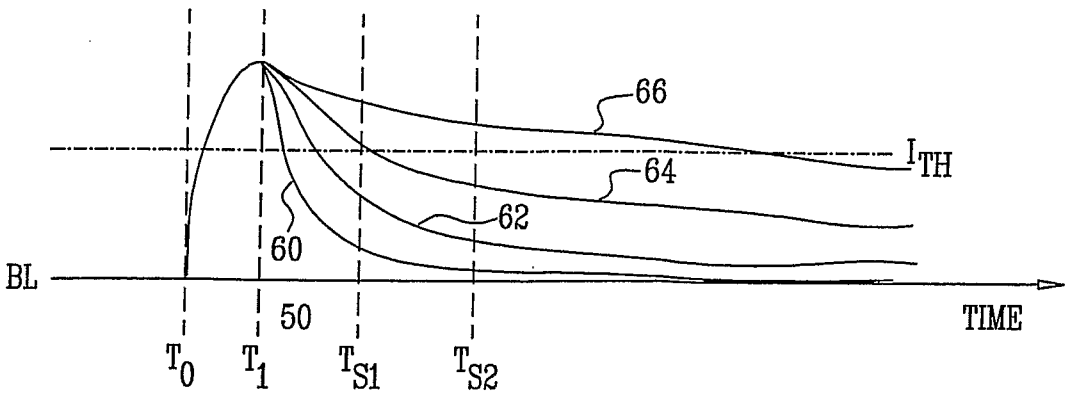
56
52
I_{TH}
BL
50
TIME
T_0
T_1
T_S

FIG. 6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62
60
BL
50
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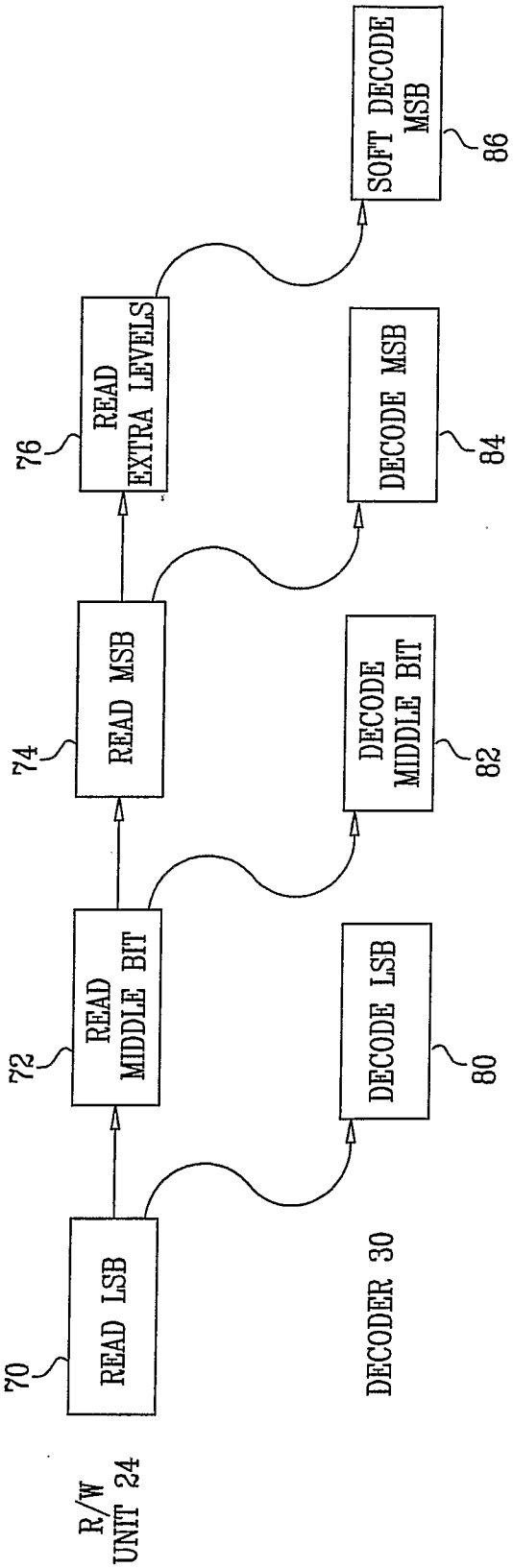
T_1
T_{S1}
T_{S2}

FIG. 7


R/W UNIT 24
READ LSB
70
READ MIDDLE BIT
72
READ MSB
74
READ EXTRA LEVELS
76
DECODER 30
DECODE LSB
80
DECODE MIDDLE BIT
82
DECODE MSB
84
SOFT DECODE MSB
86