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(71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Blvd., Santa Clara, California 95054 (US).

(72) Inventors: **SUNG, Seung Hoon**; 2459 NW Parnell Ter, Portland, Oregon 97229 (US). **TURKOT, Robert B.**; 3340 NE Jackson Road Loop, Hillsboro, Oregon 97124 (US). **RADOSAVLJEVIC, Marko**; 4129 NW Chaparral Terr, Beaverton, Oregon 97006 (US). **THEN, Han Wui**; 4191 NW 127TH Ave., Portland, Oregon 97229 (US). **RACHMADY, Willy**; 10945 SW Nutcracker Ct, Beaverton, Oregon 97007 (US). **DASGUPTA, Sansaptak**; 132 NE Greenridge Terrace, Hillsboro, Oregon 97124 (US). **KAVALIEROS, Jack T.**; 3734 NW Bronson Crest Loop, Portland, Oregon 97229 (US).

(74) Agent: **WINKLE, Robert G.**; Winkle, PLLC, c/o CPA Global, PO Box 52050, Minneapolis, Minnesota 55402 (US).

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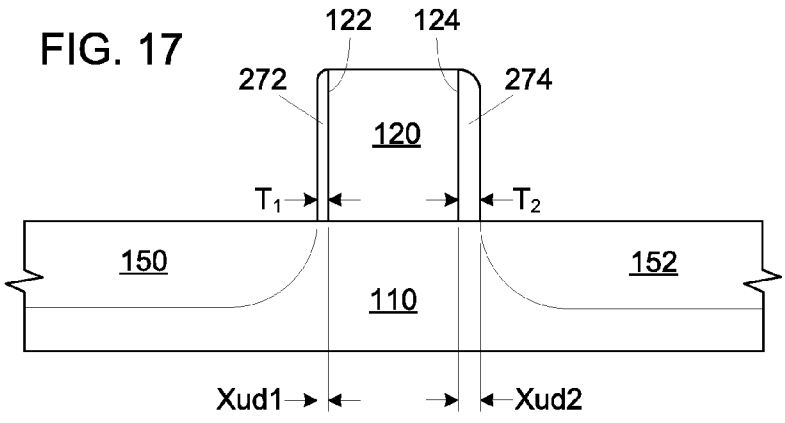
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(54) Title: MICROELECTRONIC TRANSISTOR SOURCE/DRAIN FORMATION USING ANGLED ETCHING

FIG. 17



(57) Abstract: The present description relates to the fabrication of microelectronic transistor source and/or drain regions using angled etching. In one embodiment, a microelectronic transistor may be formed by using an angled etch to reduce the number masking steps required to form p-type doped regions and n-type doped regions. In further embodiments, angled etching may be used to form asymmetric spacers on opposing sides of a transistor gate, wherein the asymmetric spacers may result in asymmetric source/drain configurations.

MICROELECTRONIC TRANSISTOR SOURCE/DRAIN FORMATION USING ANGLED ETCHING

TECHNICAL FIELD

Embodiments of the present description generally relate to the field of microelectronic devices, and, more particularly, to using angled etching to fabricate microelectronic transistors.

BACKGROUND

Higher performance, lower cost, increased miniaturization of integrated circuit components, and greater packaging density of integrated circuits are ongoing goals of the microelectronic industry for the fabrication of microelectronic devices. To achieve these goals, there is a drive to improve efficiency with improvements in their designs, materials used, and/or in their fabrication processes.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter of the present disclosure is particularly pointed out and distinctly claimed in the concluding portion of the specification. The foregoing and other features of the present disclosure will become more fully apparent from the following description and appended claims, taken in conjunction with the accompanying drawings. It is understood that the accompanying drawings depict only several embodiments in accordance with the present disclosure and are, therefore, not to be considered limiting of its scope. The disclosure will be described with additional specificity and detail through use of the accompanying drawings, such that the advantages of the present disclosure can be more readily ascertained, in which:

FIGs. 1-7 are side cross-sectional views of a process of using an angled etch to form p-type doped regions and/or n-type doped regions for a microelectronic transistor, according to an embodiment of the present description.

FIGs. 8-11 are side cross-sectional views of a process of using an angled etch to form raised doped regions by regrowth, according to one embodiment of the present description.

FIGs. 12-14 are side cross-sectional views of a process of using an angled etch to form raised doped regions by regrowth, according to another embodiment of the present description.

FIGs. 15-17 are side cross-sectional views of a process of using an angled etch to form asymmetric doped regions for a microelectronic transistor, according to still another embodiment of the present description.

FIGs. 18-20 are side cross-sectional views of microelectronic structures having asymmetric spacers, according to several embodiments of the present description.

FIG. 21 illustrates a computing device in accordance with one implementation of the present description.

DESCRIPTION OF EMBODIMENTS

In the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the claimed subject matter may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the subject matter. It is to be understood that the various embodiments, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein, in connection with one embodiment, may be implemented within other embodiments without departing from the spirit and scope of the claimed subject matter. References within this specification to "one embodiment" or "an embodiment" mean that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one implementation encompassed within the present description. Therefore, the use of the phrase "one embodiment" or "in an embodiment" does not necessarily refer to the same embodiment. In addition, it is to be understood that the location or arrangement of individual elements within each disclosed embodiment may be modified without departing from the spirit and scope of the claimed subject matter. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the subject matter is defined only by the appended claims, appropriately interpreted, along with the full range of equivalents to which the appended claims are entitled. In the drawings, like numerals refer to the same or similar elements or functionality throughout the several views, and that elements depicted therein are not necessarily to scale with one another, rather individual elements may be enlarged or reduced in order to more easily comprehend the elements in the context of the present description.

The terms "over", "to", "between" and "on" as used herein may refer to a relative position of one layer with respect to other layers. One layer "over" or "on" another layer or bonded "to" another layer may be directly in contact with the other layer or may have one or more intervening layers. One layer "between" layers may be directly in contact with the layers or may have one or more intervening layers.

Embodiments of the present description relate to the fabrication of microelectronic transistor source and drain regions using angled etching. In one embodiment, a microelectronic transistor may be formed by using an angled etch to reduce the number

masking steps required to form p-type doped regions and n-type doped regions. In further embodiments, angled etching may be used to form asymmetric spacers on opposing sides of a transistor gate, wherein the asymmetric spacers may result in asymmetric source/drain configurations.

FIGs. 1-7 illustrate a method of using an angled etch to reduce the masking steps needed to form p-type doped regions and n-type doped regions for a microelectronic transistor. For the sake of conciseness and clarity, a single microelectronic transistor will be illustrated. As illustrated in FIG. 1, a microelectronic substrate 110 may be provided or formed from any suitable material. In one embodiment, the microelectronic substrate 110 may be a bulk substrate composed of a single crystal of a material which may include, but is not limited to, silicon, germanium, silicon-germanium or a III-V compound semiconductor material. In other embodiments, the microelectronic substrate 110 may comprise a silicon-on-insulator substrate (SOI), wherein an upper insulator layer composed of a material which may include, but is not limited to, silicon dioxide, silicon nitride or silicon oxy-nitride, disposed on the bulk substrate. Alternatively, the microelectronic substrate 110 may be formed directly from a bulk substrate and local oxidation is used to form electrically insulative portions in place of the above described upper insulator layer. The microelectronic substrate 110 may also be other types of substrates, such as germanium, gallium arsenide, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, gallium antimonide, and the like, any of which may be combined with silicon.

As further shown in FIG. 1, a transistor gate 120 may be formed on the microelectronic substrate 110. The transistor gate 120 may be a sacrificial gate (shown), which would be removed and replace with a gate electrode (not shown) with a gate dielectric (not shown) disposed between the gate electrode and the microelectronic substrate 110 in subsequent processing, as will be understood to those skilled in the art. It is understood that the transistor gate 120 could include the gate dielectric (not shown) and the gate electrode (not shown) at this point. The functions and fabrication processes for the gate electrode and the gate dielectric are well known in the art and for the sake of conciseness and clarity will not be discussed herein. The transistor gate 120 may include a first sidewall 122 and an opposing second sidewall 124. In a further embodiment, the transistor gate 120 may be formed with an aspect ratio trapping, such as to form germanium and III-V material devices on silicon. Aspect Ratio Trapping is known in the art and for the sake of conciseness and clarity will not be discussed herein.

As shown in FIG. 2, a first spacer material layer 130 may be deposited over the transistor gate 120 and the microelectronic substrate 110. The first spacer material layer 130 may be made of any appropriate dielectric material, such as silicon nitride (e.g. Si_3N_4), silicon oxynitride (e.g. SiON), silicon oxycarbonitride (e.g. SiOCN), or silicon carbonitride (e.g. SiCN).

As shown in FIG. 3, a first angled etch (shown as arrow 140) may be directed toward the first sidewall 122 of the transistor gate 120. With the first angled etch 140, the transistor gate 120 shields the first spacer material layer 130 proximate the second sidewall 124 of the transistor gate 120, such that at least a portion of the first spacer material layer 130 may be removed from the transistor gate first sidewall 122 and such that the first spacer material layer 130 may be entirely removed on the microelectronic substrate 110 proximate the transistor gate first sidewall 122 to form an exposed first portion 112 of the microelectronic substrate 110, while remaining on the microelectronic substrate 110 proximate the transistor gate second sidewall 124. In one embodiment, the first spacer material layer 130 may be entirely removed from the transistor gate first sidewall 122, as shown. The angled etch proposed in the present description may be a plasma etching process wherein a stream of glow discharge (i.e. plasma) of an appropriate etchant gas mixture is direct to a target at an appropriate angle to achieve the results discussed above. In one embodiment, the first spacer material layer 130 may be silicon nitride wherein an etchant gas mixture may be a fluoromethane/argon/oxygen mixture. In a further embodiment, a distribution angle A of the glow discharge stream (direction shown by the arrow of the first angled etch 140) may be between about 5 and 25 degrees from vertical V.

As shown in FIG. 4, a first doped region 150 may then be formed in the microelectronic substrate 110 at the exposed first portion 112. The first doped region 150 may be formed any process known in the art, including but not limited to, implantation or regrowth, as will be understood to those skilled in the art. The first doped region 150 may be one of a p-type doped region or a n-type doped region. A p-type doped region may be doped with a p-type dopant, including, but not limited to, boron, aluminum, nitrogen, gallium, and indium. An n-type doped region may be doped with an n-type dopant, including but limited to, phosphorous, arsenic, antimony, bismuth, and lithium.

As shown in FIG. 5, a second spacer material layer 132 may be deposited over the remaining first spacer material layer 130 to form a spacer material bi-layer 134, over the transistor gate first sidewall 122, and over the first portion 112 of the microelectronic substrate 110. The second spacer material layer 132 may be any appropriate dielectric

material, such as silicon nitride (e.g. Si_3N_4), silicon oxynitride (e.g. SiON), silicon oxycarbonitride (e.g. SiOCN), or silicon carbonitride (e.g. SiCN).

As shown in FIG. 6, a second angled etch (shown as arrow 142) may be directed toward the second sidewall 124 of the transistor gate 120. With the second angled etch 142, the transistor gate 120 shields the second spacer material layer 132 proximate the first sidewall 122 of the transistor gate 120, such that at least a portion of the spacer material bi-layer 134 may be removed from the transistor gate first sidewall 122 and such that the spacer material bi-layer 134 may be entirely removed on the microelectronic substrate 110 proximate the transistor gate second sidewall 124 to form an exposed second portion 114 of the microelectronic substrate 110, while remaining on the microelectronic substrate 110 proximate the transistor gate first sidewall 122. In one embodiment, the first spacer material layer 130 may be entirely removed from the transistor gate second sidewall 124, as shown. In one embodiment, the second spacer material layer 132 may be silicon nitride wherein an etchant gas mixture may be fluoromethane/argon/oxygen mixture. In a further embodiment, a distribution angle B of the glow discharge stream (direction shown by the arrow of the second angled etch 142) may be between about 5 and 25 degree from vertical V, where vertical V is substantially perpendicular with the microelectronic substrate 110.

As shown in FIG. 7, a second doped region 152 may then be formed in the microelectronic substrate 110 at the second portion 114 (see FIG. 6). The second doped region 152 may be formed any process known in the art, including but not limited to, implantation or regrowth, as will be understood to those skilled in the art. The second doped region 152 may be one of a p-type doped region or an n-type doped region, which is opposite to that of the first doped region 150. As it can be further seen in FIG. 7, a portion of the microelectronic substrate 110 under the transistor gate 120 will be undoped, thereby forming an instrinic region 154. Thus, for example, when the first doped region 150 is p-type doped, the second doped region 152 will be n-type doped, which forms the basic P-I-N (p-type/intrinsic/n-type) junction for a tunnel field effect transistor (TFET), e.g. a microelectronic transistor 160.

FIGs. 8-11 illustrate another embodiment of the present description wherein raised doped regions are formed by regrowth. Beginning with FIG. 2, the first angled etch 140 may be directed toward the first sidewall 122 of the transistor gate 120, as shown in FIG. 8. With the first angled etch 140, the transistor gate 120 shields the first spacer material layer 130 proximate the second sidewall 124 of the transistor gate 120, such that at least a portion of the first spacer material layer 130 may be removed from the transistor gate first sidewall 122 and

such that the first spacer material layer 130 may be entirely removed on the microelectronic substrate 110 proximate the transistor gate first sidewall 122 to form the exposed first portion 112, while remaining on the microelectronic substrate 110 proximate the transistor gate second sidewall 124. In one embodiment, a portion of the first spacer material layer 130 may remain on the transistor gate first sidewall 122 forming a first spacer 210 to protect the transistor gate 120 during a subsequent etching process, as will be discussed.

As shown in FIG. 9, a portion of the microelectronic substrate 110 at the exposed first portion 112 (see FIG. 8) may be removed to form a recess 220 by an anisotropic etch. As shown in FIG. 10, a regrowth process may be followed to form a raised first doped region 230, i.e. where a portion of the raised first doped region 230 extends above the microelectronic substrate 110. The etching processes for forming the recess 220 and for the regrowth processes for forming the raised first doped region 230 are well known in the art and for the sake of conciseness and clarity will not be discussed herein. A similar process as described with regard to FIGs. 5 for forming the second spacer material layer 132 and similar processes with regard to FIGs. 9 and 10 may be followed to from a second spacer 212 adjacent the transistor gate second sidewall 124 and a raised second doped region 232 on the side of the transistor gate 120 opposite the raised first doped region 230, as shown in FIG. 11. With an anisotropic etch and the presence of the first spacer 210 and the second spacer 212 may result in the raised first doped region 230 and the raised second doped region 232 being spaced from the transistor gate 120, which may result in a lower overlap capacitance (Cov) and a higher external resistance (Rext) for each, as will be understood to those skilled in the art.

FIGs. 12-15 illustrate yet another embodiment of the present description wherein raised doped regions are formed by regrowth. Beginning with FIG. 9, a portion of the microelectronic substrate 110 at the exposed first portion 112 may be removed with either an isotropic etch or an appropriate anisotropic etch to form an undercut recess 240, as shown in FIG. 12. As shown in FIG. 13, a regrowth process may be followed to form an undercut raised first doped region 250. The etching processes for forming the undercut recess 240 and for the regrowth processes for forming the undercut raised first doped region 250 are well known in the art and for the sake of conciseness and clarity will not be discussed herein. A similar process as described with regard to FIG. 5 for forming the second spacer material layer 130 and similar processes with regard to FIGs. 9 and 12 may be followed to from the second spacer 212 adjacent the transistor gate second sidewall 124 and an undercut raised second doped region 252 on the side of the transistor gate 120 opposite the undercut raised

first doped region 250, as shown in FIG. 14. With an isotropic etch undercutting the first spacer 210 and the second spacer 212, the undercut first doped region 250 and the undercut second doped region 252 may be position closer to the transistor gate 120, which may result in a higher overlap capacitance (Cov) and a lower external resistance (Rext) for each, as will be understood to those skilled in the art.

In another embodiment of the present description, the angled etch may used to achieve an asymmetric source and drain design to improve transistor performance. As will be understood to those skilled in the art, external resistance (Rext) control is critical to achieving higher drain current saturation (Id sat). However, the external resistance on the source side plays a more critical role in the drain current saturation because it lowers the effective voltage gate source (Vgs) and voltage drain source (Vds). The external resistance on the drain side has more of an impact on the linear drain current (Id lin) due to the lower effective voltage drain source. This allows for design flexibility to achieve a matched current saturation while lowering an overlap capacitance (Cov) on the drain side. It is noted that the overlap capacitance (Cov) will play a role in the circuit performance because the Miller effect will make the overlap capacitance larger than that estimated by calculation, which can degrade circuit performance. However, the following embodiment of an asymmetric source/drain design and implementation can enable a lower overlap capacitance on the drain side and a matched external resistance on the source side.

FIGs. 15-17 illustrate a method of forming asymmetric doped regions for a microelectronic transistor. Beginning at FIG. 2, an angled etch 270 may be performed at an appropriate angle relative to the transistor gate 120, wherein the angled etch 270 is directed toward the transistor gate first sidewall 122, as shown in FIG. 15. As shown in FIG. 16, the angled etch 270 (see FIG. 15) may result in asymmetric gate spacers, e.g. a first asymmetric gate spacer 272 abutting the transistor gate first sidewall 122 and a second asymmetric gate spacer 274 abutting the transistor gate second sidewall 124, wherein a thickness T_1 of the first asymmetric gate spacer 272 is smaller than a thickness T_2 of the second asymmetric gate spacer 274. Furthermore, the angled etch 270 may expose a first portion 282 of the microelectronic substrate 110 proximate the first asymmetric gate spacer 272 and may expose a second portion 284 of the microelectronic substrate 110 proximate the second asymmetric gate spacer 274.

As shown in FIG. 17, the first doped region 150 (such as a source region) may then be formed in the microelectronic substrate 110 at the exposed first portion 282 and the second doped region 152 (such as a drain region) may be formed in the microelectronic substrate 110

at the exposed second portion 284. In one embodiment, the first doped region 150 and the second doped region 152 may both be formed with a p-type dopant (forming p-type doped regions) for the formation of the pMOS microelectronic transistor. In another embodiment, the first doped region 150 and the second doped region 152 may both be formed with an n-type dopant (forming n-type doped regions) for the formation of an nMOS microelectronic transistor. In still another embodiment, with additional lithographic steps (as will be understood to those skilled in the art), the first doped region 150 may be one of a p-type doped region or a n-type doped region, which is opposite to that of the second doped region 152 for the formation of a tunnel field effect transistor (TFET).

As further illustrated in FIG. 17, as the thickness T_1 of the first asymmetric gate spacer 272 is smaller than a thickness T_2 of the second asymmetric gate spacer 274, the first doped region 150 will be either closer to or further under (illustrated as first underlap Xud1) the transistor gate 120 than the second doped region 152 (illustrated as second underlap Xud2), which is achieved with without any additional mask and lithographic processes. Thus, as will be understood to those skilled in the art, the asymmetry between the first doped region 150 and the second doped region 152 relative to the transistor gate 120 can enable a lower overlap capacitance on the drain side (e.g. the second doped region 152) and a matched external resistance on the source side (e.g. the first doped region 150).

The concept of asymmetric spacers of FIGs. 15-17 may be extended to processes illustrated in FIGs. 1-14. In the process illustrated in FIGs 1-7, the formation of the first asymmetric gate spacer 272 and the second asymmetric gate spacer 274 may result in the microelectronic structure 290 of FIG. 18. In the process illustrated in FIGs 8-11, the formation of the first asymmetric gate spacer 272 and the second asymmetric gate spacer 274 may result in the microelectronic structure 292 of FIG. 19. In the process illustrated in FIGs. 12-14, the formation of the first asymmetric gate spacer 272 and the second asymmetric gate spacer 274 may result in the microelectronic structure 294 of FIG. 20.

FIG. 21 illustrates a computing device 300 in accordance with one implementation of the present description. The computing device 300 houses a board 302. The board may include a number of microelectronic components, including but not limited to a processor 304, at least one communication chip 306A, 306B, volatile memory 308, (e.g., DRAM), non-volatile memory 310 (e.g., ROM), flash memory 312, a graphics processor or CPU 314, a digital signal processor (not shown), a crypto processor (not shown), a chipset 316, an antenna, a display (touchscreen display), a touchscreen controller, a battery, an audio codec (not shown), a video codec (not shown), a power amplifier (AMP), a global

positioning system (GPS) device, a compass, an accelerometer (not shown), a gyroscope (not shown), a speaker (not shown), a camera, and a mass storage device (not shown) (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth). Any of the microelectronic components may be physically and electrically coupled to the board 302. In some implementations, at least one of the microelectronic components may be a part of the processor 304.

The communication chips 306A, 306B enable wireless communications for the transfer of data to and from the computing device 300. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 306 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 300 may include a plurality of communication chips 306A, 306B. For instance, a first communication chip 306A may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 306B may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

Any of the microelectronic components within the computing device 300 may include microelectronic devices having at least one microelectronic transistor described above and/or having at least one microelectronic transistor fabricated in the manner described above.

In various implementations, the computing device 300 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 300 may be any other electronic device that processes data.

It is understood that the subject matter of the present description is not necessarily limited to specific applications illustrated in FIGs. 1-21. The subject matter may be applied to other microelectronic device and assembly applications, as well as any other appropriate transistor applications, as will be understood to those skilled in the art.

The following examples pertain to further embodiments, wherein Example 1 is a microelectronic transistor, comprising a transistor gate disposed on a microelectronic substrate, wherein the transistor gate includes a first sidewall and an opposing side sidewall; a first transistor gate spacer abutting the first sidewall of the transistor gate; and a second transistor gate spacer abutting the second sidewall of the transistor; wherein the second transistor gate spacer has a thickness that is greater than a thickness of the first transistor gate spacer.

In Example 2, the subject matter of Example 1 can optionally include a first doped region in the microelectronic substrate proximate the transistor gate first sidewall and a second doped region proximate the transistor gate second sidewall, wherein the first doped region is either closer to or further under the transistor gate than the second doped region.

In Example 3, the subject matter of Example 2 can optionally include the first doped region comprising one of a p-type doped region and an n-type doped region; and wherein the second doped region comprises one of a p-type doped region and an n-type doped region.

The following examples pertain to further embodiments, wherein Example 4 is a method for forming a microelectronic transistor, comprising forming a transistor gate on a microelectronic substrate, wherein the transistor gate includes a first sidewall and an opposing side sidewall; depositing a first spacer material layer over the transistor gate and over the microelectronic substrate; and performing an angled etch directed toward the transistor gate first sidewall to form a first transistor gate spacer abutting the first sidewall of the transistor gate.

In Example 5, the subject matter of Example 4 can optionally include performing the angled etch forming a second transistor gate spacer abutting the second sidewall of the transistor; and wherein the second transistor gate spacer has a thickness that is greater than a thickness of the first transistor gate spacer.

In Example 6, the subject matter of Example 4 can optionally include performing the angled etch exposing a first portion of the microelectronic substrate proximate the first transistor gate spacer, and further comprising forming a first doped region in the microelectronic substrate at the first portion of the microelectronic substrate.

In Example 7, the subject matter of Example 6 can optionally include performing the angled etch exposing a second portion of the microelectronic substrate proximate the second transistor gate spacer, and further comprising forming a second doped region in the microelectronic substrate at the second portion of the microelectronic substrate.

In Example 8, the subject matter of Example 7 can optionally include the first doped region is either closer to or further under the transistor gate than the second doped region.

In Example 9, the subject matter of either Example 7 or 8 can optionally include forming the first doped region comprising forming one of a p-type doped region and an n-type doped region, and wherein forming the second doped region comprises forming one of a p-type doped region and an n-type doped region.

In Example 10, the subject matter of Example 4 can optionally include performing the angled etch directed toward the transistor gate first sidewall comprises performing the angled etch directed from between about 5 and 25 degrees from vertical.

The following examples pertain to further embodiments, wherein Example 11 is a method of fabricating a microelectronic transistor, comprising forming a transistor gate on a microelectronic substrate, wherein the transistor gate includes a first sidewall and an opposing side sidewall; depositing a first spacer material layer over the transistor gate and over the microelectronic substrate; performing a first angled etch directed toward the transistor gate first sidewall to remove at least a portion of the first spacer material layer from the transistor gate first sidewall and from the microelectronic substrate proximate the transistor gate first sidewall forming a first exposed portion of microelectronic substrate; forming a first doped region in the first exposed portion of the microelectronic substrate; depositing a second spacer material layer over the first spacer material layer, the transistor gate first sidewall, and the first doped region, wherein depositing the second spacer material layer over the first spacer material layer forms a spacer material bi-layer; performing a second angled etch directed toward the transistor gate second sidewall to remove at least a portion of the spacer material bi-layer from the transistor gate second sidewall and from the microelectronic substrate proximate the transistor gate first sidewall forming a second exposed portion of microelectronic substrate; and forming a second doped region in the second exposed portion of the microelectronic substrate.

In Example 12, the subject matter of Example 11 can optionally include performing the first angled etch directed toward the transistor gate first sidewall removing the first spacer material layer from the transistor gate first sidewall, and performing the second angled etch

directed toward the transistor gate second sidewall removing the spacer material bi-layer from the transistor gate second sidewall.

In Example 13, the subject matter of Example 11 can optionally include performing the first angled etch directed toward the transistor gate first sidewall removing a portion the first spacer material layer from the transistor gate first sidewall to form a first spacer, and performing the second angled etch directed toward the transistor gate second sidewall removing a portion of the spacer material bi-layer from the transistor gate second sidewall to form a second spacer.

In Example 14, the subject matter of Example 11 can optionally include the second spacer having a thickness that is greater than a thickness of the first spacer.

In Example 15, the subject matter of Example 11 can optionally include forming the first doped region comprising forming one of a p-type doped region and an n-type doped region and wherein forming the second doped region comprises forming the other of the p-type doped region and the n-type doped region.

In Example 16, the subject matter of Example 11 can optionally include forming at least one of the first doped region and the second doped region comprising anisotropically etching a recess in the microelectronic substrate, and performing a regrowth process.

In Example 17, the subject matter of Example 11 can optionally include forming at least one of the first doped region and the second doped region comprising isotropically etching a recess in the microelectronic substrate, and performing a regrowth process.

In Example 18, the subject matter of Example 11 can optionally include performing the angled etch directed toward the transistor gate first sidewall comprising performing the angled etch directed from between about 5 and 25 degrees from vertical.

The following examples pertain to further embodiments, wherein Example 19 is an electronic system, comprising a board; and a microelectronic device attached to the board, wherein the microelectronic device includes at least one microelectronic transistor comprising a transistor gate disposed on a microelectronic substrate, wherein the transistor gate includes a first sidewall and an opposing side sidewall; a first transistor gate spacer abutting the first sidewall of the transistor gate; and a second transistor gate spacer abutting the second sidewall of the transistor; wherein the second transistor gate spacer has a thickness that is greater than a thickness of the first transistor gate spacer.

In Example 20, the subject matter of Example 19 can optionally include a first doped region in the microelectronic substrate proximate the transistor gate first sidewall and a

second doped region proximate the transistor gate second sidewall, wherein the first doped region is either closer to or further under the transistor gate than the second doped region.

In Example 21, the subject matter of Example 20 can optionally include the first doped region comprising one of a p-type doped region and an n-type doped region; and wherein the second doped region comprises one of a p-type doped region and an n-type doped region.

Having thus described in detail embodiments of the present description, it is understood that the present description defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

CLAIMS

What is claimed is:

1. A microelectronic transistor, comprising:

a transistor gate disposed on a microelectronic substrate, wherein the transistor gate includes a first sidewall and an opposing side sidewall;

a first transistor gate spacer abutting the first sidewall of the transistor gate; and

a second transistor gate spacer abutting the second sidewall of the transistor;

wherein the second transistor gate spacer has a thickness that is greater than a thickness of the first transistor gate spacer.

2. The microelectronic transistor of claim 1, further comprising a first doped region in the microelectronic substrate proximate the transistor gate first sidewall and a second doped region proximate the transistor gate second sidewall, wherein the first doped region is either closer to or further under the transistor gate than the second doped region.

3. The microelectronic transistor of claim 2, wherein the first doped region comprises one of a p-type doped region and an n-type doped region; and wherein the second doped region comprises one of a p-type doped region and an n-type doped region.

4. A method for forming a microelectronic transistor, comprising:

forming a transistor gate on a microelectronic substrate, wherein the transistor gate includes a first sidewall and an opposing side sidewall;

depositing a first spacer material layer over the transistor gate and over the microelectronic substrate; and

performing an angled etch directed toward the transistor gate first sidewall to form a first transistor gate spacer abutting the first sidewall of the transistor gate.

5. The method of claim 4, wherein performing the angled etch forms a second transistor gate spacer abutting the second sidewall of the transistor; and wherein the second transistor gate spacer has a thickness that is greater than a thickness of the first transistor gate spacer.

6. The method of claim 4, wherein performing the angled etch exposes a first portion of the microelectronic substrate proximate the first transistor gate spacer, and further comprising

forming a first doped region in the microelectronic substrate at the first portion of the microelectronic substrate.

7. The method of claim 6, wherein performing the angled etch exposes a second portion of the microelectronic substrate proximate the second transistor gate spacer, and further comprising forming a second doped region in the microelectronic substrate at the second portion of the microelectronic substrate.

8. The method of claim 7, wherein the first doped region is either closer to or further under the transistor gate than the second doped region.

9. The method of either claim 7 or 8, wherein forming the first doped region comprises forming one of a p-type doped region and an n-type doped region, and wherein forming the second doped region comprises forming one of a p-type doped region and an n-type doped region.

10. The method of claim 4, wherein performing the angled etch directed toward the transistor gate first sidewall comprises performing the angled etch directed from between about 5 and 25 degrees from vertical.

11. A method of fabricating a microelectronic transistor, comprising:

forming a transistor gate on a microelectronic substrate, wherein the transistor gate includes a first sidewall and an opposing side sidewall;

depositing a first spacer material layer over the transistor gate and over the microelectronic substrate;

performing a first angled etch directed toward the transistor gate first sidewall to remove at least a portion of the first spacer material layer from the transistor gate first sidewall and from the microelectronic substrate proximate the transistor gate first sidewall forming a first exposed portion of microelectronic substrate;

forming a first doped region in the first exposed portion of the microelectronic substrate;

depositing a second spacer material layer over the first spacer material layer, the transistor gate first sidewall, and the first doped region, wherein depositing the second spacer material layer over the first spacer material layer forms a spacer material bi-layer;

performing a second angled etch directed toward the transistor gate second sidewall to remove at least a portion of the spacer material bi-layer from the transistor gate second sidewall and from the microelectronic substrate proximate the transistor gate first sidewall forming a second exposed portion of microelectronic substrate; and

forming a second doped region in the second exposed portion of the microelectronic substrate.

12. The method of claim 11, wherein performing the first angled etch directed toward the transistor gate first sidewall removes the first spacer material layer from the transistor gate first sidewall, and performing the second angled etch directed toward the transistor gate second sidewall removes the spacer material bi-layer from the transistor gate second sidewall.

13. The method of claim 11, wherein performing the first angled etch directed toward the transistor gate first sidewall removes a portion the first spacer material layer from the transistor gate first sidewall to form a first spacer, and performing the second angled etch directed toward the transistor gate second sidewall removes a portion of the spacer material bi-layer from the transistor gate second sidewall to form a second spacer.

14. The method of claim 13, wherein the second spacer has a thickness that is greater than a thickness of the first spacer.

15. The method of claim 11, wherein forming the first doped region comprises forming one of a p-type doped region and an n-type doped region and wherein forming the second doped region comprises forming the other of the p-type doped region and the n-type doped region.

16. The method of claim 11, wherein forming at least one of the first doped region and the second doped region comprises anisotropically etching a recess in the microelectronic substrate, and performing a regrowth process.

17. The method of claim 11, wherein forming at least one of the first doped region and the second doped region comprises isotropically etching a recess in the microelectronic substrate, and performing a regrowth process.

18. The method of claim 11, wherein performing the angled etch directed toward the transistor gate first sidewall comprises performing the angled etch directed from between about 5 and 25 degrees from vertical.

19. An electronic system, comprising:

a board; and

a microelectronic device attached to the board, wherein the microelectronic device includes at least one microelectronic transistor comprising:

a transistor gate disposed on a microelectronic substrate, wherein the transistor gate includes a first sidewall and an opposing side sidewall;

a first transistor gate spacer abutting the first sidewall of the transistor gate; and

a second transistor gate spacer abutting the second sidewall of the transistor;

wherein the second transistor gate spacer has a thickness that is greater than a thickness of the first transistor gate spacer.

20. The electronic system of claim 19, wherein the microelectronic transistor further comprises a first doped region in the microelectronic substrate proximate the transistor gate first sidewall and a second doped region proximate the transistor gate second sidewall, wherein the first doped region is either closer to or further under the transistor gate than the second doped region.

21. The electronic system of claim 20, wherein the first doped region comprises one of a p-type doped region and an n-type doped region; and wherein the second doped region comprises one of a p-type doped region and an n-type doped region.

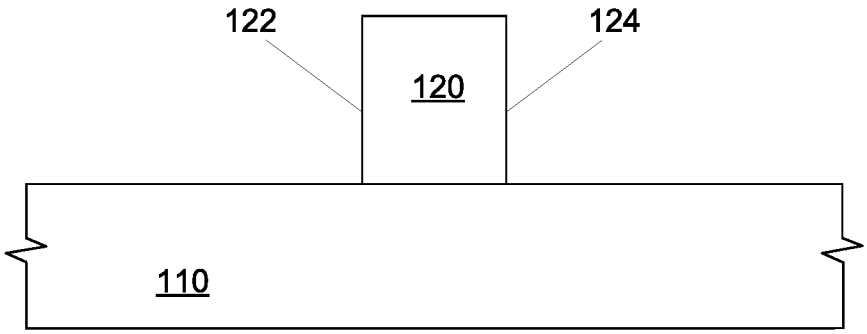


FIG. 1

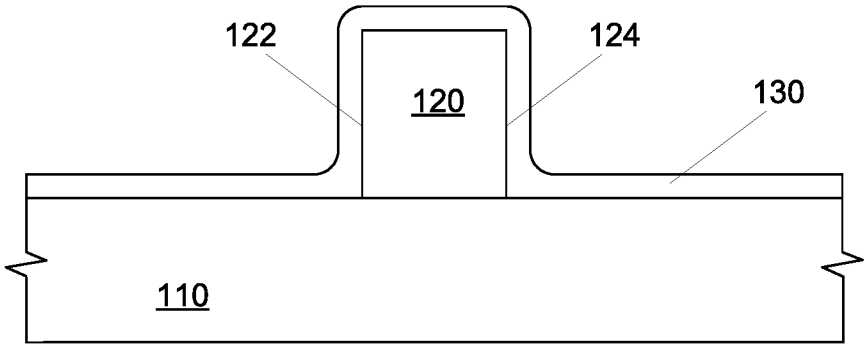


FIG. 2

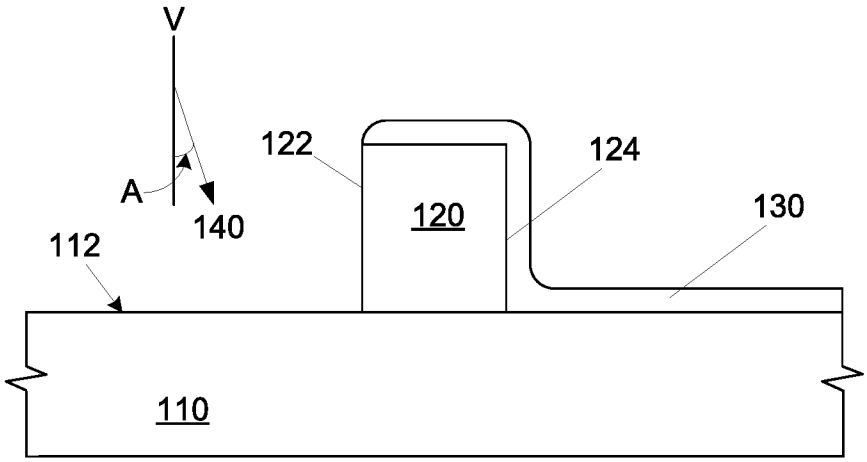


FIG. 3

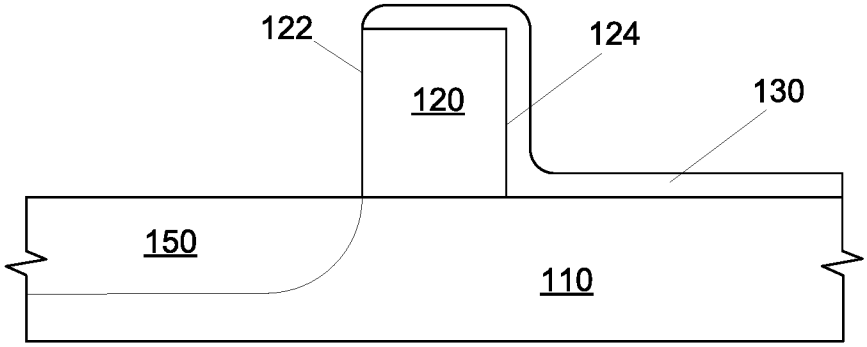


FIG. 4

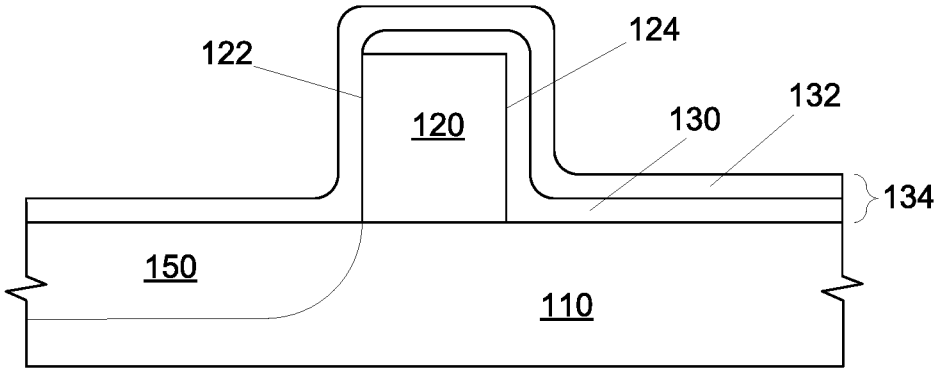


FIG. 5

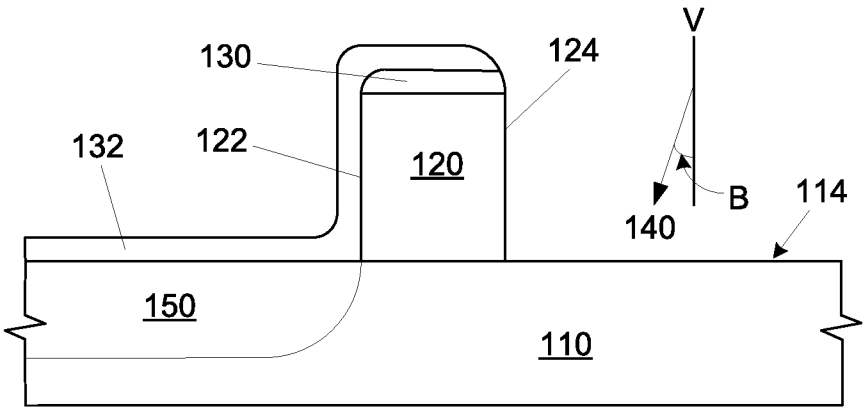


FIG. 6

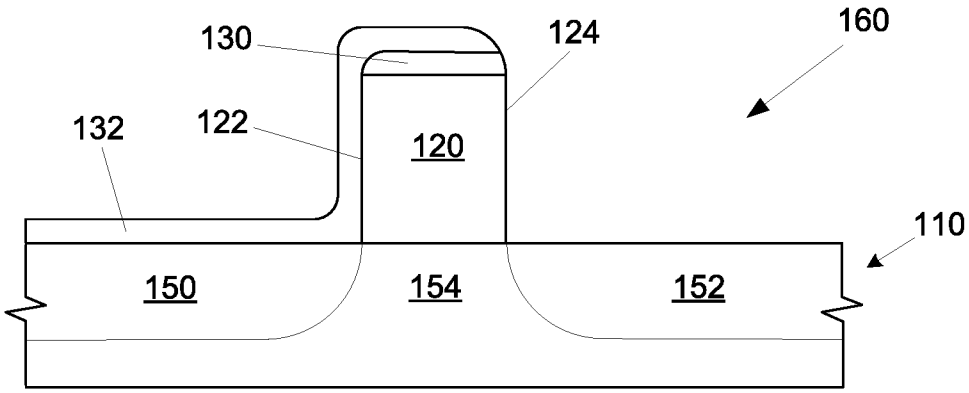


FIG. 7

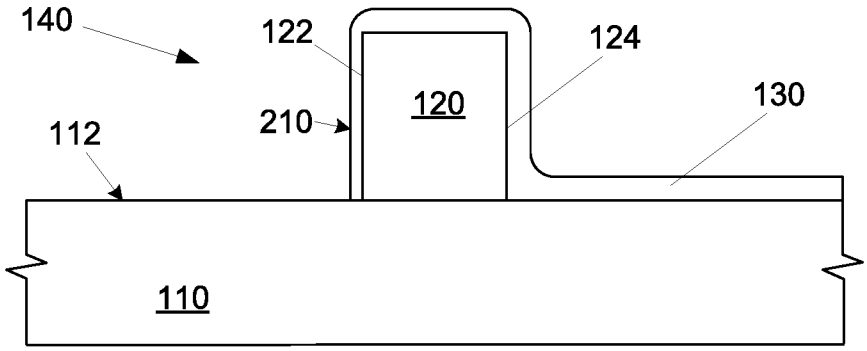


FIG. 8

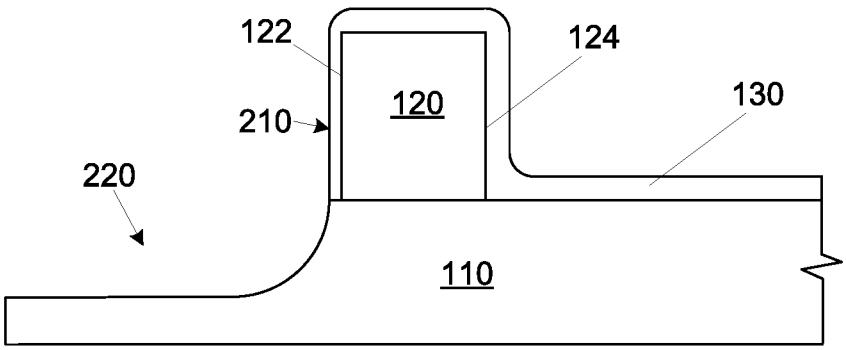


FIG. 9

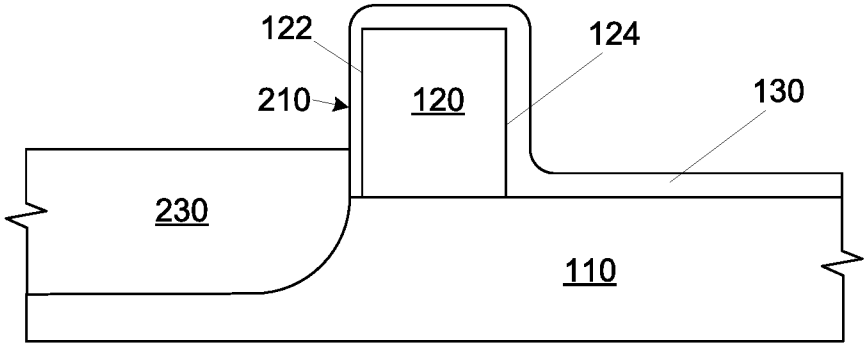


FIG. 10

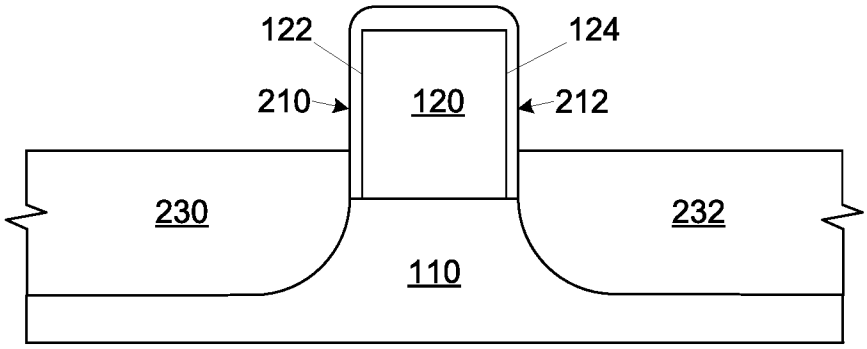


FIG. 11

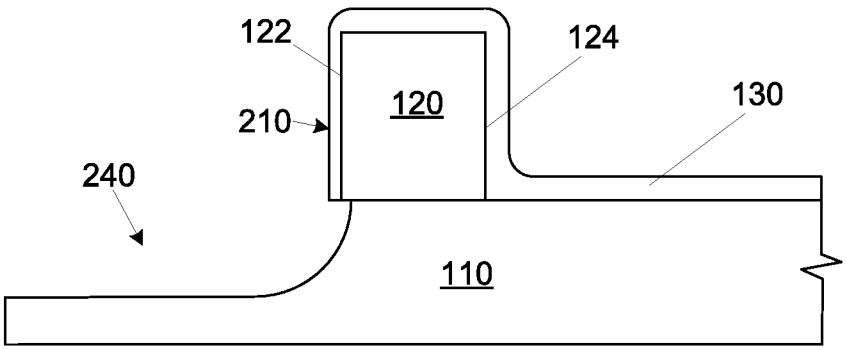


FIG. 12

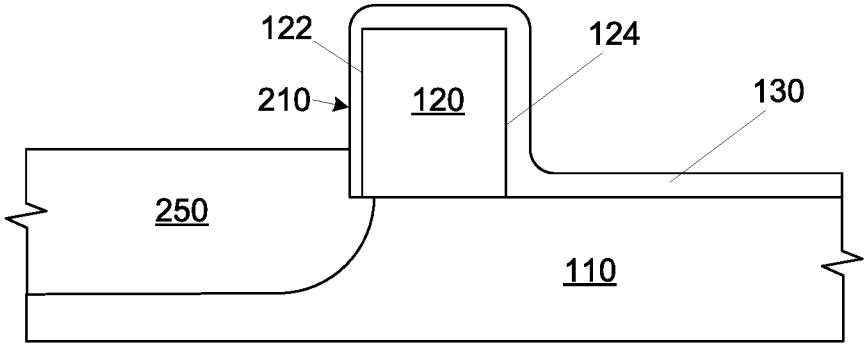


FIG. 13

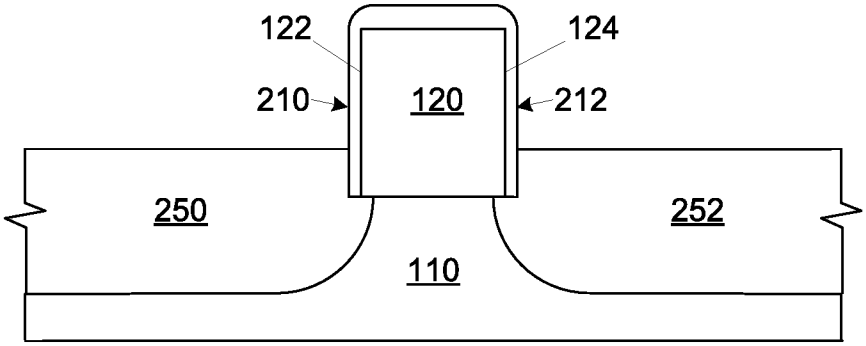


FIG. 14

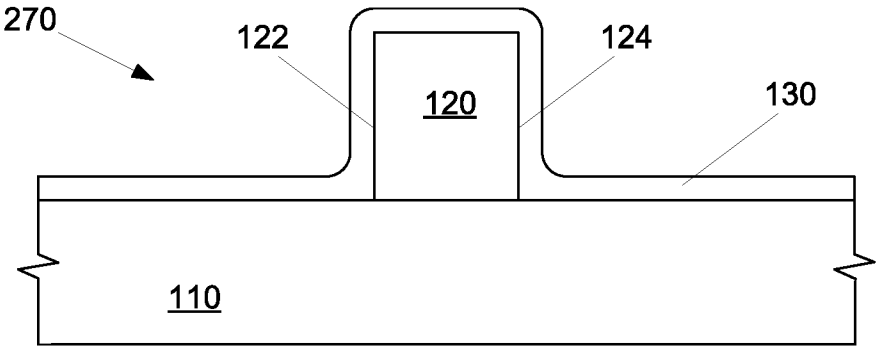


FIG. 15

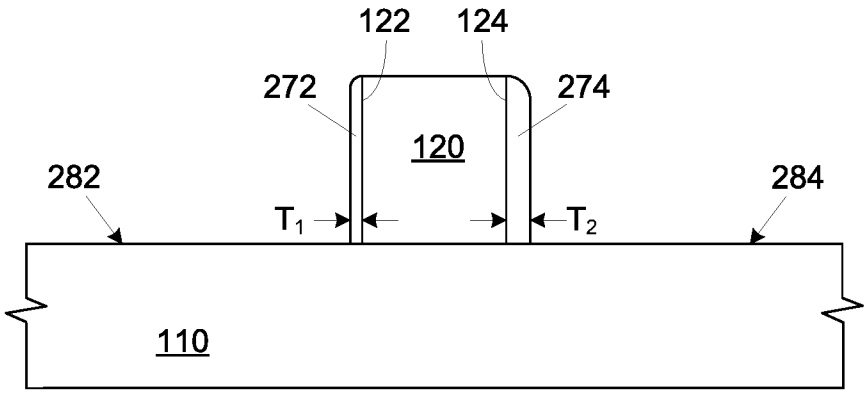

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FIG. 16

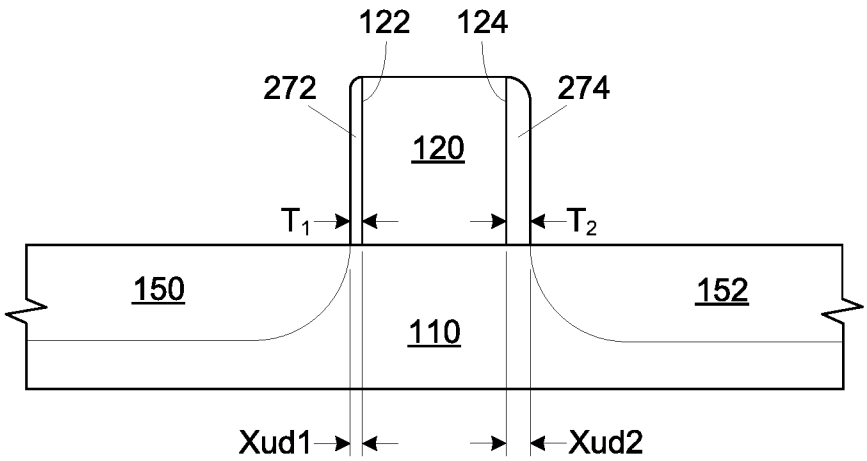

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FIG. 17

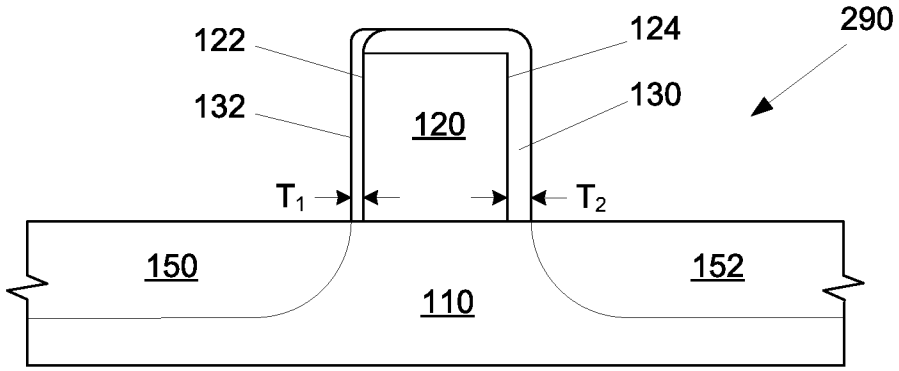


FIG. 18

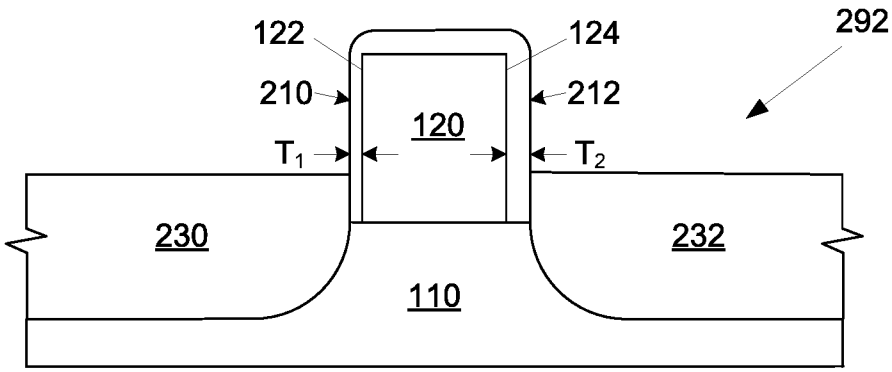


FIG. 19

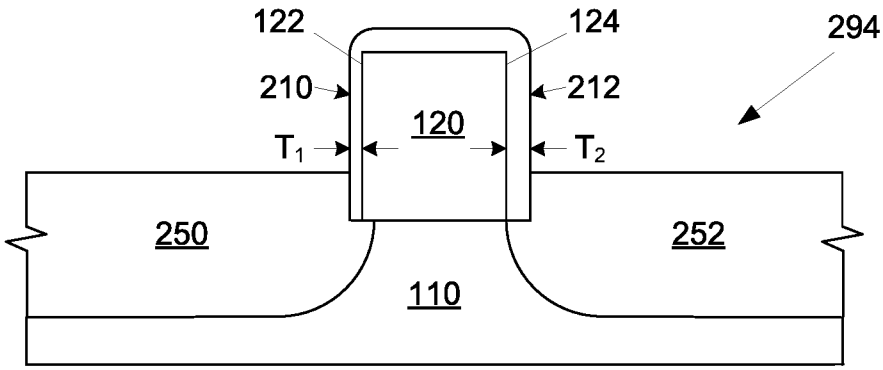


FIG. 20

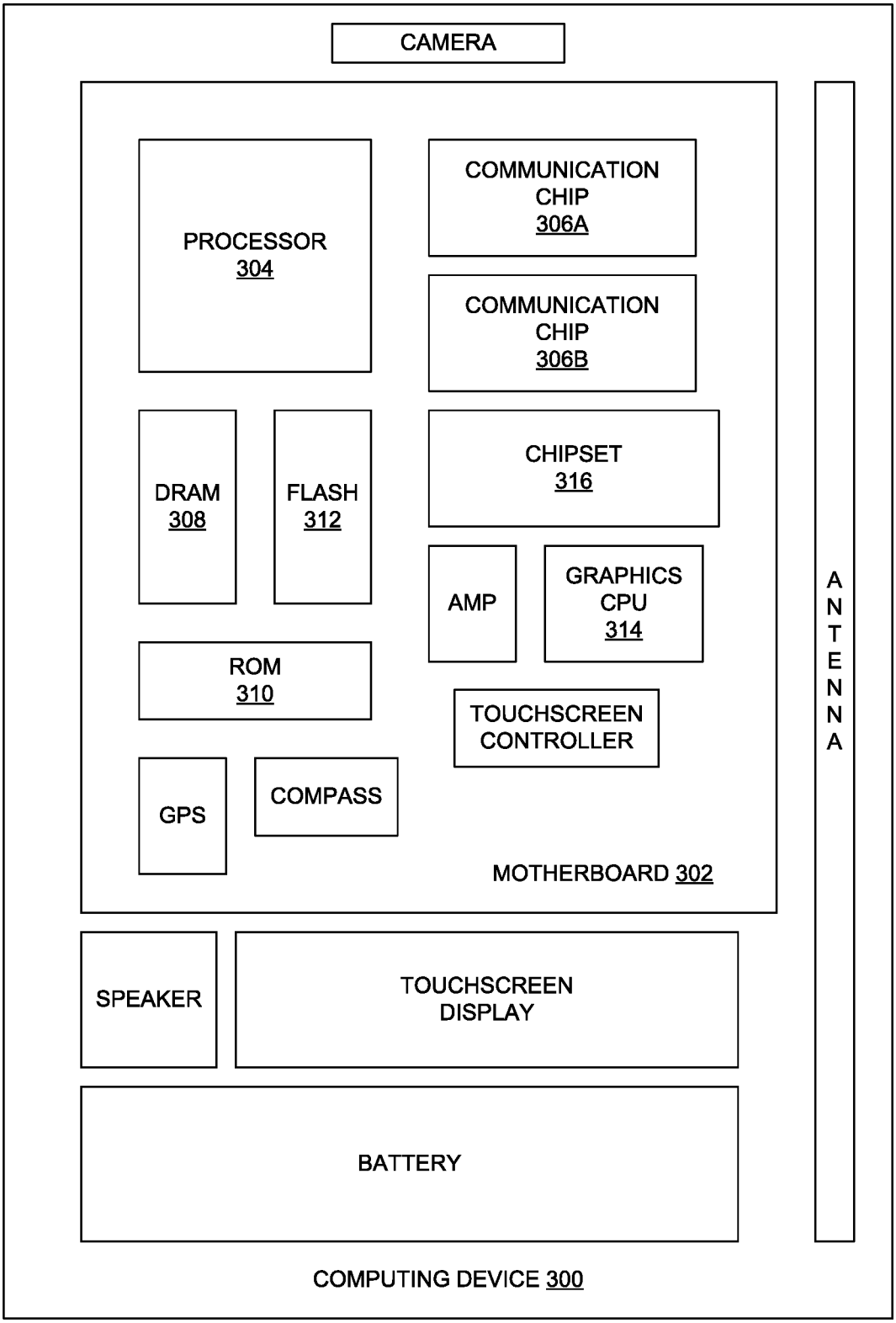

CAMERA
PROCESSOR
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COMMUNICATION
CHIP
306A
COMMUNICATION
CHIP
306B
DRAM
308
FLASH
312
CHIPSET
316
AMP
GRAPHICS
CPU
314
ROM
310
TOUCHSCREEN
CONTROLLER
GPS
COMPASS
MOTHERBOARD 302
ANTENNA
SPEAKER
TOUCHSCREEN
DISPLAY
BATTERY
COMPUTING DEVICE 300

FIG. 21

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/024866

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/78(2006.01)i, H01L 21/336(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 29/78; H01L 27/088; H01L 21/336; H01L 29/772; H01L 21/8238; H01L 27/092

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: sidewall, spacer, thickness, gate, substrate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012-0235244 A1 (HAIZHOU YIN et al.) 20 September 2012 See abstract, paragraphs [0039]-[0068] and figures 2(a)-2(k).	1,4-5,10,19
Y		2-3,6-9,20-21
A		11-18
Y	US 2010-0181618 A1 (PHILLIPPE MEUNIER-BELLARD et al.) 22 July 2010 See abstract, paragraphs[0062]-[0065] and figure 1.	2-3,6-9,20-21
A	US 2010-0019323 A1 (EUN JONG SHIN) 28 January 2010 See abstract, paragraphs [0033]-[0053] and figures 6-9.	1-21
A	US 2009-0159936 A1 (UDAY SHAH et al.) 25 June 2009 See abstract, paragraphs [0016]-[0021] and figures 3-6.	1-21
A	US 2010-0025744 A1 (TOSHIHIKO MIYASHITA et al.) 04 February 2010 See abstract, paragraphs [0047]-[0058] and figures 9A-9H.	1-21

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 December 2016 (26.12.2016)	**26 December 2016 (26.12.2016)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
CHOI, Sang Won
Telephone No. +82-42-481-8291

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2016/024866

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