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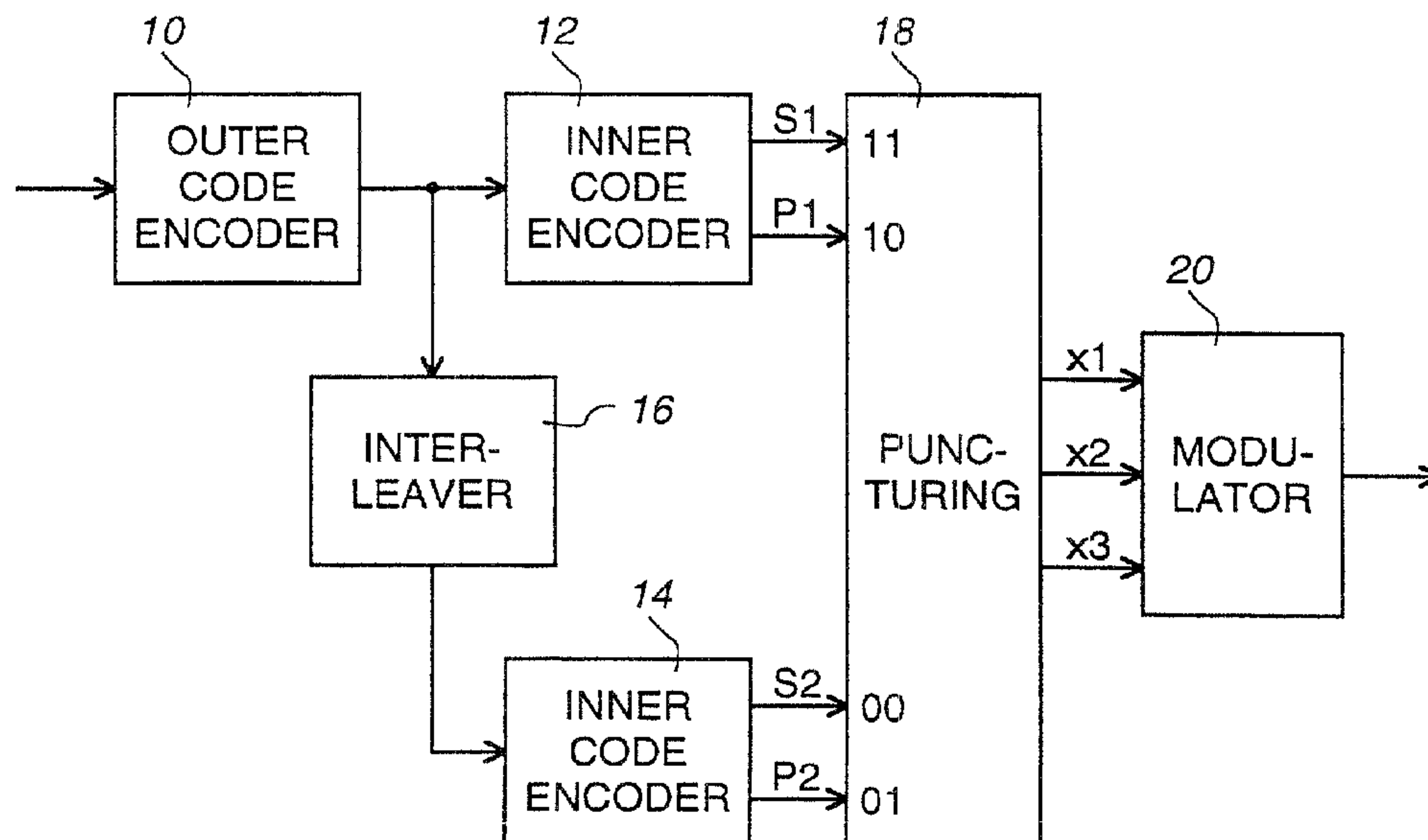
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(54) Title: ENCODING AND DECODING METHODS AND APPARATUS



(57) Abrégé/Abstract:

An encoder for a wideband CDMA communications system comprises an outer Reed-Solomon code encoder and an inner parallel concatenated convolutional code (PCCC) or turbo code encoder. An iterative PCCC decoder, for decoding the inner code, includes summing functions in forward and feedback paths for producing extrinsic information to enhance soft decoding decisions by first and second decoders in successive decoding iterations. An outer code decoder connected following the PCCC decoder also can provide serial feedback information for enhancing iterative decisions by the PCCC decoder.



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Abstract

An encoder for a wideband CDMA communications system comprises an outer Reed-Solomon code encoder and an inner parallel concatenated convolutional code (PCCC) or turbo code encoder. An iterative PCCC decoder, for decoding the inner code, includes summing functions in forward and feedback paths for producing extrinsic information to enhance soft decoding decisions by first and second decoders in successive decoding iterations. An outer code decoder connected following the PCCC decoder also can provide serial feedback information for enhancing iterative decisions by the PCCC decoder.

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ENCODING AND DECODING METHODS AND APPARATUS

This is a divisional application of Canadian Patent Application Serial No. 2,234,006 filed April 6, 1998.

This invention relates to encoding and decoding methods and apparatus. The invention can be applied to various systems which may be used for example for the communication or storage of signals, but is particularly applicable to, and is described below in the context of, CDMA (code division multiple access) communications which are increasingly being used in cellular wireless communications systems. As can be fully appreciated from the description below, the term "decoding" is used herein to embrace not only the function of decoding but also, where applicable, the functions of demodulation or other detection of a signal using soft and/or hard decisions, and the term "decoder" is used correspondingly.

Background

A class of parallel concatenated convolutional codes, also known as PCCCs or turbo codes, is known for example from an article by C. Berrou et al. entitled "Near Shannon Limit Error-Correcting Coding And Decoding: Turbo-Codes", Proceedings of the IEEE International Conference on Communications, 1993, pages 1064-1070. That article showed that a turbo code together with an iterative decoding algorithm could provide performance in terms of BER (Bit Error Rate) that is close to the theoretical limit. A turbo code encoder provides a parallel concatenation of two (or more) RSC (Recursive Systematic Convolutional) codes which are typically, but not necessarily, identical, applied to an input bit sequence and an interleaved version of this input bit sequence. The output of the encoder comprises systematic bits (the input bit sequence itself) and parity

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bits which can be "punctured" (selected) to provide a desired rate of encoding.

Various schemes are being proposed and developed to provide, especially for the communication of data in a CDMA (code division multiple access) communications system, a greater bandwidth (signal transmission rate) than is provided in a so-called IS-95 system which is compatible with TIA/EIA (Telecommunications Industry Associate/Electronic Industries Association) Interim Standard IS-95-A, "Mobile Station-Base Station Compatibility Standard for Dual-Mode Wideband Spread Spectrum Cellular System". Turbo coding has been proposed for such WCDMA (wideband CDMA) systems. However, turbo coding does not provide a great increase in code distance, which is a significant disadvantage for a BER of less than about 10^{-5} which is desirable for WCDMA systems.

It is desirable to optimize the application of turbo coding to WCDMA systems, in order to obtain maximum coding gains.

An object of this invention is to provide improved encoding and decoding methods and apparatus.

Summary of the Invention

According to one aspect the invention provides a method of encoding information comprising: a first step of encoding said information in accordance with an outer code to produce encoded information; and a subsequent step of encoding said encoded information in accordance in a parallel concatenated convolutional code encoder.

According to another aspect the invention provides encoding apparatus comprising a first encoder for encoding

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information in accordance with an outer code serially concatenated with a second encoder for encoding in accordance with an inner code the information encoded by the first encoder, the second encoder comprising a parallel concatenated convolutional code encoder comprising an interleaver for interleaving the information encoded by the first encoder and two recursive systematic convolutional encoders for encoding the information encoded by the first encoder at an input and an output of the interleaver.

10 Brief Description of the Drawings

The invention will be further understood from the following description with reference to the accompanying drawings, in which:

Fig. 1 illustrates a block diagram of a concatenated turbo code encoder in accordance with an embodiment of this invention;

Fig. 2 illustrates a block diagram of an RSC encoder which may be used in the encoder of Fig. 1; and

Fig. 3 illustrates a block diagram of a concatenated turbo code decoder in accordance with another embodiment of this invention.

Detailed Description

As discussed above, turbo coding does not provide a great increase in code distance. In the encoder of Fig. 1 this disadvantage is avoided by serially concatenating an outer code with an inner turbo code.

Referring to Fig. 1, the encoder comprises an outer code encoder 10 which is serially concatenated with an inner PCCC or turbo code encoder which is constituted in

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In a preferred form of the encoder of Fig. 1, the outer code is a Reed-Solomon (RS) code, which has the advantages that it provides a maximal code distance for given code parameters and that sophisticated decoding methods are known. An information sequence supplied to the outer code encoder 10 is encoded in accordance with a desired RS code in known manner, and the resulting encoded bit sequences are supplied to the inner code encoder 12 directly and to the inner code encoder 14 via the interleaver 16. For example, the desired RS code may be a (15,9) code with the generating polynomial:

$$g(x) = x^6 + \alpha^{10}x^5 + \alpha^{14}x^4 + \alpha^4x^3 + \alpha^6x^2 + 0x + \alpha^6 \quad (1)$$

where α is a primitive element of the Galois field GF(16) having the 16-element alphabet $0, \alpha^0, \alpha^1, \alpha^2, \dots, \alpha^{14}$.

The inner code encoders 12 and 14 are preferably identical RSC (recursive systematic convolutional) encoders which may for example be rate $\frac{1}{2}$ encoders operating in accordance with a generation matrix $G(D)$ given by:

$$G(D) = \left[\frac{1 + D^2 + D^3 + D^4}{1 + D + D^4} \right] \quad (2)$$

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Each of the encoders 12 and 14 produces at its outputs both systematic bits S, constituted directly by information bits supplied to the input of the encoder, and parity bits P which are produced by the encoding operation of the encoder. In the case of rate 1/2 encoders as described and illustrated here, for each information bit supplied to the input of the encoder 12 or 14 the encoder produces this information bit at its output as a systematic bit S1 or S2 respectively, and also produces by its encoding operation a parity bit P1 or P2 respectively so that there are two output bits for each input information bit (i.e. rate 1/2).

An implementation of each RSC encoder 12 or 14 is illustrated in Fig. 2, comprising four delay elements 22 each providing a delay T of one information bit period, and two modulo-2 adders 24 and 26. The systematic bit S is produced directly from the input, and the parity bit P is produced at the output of the adder 26.

The systematic and parity bits produced by the encoders 12 and 14 are supplied to the puncturing block 18 in the encoder of Fig. 1. These bits S1, P1 and S2, P2 are selected and passed by the puncturing block 18 in accordance with respective 2-bit puncturing codes that are shown in Fig. 1 at the respective inputs of this block. Thus the non-interleaved systematic bits S1 are all selected (code 11) to produce output bits x1, none of the interleaved systematic bits S2 are selected (code 00), and the parity bits P1 and P2 are selected alternately (codes 10 and 01 respectively) to produce output bits x2 and x3 respectively. Consequently, the block 18 selects four bits (two S1, one P1, and one P2) for every two information bits supplied to the input of the turbo coder, so that the entire turbo coder provides rate 1/2 encoding. The output bits x1, x2, and x3 of the puncturing block 18 are supplied to the modulator 20, which can operate in accordance with any desired modulation scheme, such as BPSK (binary phase shift keying).

Fig. 3 illustrates a decoder in accordance with another embodiment of this invention, for decoding information encoded by a serially concatenated RS outer encoder and a turbo code inner encoder for example as described above with reference to Figs. 1 and 2. Referring to Fig. 3, the decoder comprises a soft demodulator 30, first and second RSC decoders 32 and 34, interleavers 36 and 38, deinterleavers 40 and 42, an RS decoder 44, and summing functions 46, 48, and 50.

The demodulator 30 has soft demodulation outputs y1, y2, and y3 corresponding respectively to the bits x1, x2, and x3; thus the soft demodulation output y1 represents (non-interleaved) systematic bits and the soft demodulation outputs y2 and y3 represent the parity bits for the non-interleaved path (encoder 12) and the interleaved path (interleaver 16 and encoder 14) of the turbo code encoder of Fig. 1. As is well known, each soft output or soft decision for a respective bit is a probability that the bit is a binary 0 or 1, or a ratio of such probabilities or a maximum likelihood ratio.

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The units 32, 34, 36, 38, 40, 46, and 48 of Fig. 3 constitute a turbo inner code decoder having a parallel feedback path 52 for iterative decoding in successive passes through the decoder. The general nature of turbo or iterative decoding is known for example from the article by C. Berrou et al. referred to above. Each iteration or pass of information through the decoders 32 and 34 serves to enhance soft decisions produced by the decoders for the received signals in each frame of interleaved blocks, so that a few iterations can provide a substantial error correction if the input signals to the decoder and so-called extrinsic information are uncorrelated. Extrinsic information is a likelihood or probability function of redundant information introduced by the encoding process, and is also explained for example in the article by C. Berrou et al. By way of example, each of the soft decision decoders 32 and 34 can perform maximal *a posteriori* probability (MAP) decoding in accordance with a so-called BCJR algorithm known for example from an article by L. R. Bahl et al. entitled "Optimal Decoding of Linear Codes for Minimizing Symbol Error Rate", IEEE Transactions on Information Theory, vol. IT-20, pages 248-287, March 1974. Alternatively the decoders 32 and 34 may perform maximum MAP (MAX-MAP) decoding or Soft-Output Viterbi Algorithm (SOVA) decoding which are also known in the art.

The non-interleaved soft demodulation outputs y_1 and y_2 are supplied to the first decoder 32, whose soft decision outputs in a first pass through the decoder are supplied via the summing function 46 to the interleaver 38, where they are interleaved in the same manner as in the interleaver 16 in the encoder of Fig. 1. The soft demodulation output y_1 representing systematic bits is also similarly interleaved by the interleaver 36, and the outputs of the interleavers 36 and 38, and the (interleaved) soft demodulation output y_3 of the demodulator 30, are supplied to the second decoder 34. The soft decisions produced by the second decoder 34 are fed back on the parallel feedback path 52 to the summing function 50, to a subtracting input of which the output of the interleaver 38 is also supplied, so that the summing function 50 produces feedback extrinsic information which is supplied to and deinterleaved by the deinterleaver 40.

In one or more subsequent decoding iterations, the extrinsic information from the output of the deinterleaver 40 is supplied via the summing function 48 (discussed further below) to be used by the first decoder 32 to enhance its soft decoding decisions, and is supplied to a subtractive input of the summing function 46 to provide forward extrinsic information which is interleaved by the interleaver 38 and used by the second decoder 34 to enhance its soft decoding decisions.

The soft decoding decisions of the second decoder 34 are also deinterleaved by the deinterleaver 42 and supplied to the outer code decoder 44, which in a preferred embodiment of the invention is a soft decision RS decoder for decoding the outer RS code. The soft decision outputs of this decoder 44 are optionally supplied to a serial

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information which is interleaved by the interleaver 38 and used by the second decoder 34 to enhance its soft decoding decisions.

The soft decoding decisions of the second decoder 34 are also deinterleaved by the deinterleaver 42 and supplied to the outer code decoder 44, which in a preferred embodiment of the invention is a soft decision RS decoder for decoding the outer RS code. The soft decision outputs of this decoder 44 are optionally supplied to a serial feedback path 54 to the summing function 48, so that this information is combined with the parallel feedback extrinsic information supplied to the first decoder 32 to further enhance its soft decisions in a further iterative process.

After a desired number of iterations, a hard (binary) output which constitutes the final decision output of the overall decoder is produced by the outer code decoder 44 by comparing each respective soft decision with a threshold. Conveniently each soft decision is a number whose magnitude represents probability and whose sign represents whether this probability refers to a 0 or 1 bit, in which case the threshold comparison can be constituted by a sign function in the decoder 44.

Although not illustrated in Fig. 3, it can be appreciated that weighting functions can be provided as desired or necessary in the paths to any of the summing functions 46, 48, and 50.

Instead of deriving the input to the decoder 44 from the output of the second decoder 34 via the deinterleaver 42, it could be derived directly from the output of the first decoder 32. The serial feedback path could instead be coupled to the second decoder 34.

Although the functions of the encoder of Figs. 1 and 2 and the decoder of Fig. 2 are represented as separate units, it should be appreciated that these functions can be implemented by functions of one or more digital signal processors (DSPs) and/or application specific integrated circuits (ASICs).

In addition, although as indicated above the invention can be of particular advantage in WCDMA communications systems, it can be appreciated that the principles of the invention can also be applied advantageously in other types of communications system, especially for example in satellite wireless communications systems.

Thus although specific embodiments of the invention have been described above, it can be appreciated that numerous modifications, variations, adaptations and combinations of the aspects thereof may be made within the scope of the invention as defined in the claims.

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CLAIMS:

1. A method of encoding information comprising:

 a first step of encoding said information in
accordance with an outer code to produce encoded
5 information; and

 a subsequent step of encoding said encoded
information in accordance in a parallel concatenated
convolutional code encoder.
2. A method as claimed in claim 1 wherein the first
10 step comprises Reed-Solomon encoding.
3. Encoding apparatus comprising a first encoder for
encoding information in accordance with an outer code
serially concatenated with a second encoder for encoding in
accordance with an inner code the information encoded by the
15 first encoder, the second encoder comprising a parallel
concatenated convolutional code encoder comprising an
interleaver for interleaving the information encoded by the
first encoder and two recursive systematic convolutional
encoders for encoding the information encoded by the first
20 encoder at an input and an output of the interleaver.
4. Encoding apparatus as claimed in claim 3 and
including means for selectively passing systematic and
parity information produced by the two recursive systematic
convolutional encoders.
- 25 5. Encoding apparatus as claimed in claim 3 or 4
wherein the first encoder comprises a Reed-Solomon encoder.

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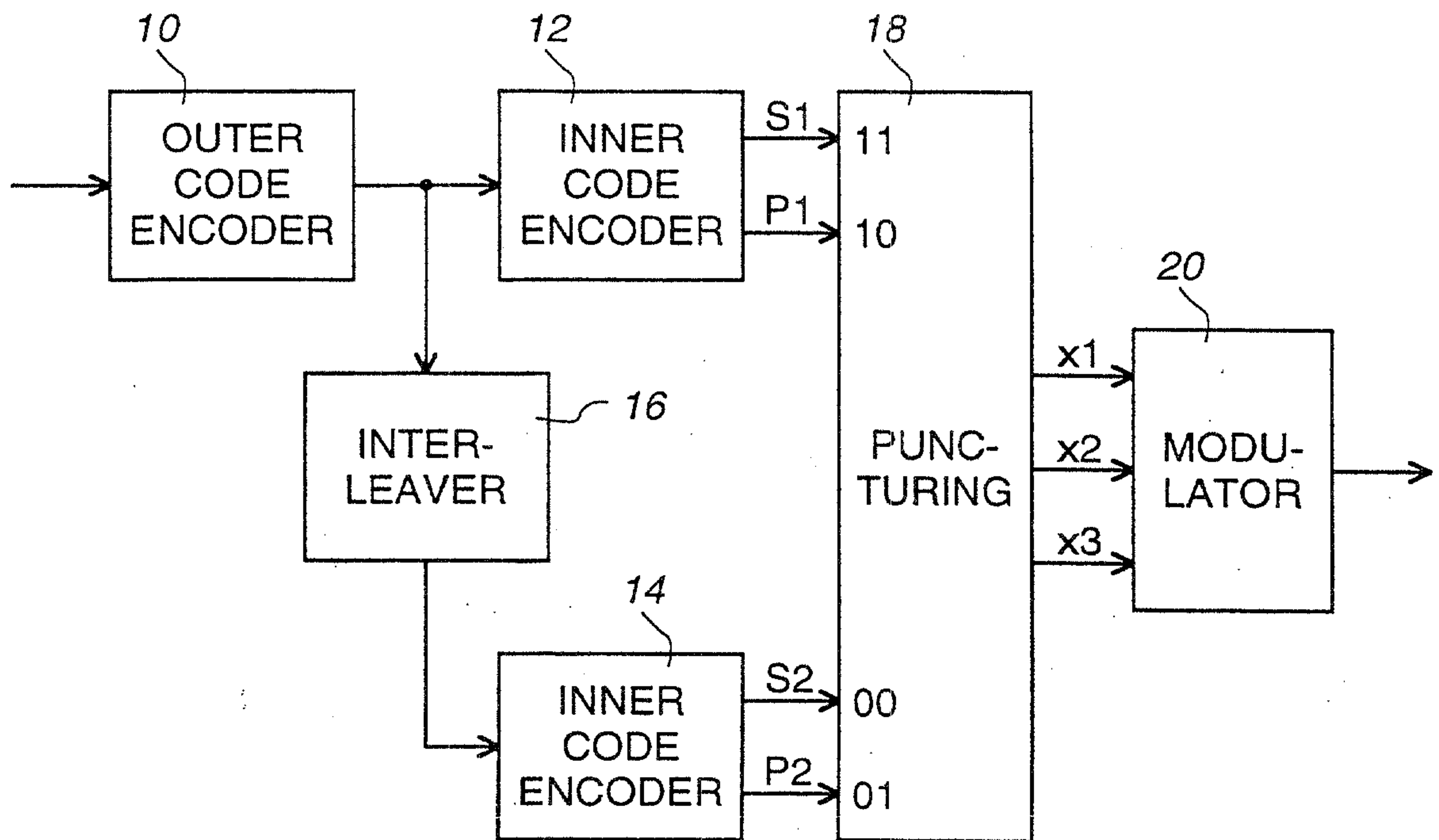


Fig. 1

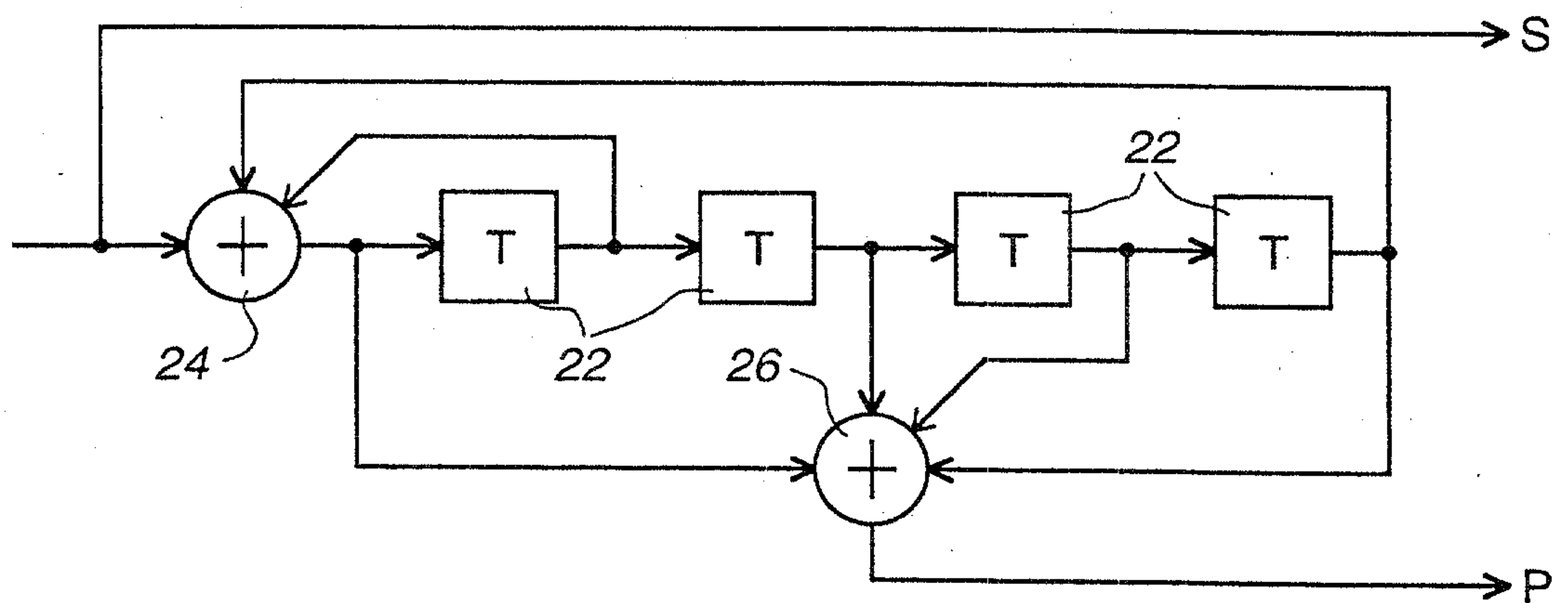


Fig. 2

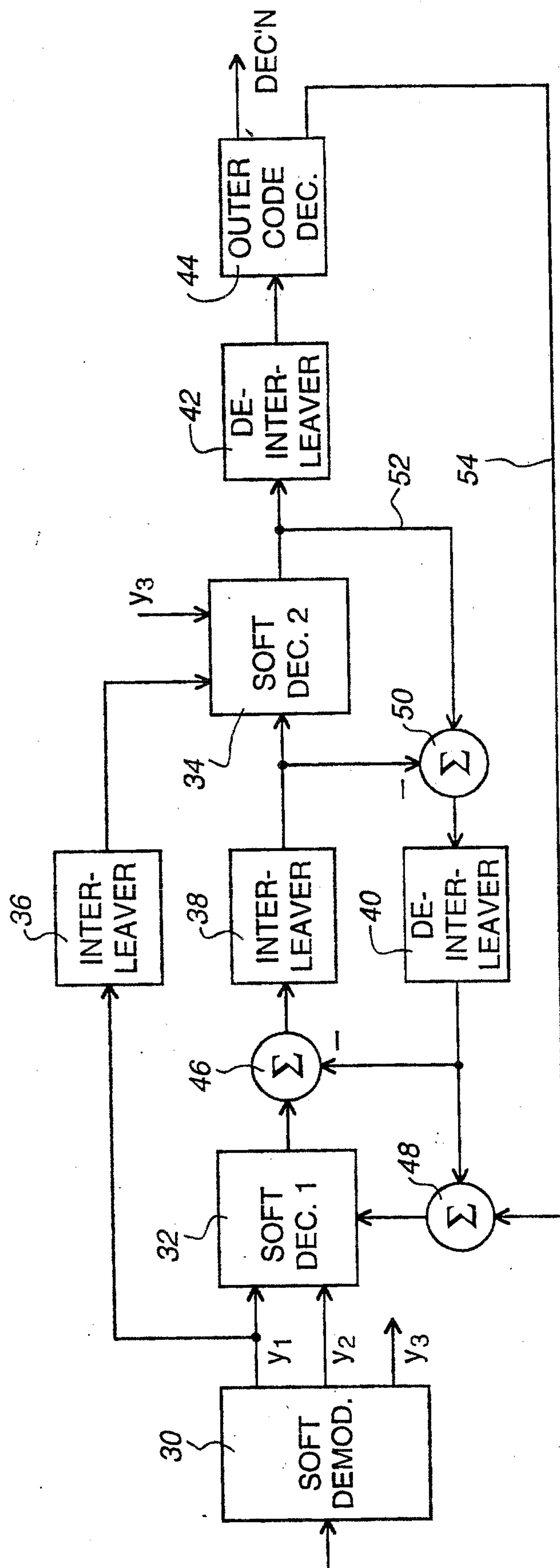


Fig. 3

