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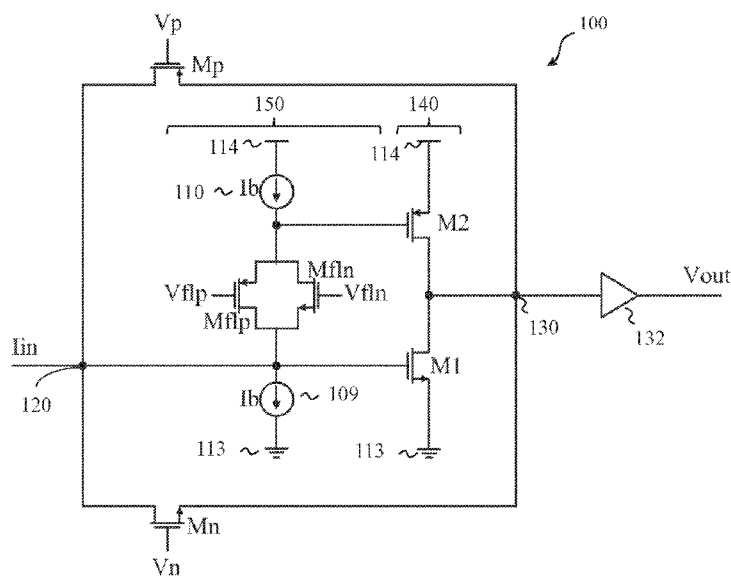


Fig. 1

(57) Abstract: Systems and methods according to one or more embodiments are provided for a current comparator with biasing circuitry to provide for low power consumption and high-speed performance. In one example, a system includes an input port to receive a current pulse and an amplifier configured to provide a voltage pulse at an output port in response to the current pulse. The system also includes a first biasing circuit coupled between the output port and the input port to selectively limit a voltage at the input port. The system further includes a second biasing circuit coupled to the amplifier to selectively adjust a bias of the amplifier.



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HIGH-SPEED CURRENT COMPARATOR SUITABLE FOR NANO-POWER CIRCUIT DESIGN

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CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of and priority to U.S. Provisional Patent Application No. 62/419,416 filed November 8, 2016 and entitled “HIGH-SPEED CURRENT COMPARATOR SUITABLE FOR NANO-POWER CIRCUIT DESIGN,” which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] The present invention relates generally to analog signal processing and, more particularly, to a high-speed current comparator circuit suitable for nano-power circuits.

BACKGROUND

[0003] In the field of analog signal processing, it is becoming increasingly critical to reduce power consumption and increase speed in advanced analog integrated circuits used in battery operated systems such as mobile devices, for example. To meet this need, DC to DC converters and data converters are being designed with nanoampere or microampere range power consumptions. However, current comparators used in DC to DC converters and data converters, for example, may require a tradeoff with current comparator speed to reduce power consumption.

[0004] Current comparator speed may be defined as the inverse of the delay between the time at which the input current changes polarity and the time at which the comparator output toggles. To reduce the delay, and subsequently increase comparator speed, internal parasitic capacitors must be charged at a faster rate. Therefore, conventional current comparators designed for a reduction in power consumption may lack the necessary speed required to support advanced DC to DC converters and data converter applications. Thus, there is a need in the art for improved current comparator solutions that reduce power consumption while achieving a speed suitable for applications in DC to DC converters.

SUMMARY

[0005] In accordance with various embodiments further discussed herein, method and systems for implementing a high-speed current comparator suitable for non-power circuits are provided.

[0006] In one or more embodiments, a system includes an input port, an amplifier, a first biasing circuit and a second biasing circuit. The input port is arranged to receive a current pulse. The amplifier (e.g., a class AB amplifier with a CMOS output stage) is operable to provide a voltage pulse at an output port in response to the received current pulse. The first biasing circuit is coupled between the output port and the input port and is operable to selectively limit a voltage at the input port. In one embodiment, the first biasing circuit includes a non-linear feedback circuit coupled between the output port and the input port to provide the selectively limited voltage at the input port. The second biasing circuit is coupled to the amplifier and configured to selectively adjust the bias of the amplifier. In various embodiments, the second biasing circuit includes one or more of a class AB amplifier biasing circuit, a positive bias voltage circuit providing a selectively adjustable positive bias voltage to the amplifier, and a negative bias voltage circuit providing a selectively adjustable negative bias voltage to the amplifier.

[0007] In one or more embodiments, the system may also include a bias current circuit providing a selectively adjustable bias current to the amplifier to control a quiescent current of the amplifier. The system may also include a selectively adjustable positive power source coupled to the first biasing circuit and a selectively adjustable negative power source coupled to the first biasing circuit.

[0008] A method in accordance with one or more embodiments, includes receiving, at an input port, a current pulse and providing, by an amplifier, a voltage pulse at an output port in response to the current pulse. The method further includes selectively limiting, by a first biasing circuit coupled between the output port and the input port, a voltage at the input port, and selectively adjusting, by a second biasing circuit coupled to the amplifier, a bias of the amplifier. In various embodiments of the method, the amplifier is configured as a class AB amplifier comprising a CMOS output stage, and the second biasing circuit is configured as a class AB amplifier biasing circuit. In one embodiment, the first biasing circuit includes a non-linear feedback circuit coupled between the output port and the input port to provide the selectively limited voltage at the input port. The second biasing circuit may include a positive bias voltage circuit and a negative bias voltage circuit.

[0009] The method may further include selectively adjusting, by the positive bias voltage circuit, a positive bias voltage provided to the amplifier, and selectively adjusting, by the negative bias voltage circuit, a negative bias voltage provided to the amplifier. In one or more embodiments the method may include selectively adjusting, by a bias current circuit, a bias current provided to the amplifier to control a quiescent current of the amplifier. The method may also include selectively adjusting a positive power source coupled to the first biasing circuit, and selectively adjusting a negative power source coupled to the first biasing circuit.

[0010] The scope of the present disclosure is defined by the claims, which are incorporated into this section by reference. A more complete understanding of the present disclosure will be afforded to those skilled in the art, as well as a realization of additional advantages thereof, by a consideration of the following detailed description of one or more embodiments. Reference will be made to the appended sheets of drawings that will first be described briefly.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Fig. 1 illustrates a schematic diagram of a high-speed low power current comparator in accordance with an embodiment of the disclosure.

[0012] Fig. 2 illustrates a process of using a high-speed low power current comparator in accordance with an embodiment of the disclosure.

[0013] Fig. 3 illustrates a high-speed low power current comparator implemented in a voltage-mode comparator in accordance with an embodiment of the disclosure.

[0014] Fig. 4 illustrates a schematic diagram of a voltage-mode comparator in accordance with an embodiment of the disclosure.

[0015] Fig. 5 illustrates a high-speed low power current comparator implemented in a low power successive approximation analog to digital converter in accordance with an embodiment of the disclosure.

[0016] The included drawings are for illustrative purposes and serve only to provide examples of possible systems and methods for the disclosed methods and system for providing a high-speed low power current comparator circuit. These drawings in no way limit any changes in form and detail that may be made to that which is disclosed by one skilled in the art without departing from the spirit and scope of this disclosure.

DETAILED DESCRIPTION

[00017] The present disclosure describes systems and methods that address a need in the art of signal processing for providing a current comparator with low power consumption and high-speed performance. The current comparator in the present disclosure describes a current comparator that operates with a bias current in the nanoampere range while achieving a speed suitable for applications in DC to DC converters.

[00018] In one embodiment, a high-speed low power current comparator is designed with a non-linear feedback circuit coupled between input and output ports to fix a voltage at the input port less than the supply voltage. The non-linear feedback circuit fixes the voltage at the input port for both a positive voltage and a negative voltage to avoid rail to rail voltage excursions. In this regard, a faster comparator output response time results in fixing the input voltage less than the supply voltage. As used herein, the term “couple” and its cognate terms such as “couples” and “coupled” can include a direct connection, a connection through intervening devices or elements, a hard-wired connection, an integrated circuit connection, a bus or other suitable connections.

[00019] In various embodiments, an output stage of a current comparator class AB amplifier is biased with a biasing circuit. The biasing circuit includes positive and negative bias circuits to selectively adjust a bias voltage and a bias current of the current comparator amplifier. Bias voltage and bias current may be set to reduce power consumption within the current comparator. Furthermore, comparator output response time may be decreased by adjusting a channel length and channel width of the current comparator amplifier output transistors to minimize transistor internal parasitic capacitance. In this regard, a faster output response time may be realized by minimizing channel length and channel width to reduce the time to charge internal parasitic capacitance. Significantly, bias voltages, bias currents, and quiescent currents of the current comparator may be controlled independent of transistor channel length and channel width to optimize both power consumption and speed of the current comparator. In this regard, the present current comparator may operate with a bias current in the nanoampere range and achieve a faster output response time suitable for DC to DC converter applications.

[00020] Embodiments of the present disclosure may be contrasted to pre-existing solutions for reducing current comparator power consumption and providing a faster output response time. Such solutions typically achieve a faster output response time, but with an increase in power consumption. For example, conventional current comparators may utilize the non-linear feedback circuit coupled between input and output ports to provide a faster output

response time by fixing the voltage at the current comparator input to approximately one half the supply voltage. However, utilizing this technique in conventional current comparators causes a quiescent current to flow through the output amplifier stage. The quiescent current depends on the on-resistance of the output stage transistors. Additionally, the quiescent current may change with variations in transistor process, temperature, and supply voltages resulting in a current of approximately ten to hundreds of microamperes. In this regard, the quiescent current may provide a faster output response time by reducing the time to charge internal parasitic capacitance. However, there may be a resultant increase in power consumption due to the high quiescent current.

[00021] Conventional solutions for reducing quiescent current and reducing power consumption rely on adjusting a channel length and channel width of current comparator output transistors. In this regard, in order to reduce quiescent current, the ratio between channel width and channel length (e.g., W/L) of the amplifier stage transistors must be decreased. After the channel width is reduced to the minimum allowed by the transistor technology, the ratio can only be decreased by increasing the channel length. However, increasing the channel length causes a subsequent increase in transistor internal parasitic capacitance resulting in a longer comparator delay. Thus, conventional solutions may provide for either a faster current comparator output response time or a reduction in power consumption. Therefore, conventional solutions do not provide for both a reduction in power consumption and a faster output response time as in the present disclosure.

[00022] Fig. 1 illustrates a schematic diagram of a high-speed low power current comparator system 100 in accordance with an embodiment of the disclosure. System 100 may be used in audio analog signal processing applications to convert a current pulse to a voltage pulse in accordance with various techniques described herein. System 100 may be used on a variety of platforms, such as computers, smartphones, tablets, and other devices requiring audio analog signal processing techniques. In some embodiments, system 100 may be used in applications requiring both high speed and low DC power consumption.

[00023] In some embodiments, system 100 converts a positive input current pulse to a corresponding positive output voltage pulse of approximately the same duration. Additionally, system 100 converts a negative input current pulse to a corresponding negative output voltage pulse of approximately the same duration. System 100 may be used in a variety of circuits such as DC to DC converters and/or data converters operating in a nanoampere or microampere range. Current comparator may be implemented in silicon or

other suitable materials, and may be constructed from discrete devices, formed as integrated circuits, or can be constructed in other suitable manners.

[00024] In one embodiment, system 100 includes a PMOS transistor M_p and an NMOS transistor M_n which form a feedback clamp (e.g., a first biasing circuit) to selectively limit a voltage at an input port 120. The drain of PMOS transistor M_p is coupled to the drain of NMOS transistor M_n to provide a negative feedback and prevents the input voltage from swinging to either rail such as positive bias voltage V_p and/or negative bias voltage V_n . For example, as a positive current I_{in} is flowing into input port 120, NMOS transistor M_n is driven into an ON state and a negative feedback is created, fixing a positive voltage at input port 120. Similarly, when a negative current I_{in} is flowing from input port 120, PMOS transistor M_p is driven into an ON state and a feedback is created, fixing a negative voltage at input port 120. The voltage at input port 120 is limited to approximately the average voltage of a positive power source 114 and a negative power source 113 (e.g., such as DC ground). Limiting a positive and negative input voltage range avoids rail-to-rail commutation and provides for faster response times of system 100. Furthermore, the input voltage range may be limited due to a high gain of amplifier 140, discussed herein.

[00025] In some embodiments, positive bias voltage 103 may be a positive five volts direct current (DC) voltage power source. In some embodiments, negative bias voltage V_n may be a negative five volts DC voltage power source. However, in various embodiments, positive bias voltage V_p is less than positive power source 114 voltage by at least a PMOS threshold voltage (e.g., such as PMOS M_p), and negative bias voltage V_n is greater than negative power source 113 voltage by at least an NMOS threshold voltage (e.g., such as NMOS M_n). In various embodiments, the voltage V_p may be greater than or less than the voltage V_n . Other positive and negative DC voltage power sources may be provided in other embodiments.

[00026] The gate of PMOS transistor M_p is coupled to positive bias voltage V_p . The source of PMOS transistor M_p is coupled to output port 130. Positive bias voltage V_p may be adjusted to limit a positive output voltage at output port 130. In this regard, transistor M_p limits positive output voltage at output port 130 to a voltage less than the sum of positive bias voltage 103 plus V_{thp} . The gate of NMOS transistor M_n is coupled to negative bias voltage V_n . The source of NMOS transistor M_n is coupled to output port 130. Negative bias voltage V_n may be adjusted to limit a negative output voltage at output port 130. In this regard, transistor M_n limits negative output voltage at output port 130 to a voltage greater than the sum of negative bias voltage V_n plus V_{thn} . Line buffer 132 may be coupled to the output port 130 to provide buffering of output voltage signal V_{out} 102.

[00027] In some embodiments, system 100 includes an NMOS transistor M1 and a PMOS transistor M2 formed as amplifier 140. In some embodiments, amplifier 140 is formed as a class AB amplifier. NMOS transistor M1 and PMOS transistor M2 may be arranged as a CMOS output stage. The source of NMOS transistor M1 may be coupled to the negative power source 113 (e.g., DC ground). The gate of transistor M1 may be coupled to a bias current circuit 109. The source of PMOS transistor M2 may be coupled to positive power source 114. The gate of transistor M2 may be coupled to a bias current circuit 110. Drains of NMOS transistor M1 and PMOS transistor M2 may be coupled to output port 130 to provide a positive magnitude output voltage V_{out} 102 and/or a negative magnitude output voltage V_{out} 102 in response to input current I_{in} . In some embodiments, positive power source 114 may be a positive five volts DC voltage power source. However, other positive and/or negative DC voltage power sources may be provided in other embodiments.

[00028] PMOS transistor Mflp, NMOS transistor Mfln, bias current circuit 109, and bias current circuit 110 form a biasing circuit 150 (e.g., a second biasing circuit) for biasing amplifier 140. Biasing circuit 150 may be used to selectively adjust a bias of amplifier 140 and limit amplifier 140 quiescent current. Quiescent current is the current drawn by amplifier 140 when it is not amplifying an input signal. Quiescent current adds to system 100 power consumptions and by selectively limiting quiescent current in amplifier 140, power consumption may be reduced in system 100.

[00029] In some embodiments, biasing circuit 150 is implemented as a class AB amplifier biasing circuit. Biasing circuit 150 may include a positive bias voltage circuit formed by PMOS transistor Mflp and a negative bias voltage circuit formed by NMOS transistor Mfln. The gate of PMOS transistor Mflp is coupled to adjustable positive bias voltage source Vflp to selectively adjust a positive bias voltage of amplifier 140. The gate of NMOS transistor Mfln is coupled to adjustable negative bias voltage source Vfln to selectively adjust a negative bias voltage of amplifier 140.

[00030] In some embodiments, biasing circuit 150 includes bias current circuits 109/110 to selectively limit a bias current of amplifier 140. In some embodiments, bias current circuit 109 is coupled to gate of NMOS transistor M1 at a first end and the negative power source 113 at a second end. Bias current circuit 109 selectively limits bias current to NMOS transistor M1. In some embodiments, bias current circuit 110 is coupled to positive power source 114 at a first end and gate of PMOS transistor M2 at a second end. Bias current circuit 110 selectively limits bias current to PMOS transistor M2. In some embodiments, bias currents 109/110 may be selectively adjusted to provide a bias current in an approximate

range of nanoamperes to reduce power consumption of system 100. However, other bias currents 109/110 ampere ranges are possible in other embodiments.

[00031] Various biasing techniques suitable for the present embodiment are described in “Advanced Low Voltage and High-Speed Techniques for BiCMOS, CMOS and Bipolar Operational Amplifier”, K. De Langen, Delft University Press, November 1999, which is hereby incorporated by reference. Other class AB biasing techniques may also be used for biasing amplifier 140.

[00032] In general, bias voltages V_{flp} , V_{fln} , the bias current generated by bias current circuit 109, and the bias current generated by bias current circuit 110 may be selectively adjusted to reduce a quiescent current of transistor M1, and transistor M2 of amplifier 140 to minimize power consumption. Furthermore, comparator delay (e.g., delay between the time at which the input current changes polarity and the time at which the comparator output toggles) may be reduced in system 100 by adjusting a channel length and channel width of each of amplifier 140 transistors M1, and M2 to minimize transistor internal parasitic capacitance. In this regard, a decrease in output response time of system 100 may be realized by a reduction in time to charge internal parasitic capacitance.

[00033] Bias voltages, bias currents, and quiescent currents of system 100 may be controlled independent of transistor channel length and channel width to provide for both a reduction in power consumption and a faster output response time. Significantly, system 100 may operate with a bias current in the nanoampere range while achieving a speed suitable for application in a DC to DC converter, for example.

[00034] Fig. 2 illustrates a process of using the high-speed low power current comparator system 100 in accordance with an embodiment of the disclosure.

[00035] In block 201, system 100 may receive a current pulse I_{in} of a specified duration at input port 120. In some embodiments, current pulse I_{in} may be a positive magnitude current pulse and/or a negative current magnitude pulse.

[00036] In block 202, amplifier 140 may convert current pulse I_{in} to a corresponding voltage pulse V_{out} 102. In some embodiments, voltage pulse V_{out} 102 may be a positive magnitude voltage pulse and/or a negative magnitude voltage pulse in accordance with the corresponding current pulse I_{in} . Voltage pulse V_{out} 102 may be delayed relative to current pulse I_{in} , such as a delay between the time at which the input current changes polarity and the time at which the comparator output toggles, as discussed herein. Biasing circuit 150 may reduce the delay in system 100, as discussed herein.

[00037] In block 203, PMOS transistor Mp 101 and NMOS transistor Mn 102, which form a feedback clamp (e.g., a first biasing circuit), selectively limit the positive and negative voltage magnitude at input port 120. Furthermore, positive bias voltage Vp 103 may be adjusted to limit a positive output voltage at output port 130 and negative bias voltage Vn may be adjusted to limit a negative output voltage at output port 130.

[00038] In block 204, biasing circuit 150 may selectively adjust a bias of amplifier 140. In this regard, biasing circuit 150 may selectively adjust bias voltages, bias currents, and quiescent currents of NMOS transistor M1 111 and/or PMOS transistor M2 112.

[00039] Fig. 3 illustrates a high-speed low power current comparator system 100 implemented in a voltage-mode comparator 300 in accordance with an embodiment of the disclosure. For example, operational trans-impedance amplifier (OTA) 305 may receive two voltage signals, a voltage signal Vin and a voltage signal Vref at corresponding OTA input ports 307 and 309, respectively. OTA 305 may process signals Vin and Vref and generate an output current signal proportional to the difference between signals Vin and Vref at an OTA output port 311. The output current signal is received at input port 120, processed by system 100, and a corresponding output voltage Vout 302 is provided at output port 130. In this regard, the high-speed low power current comparator system 100 is capable of combining with other analog signal processing elements to provide a robust comparator circuit.

[00040] Fig. 4 illustrates a schematic diagram of a voltage-mode comparator 300 in accordance with an embodiment of the disclosure. As shown in Fig. 4, voltage-mode comparator 300 functions as a voltage-mode continuous-time comparator without hysteresis. As illustrated in Fig. 4, transistor Mp 101 and transistor Mn 102 form a feedback clamp to selectively limit positive bias voltage Vp 103 and/or negative bias voltage Vn at input port 120. In this regard, the parasitic capacitance associated with transistors of OTA 305 (e.g., gate, drain, and source parasitic capacitance) coupled to OTA output port 311 are biased near the selectively limited voltages, as discussed herein. Advantageously, the time required to charge parasitic capacitances of OTA 305 are reduced in response to a polarity change of the difference voltage Vin minus Vref, resulting in a lower time delay of electrical signal propagation from input port 120 to output port 130 in system 100.

[00041] Fig. 5 illustrates a high-speed low power current comparator implemented in a low power successive approximation analog to digital converter 500 in accordance with an embodiment of the disclosure. In some embodiments, the low power successive approximation analog to digital converter (e.g., low power SAR ADC) may be used in an audio circuit where low power and high speed are required. In this regard, an input voltage

V_{in} and a reference voltage V_{ref} are received at OTA input ports 307 and 309, respectively. OTA 305 and high-speed low power current comparator system 100 perform voltage to current operations and comparator operations, respectively, to provide an output signal V_{out} at output port 130. A SAR logic circuit, based on the value of V_{out} , adjusts the DAC code 503 until an output current 505 of a Current DAC is arbitrarily close to the current I_{in} provided at OTA output port 311. Thus, the successive approximation analog to digital converter 500 converts an analog waveform (e.g., V_{in}) into a discrete digital signal representative of V_{in} for use in various embodiments of the audio analog signal processing circuits, as discussed herein.

[00042] Where applicable, various embodiments provided by the present disclosure may be implemented using hardware, software, or combinations of hardware and software. Also, where applicable, the various hardware components and/or software components set forth herein may be combined into composite components comprising software, hardware, and/or both without departing from the spirit of the present disclosure. Where applicable, the various hardware components and/or software components set forth herein may be separated into sub-components comprising software, hardware, or both without departing from the scope of the present disclosure. In addition, where applicable, it is contemplated that software components may be implemented as hardware components and vice-versa.

[00043] Software, in accordance with the present disclosure, such as program code and/or data, may be stored on one or more computer readable mediums. It is also contemplated that software identified herein may be implemented using one or more general purpose or specific purpose computers and/or computer systems, networked and/or otherwise. Where applicable, the ordering of various steps described herein may be changed, combined into composite steps, and/or separated into sub-steps to provide features described herein.

[00044] Embodiments described above illustrate but do not limit the invention. It should also be understood that numerous modifications and variations are possible in accordance with the principles of the present invention. Accordingly, the scope of the invention is defined only by the following claims.

CLAIMS

What is claimed is:

1. A system comprising:
an input port arranged to receive a current pulse;
an amplifier configured to provide a voltage pulse at an output port in response to the current pulse;
a first biasing circuit coupled between the output port and the input port and configured to selectively limit a voltage at the input port; and
a second biasing circuit coupled to the amplifier and configured to selectively adjust a bias of the amplifier.
2. The system of claim 1, wherein the amplifier is configured as a class AB amplifier comprising a CMOS output stage.
3. The system of claim 1, wherein the second biasing circuit is configured as a class AB amplifier biasing circuit.
4. The system of claim 3, wherein the second biasing circuit comprises a positive bias voltage circuit and a negative bias voltage circuit.
5. The system of claim 4, wherein the positive bias voltage circuit provides a selectively adjustable positive bias voltage to the amplifier.
6. The system of claim 4, wherein the negative bias voltage circuit provides a selectively adjustable negative bias voltage to the amplifier.
7. The system of claim 4, further comprising a bias current circuit, wherein the bias current circuit provides a selectively adjustable bias current to the amplifier to control a quiescent current of the amplifier.
8. The system of claim 1, wherein the first biasing circuit comprises a non-linear feedback circuit coupled between the output port and the input port to provide the selectively limited voltage at the input port.

9. The system of claim 1, further comprising a selectively adjustable positive power source coupled to the first biasing circuit.

10. The system of claim 1, further comprising a selectively adjustable negative power source coupled to the first biasing circuit.

11. A method comprising:
receiving, at an input port, a current pulse;
providing, by an amplifier, a voltage pulse at an output port in response to the current pulse;
selectively limiting, by a first biasing circuit coupled between the output port and the input port, a voltage at the input port; and
selectively adjusting, by a second biasing circuit coupled to the amplifier, a bias of the amplifier.

12. The method of claim 11, wherein the amplifier is configured as a class AB amplifier comprising a CMOS output stage.

13. The method of claim 11, wherein the second biasing circuit is configured as a class AB amplifier biasing circuit.

14. The method of claim 13, wherein the second biasing circuit comprises a positive bias voltage circuit and a negative bias voltage circuit.

15. The method of claim 14, further comprising selectively adjusting, by the positive bias voltage circuit, a positive bias voltage provided to the amplifier.

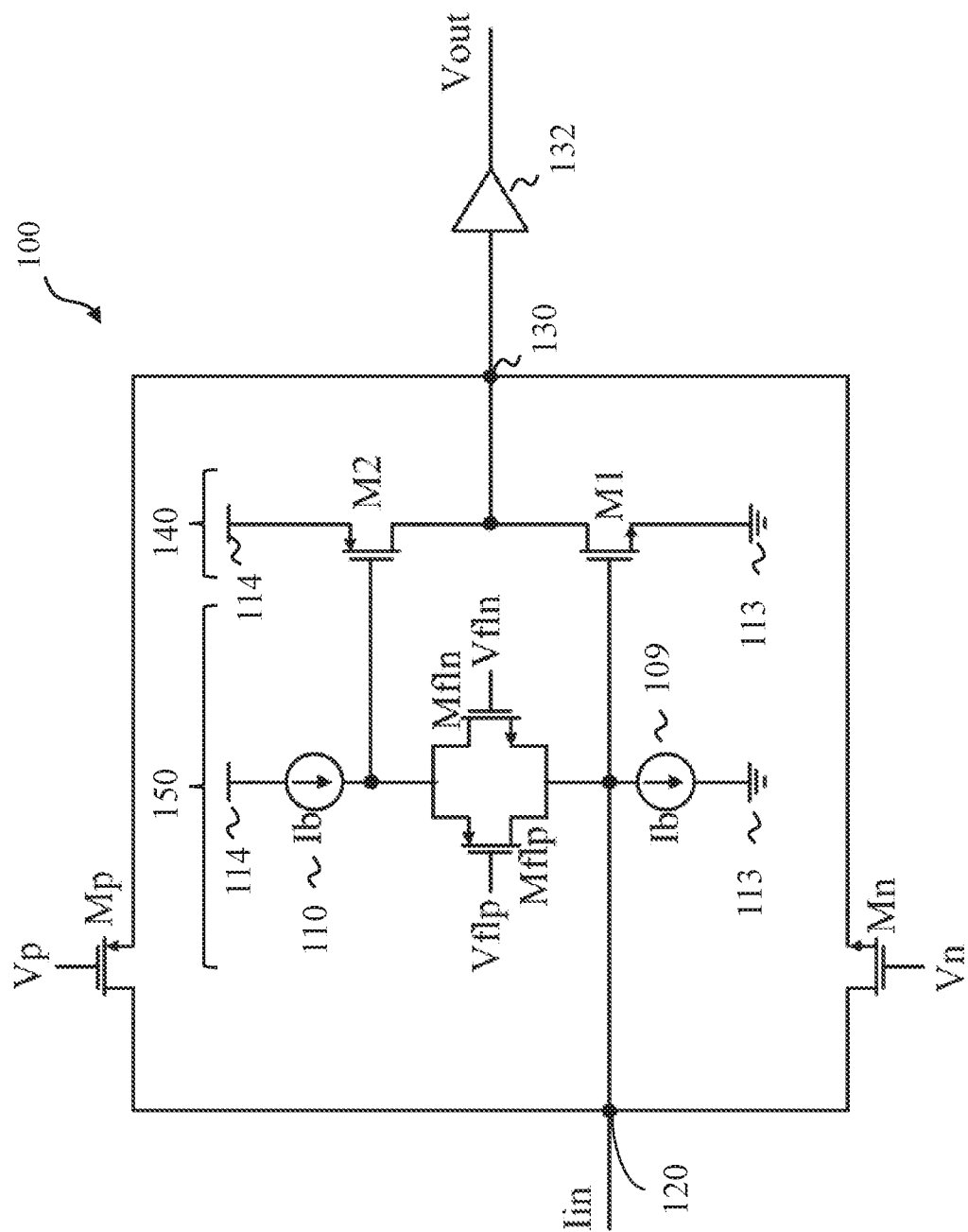
16. The method of claim 14, further comprising selectively adjusting, by the negative bias voltage circuit, a negative bias voltage provided to the amplifier.

17. The method of claim 14, further comprising selectively adjusting, by a bias current circuit, a bias current provided to the amplifier to control a quiescent current of the amplifier.

18. The method of claim 11, wherein the first biasing circuit comprises a non-linear feedback circuit coupled between the output port and the input port to provide the selectively limited voltage at the input port.

19. The method of claim 11, further comprising selectively adjusting a positive power source coupled to the first biasing circuit.

20. The method of claim 11, further comprising selectively adjusting a negative power source coupled to the first biasing circuit.



100

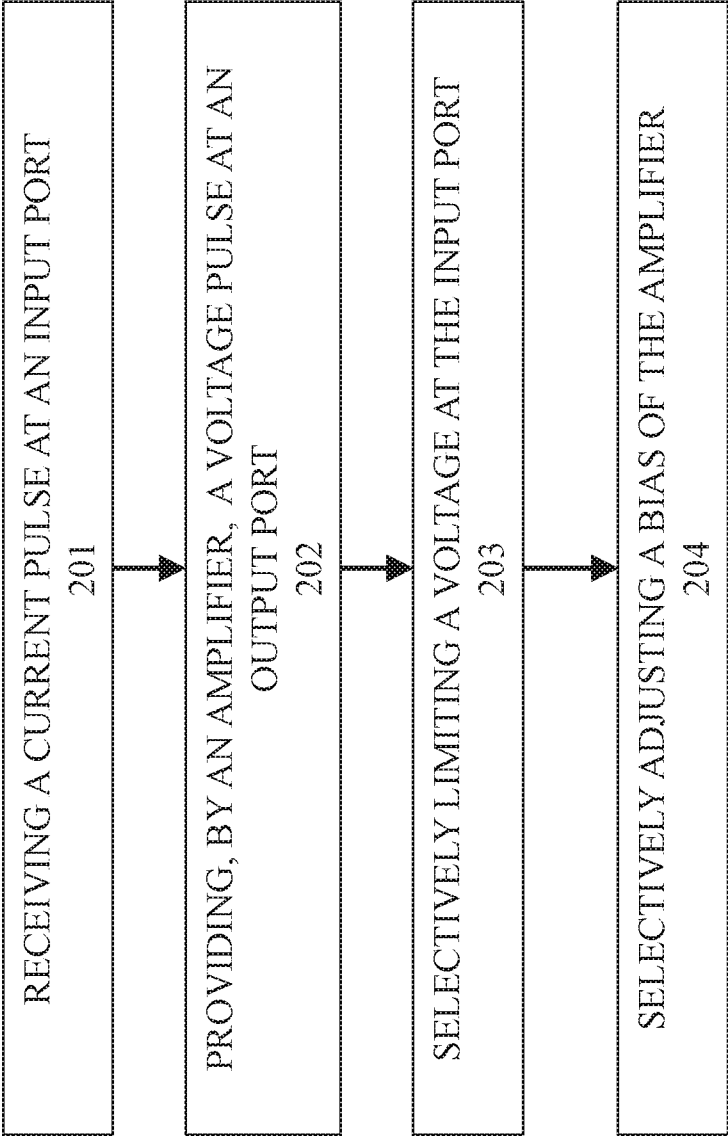


FIG. 2

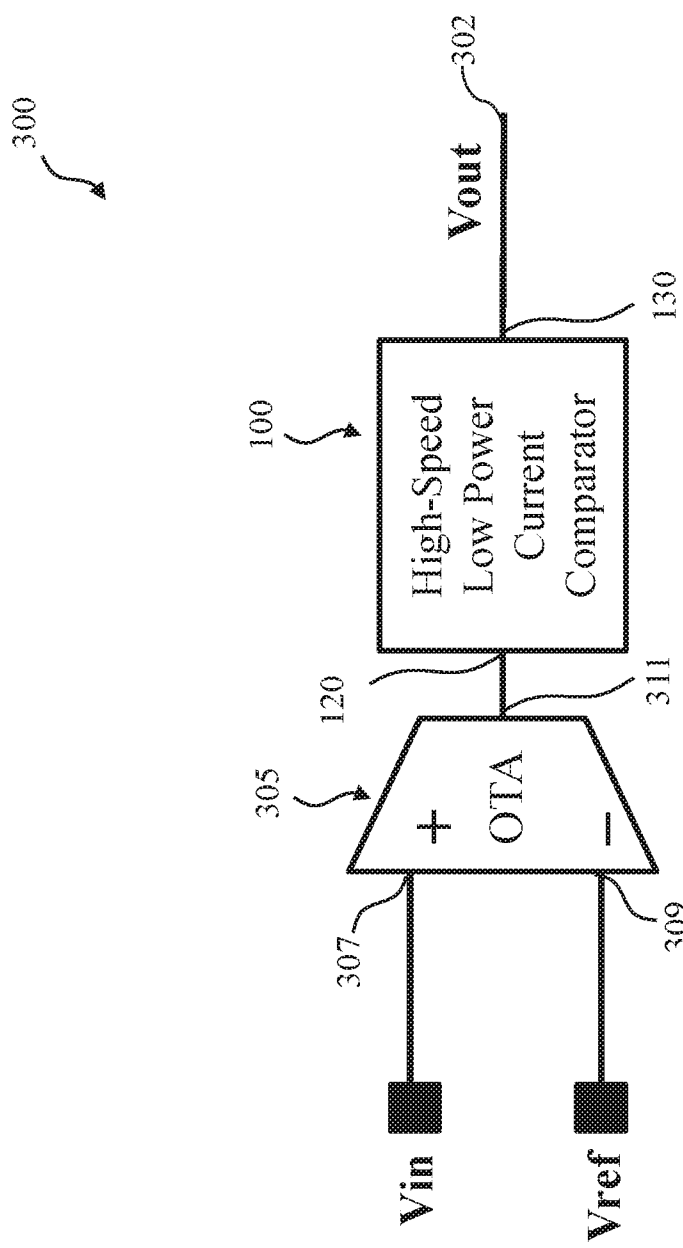


FIG. 3

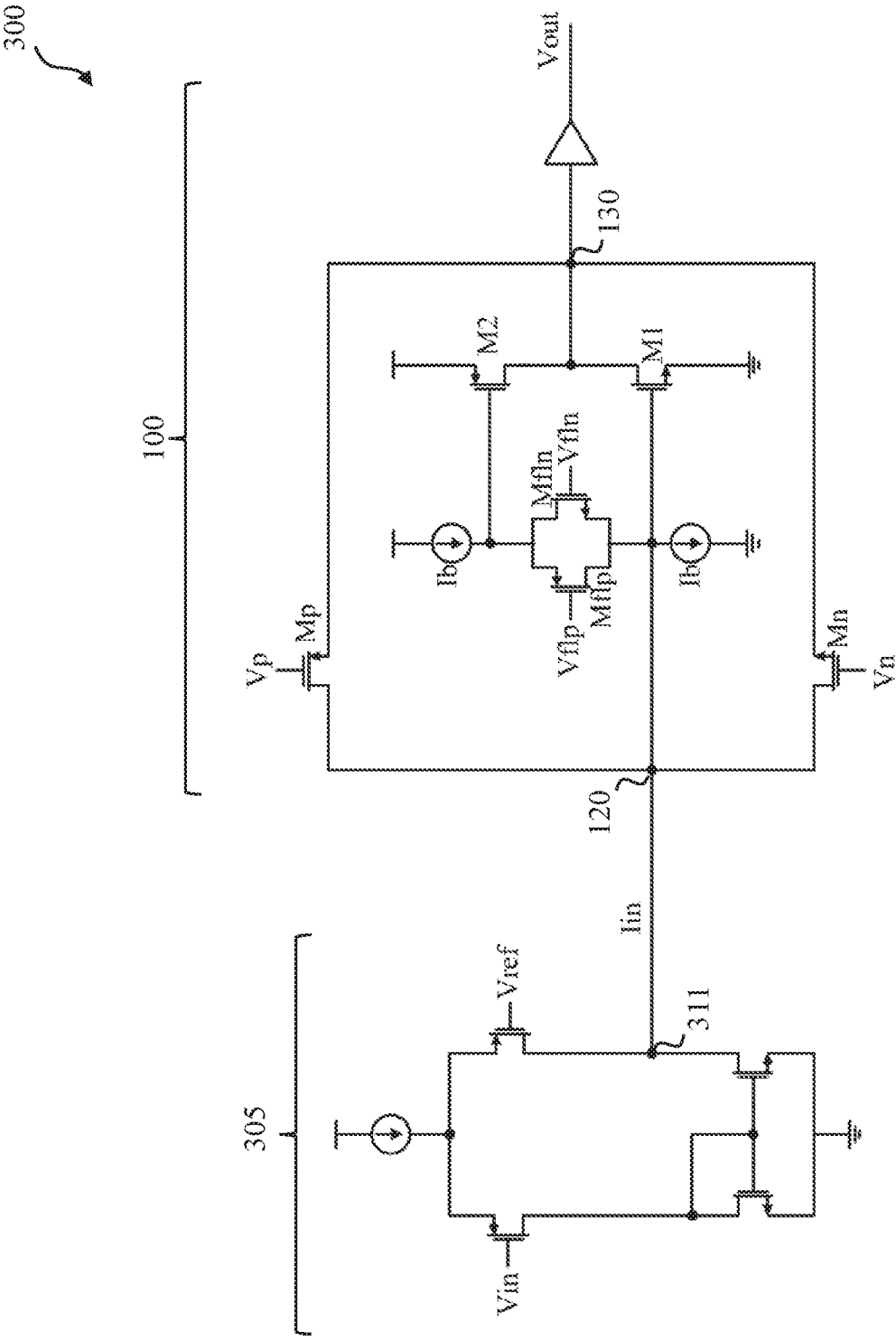
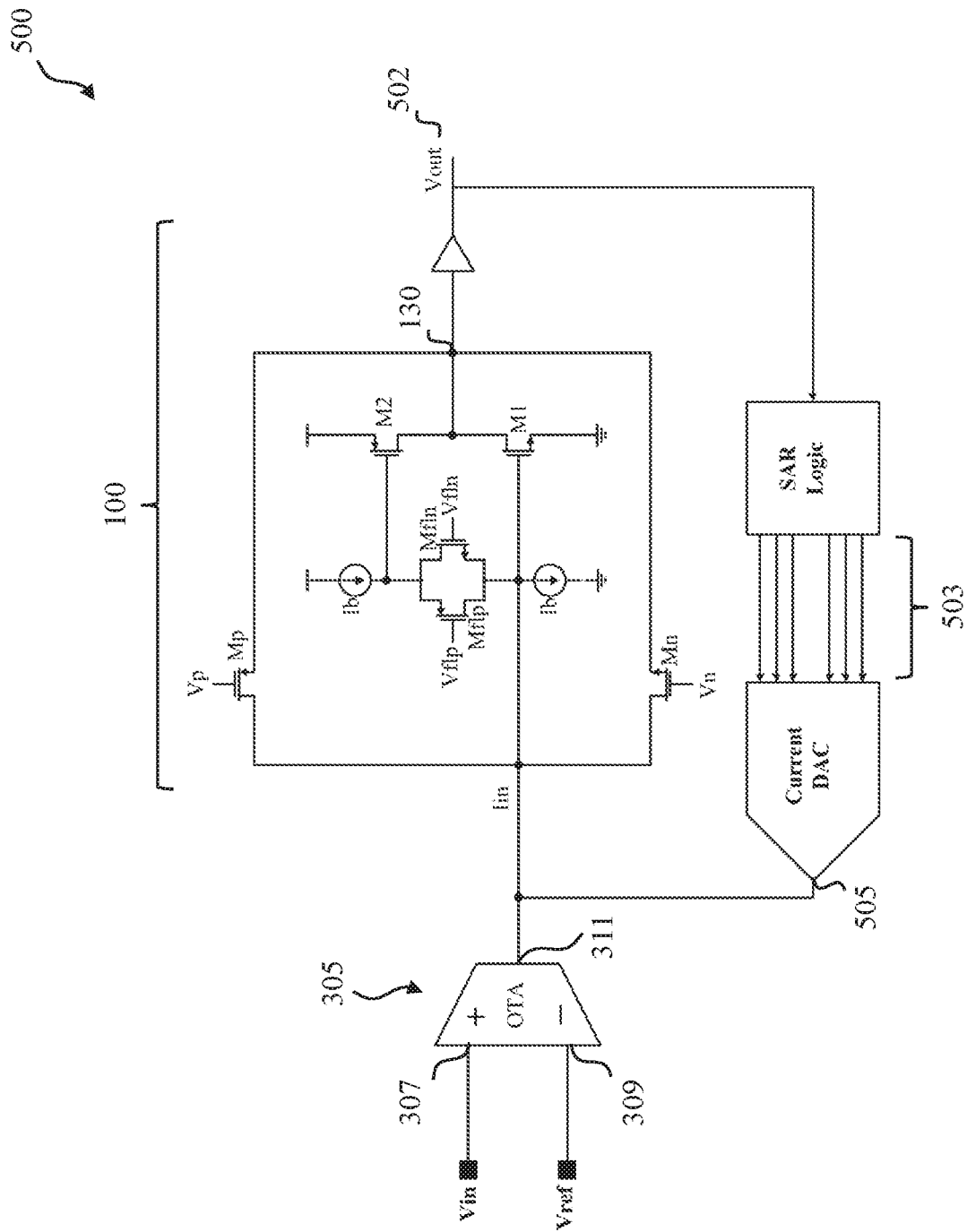


FIG. 4



SHS

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/060714**A. CLASSIFICATION OF SUBJECT MATTER****H03F 3/45(2006.01)i, H03F 3/21(2006.01)i, H03F 1/30(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03F 3/45; H03F 3/30; H03F 1/30; G05F 1/10; H03F 3/21

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: comparator, input, current, amplifier, first biasing circuit, second biasing circuit

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2013-0200872 A1 (BRIAN W. FRIEND et al.) 08 August 2013 See paragraph [0017], claims 1-6 and figure 3.	1, 8, 11, 18
Y		2-7, 9-10, 12-17 , 19-20
Y	WO 2016-001207 A1 (BANG & OLUFSEN A/S) 07 January 2016 See page 2, line 15 - page 3, line 18 and figure 1.	2-7, 9-10, 12-17 , 19-20
A	US 2010-0164627 A1 (SUNG-MIN PARK et al.) 01 July 2010 See paragraphs [0020]-[0029] and figure 3.	1-20
A	US 2012-0206203 A1 (CARMINE COZZOLINO) 16 August 2012 See paragraphs [0014]-[0021] and figure 3.	1-20
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Further documents are listed in the continuation of Box C.



See patent family annex.

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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