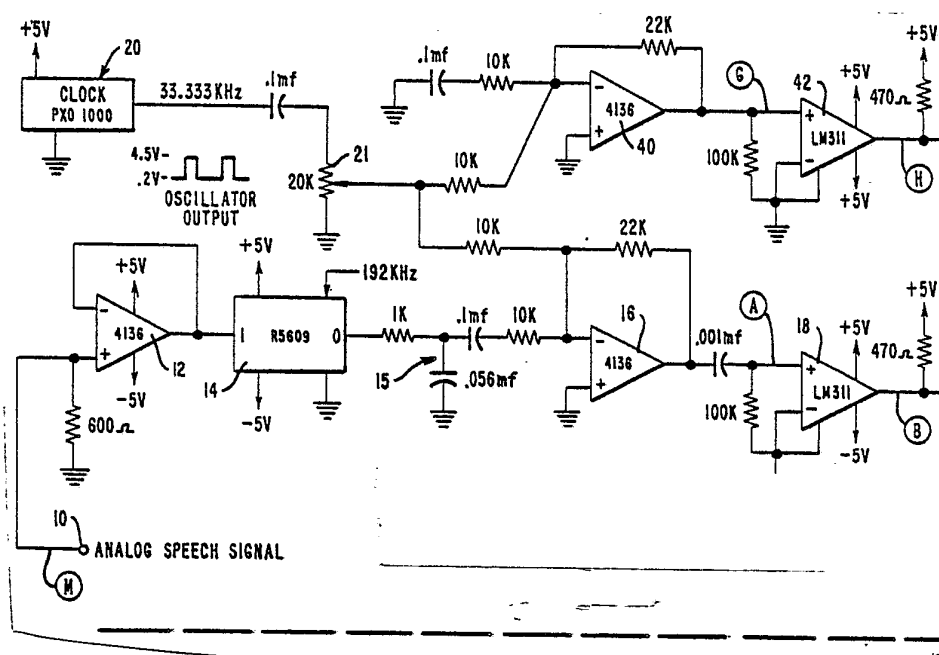


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(54) Title: DIGITAL PROCESSOR FOR SPEECH SIGNALS



(57) Abstract

A digital processor for converting an analog input signal, such as a speech signal, into a digital bit stream output signal. In order to enhance the fidelity of the information carried by the digital bit stream signal, the processor includes source means (20) for providing a dither signal, a mixing circuit (16) for summing the dither signal with an analog signal derived from said input signal, the dither signal having a frequency substantially greater than that of the analog signal applied to the mixing circuit (16), clipping means (18) for clipping the summed signal from the mixing circuit, and first and second flip-flops (22, 36) which together sample the clipped signal at a desired rate so as to produce the digital output signal at an output terminal (37).

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DIGITAL PROCESSOR FOR SPEECH SIGNALS

Technical Field

The present invention relates to an apparatus and method for converting an analog input signal into a digital bit stream signal. The invention has application, for example, to the field of conditioning speech signals so that they may act as inputs to computerized systems and more particularly to the field of converting analog speech signals into digital data.

Background Art

From International Patent Application having Publication No. WO 83/02190 there is known a speech recognition system including a clipping circuit arranged to receive an analog input signal representative of a spoken utterance and to generate a clipped input signal, sampling means arranged to sample the clipped input signal and to generate a plurality of discrete binary values each representing a sample value of the clipped input signal, and means for analyzing the plurality of sample values so as to identify the spoken utterance.

When an analog signal is processed into a digital signal by a system which utilizes a clipping circuit, non-linearities are introduced because the clipping circuit is intrinsically non-linear. Non-linearities generally create harmonic contents in electronic signals which are difficult to filter out. In addition, non-linearities cause signal distortions which affect the fidelity of the information carried by the signal.

As will be made clear later, in an apparatus and a method in accordance with the present invention use is made of dither signals. A general discussion of the effect of dither type signals on quantized

signals is given in an article entitled: "Dither Signals and Their Effect on Quantization Noise" by L. Schuchman, IEEE Transaction Communication Technology, Vol. COM-12, pages 162-165, December 1964.

Disclosure of the Invention

It is an object of the invention to provide an apparatus and method for converting an analog input signal into a digital bit stream signal, which apparatus and method achieve high fidelity of the information carried by the digital bit stream signal.

According to one aspect of the invention there is provided a digital processor for converting an analog input signal into a digital bit stream signal characterized by source means for providing a dither signal, summing means for summing said dither signal with an analog signal derived from said input signal, said dither signal having a frequency substantially greater than that of the analog signal summed therewith, clipping means for clipping the summed signal from said summing means, and sampler means for sampling the clipped signal from said clipping means at a desired rate so as to produce said digital bit stream signal.

According to another aspect of the invention there is provided a method for converting an analog input signal into a digital bit stream signal comprising the steps of:

- a) summing a dither signal with an analog signal derived from said input signal, said dither signal having a frequency substantially greater than that of the analog signal summed therewith;
- b) clipping the amplitude excursions of the analog signal produced as the result of step a) to produce a digital signal; and
- c) sampling the amplitude of the digital signal produced as the result of step b) at a rate

corresponding to the desired bit rate to provide said digital bit stream signal.

Brief Description of the Drawings

One embodiment of the invention will now be described by way of example with reference to the accompanying drawings, in which:-

Fig. 1 is a map illustrating the physical relationships of Figs. 1A, 1B, 1C and 1D;

Figs. 1A, 1B, 1C and 1D illustrate in schematic form a digital processor in accordance with the present invention; and

Figs. 2, 3, 4, 5, 6, 7, 8, 9 and 10 are waveforms, useful in understanding the operation of the invention, taken from selected points of the digital processor of Figs. 1A, 1B, 1C and 1D.

Best Mode for Carrying Out the Invention

At various locations in Figs. 1A, 1B, and 1D there appear capital letters A through M, each surrounded by a circle. The waveforms sampled at these locations correspond to the like labeled waveforms in Figs. 2 through 10. Due to the wide range of frequencies used in the preferred embodiment of the invention it was necessary to change the time base in Figs. 2 through 10 to more clearly illustrate the various waveform relationships. For example, in Fig. 2 the waveform (B) corresponds to the like labeled waveform in Figs. 3, 4, 5 and 6. The time base used for each Fig. appears in the upper right hand corner of the Figs., e.g., 5 ms for Fig. 2, 20 μ s for Fig. 3 and 100 ms for Fig. 4. The advantage of this approach is readily apparent by an examination of Figs. 2 and 3 wherein the waveform (B) is compared to waveforms (M) and (A) in Fig. 2 and to waveforms (C) and (D) in Fig. 3.

Referring to the drawings at terminal 10, an analog signal, such as the analog speech signal (M),

illustrated in Fig. 2, is applied to the system and is received by an amplifier 12. The amplified analog signal is directed to a low-pass filter 14 which, in the preferred embodiment, cuts off frequency components above 3.8 KHz. The filtered output signal is directed to a differentiating circuit 15 comprised of resistors and capacitors. The analog signal from the circuit 15 is then applied to the input of a mixing circuit 16, which circuit also receives the output from a crystal controlled oscillator circuit 20, via a potentiometer circuit 21. The oscillator 20 provides a dither signal which signal in the preferred implementation is a square wave and has a frequency of 33.333 KHz, which is substantially greater than the frequency of the analog signal applied to the mixing circuit 16. Mixing circuit 16 acts as a summing means for summing the analog and dither signals applied to its input. The summed signals are directed to an input of a zero crossing clipper 18. The summed signals (A) are illustrated in Figs. 2 and 5. Clipper 18 is of the infinite clipping type. The clipped dithered speech signal (B), appearing at the output of clipper 18, is shown in Figs. 2, 3, 4, 5 and 6.

An edge triggered D-type flip-flop 22 receives at its D input the clipped dithered signal (B). The flip-flop operates as a sampler in response to a clocking signal (C), which signal appears on its clocking input CK and is illustrated in Figs. 3, 4 and 7. The clocking signal is derived from a clock signal generator comprised of a crystal controlled oscillator 30, the output of which is a signal of 384 KHz, that is directed to a divide by 2 circuit 32. The output signal from the divide by 2 circuit is a 192 KHz signal that is directed to the input of a divide by 10 circuit 34 and to the filter the circuit 14 and to a further filter circuit 72. The output signal from the divide by 10 circuit is a 19.2 KHz signal that is the

signal used to clock flip-flop 22. A D-type flip-flop has the characteristic that the signal present at the D input, upon the transition of the clock signal in the positive direction, will be transferred to the Q output and the Q output will remain in the state sampled until the occurrence of the next positive clock transition.

If oscillators 20 and 30 were ideal, so as to maintain their output frequencies exactly, the signal ① appearing at the Q output of flip-flop 22 (illustrated in Figs. 3, 4 and 6) would be the usable digital data signal but, in reality, the output frequencies from these oscillators vary. It is highly desirable to maintain the difference in frequency of the dithering signal and the sampling rate at a substantial constant. Oscillator variations in turn create a frequency variation that would degrade the fidelity of the transmitted signal and increase the reproducibility problems. In the preferred environment the digital data signal is transmitted over a digital communications channel operating at 9.6 kilobits per second. Therefore, additional circuitry is needed to lock and/or stabilize the sampling rate. A band pass filter network, comprised of circuits 46, 47, 48 and 49, receives from a flip-flop 44 the signal ② appearing at its Q output which signal is illustrated in Figs. 7, 8, 9 and 10. (Figs. 7, 8 and 9 illustrate waveforms without the ③ signal applied to terminal 10). The dither signal ④, illustrated in Fig. 7, follows a parallel path from potentiometer 21 through a mixing circuit 40 and a clipper 42, the output of the clipper 42 being the signal ⑤ shown in Figs. 7 and 8. Elements 40 and 42 correspond to elements 16 and 18, respectively, so that the signal from the oscillator 20 will receive the same propagation delays and other distortions which may be present within the like paralleled circuits. Flip-

flop 44 is clocked with the same signal as is used to clock flip-flop 22. The band pass filter 46-49 has a center frequency of 5065 Hz and a band pass of 1 KHz. The output signal (L) from the band pass filter, illustrated in Figs. 9 and 10, is directed to a phase lock loop 50 which loop typically provides at its output a signal of 5065 Hz. A feedback path consisting of a 4 bit binary counter circuit 52 and a D-type flip-flop 56 provides feedback from the phase lock loop 50 and corrects the timing of the sampling signal (E), illustrated in Figs. 6, 8, 9 and 10, that is applied to the clocking inputs of D-type flip-flops 36 and 69. The signals from circuit 52 and the phase lock loop 50 are directed as inputs to a 1 of 16 decoder circuit 54. The output of circuit 54 is the corrected sampling signal (E), which signal in the preferred implementation has an average center frequency of 10.130 KHz. In operation, the phase lock loop 50 has a range of operation between 4.5 KHz and 5.5 KHz to provide the correctly sampled digital data signal (F), illustrated in Figs. 5, 6, 9 and 10, that appears at the output terminal labeled 37. From the foregoing it can be appreciated that flip-flop 36 operates as a second sampler. It should be understood that the sampling frequency of the flip-flop 36 is variable, being dependent on the sampling frequency of the flip-flop 22.

The digital data signal (F), appearing at terminal 37, may be directed to any communications channel apparatus for further transmission and/or processing.

An oscillator circuit with feedback 60, comprised of inverters 61 and 62, is the source of a 605 KHz signal used by the band pass filter elements 46 and 48. The feedback inverting circuit 66, comprised of inverter 67 and inverter 68, generates a 2.46 MHz signal which is used by the filter elements 47 and 49.

From the foregoing description of the preferred implementation it can be seen that an analog signal is received on terminal 10 and that the analog signal is mixed with a dither signal. The mixed signals are then clipped and the clipped signals are sampled at the desired bit rate to provide a digital data output signal.

In order to reconstruct the analog signal from the digitized audio output signal appearing at terminal 37, the digitized audio output signal is applied to input terminal 70 shown in Fig. 1B. The output of flip-flop 44 is directed, as previously stated, to the D input of flip-flop 69. The signal (J), at the Q output of flip-flop 69, illustrated in Fig. 8, should correspond, except for the sampled analog speech component, to the signal (F) at the Q output of flip-flop 36. Therefore, if the signal at the Q output of flip-flop 69 is subtracted from the signal at terminal 70, the remaining component is the analog input signal. This subtraction process is accomplished at the point labeled 80 in the circuit and the result therefrom is directed to a low-pass filter 72 to provide to terminal 73 the reconstructed analog speech signal.

CLAIMS

1. A digital processor for converting an analog input signal into a digital bit stream signal characterized by source means (20) for providing a dither signal, summing means (16) for summing said dither signal with an analog signal derived from said input signal, said dither signal having a frequency substantially greater than that of the analog signal summed therewith, clipping means (18) for clipping the summed signal from said summing means (16), and sampler means (22, 36) for sampling the clipped signal from said clipping means (18) at a desired rate so as to produce said digital bit stream signal.

2. The digital processor according to claim 1, characterized in that said clipping means (18) is an infinite clipper.

3. The digital processor according to either claim 1 or claim 2, characterized by amplifier means (12) preceding said summing means (16) for amplifying said input signal, and low-pass filter means (14) interposed between said amplifier means (12) and said summing means (16) for filtering the amplified input signal.

4. A digital processor according to any one of the preceding claims, characterized in that said sampler means (22, 36) includes a first sampler circuit (22) arranged to receive the output of said clipping means (18), and a second sampler circuit (36) arranged to receive the output of said first sampler circuit (22) and to produce at its output said digital bit stream signal, and further characterized by means (46-56) for varying the sampling frequency of said second sampler circuit (36) in dependence on the sampling frequency of said first sampler circuit (22).

5. A method for converting an analog input signal into a digital bit stream signal comprising the steps of:

a) summing a dither signal with an analog signal derived from said input signal, said dither signal having a frequency substantially greater than that of the analog signal summed therewith;

b) clipping the amplitude excursions of the analog signal produced as the result of step a) to produce a digital signal; and

c) sampling the amplitude of the digital signal produced as the result of step b) at a rate corresponding to the desired bit rate to provide said digital bit stream signal.

6. A method according to claim 5, characterized by the step of filtering said input signal to produce the analog signal summed with the dither signal in step a).

7. A method according to either claim 5 or claim 6, characterized in that the sampling step c) includes the steps of:

d) sampling the result of clipping step b) at a first sampling rate; and

e) sampling the result of step d) at a second sampling rate.

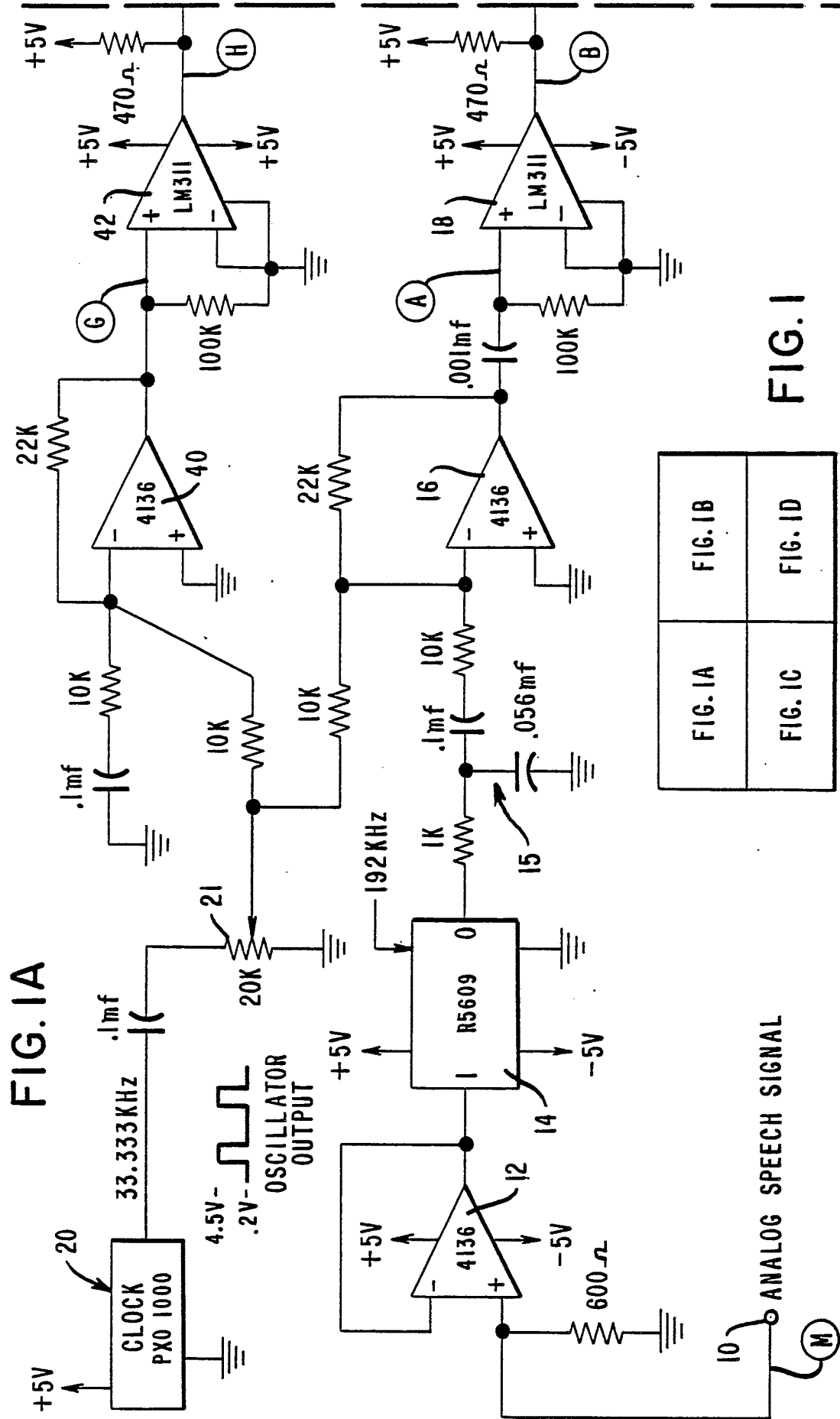
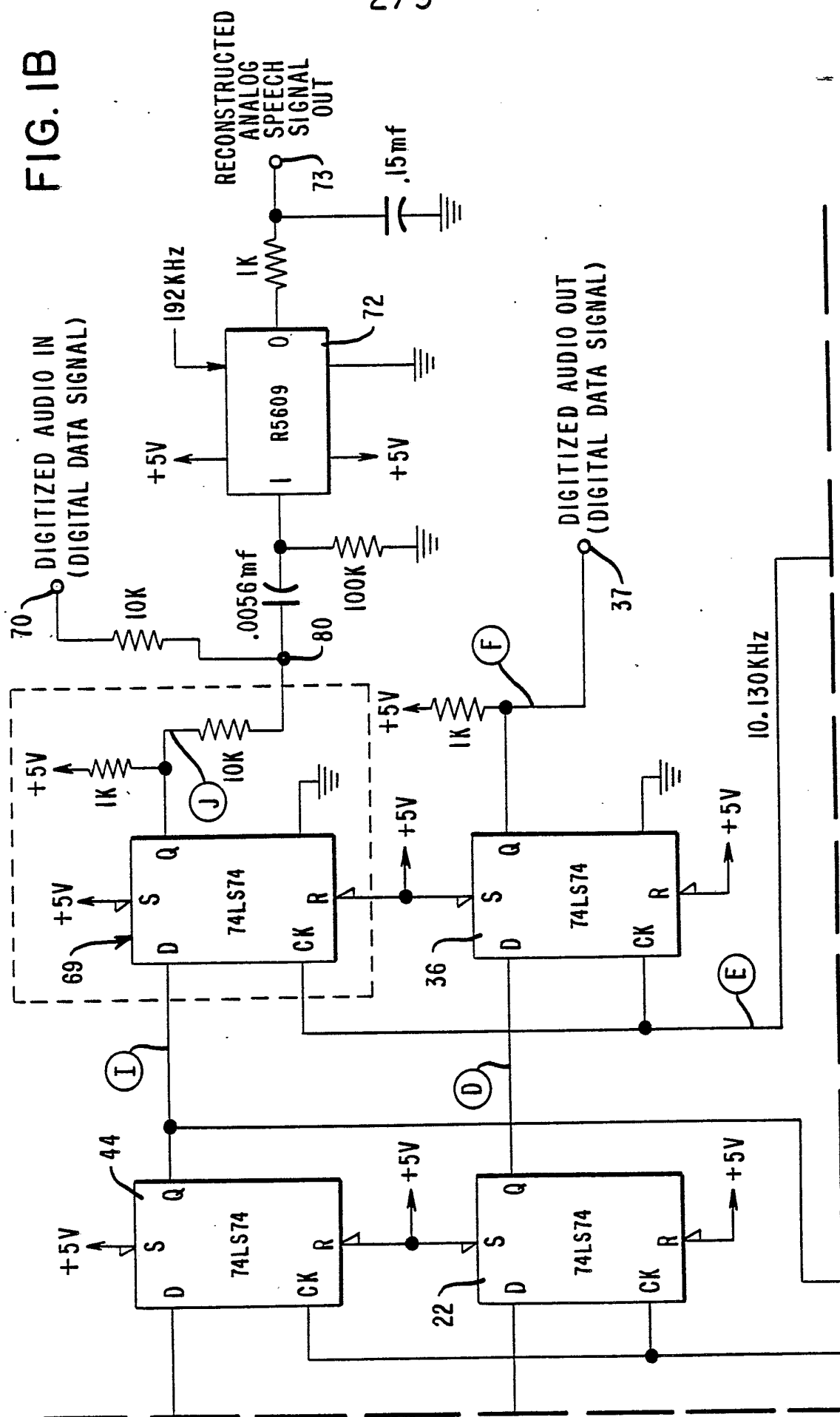
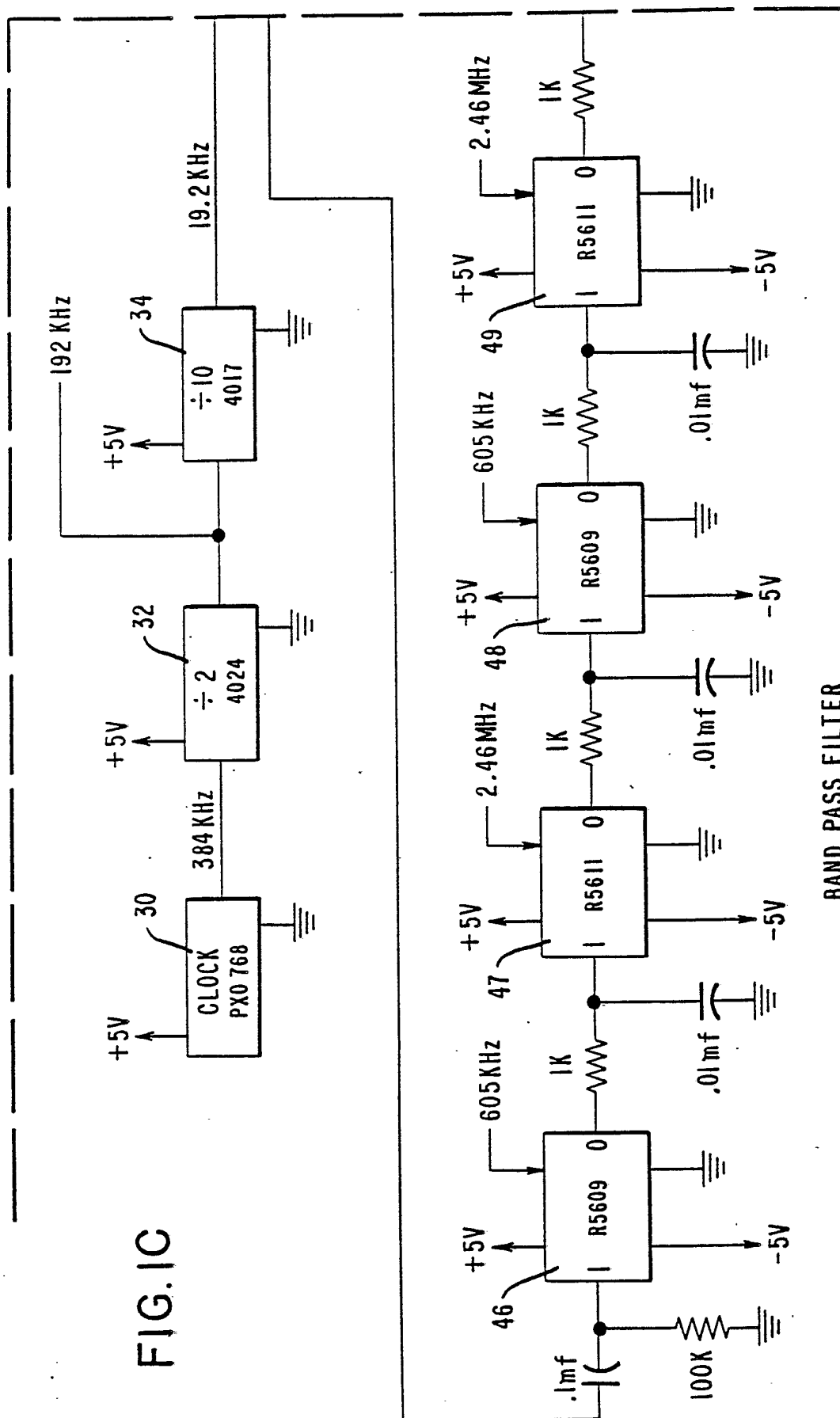


FIG. 1B



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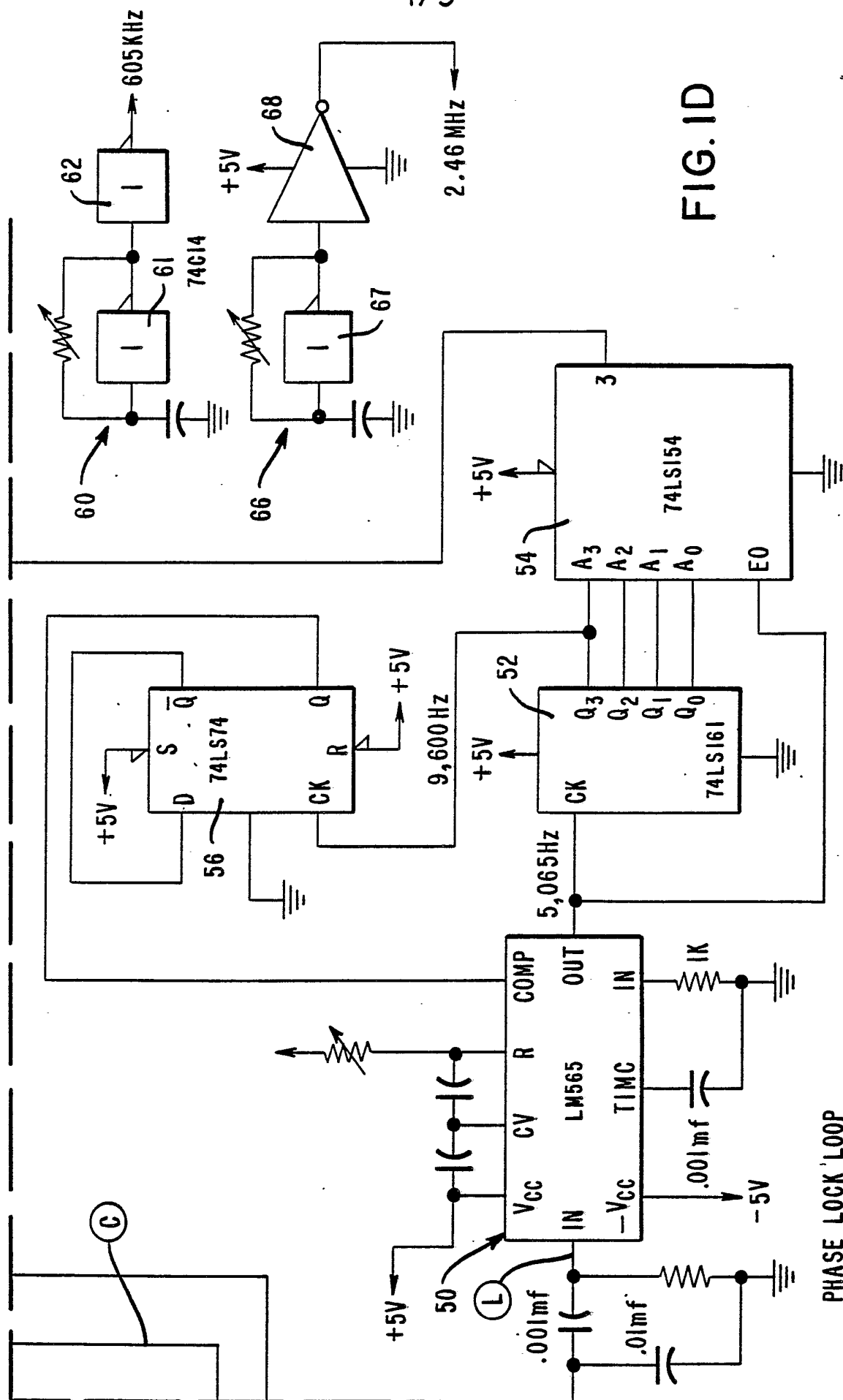


FIG. 1D

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FIG. 2

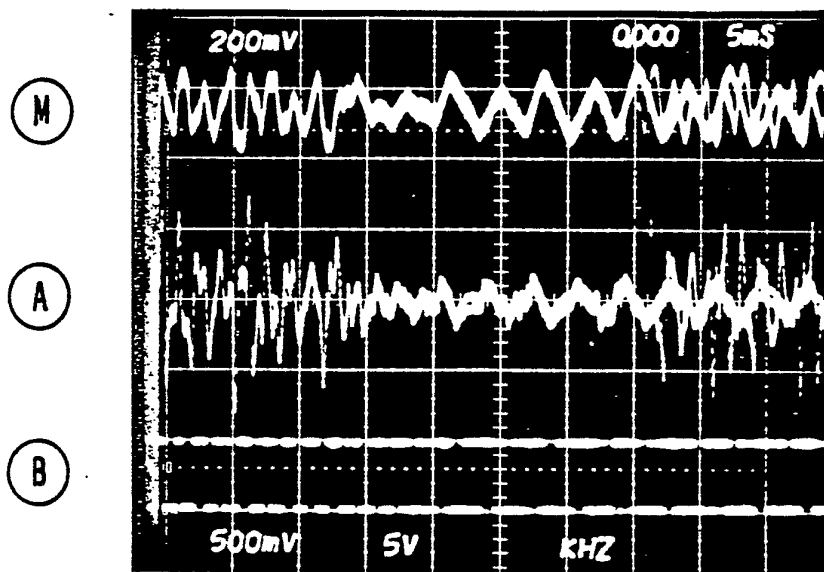


FIG. 3

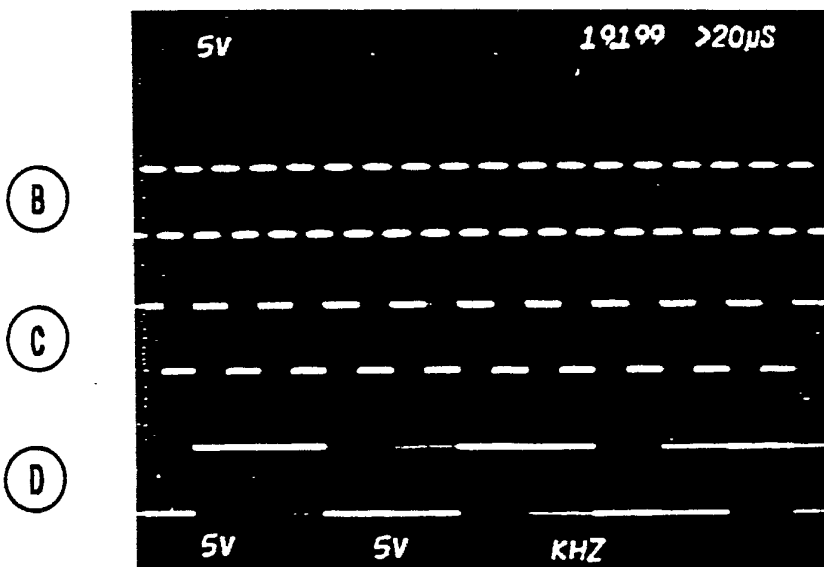


FIG. 4

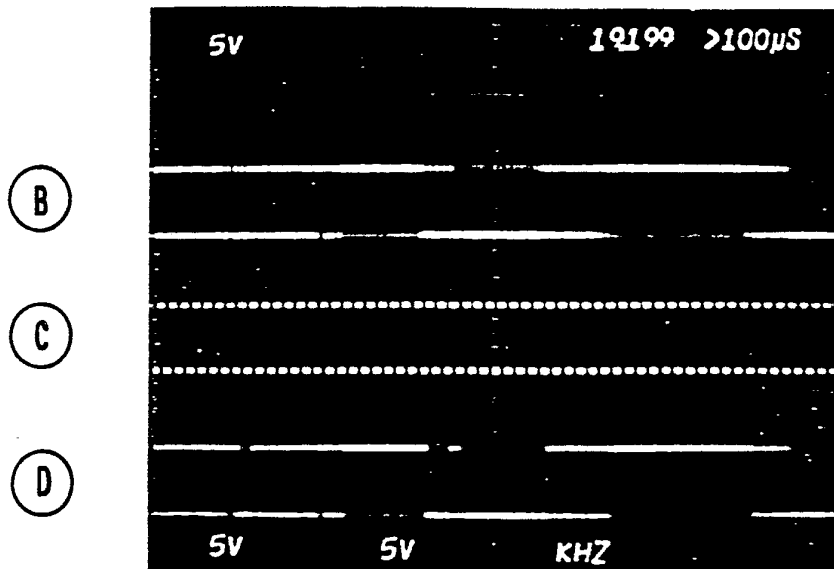
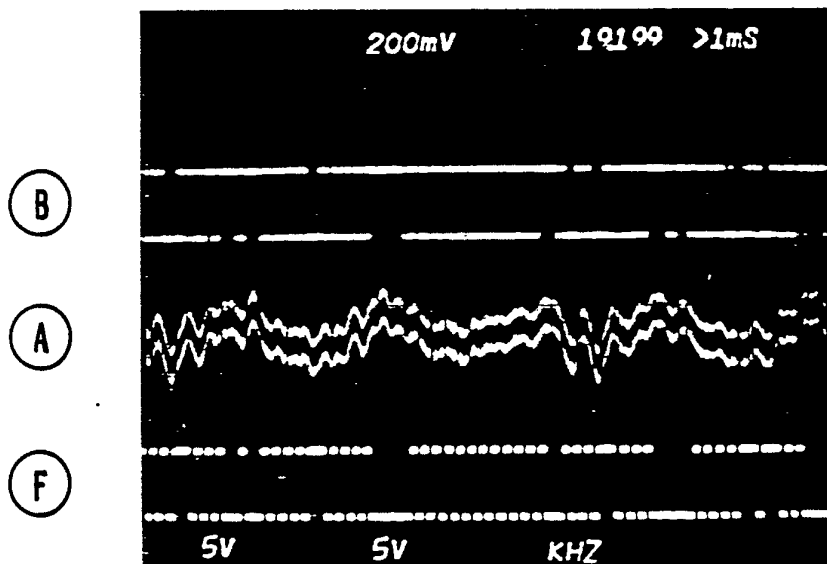


FIG. 5



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FIG. 6

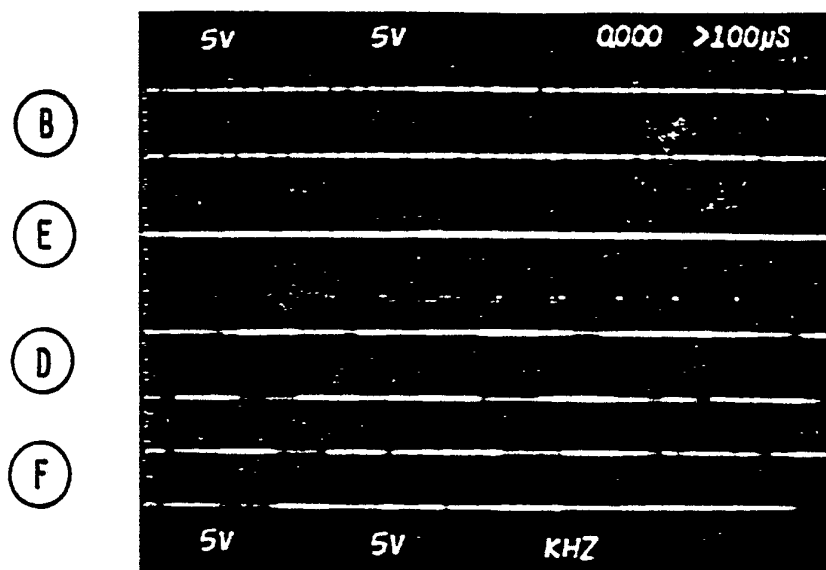


FIG. 7

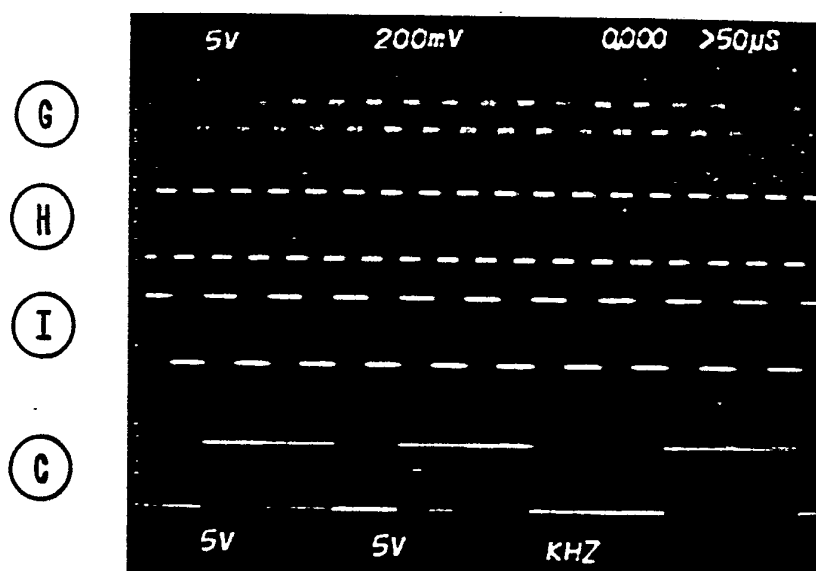


FIG. 8

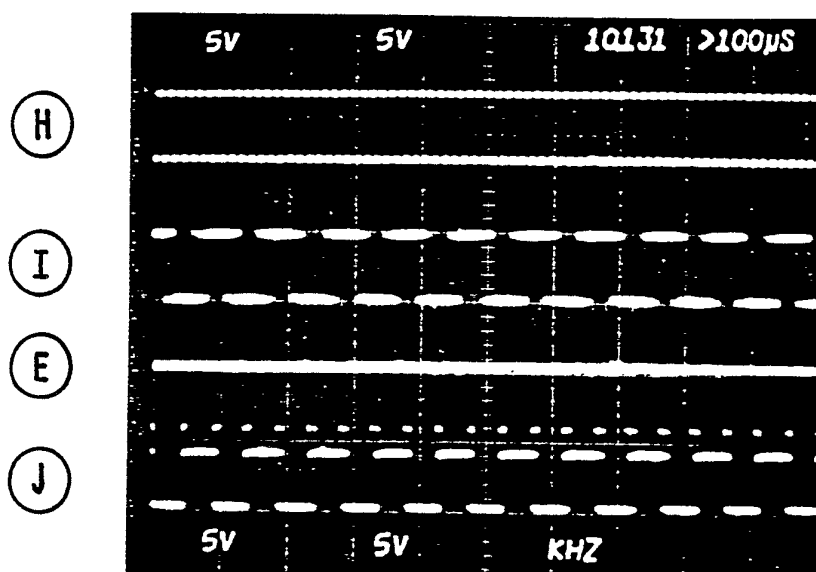


FIG. 9

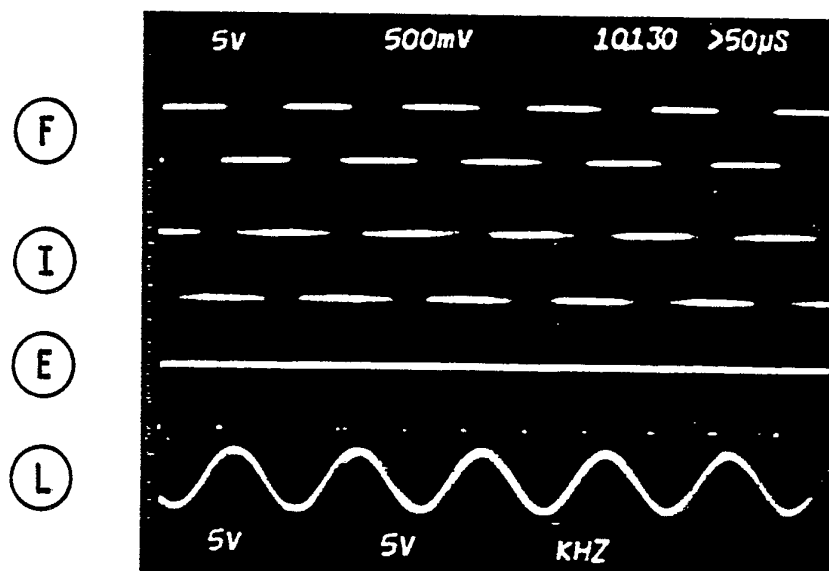
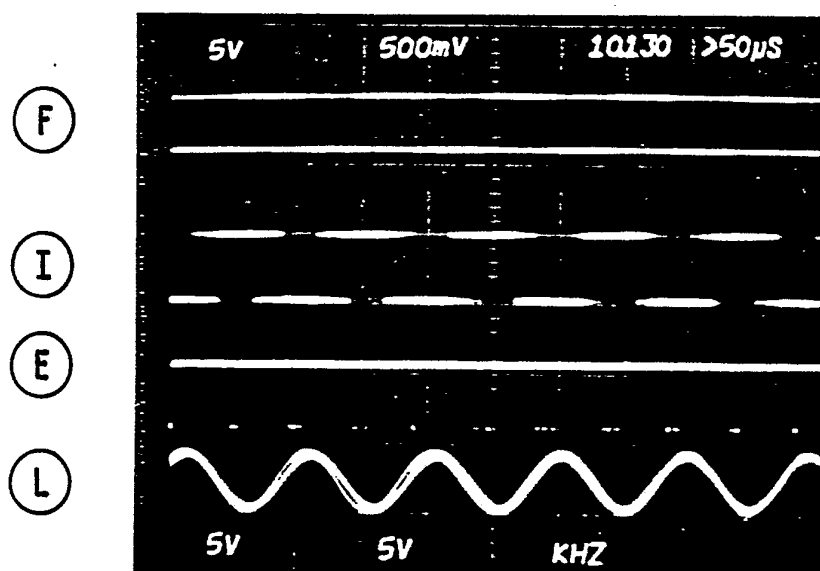


FIG. 10



INTERNATIONAL SEARCH REPORT

International Application No PCT/US 85/01430

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) ⁶ According to International Patent Classification (IPC) or to both National Classification and IPC IPC ⁴ : G 10 L 9/12		
II. FIELDS SEARCHED		
Minimum Documentation Searched ⁷		
Classification System	Classification Symbols	
IPC ⁴	H 04 B H 03 M G 10 L	
Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched ⁸		
III. DOCUMENTS CONSIDERED TO BE RELEVANT ⁹		
Category ⁹	Citation of Document, ¹¹ with Indication, where appropriate, of the relevant passages ¹²	Relevant to Claim No. ¹³
X	Journal of the Acoustical Society of America, volume 32, nr. 4, April 1960, New York, (US) Sakai et al.: "New Instruments and Methods for Speech Analysis", pages 441-450, see page 442, right-hand column, lines 1- 19	1,2,5

A	DE, A1, 2749752 (SIEMENS) 10 May 1979, see page 5, line 24 - page 6, line 32; page 7, last paragraph	1,5

A	EP, A1, 0037259 (JVC) 7 October 1981, see page 8, line 3 - page 9, line 14	1,3,5

¹⁰ Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art. "&" document member of the same patent family		
IV. CERTIFICATION		
Date of the Actual Completion of the International Search 24th October 1985	Date of Mailing of this International Search Report 19 NOV. 1985	
International Searching Authority EUROPEAN PATENT OFFICE	Signature of Authorized Officer G.L.M. Kruidenberg	

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO.

PCT/US 85/01430 (SA 10307)

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
DE-A- 2749752	10/05/79	None	
EP-A- 0037259	07/10/81	JP-A- 56136027	23/10/81

For more details about this annex :
see Official Journal of the European Patent Office, No. 12/82