United States Patent [19]

Trogdon

[11] **3,792,311**

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[54] **SPLIT-SUSTAINER OPERATION FOR GASEOUS DISCHARGE DISPLAY PANELS**

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[52] **U.S. Cl.** ..... **315/169 TV,** 315/169 R

[51] **Int. Cl.** **H05b 37/00**

[58] **Field of Search** ..... 315/169 R, 169 TV

[56] **References Cited**

UNITED STATES PATENTS

3,665,400 5/1972 Leuck ..... 315/169 R X

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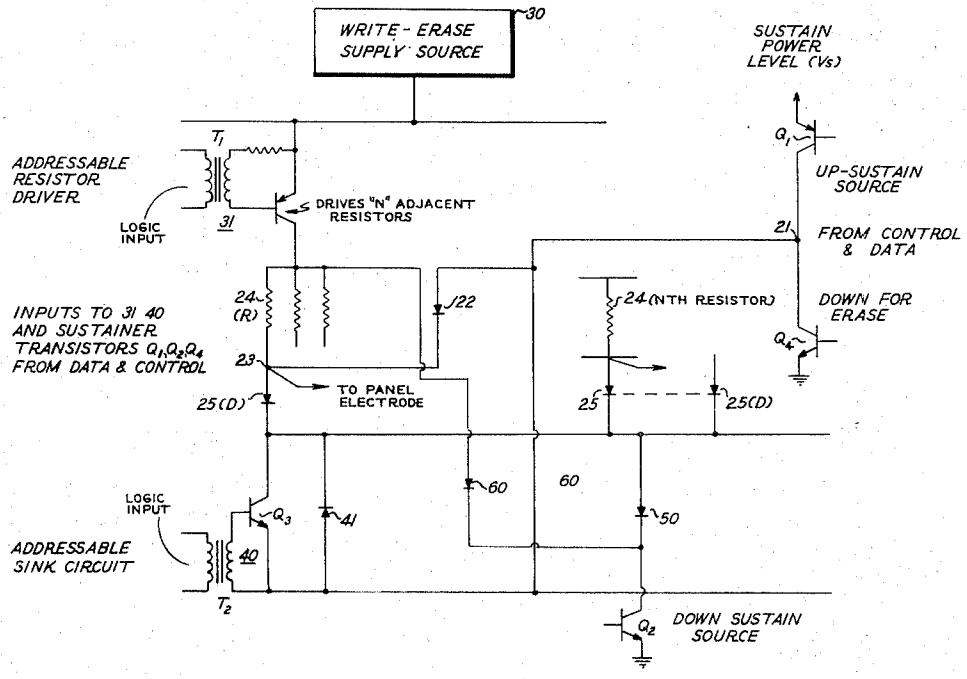
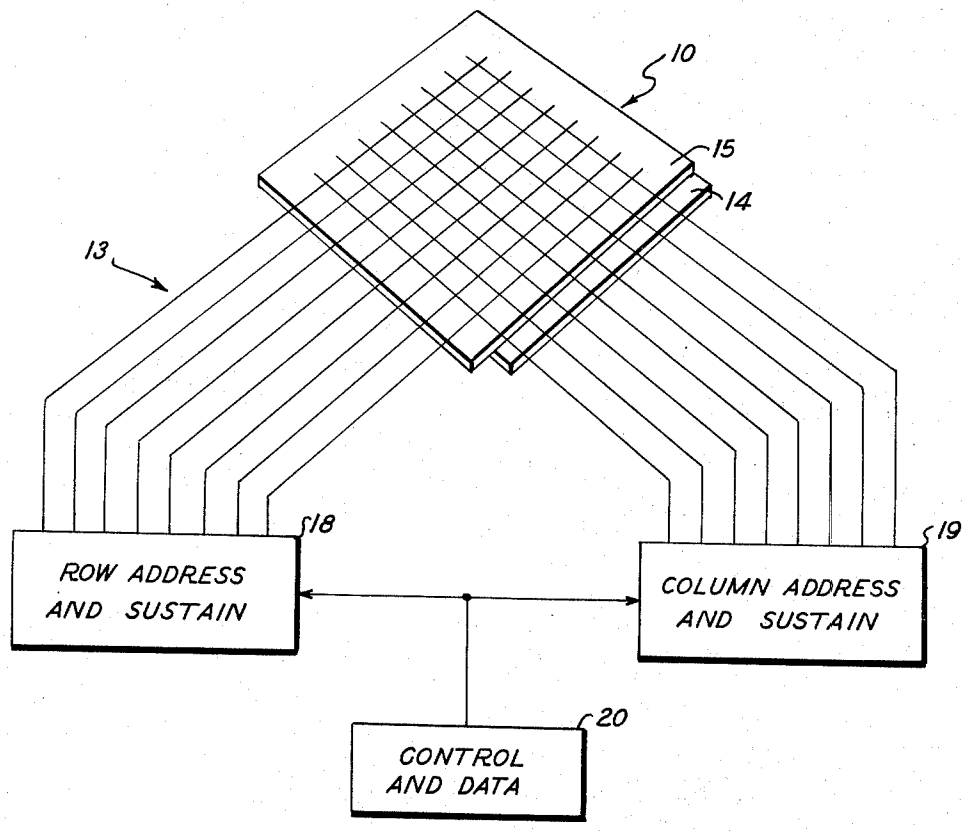
[57] **ABSTRACT**

There is disclosed an improved sustainer supply system that allows more economical addressing techniques for gaseous discharge display panels. There is particularly disclosed a sustainer supply system wherein the panel discharge currents need not be carried by the addressing drive circuitry. According to the invention each panel electrode or conductor line is addressable by a resistor-diode addressing matrix. The invention provides an addressable sink circuit which sinks current from any diode resistor combination.

6 Claims, 2 Drawing Figures




10
15
14
13
18
19
ROW ADDRESS AND SUSTAIN
COLUMN ADDRESS AND SUSTAIN
20
CONTROL AND DATA

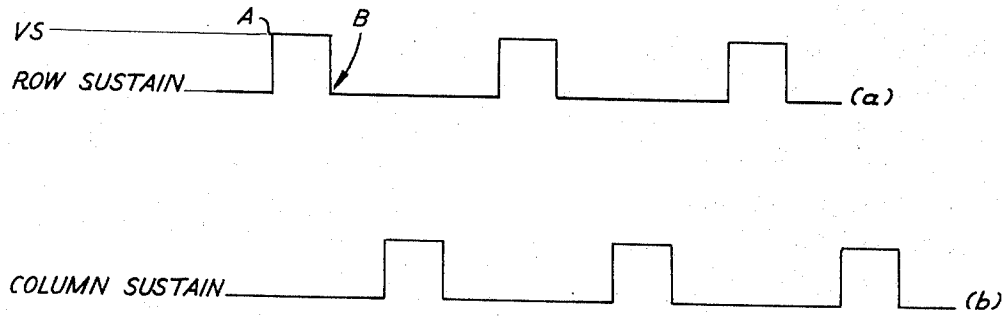

VS
A
B
ROW SUSTAIN
(a)
COLUMN SUSTAIN
(b)

FIG. 1

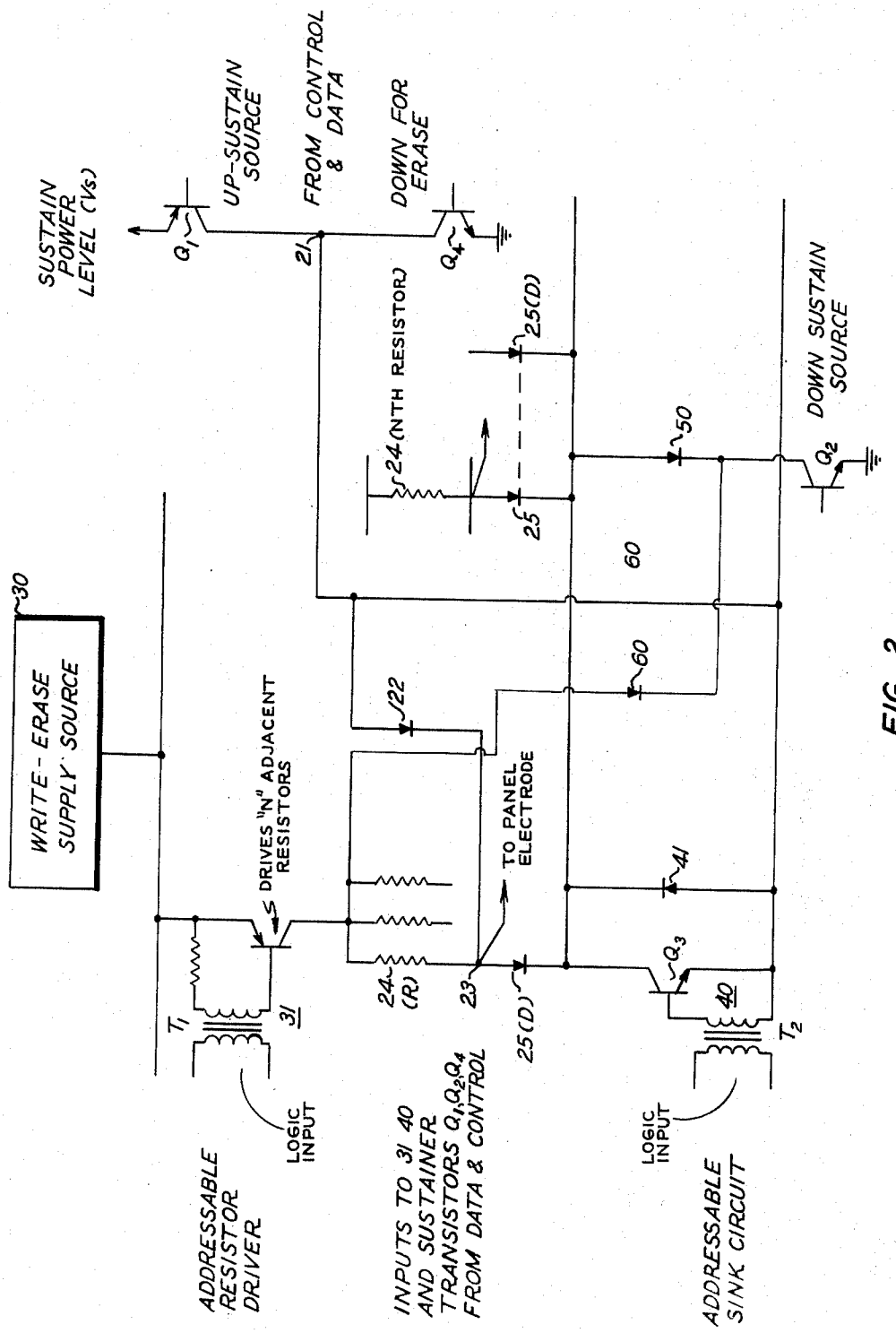

SUSTAIN POWER LEVEL (Vs)
UP-SUSTAIN SOURCE
FROM CONTROL & DATA
DOWN FOR ERASE
DOWN SUSTAIN SOURCE
WRITE - ERASE SUPPLY SOURCE
DRIVES "N" ADJACENT RESISTORS
TO PANEL ELECTRODE
NTH RESISTOR
ADDRESSABLE RESISTOR DRIVER
LOGIC INPUT
INPUTS TO 31 40 AND SUSTAINER TRANSISTORS Q1,Q2,Q4 FROM DATA & CONTROL
ADDRESSABLE SINK CIRCUIT
LOGIC INPUT

FIG. 2

SPLIT-SUSTAINER OPERATION FOR GASEOUS DISCHARGE DISPLAY PANELS

The present invention is directed to split-sustainer systems for operating gaseous discharge display panels and provides improved and more economical operation for such panels. Such panels are disclosed in Baker, et al., U.S. Pat. No. 3,499,167 and Bitzer, et al., U.S. Pat. No. 3,559,199. In the Baker, et al. patent, such a panel is constituted by a pair of glass plate members joined in spaced apart relation by a spacer sealant member. The glass plate members carry dielectrically coated multiple conductor arrays, the row and column conductors typically being orthogonally related with the crossing points of the conductors in such matrix being addressable by the application of pulse potentials to the respective conductors in the arrays. Moreover, in such systems, a sustainer voltage is typically applied one-half to the row conductors and one-half to the column conductors. An existing method and system of implementing a diode resistor addressing circuitry employs a transistor in series with the sustainer output and a group of addressing diodes. The series transistor is normally biased "ON" to insure a low impedance between panel electrodes and the sustaining source. See Johnson U.S. Pat. No. 3,513,327, which discloses the advantages of having a low impedance at this point. When addressing, the transistor must be turned "OFF" in order for the selected panel electrode to assume a voltage level different from the sustainer voltage. In other words, a pulse voltage "ON" is algebraically added to the sustainer voltage at selected time intervals (to turn on the panel, for example). Thus, the panel discharge and charging currents (the panel is a capacitive load) passes through the addressing circuits. The present invention is directed to an alternative way of controlling the operation of such discharge panels in that the circuit panel discharge and charging currents do not pass through the addressable sink circuit.

The above and other objects, advantages and features of the invention will become more apparent from the following specification and drawings wherein:

FIGS. **1**, **1***a* and **1***b* illustrates a typical gaseous discharge display panel and sustainer and addressing matrix system, including typical square wave sustainer waveforms, and

FIG. **2** is a partial circuit diagram which illustrates the split-sustainer operation according to the invention.

Referring now to FIG. **1** of the drawings, gaseous discharge display panel **10** which is constructed in accordance with the teachings of Baker, et al., U.S. Pat. No. 3,499,167, is constituted by a pair of plates **11** and **12**, respectively, support row conductor array **13** and column conductor array **14**, each of which is provided with a dielectric coating, it being understood that other arrangements of conductors and dielectric coatings are permissible within the teachings of this invention. A lead oxide overcoat, as disclosed in Ernsthausen U.S. Pat. No. 3,634,719 may be applied to the units. Finally, the plates are joined in spaced apart relation by a spacer sealer element **15** and the thin chamber, typically of about 4 to 6 mils but under 10 mils thickness is filled with a operating medium, preferably such medium being a gas as disclosed in said U.S. Pat. No. 3,634,719.

Panels constructed as described above are supplied with operating potential timed in the manner disclosed in Johnson and Schmersal U.S. Pat. application No. 699,170, filed Jan. 19, 1968, now U.S. Pat. No. 3,618,071.

As disclosed in said Johnson and Schmersal patent, one-half the sustainer potential is applied to row conductor array **13** and the other half is applied to the column conductor array **14**, typical row sustainer being shown in FIG. **1A** and typical column sustainer waveform being shown in FIG. **1B**. In FIG. **1**, the supply systems for the row conductor array **13** is designated row address and sustain circuit **18** and the corresponding supply system for column conductor array **14** is designated column address and sustain circuit **19**. In FIG. **1**, these are shown as a combined unit because of the split nature of the sustain source. Referring now to FIG. **2**, a partial circuit schematic diagram of the invention is shown, it being understood that in accordance with the legends and plans of connection and development of the circuit for a full panel array not being shown so as to simplify and avoid complication of this disclosure.

Referring now to FIG. **2**, the sustainer system is constituted by transistors Q_1 which is the pull up sustaining source and transistor Q_2 which is the pull down sustaining source. The bases of transistors Q_1 and Q_2 are controlled in accordance with control signals from a control and data source **20** shown in FIG. **1**. In accordance with the system shown with respect to the row sustainer, the pull up sustaining power level is constituted by a variable direct current voltage supply (not shown) but which is known in the art. Thus, in typical square wave sustainer operation, transistor Q_1, on being rendered conductive, raises the voltage at point **21** to the sustaining power level and this voltage is applied through coupling diode **22** to node points **23** of a typical resistor-diode address module or element. Such elements are constituted by a resistor **24** and a diode **25** which, in a quiescent state, do not affect the sustained operation. Thus, when point **21** rises to the sustaining power level, corresponding to point A on the row sustainer voltage curve, the panel electrodes connect to that particular nodal point **23** rise to the voltage level V_s of FIG. **1A** to thereby charge the panel capacitance. The panel is discharged or returned to a normal level by turning on transistor Q_2 which is the down sustaining source. This returns the panel electrode to the level at the point labelled B in FIG. **1**. Note that in accordance with the invention the down sustain transistor switch Q_2 is coupled to the gate diodes **25** by way of a coupling diode **50**, so the sustainer generator is split. For erase operations, a pull down transistor switch Q_4 is provided and controlled to connect panel electrodes to a neutral voltage level for erase or removal of information from the panel. The same functional operation occurs with respect to the column sustainer waveform illustrated in FIG. **1***b* at a displaced time interval so that the sustainer potential seen by the gas is, in effect, the difference between the true sustainer waveforms illustrated. The write and erase potentials are applied to the panel electrodes from a supply **30** via the resistor-diode multiplex matrix and combined with the sustainer source as illustrated in FIG. **2**. Diode **60** serves to connect Q_2, which is normally "off" during addressing operations, to the appropriate write or erase voltage level. This prevents having to charge the collector capacitance of Q_2 through R24.

The logic inputs to the addressable resistor driver circuits **31** are received from the source of data to be entered to the panel, it being appreciated that there may be a plurality of such resistor driver circuits for selected groups of resistors.

An addressable sink circuit **40** is used to sink current from any of "M" non-adjacent diode-resistor combinations where M × N is the total number of conductors in the conductor array on the panel. This circuit includes input transformer T_2, transistor switch Q_3 and diode **41.** The diode **41** is for reducing currents through diodes **22** and **25** in the event that Q_1 and Q_2 are both on. Thus, as shown the discharge and charging (displacement) currents do not pass through the addressable sink circuit **40.**

Transistor Q_4 is used, during erase intervals, as the down sustain path instead of transistor Q_2.

The invention has several advantages over prior art, including:

1. being normally "off," no bias supply is required for the addressable sink circuits (such as Q_3);

2. the addressable sink circuits being normally "off," the addressing circuitry is not required to provide power to remove stored charge from an "on" transistor;

3. the addressable sink circuits being normally "off," the leading edge of addressing signals to the various electrodes is not subject to differences in delay and reset time caused by non-uniform transistor storage characteristics;

4. since the addressable sink transistors Q_3 do not pass panel discharge current, they may have a reduced current capability, which makes for a lower cost, better performance device;

5. the trailing edge of "write" and "erase" address signals in the system illustrated is controlled by turning all addressable sink circuits **40** "on" at the desired time. Thus, both leading and trailing edges of write and erase pulses are controlled by turning transistors "on" and the difficult to control and non-uniform process of turning transistors "off" does not encumber the process of providing address signals to selected electrodes.

While there has been described and illustrated a preferred embodiment of the invention, it will be appreciated that various modifications thereof, obvious to those skilled in the art, are possible, and it is intended to encompass such obvious modifications in the claims hereof.

What is claimed is:

1. A system for supplying electrical operating voltage to conductor arrays of a gas discharge display panel including (1) discharge condition manipulating voltages, and (2) periodic sustain voltages, a resistor diode matrix means for addressing selected ones of the conductors in at least one of said conductor arrays,

said resistor-diode addressing matrix including a plurality of resistor-diode gate elements with a node point between each resistor-diode element, means connecting each node point to a conductor in said array, a plurality of resistor voltage pulsers, means connecting the opposite end of selected N groups of said resistors to a selected one of said resistor voltage pulsers, a plurality of addressable sink circuits, each addressable sink circuit being connected to the opposite ends, respectively, of a selected group of diodes of said resistor-diode elements, and controlled on entry and removal of information to said panel to sink current from any "M" non-adjacent diode-resistor elements where M × N equals the total number of conductors on said panel,

means for supplying said periodic sustaining voltage including a direct current sustain power supply, having a pair of output terminals,

an up sustain transistor switch connected between one terminal of said supply and an intermediate point, means coupling said intermediate point to the node point of all said resistor-diode elements,

a down sustain transistor switch means, means coupling said down sustain switch to the sides of said diodes opposite said node point.

2. The invention defined in claim **1** including a further transistor switch means connected to said intermediate point for connecting said intermediate point to a neutral voltage level for erase of information from said panel.

3. The invention defined in claim **1** wherein said means coupling said intemediate point to said node point includes a diode.

4. The invention defined in claim **3** wherein said means coupling said down sustain switch to the sides of said diodes opposite said node points includes a diode.

5. The invention defined in claim **1** wherein said means coupling said down sustain switch to the sides of said diodes opposite said node points is consitituted by a further diode.

6. The invention defined in claim **1** including a further diode connected between said down sustainer switch means the resistor ends of said resistor-diode gate elements opposite the node points.

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