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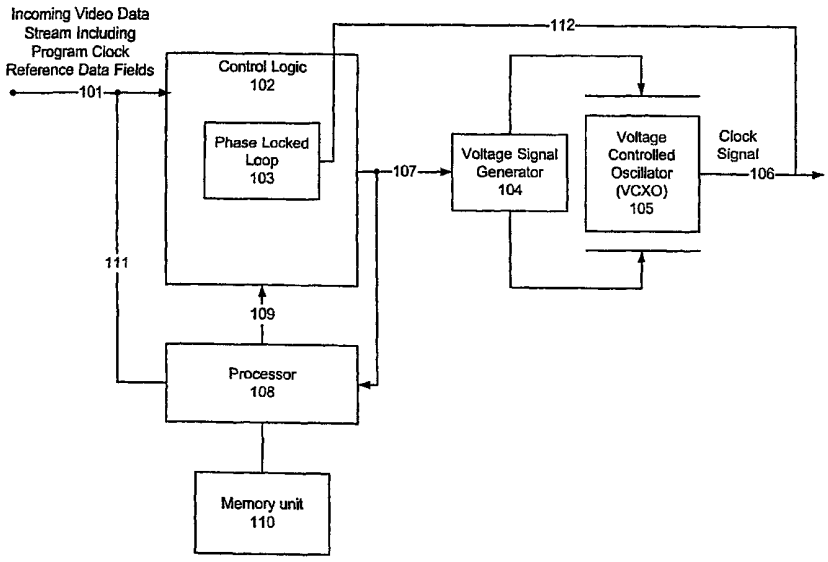
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(54) Title: METHOD AND APPARATUS FOR PROVIDING A CLOCK SIGNAL WITH HIGH FREQUENCY ACCURACY



(57) Abstract: A circuit for providing a sufficiently accurate clock signal for reconstruction of an image from a video signal can function with or without receiving an incoming video signal containing clock data. In this way, a clock signal for supporting an on-screen display can be created in the absence of an incoming video signal. Control data used to control a voltage controlled oscillator generating a clock signal is recorded when the control logic of the oscillator is locked to the timing data in an incoming video signal. In the absence of an incoming video signal, the recorded control data is retrieved and resubmitted to the control logic so that the oscillator can be made to output an appropriate clock signal even in the absence of an input video signal.

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TITLE OF THE INVENTION

Method and Apparatus for Providing a Clock Signal with High Frequency Accuracy

FIELD OF THE INVENTION

The present invention relates to the field of video equipment and visual displays. More particularly, the present invention relates to on-screen displays generated by video equipment, such as set-top terminals and video cassette recorders, in the absence of an incoming video signal.

BACKGROUND OF THE INVENTION

Modern video equipment including televisions, video cassette recorders (VCRs), and set-top terminals provide users with tremendous access to television programming. In particular, cable and satellite television systems may provide access to hundreds of channels of video programming. A set-top terminal is a box of electronic circuitry connected between a user's television and a cable or satellite television system for assisting the user in accessing that system.

As the equipment for providing video programming becomes more complicated and offers more features and flexibility to users, the sophistication and programming required to operate such equipment also increases. In fact, some video equipment, particularly VCRs and set-top terminals, now require substantial computing power to optimally process video and audio signals and provide user

features such as timed program recording, premium channel de-scrambling, etc.

To support all these features, such video equipment must be readily programmable by users, i.e. receive user input and instructions. To facilitate the programming of such video equipment as VCRs and set-top terminals, on-screen displays ("OSDs") are commonly used. With an OSD, the equipment being programmed takes temporary control of the television set or monitor to which it is connected in order to display menus, user prompts or echoes of user input to assist the user in properly programming the equipment or accessing equipment features.

In general, to generate a visual display on a display device, such as a television set or monitor, the information for the images to be displayed must be provided as a video signal. This is also true of an on-screen display which is derived from a video signal generated by the video equipment. Conversion of a video signal into a visual image on a display screen requires the use of a clock signal with a highly accurate frequency. For example, the generation of images on a video display device, e.g., a television set or monitor, may require a clock signal accurate to within 3 to 50 ppm. Some televisions require higher clocking accuracy than others. The first manifestation of an inaccurate clock signal is loss of color, i.e., the displayed image degrades to black and white.

With television signals provided by network broadcasters, or cable or satellite companies, the required clock signal is inherently a part of an analog television signal and is always included as

part of a digital television signal. Therefore, when a piece of video equipment takes control of a display device, e.g. a television set, and overrides an incoming video signal to provide an on-screen display, the necessary clock signal with a sufficiently accurate frequency can be derived or borrowed from the incoming video signal.

However, a problem arises when the video equipment needs to provide an on-screen display and no video signal is being received from which to extract a clock signal. This occurs, for example, when the video equipment is connected to a television or monitor on which an OSD can be displayed, but is not connected to a cable or satellite system or to a television antenna, or when the video equipment is connected to a signal source, but is not tuned to and receiving any particular channel carrying a video signal.

When no video signal is provided, video equipment, e.g. a set-top terminal, must generate its own clock signal to support an on-screen display. As noted above, generating a high-quality on-screen display requires a precise clock signal with a highly accurate frequency that is used to construct images from the video signal carrying the information for the on-screen display. Generating such a clock signal can be difficult.

In the past, video equipment with the need to generating a high-accuracy clock signal for supporting an on-screen display has been provided with an internal clock circuit built around a dedicated crystal oscillator. The oscillator is calibrated at the factory to provide a sufficiently accurate clock signal to support an on-screen

display. However, the expense associated with the calibration of such oscillators and the tendency of such oscillators to drift out of calibration with age or in response to changing temperatures make this solution less than ideal.

Consequently, a better solution has been developed by General Instrument Corporation of Horsham, Pennsylvania in connection with its set-top terminals. In this solution, a voltage controlled crystal oscillator (VCXO) is used to generate the necessary high-accuracy clock signal. Because the oscillator is voltage-controlled, it requires little or no factory calibration and can be continually controlled to adjust for the effects of initial accuracy, aging or extreme temperatures.

In this arrangement, the control voltage applied to the VCXO is measured and recorded when a video signal is being received and properly displayed. Then, if the video equipment needs to generate a video signal for an on-screen display when no incoming video signal is being received, the recorded voltage value is retrieved from memory, and a corresponding voltage is applied to the VCXO to generate the required clock signal for supporting the on-screen display.

In a specific embodiment, an additional A/D converter (1 bit pwm and comparator) is used to measure the VCXO control voltage when the VCXO is locked to the timing of the incoming video signal. This control voltage is then used to adjust the control voltage of the VXCO to the same value when no video signal is being input to the equipment.

This arrangement, however, requires that the set-top terminal incorporate the electronic means

for making a measurement of the voltage on the VCXO during reception and display of an incoming video signal. It would be advantageous if this need to measure a voltage value could be eliminated. Consequently, there is a need in the art for a method and apparatus of providing a circuit that can generate a clock signal with a sufficiently accurate frequency to support an on-screen display without requiring factory calibration, being susceptible to aging or temperature or requiring a previous voltage measurement.

SUMMARY OF THE INVENTION

It is an object of the present invention to meet the above-described needs and others. Specifically, it is an object of the present invention to provide a method and apparatus for controlling a VCXO in the absence of an incoming video signal to produce a clock signal with a sufficiently accurate frequency to support an on-screen display, particularly without requiring a previous voltage measurement.

Additional objects, advantages and novel features of the invention will be set forth in the description which follows or may be learned by those skilled in the art through reading these materials or practicing the invention. The objects and advantages of the invention may be achieved through the means recited in the attached claims.

To achieve these stated and other objects, the present invention may be described as a clock circuit for outputting a clock signal for video reconstruction in the absence of an incoming video signal. The present invention may be embodied in a

clock circuit that includes a control logic circuit with a phase locked loop for receiving an incoming video signal and phase locking to the clock signal component within the incoming video signal. The control logic circuit then outputs a control signal based on the phase lock to control the output of a voltage controlled oscillator.

The clock circuit also includes a circuit for recording control data from the control signal during the phase lock. The recorded control data is then used by the clock circuit to control the voltage controlled oscillator in the absence of an incoming video signal. Preferably, the circuit for recording control data includes a processor and a memory unit. The processor may monitor the incoming video signal and automatically provide the recorded control data from the memory unit in the absence of the incoming video signal.

The voltage controlled oscillator outputs a clock signal with a sufficiently accurate frequency to support an on-screen display in the absence of the incoming video signal from which a clock signal can be obtained. A voltage signal generator is preferably used to receive the control signal from the control logic circuit and to drive the voltage controlled oscillator in accordance with that control signal.

The present invention may be applied regardless of whether the incoming video signal is analog or digital. Where the incoming video signal is a digital signal, the phase locked loop locks to program clock reference data in the incoming video signal. Where the incoming video signal is an

analog signal, the phase locked loop locks to the horizontal frequency of the incoming video signal.

The present invention also encompasses a corresponding method of producing a clock signal for video reconstruction in the absence of an incoming video signal. The method includes the steps of retrieving previously recorded control data for a voltage controlled oscillator which was output by a control logic circuit with a phase locked loop and recorded when the phase locked loop was locked to a clock signal component within an incoming video signal.

The method further includes the steps of:
(1) recording the control data that is output by the control logic circuit with a phase locked loop when the phase locked loop is locked to a clock signal component within an incoming video signal; and
(2) monitoring the status of the incoming video signal so as to initiate the retrieval of the recorded control data when the incoming video signal is not present.

The present invention further encompasses an embodiment comprising: a voltage controlled oscillator for outputting a clock signal and a control logic circuit for outputting a control signal to control the voltage controlled oscillator. The control logic circuit compares the clock signal with a reference clock signal, when present, and adjusts the control signal in accordance with the comparison. The clock signal is not necessarily the same frequency as the reference clock signal. Moreover, the clock signal being adjusted does not interfere with the display of a video signal using its own clock signal component. The reference clock

signal may be taken from an in-band or out-of-band digital data recovered clock.

A recording circuit records the control data of the control signal during the comparison. The recorded control data is then used by the clock circuit to control the voltage controlled oscillator in the absence of an incoming video signal.

Finally, the present invention encompasses a corresponding method of generating a clock signal for video reconstruction in the absence of an incoming video signal. The method includes using stored control data to control a voltage controlled oscillator to output a clock signal, where the stored control data was taken from a control signal output by a control logic circuit while the control logic circuit compared the clock signal from the voltage controlled oscillator with a reference clock signal and output the control signal in accordance with said comparison.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings illustrate the present invention and are a part of the specification. Together with the following description, the drawings demonstrate and explain the principles of the present invention.

Fig. 1 is a block diagram of an embodiment of a clock signal generator using a digital video signal according to the principles of the present invention.

Fig. 2 is a block diagram of a clock signal generator according to the principles of the present invention using an analog video signal input.

Fig. 3 is a block diagram of third embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Using the drawings, the preferred embodiments of the present invention will now be explained. Stated in broad principle, the present invention provides a device and method whereby the control information for controlling a voltage controlled oscillator ("VCXO") to produce a clock signal required for video reconstruction, when locked to the timing of an incoming video signal, is recorded. Then, in the absence of an incoming video signal, the recorded control information is retrieved to control the VCXO to produce the needed clock signal. In this way, a sufficiently accurate clock signal can be provided to support an on-screen display ("OSD") even in the absence of an incoming video signal. The principles of the invention apply regardless of whether the incoming video signal is in digital or analog format.

Fig. 1 illustrates an embodiment of the present invention as a device for generating a clock signal for an on-screen display in a piece of video equipment, such as a set-top terminal, when the incoming video signal (101) is a digital signal. As shown in Fig. 1, the incoming digital video signal (101), i.e. the video data stream, is provided to a control logic circuit (102). The digital video signal (101) includes data fields in which a program clock reference ("PCR") is provided. The PCR is a part of the MPEG-2 (Motion Picture Experts Group) digital signal format and functions as a digital clock signal that is used to reconstruct the images

carried in the digital data stream (101) for display on a television set or monitor (not shown).

The control logic circuit (102) using an internal phase locked loop circuit (103) will lock to the PCR data and output a corresponding control signal (107) to a voltage signal generator (104). The voltage signal generator (104) responds to the control signal (107) and controls the voltage controlled oscillator (VCXO) (105) to output a clock signal (106) based on the timing from the PCR. The clock signal (106) is fed back to the phase locked loop circuit (103) on line (112) to complete the loop.

The circuit of Fig. 1, as described thus far, may be dedicated to providing a clock signal for on-screen display only. In which case, the clock signal (106) is not used in the actual reconstruction of the images from the video data stream (101). Rather, another circuit similar or identical to that of Fig. 1, as described thus far, would be provided for generating the clock signal used in the actual reconstruction of the images from the video data stream (101). Alternatively, the VCXO (105) illustrated in Fig. 1 may be used for producing a clock signal (106) which is used for both supporting an on-screen display and for processing the video data stream (101) for actual display.

Under the principles of the present invention, a processor (108) which may be part of, or separate from, the control logic circuit (102) monitors the control signal (107) output to the voltage signal generator (104). When the phase locked loop (103) has locked to the program clock reference (PCR) data

in the incoming video stream using the loop, including timing signal (106) carried over line (112), and is outputting a control signal (107) based on that lock, the processor (108) records the control data from the control signal (107). A memory unit (110) may be provided in which the processor (108) stores this information.

When a clock signal (106) is needed and the incoming video data stream (101) is not present, the processor (108) can retrieve the control data from the memory unit (110) and provide the control data (109) to the control logic circuit (102). The control logic circuit (102) then generates a control signal (107) equivalent to that represented by the recorded control data (109) from which the voltage signal generator (104) can control the VCXO (105) to produce an appropriate clock signal.

The processor (108) may also monitor the presence or absence of the incoming data stream (101) over line (111) so as to automatically provide the control data (109) when the incoming data stream (101) is absent. In this way, an appropriate clock signal for an on-screen display can be provided automatically in the absence of an incoming video data stream. Other means of noting the absence of the incoming video signal and initiating retrieval of the control data stored in memory are also within the scope of the present invention.

The same principles can be applied if the incoming video signal is an analog signal as opposed to a digital bitstream. Fig. 2 illustrates an embodiment of the invention for working with a incoming analog video signal (201). The timing for reconstructing video data from the analog video

signal is indicated by the horizontal frequency of the analog video signal. Consequently, the control logic circuit (102) uses its phase locked loop (103, 112) to lock to the horizontal frequency of the analog video signal (201).

Based on this phase lock, the control logic circuit (102) outputs a corresponding control signal (107) which drives the voltage signal generator (104) causing the VXCO (105) to output a clock signal (106) that corresponds to the timing data from the horizontal frequency of the analog video signal (201). As before, this clock signal (106) may or may not be used in the actual reconstruction of video images from the analog video signal (201).

The processor (108) will monitor the control signal (107) and record the control data represented thereby, preferably in the memory unit (110) when the phase locked loop (103) is locked to the horizontal frequency of the incoming analog signal (201). In the absence of the analog signal (201), the processor (108) provides a signal (109) to the control logic conveying the recorded control data so that an equivalent control signal (107) can be generated and output to the voltage signal generator (104). The generator (104) then drives the VCXO to produce an appropriate clock signal for use in supporting an on-screen display even in the absence of an incoming video signal (201).

There are other reference signals that can be used to ensure the accuracy of the frequency of the clock signal (106) produced by the VCXO (105) in the absence of an incoming video signal. As illustrated in Fig. 3, a demodulator (302) can be used to

provide a clock signal (301) based on the out-of-band or in-band digital data recovered clock.

This clock signal (301) does not necessarily or even likely have the frequency needed for a clock signal (106). For example, the out-of-band reference clock signal has a frequency of 2.048 MHz. While the frequency desired for clock signal (106) to support an on-screen display is 27 MHz. However, the reference clock signal (301) can still be used as a basis to generate a control signal (107) that will result in a clock signal (106) with the appropriate frequency. The clock signal (301) is fed to the control logic circuit (102) which outputs the control signal (107) for the voltage signal generator (104) based thereon. The voltage signal generator (105) then outputs a clock signal (106). The processor (108) may ensure the validity of the reference clock signal (301) over line (111) by monitoring the lock status of the demodulator (302).

The clock signal (106) is fed back to a frequency comparator (303) in the control logic circuit (102) over feed back line (112). The frequency comparator (303) will compare the frequency of the resulting clock signal (106) to that of the reference clock signal (301). As noted, clock signal (106) has a different frequency than that of the reference clock signal (301). Therefore, the comparator (303) adjusts for the difference and then compares the accuracy of the clock signal (106) against that of the reference clock signal (301). The control logic (102) will adjust the control signal (107) appropriately if the clock signal (106) is not sufficiently accurate as compared to the reference clock signal (301).

It will be understood by those skill in the art that such adjustments can only be made if the clock signal (106) is not being used to support display of an incoming video signal. An incoming video signal might, however, be displayed based on its own clock signal component while the unused clock signal (106) is being adjusted for eventual use in support of an on-screen display in the absence of an incoming video signal.

When the voltage control oscillator (105) is outputting a stable clock signal (106) which is based on the reference clock signal (301) and achieving sufficient accuracy, the processor (108) will obtain and record the control data from the control signal (107). Again, the memory unit (110) may be used to store this information.

When a clock signal (106) is needed and an input video signal is not present, the processor (108) can retrieve the control data from the memory unit (110) and provide the control data (109) to the control logic circuit (102). The control logic circuit (102) then generates a control signal (107) equivalent to that represented by the recorded control data (109) from which the voltage signal generator (104) can control the VCXO (105) to produce an appropriate clock signal.

The processor (108) may also monitor the presence or absence of an incoming video signal so as to automatically provide the control data (109) when an incoming video signal is absent. In this way, an appropriate clock signal for an on-screen display can be provided automatically in the absence of an incoming video signal.

The preceding description has been presented only to illustrate and describe the invention. It is not intended to be exhaustive or to limit the invention to any precise form disclosed. Many modifications and variations are possible in light of the above teaching.

The preferred embodiment was chosen and described in order to best explain the principles of the invention and its practical application. The preceding description is intended to enable others skilled in the art to best utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the following claims.

WHAT IS CLAIMED IS:

1. A clock circuit for outputting a clock signal for video reconstruction in the absence of an incoming video signal comprising:

a control logic circuit with a phase locked loop circuit for receiving an incoming video signal and phase locking to a clock signal component within said incoming video signal, wherein said control logic circuit outputs a control signal to control an output of a voltage controlled oscillator based on said phase lock; and

a circuit for recording control data of said control signal during said phase lock;

wherein said recorded control data is used by said clock circuit to control said voltage controlled oscillator in the absence of an incoming video signal.

2. The clock circuit of claim 1, wherein said circuit for recording control data comprises a processor and a memory unit.

3. The clock circuit of claim 2, wherein said processor monitors said incoming video signal and provides said recorded control data from said memory unit in the absence of said incoming video signal.

4. The clock circuit of claim 1, wherein said voltage controlled oscillator outputs a clock signal with a sufficiently accurate frequency to support an on-screen display in the absence of said incoming video signal.

5. The clock circuit of claim 1, wherein said incoming video signal is a digital signal and said phase locked loop locks to program clock reference data in said incoming video signal.

6. The clock circuit of claim 1, wherein said incoming video signal is an analog signal and said phase locked loop locks to a horizontal frequency of said incoming video signal.

7. The clock circuit of claim 1, further comprising a voltage signal generator which receives said control signal of said control logic circuit and drives said voltage controlled oscillator in accordance with said control signal.

8. A method of producing a clock signal for video reconstruction in the absence of an incoming video signal, the method comprising:

retrieving previously recorded control data for a voltage controlled oscillator which was output by a control logic circuit with a phase locked loop and recorded when said phase locked loop was locked to a clock signal component within an incoming video signal.

9. The method of claim 8, further comprising recording said control data that is output by said control logic circuit with a phase locked loop when said phase locked loop is locked to a clock signal component within an incoming video signal.

10. The method of claim 8, further comprising monitoring a status of said incoming video signal so

as to initiate said retrieving when said incoming video signal is not present.

11. The method of claim 8, further comprising generating a clock signal with a voltage controlled oscillator based on said retrieved control data.

12. The method of claim 9, wherein said incoming video signal is a digital signal and said phase locked loop locks to program clock reference data in said incoming video signal.

13. The method of claim 9, wherein said incoming video signal is an analog signal and said phase locked loop locks to a horizontal frequency of said incoming video signal.

14. A means for outputting a clock signal for video reconstruction in the absence of an incoming video signal comprising:

means for receiving an incoming video signal and phase locking to a clock signal component within said incoming video signal, wherein said means for receiving an incoming video signal outputs a control signal based on said phase lock to control an output of a means for generating a clock signal; and

means for recording control data of said control signal during said phase lock;

wherein said recorded control data is used to control said means for generating a clock signal in the absence of an incoming video signal.

15. The means of claim 14, wherein said means for recording control data comprises a processor and a memory unit.

16. The means of claim 15, wherein said processor monitors said incoming video signal and provides said recorded control data from said memory unit in the absence of said incoming video signal.

17. The means of claim 14, wherein said means for generating a clock signal comprises a voltage controlled oscillator that outputs a clock signal with a sufficiently accurate frequency to support an on-screen display in the absence of said incoming video signal.

18. The means of claim 14, wherein said incoming video signal is a digital signal and said means for phase locking locks to program clock reference data in said incoming video signal.

19. The means of claim 14, wherein said incoming video signal is an analog signal and said means for phase locking locks to a horizontal frequency of said incoming video signal.

20. The means of claim 17, wherein said means for generating a clock signal further comprises a voltage signal generator which receives said control signal and drives said voltage controlled oscillator in accordance with said control signal.

21. A clock circuit for outputting a clock signal for video reconstruction in the absence of an incoming video signal comprising:

a voltage controlled oscillator for outputting a clock signal;

a control logic circuit for outputting a control signal to control said voltage controlled oscillator, wherein said control logic circuit compares said clock signal with a reference clock signal and adjusts said control signal in accordance with said comparison; and

a circuit for recording control data of said control signal during said comparison;

wherein said recorded control data is used by said clock circuit to control said voltage controlled oscillator to generate an on-screen display in the absence of said incoming video signal.

22. The clock circuit of claim 21, wherein a processor monitors said incoming video signal and provides said recorded control data from a memory unit in the absence of said incoming video signal.

23. The clock circuit of claim 21, wherein said reference clock signal is output by an out-of-band demodulator in accordance with an out-of-band digital data recovered clock.

24. The clock circuit of claim 21, wherein said reference clock signal is output by an in-band demodulator in accordance with an in-band digital data recovered clock.

25. The clock circuit of claim 21, wherein said reference clock signal has a different frequency than said clock signal.

26. A method of generating a clock signal for video reconstruction in the absence of an incoming video signal, the method comprising using stored control data used to control a voltage controlled oscillator to output a clock signal, wherein said stored control data was taken from a control signal output by a control logic circuit while said control logic circuit compared said clock signal from said voltage controlled oscillator with a reference clock signal and output said control signal in accordance with said comparison.

27. The method of claim 26, further comprising monitoring said incoming video signal and providing said recorded control data to said control logic circuit in the absence of said incoming video signal.

28. The method of claim 26, generating said reference clock signal with an out-of-band demodulator in accordance with an out-of-band digital data recovered clock.

29. The method of claim 26, generating said reference clock signal with an in-band demodulator in accordance with an in-band digital data recovered clock.

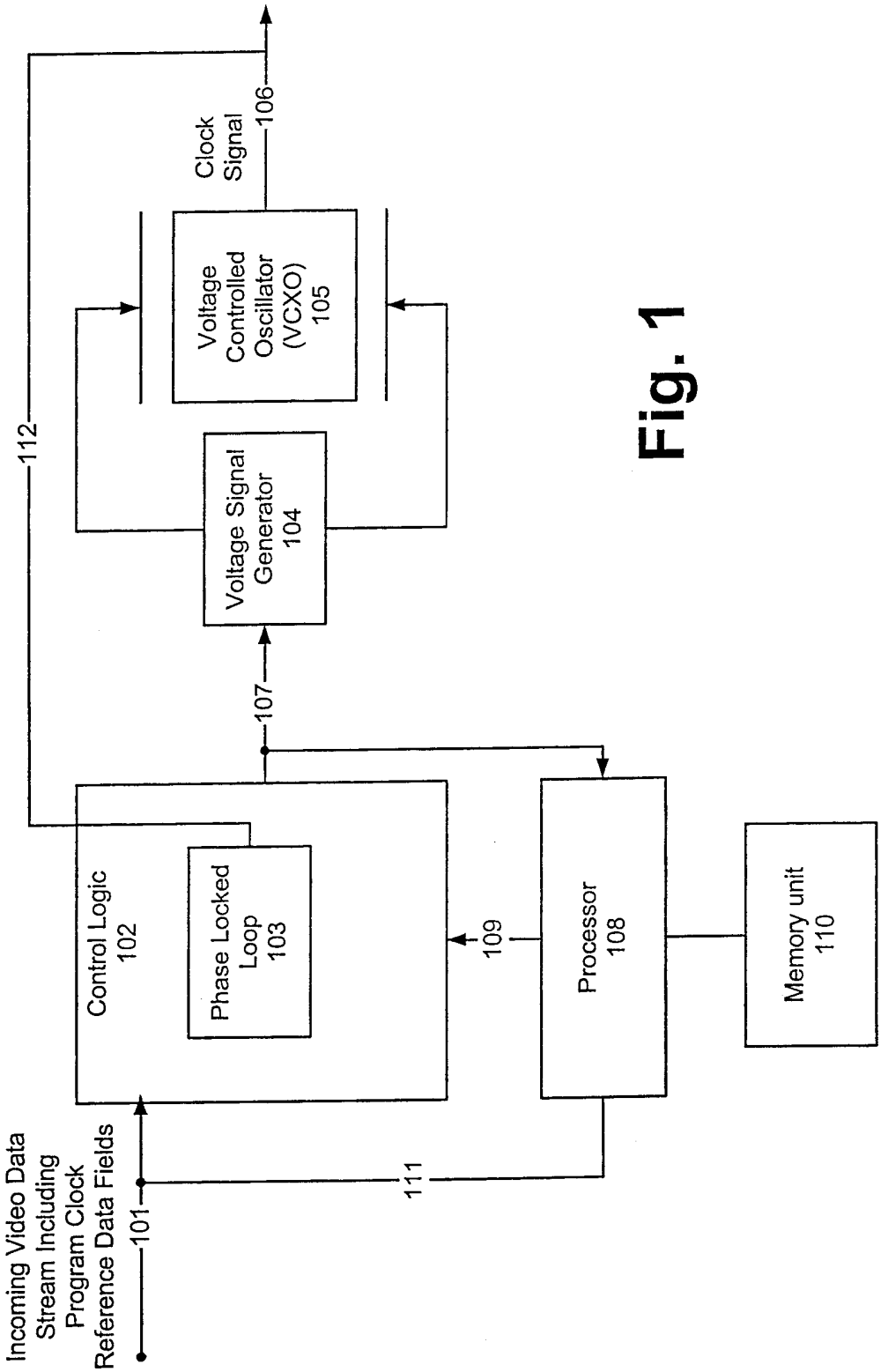

Incoming Video Data Stream Including Program Clock Reference Data Fields
101
Control Logic 102
Phase Locked Loop 103
Voltage Signal Generator 104
Voltage Controlled Oscillator (VCXO) 105
Clock Signal
106
107
109
111
112
Processor 108
Memory unit 110

Fig. 1

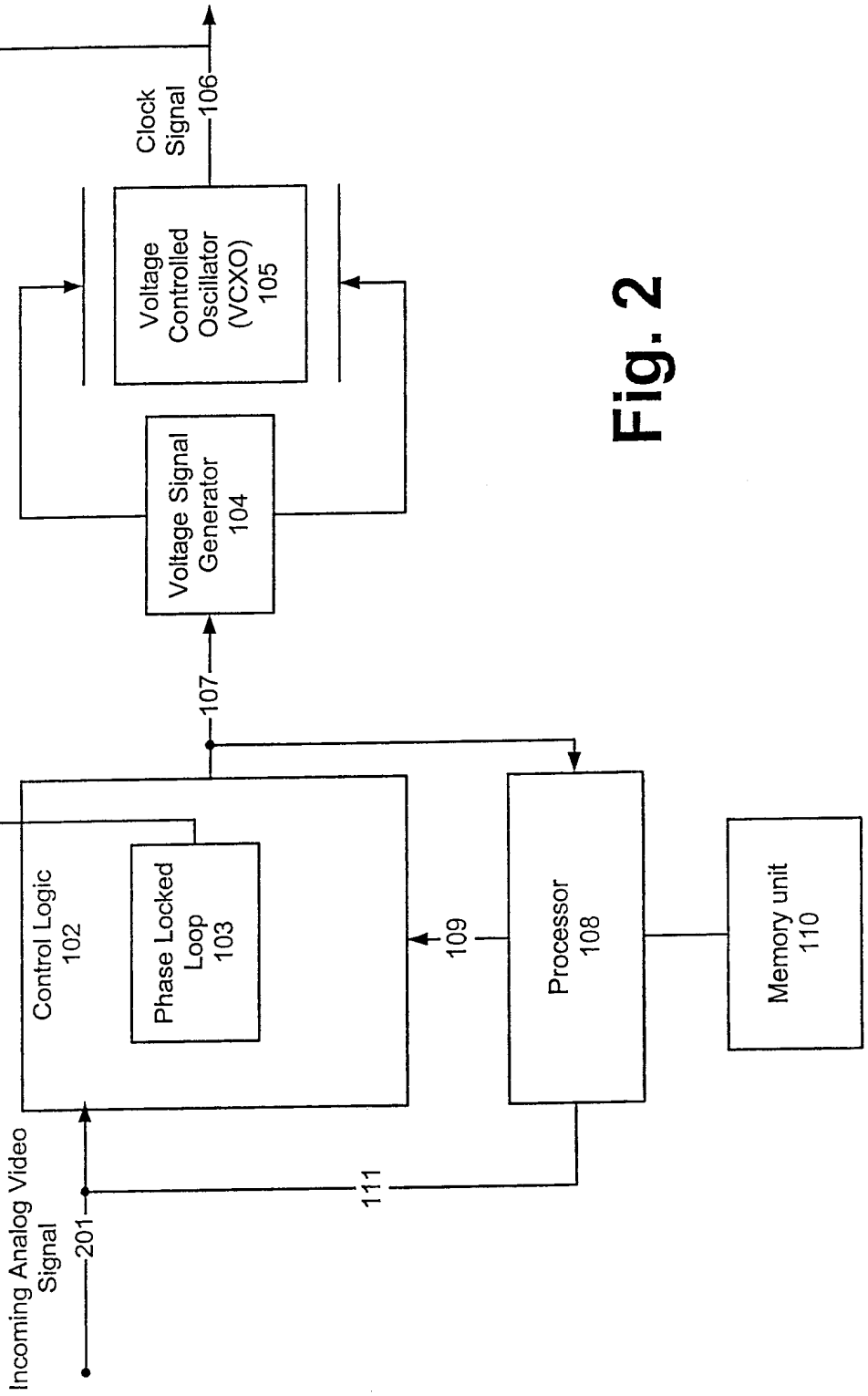

Clock Signal
106
Voltage Controlled Oscillator (VCXO) 105
Voltage Signal Generator 104
112
107
Control Logic 102
Phase Locked Loop 103
109
Processor 108
Memory unit 110
111
Incoming Analog Video Signal
201

Fig. 2

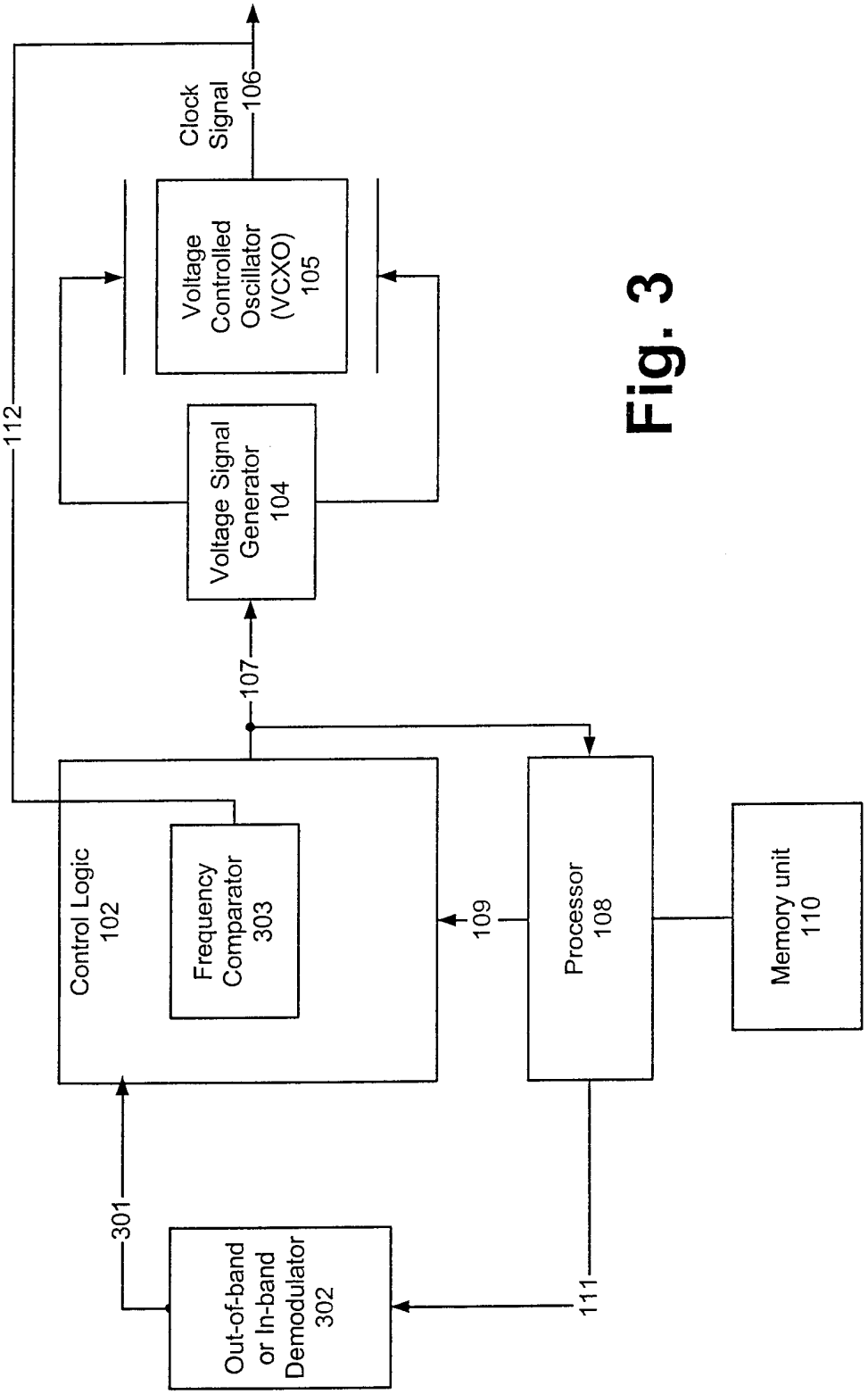

Clock Signal 106
Voltage Controlled Oscillator (VCXO) 105
Voltage Signal Generator 104
112
107
Control Logic 102
Frequency Comparator 303
109
Processor 108
Memory unit 110
301
Out-of-band or In-band Demodulator 302
111

Fig. 3

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/21578

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04N5/445 G09G5/18 H03L7/14

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G09G H04N H03L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y	column 6, line 63 - line 66	4,5,12, 17,18, 20-22,25

Y	US 4 631 588 A (BARNES LAWRENCE C ET AL) 23 December 1986 (1986-12-23) column 3, line 43 -column 5, line 23	4,17, 20-22,25

Y	US 5 612 981 A (HUIZER CORNELIS M) 18 March 1997 (1997-03-18) column 7, line 8 -column 9, line 56; figure 5	5,12,18

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
8 November 2000	16/11/2000

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/21578

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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