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(54) IMPROVEMENTS IN OR RELATING TO FIRE ALARMS

(71) We, SIEMENS AKTIENGESELLSCHAFT, a German Company of Berlin and Munich, German Federal Republic, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to fire alarms comprising a plurality of fire detector units connected in cascade and means to successively interrogate each unit in turn to establish the instantaneous condition of a respective sensing device provided in each unit to produce an analogue signal whose value represents the ambient conditions, and in particular the temperature level, in order to establish the presence or absence of any fire, this signal being analysed in a central control apparatus.

Such fire alarms require the provision of an emergency supply to maintain operational reliability in the event of any failure of the normal mains supply, at least for a definite period of time, and independent battery supply means are generally provided. The requisite storage capacity is dependent upon the current requirements of the central control apparatus, and the number of detectors connected thereto.

One object of the present invention is to provide an alarm whose circuit arrangement is such that the energy consumption of individual detectors is significantly reduced without endangering any signal transmission from a detector alarm to the central control apparatus, so that a lower energy consumption is obtained without adversely effecting efficiency.

The invention consists in a fire alarm in which a plurality of detector units are connected in cascade to form a two-wire alarm current loop from a central control apparatus, each detector unit including a sensor to produce a voltage forming an analogue value signal representative of an ambient condition at its unit and a timing element which introduces a response delay determined by the associated value signal, and said central control apparatus including means for initiating an interrogation cycle during which respective series-connected interrogation switches in the individual units are successively rendered conductive to pass a current signal whose delay is representative of the value of said analogue value signal, and each detector unit having an output load resistor that is connected in a shunt arm across the loop by the associated timing element to cause an increase in the loop current signal produced by interrogation of that detector unit.

Advantageously, said load resistor forms part of a RC element.

Preferably said load resistor is incorporated in a monostable trigger stage Advantageously, selective interrogation of individual detector units is effected by a disconnection of the supply loop from the cascaded detectors prior to an interrogation cycle in which reconnection of the detectors to the alarm loop is effected successively.

The invention will nowe be described with reference to the drawings, in which:—

Figure 1 schematically illustrates one exemplary embodiment of a fire alarm constructed in accordance with the invention;

Figure 2 is a circuit diagram of one detector unit of the alarm shown in Figure 1;

Figure 3 is a set of explanatory waveform diagrams;

Figure 4 is a circuitry detail illustrating a monostable trigger stage with a load resistor used in a preferred embodiment; and

Figure 5 is an explanatory waveform diagram relating to the circuit shown in Figure 4.

In the exemplary embodiment shown in Figure 1, detector units Md1 to Md30 are connected in cascade to a central control apparatus Ze, which includes an analysis micro-computer Mc, the illustration being purely schematic, and serving merely to explain the function.

An alarm current loop path *Ms* is connected between terminals of batteries B*a*1 and B*a*2, which are connected in series in a central control apparatus *Ze*, a change-over switch Us being included in the loop path.

Interrogation windings W*i*1, W*i*2 are symmetrically connected into the respective supply lines to the terminals of the battery B*a*1, and any change in the loop current flowing when these two windings are conductive will cause pulses to be fed via a common core Ke to an output winding W*i*3. The windings Wi1 to W*i*3 form a transformer Ue which is tuned by a capacitor Co to form a resonant circuit that is heavily damped by a parallel resistor R*e*. Any received pulses which form interrogation response signals, are amplitude limited by two oppositely connected limiting diodes D*i* and D*i*[1], and fed to an input of a threshold value switch Sw to produce rectangular pulses which are fed, for further analysis, to a micro-computer Mc, to be described.

The current loop path Ms is formed by a cascade of detector units M*d*1 to M*d*30, with respective series limiting resistors R*e*1 and R*e*2 in each conductor, and a terminating resistor R*e*3 (not shown). Each detector unit includes a respective series-connected interrogation transistor switch S*c*1 to S*c*30 respectively, and to initiate an interrogation cycle the switch U*s* is first open-circuited to remove the application of battery potential from the loop path conductors, and then moved into an interrogation position in which it connects its associated conductor via the winding W*i*1 to the battery B*a*1. As a result, a voltage is again applied to cause current to flow into the loop path M*s*.

Following the removal of the voltage supply to the measuring loop path M*s*, timing elements Zg1 to Zg30 in the respective units open each associated interrogation switch Sc1 to Sc30 in the individual detector units M*d*1 to M*d*30, and thus disconnect the cascade into individual units unconnected to the central control apparatus Ze. When the voltage supply is reconnected to the first detector unit M*d*1 by operation of the switch U*s*, the measuring transformer W*d*1 in that unit controls the timing element Zg1 in accordance with the ambient condition at that unit, and the said timing element closes the associated interrogation switch S*c*1 after a length of time, whose duration thus forms an analog signal of the local ambient condition, and at the same time reconnects the following unit M*d*2 to the central control apparatus Z*e*. All the units are thus consecutively connected to the central control apparatus Z*e*, which will be described in more detail with reference to Figure 3. Reverting to Figure 1, in each unit a series connection of diode D*i*1 and capacitor C*o*1 is simply a means to supply the respective measuring transformer W*d*1 etcetera, and possibly also the respective timing element Z*g*1 etcetera, with an operating voltage during the time in which the voltage supply is disconnected by the switch U*s* in the central control apparatus Z*e*. The terminating resistor Re3 which lies at the end of the cascade provides for the requisite increase in current on the closure of the interrogation switch S*c*30, so enabling this switch closure to be detected in the central control apparatus.

Figure 2 shows further details each detector unit M*d*. A Zener diode D1 serves to provide protection against excess voltages or any reversal of polarity when the alarm M*d* is first connected A diode D2 (D*i*1 in Figure 1) is to charge the capacitor C1 (C*o*1 in Figure 1) whilst voltage is connected to the alarm current loop path M*s*, the diode serving to prevent the capacitor discharging rapidly when the alarm loop path M*s* is disconnected from the central control apparatus Z*e*. Thus the capacitor C1 bridges the intervals when no voltage is applied to the alarm loop path M*s*. A transistor T1, in combination with a resistor R1 and a Zener diode D3 serves to stabilise the voltage fed to an ionisation chamber J, which forms the detector means for sensing the ambient conditions. A field effect transistor F, in combination with its operating resistor R2, amplifies the output voltage of the ionisation chamber J, so that the voltage level at a measuring point M changes in dependence upon the state of the ionisation chamber J. The timing element Zg consists of resistors R3 to R7 and two transistors T2 and T3, together with a capacitor C2. The latter discharges during each disconnection of the voltage supply from the central control apparatus Z*e*, and on reconnection of the supply the transistors T2 and T3 are conductive, so that the interrogation transistors T4 and T5 are held blocked. The capacitor C2 recharges when the supply is reconnected, until the voltage across the capacitor C2 has reached the value predetermined by the measuring point M, when the transistors T2 and T3 block, and render the transistors T4 and T5 conductive, so as to reconnect the next unit M*d* in the cascade. The resultant increase in the current in the alarm current loop path M*s* serves as an indication of the time of closure, as will be described later. The resistor R7 determines the base current for T4. The capacitor C3 prevents the transistor T4 being temporarily switched through, as a result of the transit times, when a voltage is applied between the points 1 and 2. The diode D5 serves to assist the drive of the transistor T4, but does not form the subiect of this application and therefore will not be discussed in further detail here.

In each case, the connection of the next detector unit in the cascade into the alarm loop M*s* by any preceding detector unit results in the connection of an arrangement comprising a load resistor R8 and a capacitor C4 of the first mentioned detector unit to the alarm loop M*s*, so that the latter capacitor is recharged, because during the voltage disconnection it will have discharged via the alarm current loop M*s*.

Figure 3 shows the voltage applied to the loop in an upper waveform diagram, in which a period 00 represents the initial time when the switch U*s* is connecting maximum potential, a period 01 represents the time during which the switch U*s* is open and no potential is applied, so that the loop is prepared for interrogation, and a period 02 represents an actual interrogation, during which current signals are received, as shown in the lower waveform of Figure 3.

The charging current of the capacitor C4 produces switch-on peaks in the current diagram JM shown in the lower waveform of Figure 3 at the end of respective time intervals t_1, t_2 etc., when each "next" unit is connected, as described above, and thus clearly characterise the instant of switching on of the particular next detector unit.

Figure 4 shows a preferred embodiment of the circuit, in which a transistors T6 is connected via a resistor R9 to the connection point N between the capacitor C4 and load resistor R8 of Figure 2. In this embodiment, a collector resistor R10 fundamentally produces the requisite current amplification in the measuring loop M*s*, on reconnection.

An explanatory waveform shown in Figure 5 illustrates the current curve produced in the alarm current loop M*s*, by the action of this monostable trigger stage.

The upper waveform shown in Figure 3 is obtained by controlled actuation of the switch U*s*. For example, a motor-driven cam could be used to hold the switch in the illustrated position for a reset period "00", and then move the switch-contact to an intermediate position for a period "01" during which no voltage is applied to the loop path and the individual interrogation switches allowed to "open", i.e. to become non-conductive, whilst the load resistors R8 discharge their associated capacitors C4.

After this intermediate preparation period an actual interrogation period is commenced by moving the switch U*s* to its other contact-position, so that current is fed to the loop path via the windings of the transformer U*e*, for a period "02" long enough to ensure there is time to analyse the respective response signals from each detector unit in the cascade. At the end of this period the switch U*s* is moved back to its reset position and a further period "00" commences. Naturally, in most applications this switching programme can be effected in known manner by electronic switching stages, rather than the use of electromechanical means. The response signals thus produced for analysis are shown in the lower waveform of Figure 3. During the period "02", the opening of each successive interrogation switch causes a stepped increase in the current flowing in the loop path, as already described with reference to Figure 1, the resultant pulses in the transformer output winding W*i*3 are clipped and shaped to produce an output signal of determined form from the threshold switch S*w*. Thus, at a time *t*1, when the interrogation period starts, current is fed to the detector unit M*d*1, and at a time *t*2, when the capacitor C2 (Figure 2) of that unit is charged to the particular value of the associated monitoring point M, which is determined by the associated ionisation chamber, the switch S*c*1 is closed, to connect the unit M*d*2, and so cause a further increase in the loop current, and a new pulse from the threshold switch S*w*. The magnitude of the increase is virtually equal in each case, but the time before the next increase occurs is an analog representation of the state of the relevant ionisation chamber, as described with reference to Figure 2. Thus, the interval between instants *t*1 and *t*2 give the value of the potential level at point M in the first unit, whilst the interval between *t*2 and *t*3 gives the corresponding information for the next unit in the cascade, and so on. The pulses fed to the microcomputer M*c* are selectively passed to respective stores, one for each detector unit, by means of a rotary switch, ring counter circuit, or the like.

During each analog signal, e.g. for the time interval between *t*1 and *t*2 in the case of the first unit, a pulse generator (not shown) feeds pulses to a respective counter store which has an alarm output set at a significant count value that would indicate an alarm condition in the first unit. If this value is not reached by the time *t*2, then no alarm is triggered, and a similar counting process commences for the second unit, and so on. A test key may be provided to manually trigger an alarm during any required unit setting, to check that all units are functioning properly in the required manner.

WHAT WE CLAIM IS:—

1. A fire alarm in which a plurality of detector units are connected in cascade to form a two-wire alarm current loop from a central control apparatus, each detector unit including a sensor to produce a voltage forming an analogue value signal representative of an ambient condition at its unit and a timing element which introduces a response delay determined by the associated value signal, and said central control apparatus including means for initiating an interrogation cycle during which respective series-connected interrogation switches in the individual units are successively rendered conductive to pass a current signal whose

delay is representative of the value of said analogue value signal, and each detector unit having an output load resistor that is connected in a shunt arm across the loop by the associated timing element to cause an increase in the loop current signal produced by interrogation of that detector unit.

2. A fire alarm as claimed in Claim 1, in which each said load resistor forms part of a RC-element in the associated detector unit.

3. A fire alarm as claimed in Claim 2, in which means are provided for the capacitor of said RC-element to be discharged shortly prior to each interrogation.

4. A fire alarm as claimed in Claim 2, in which means are provided for said capacitor of the RC-element to be recharged directly following each interrogation.

5. A fire alarm system as claimed in Claim 1, in which said load resistor forms part of a monostable trigger stage.

6. A fire alarm as claimed in any preceding Claim, in which the selective interrogation of the individual detector units is initiated by a common disconnection of all the detectors from the alarm current loop supply source.

7. A fire alarm substantially as described with reference to Figures 1 and 2, or Figures 1, 2 and 4.

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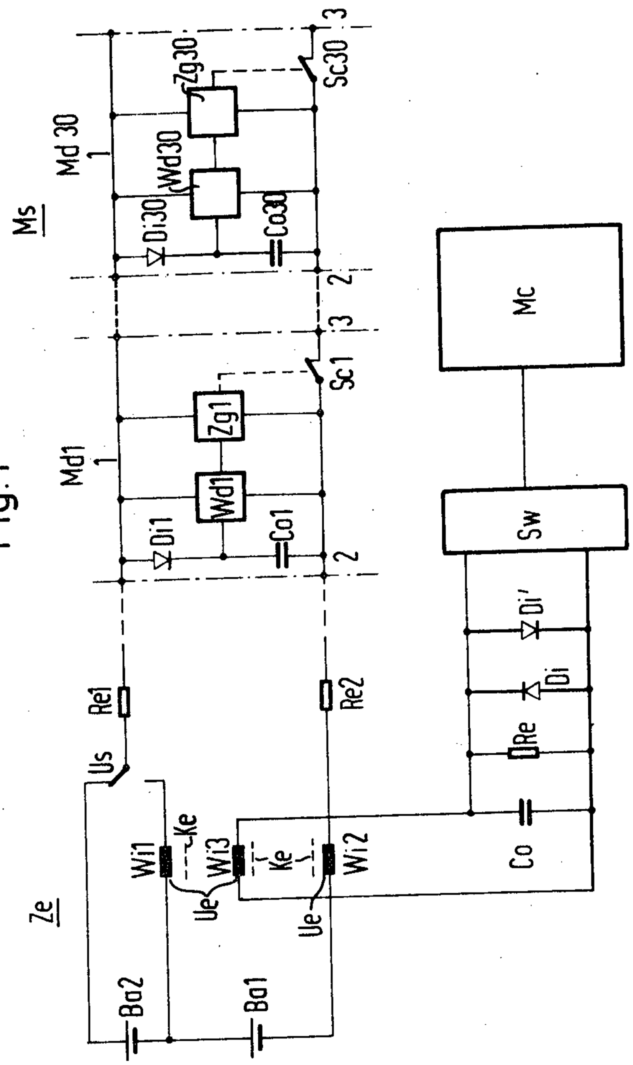
Sheet 1

Fig. 1



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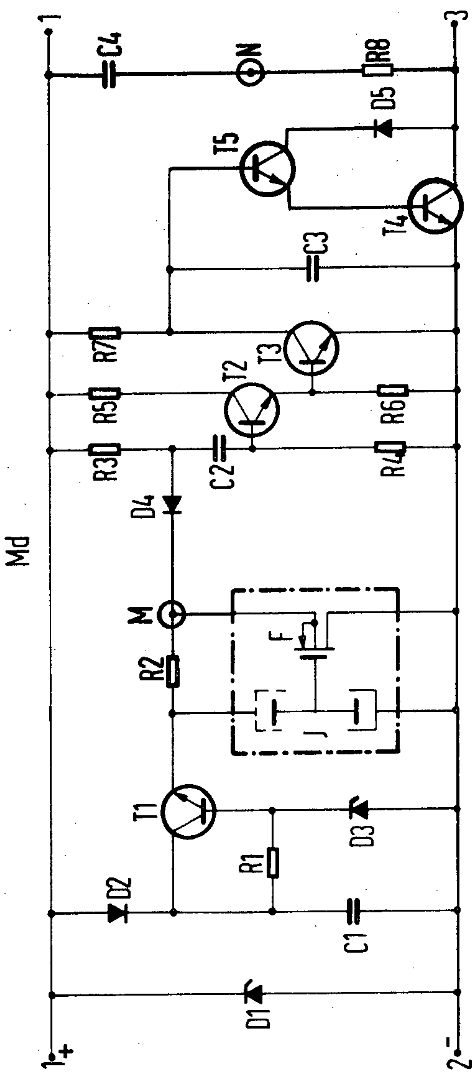
Sheet 2

Fig. 2



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Sheet 3

Fig.3

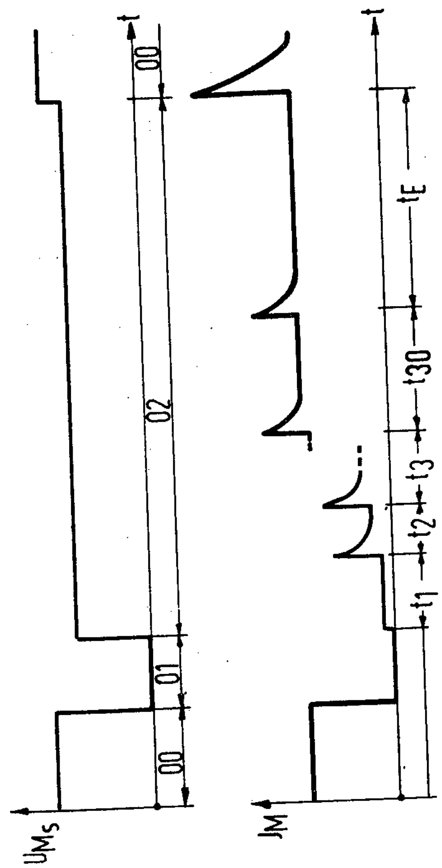

Fig. 4

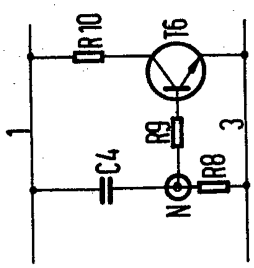

Fig. 5