June 16, 1964 J. WIEGAND 3,137,842

INTERCEPTOR TRANSFORMER FOR DATA STORAGE

Filed Aug. 5, 1960 2 Sheets-Sheet 1

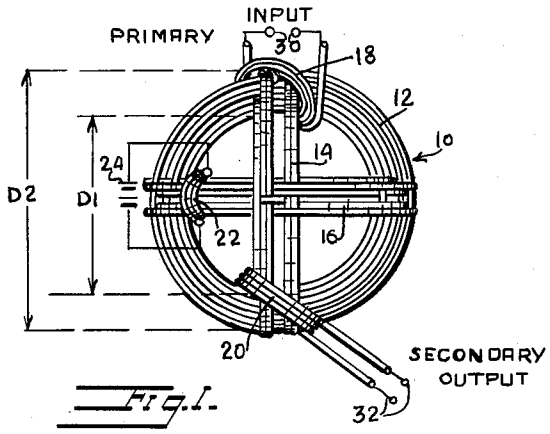


Fig. 1.

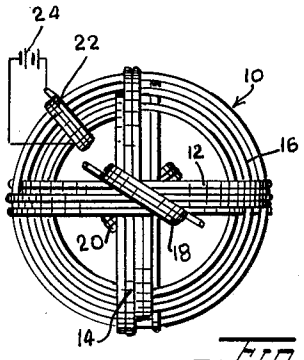


Fig. 2.

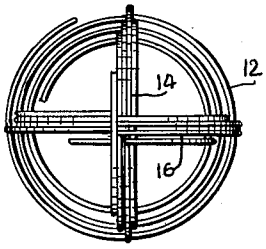


Fig. 3.

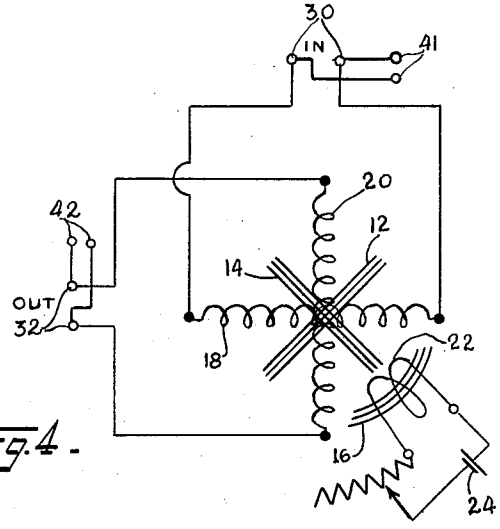


Fig. 4.

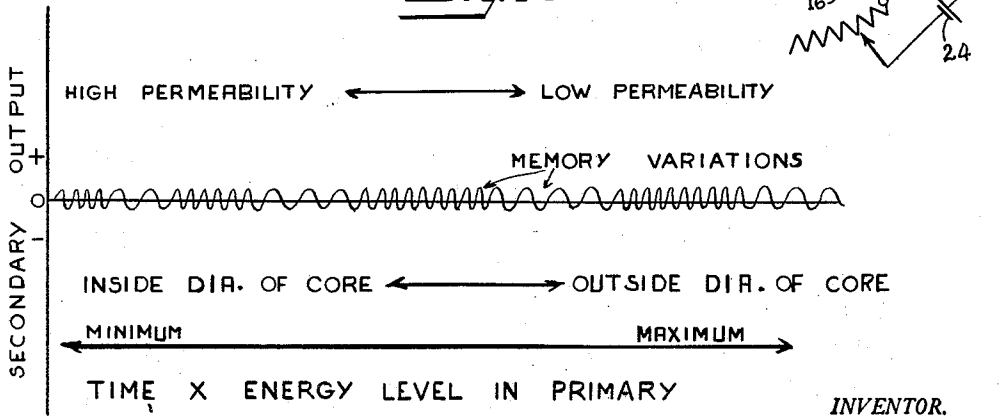


Fig. 5.

INVENTOR.
JOHN WIEGAND
BY
ATTORNEY

June 16, 1964 J. WIEGAND 3,137,842

INTERCEPTOR TRANSFORMER FOR DATA STORAGE

Filed Aug. 5, 1960 2 Sheets-Sheet 2

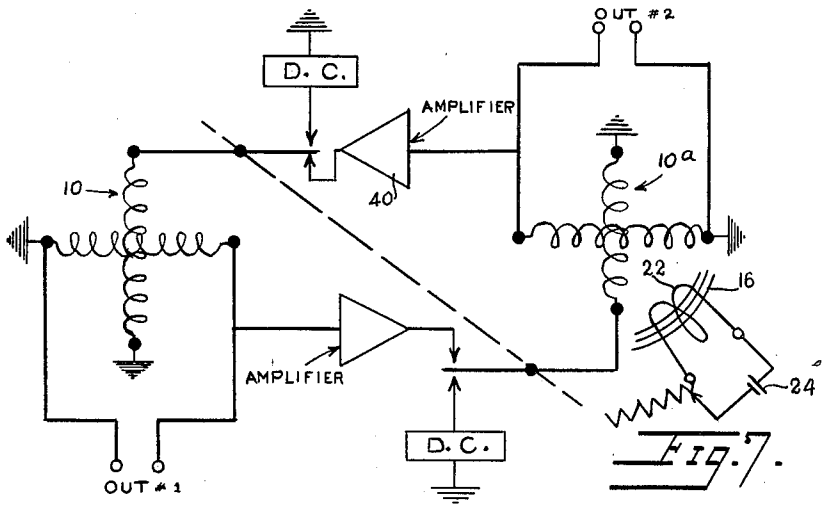


Fig. 7.

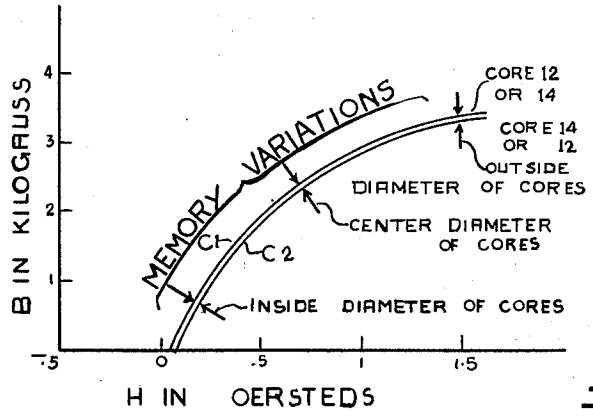


Fig. 6.

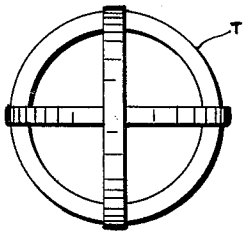


Fig. 8.

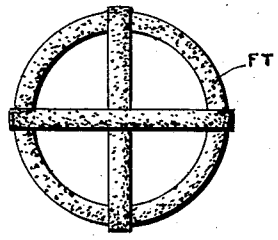


Fig. 9.

INVENTOR.
JOHN WIEGAND

BY Zoltan A. Polacheck

ATTORNEY

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3,137,842

INTERCEPTOR TRANSFORMER FOR DATA STORAGE

John Wiegand, 882 Balfour St., North Valley Stream, Long Island, N.Y.

Filed Aug. 5, 1960, Ser. No. 47,832
12 Claims. (Cl. 340—174)

This invention relates to improvements in interceptor transformers particularly useful as memory units for electronic computers, automatic controls, telemetering and the like.

This invention is an improvement over my prior Patents 2,740,096; 2,798,987 and 2,910,654.

According to the invention, there is provided an interceptor transformer including a magnetic core assembly consisting of three annular magnetic cores, each composed of wires, magnetic tapes or ferric powder members meshed and interwoven at points where the cores cross each other. The cores are disposed perpendicular to each other in three planes and cross each other at diametrally opposed points. Primary and secondary windings are wound on the magnetic core assembly at diametrally opposed points on two of the cores designated as "work cores." Primary and secondary windings are in a zero mutual induction condition. The third core designated the "bias core" carries a bias coil which is electrically energized to keep a predetermined residual magnetism in the bias core. The several cores have high magnetic permeability at inner circumferences or diameters; and this permeability gradually decreases to a minimum at the extreme outer circumferences or diameters.

A principal object of the invention is to provide a memory unit into which information can be "written" and out of which stored information can be "read."

Another object is to provide a device into which information having variable amplitudes can be written and out of which identical information can be read, the device employing a unitary magnetic core assembly, a primary coil for feeding data electrically and a secondary coil for extracting data electrically.

Another object is to provide a unitary electric device for registering a signal having a certain frequency for a certain length of time and for reading out the signal at a faster or slower rate, without employing mechanical moving means such as tape recorders or the like.

A further object is to provide a memory unit having a primary coil used to write data into the core electromagnetically with a decreasing energy level of alternating current and having a secondary coil out of which a steady level output can be derived representing the data written into the core, the "read out" of the secondary coil being triggered or pulsed by applying direct current of increasing energy level to the primary coil.

For further comprehension of the invention, and of the objects and advantages thereof, reference will be had to the following description and accompanying drawings, and to the appended claims in which the various novel features of the invention are more particularly set forth.

In the accompanying drawings forming a material part of this disclosure:

FIG. 1 is an elevational view of an interceptor transformer embodying the invention.

FIG. 2 is a top plan view of the transformer of FIG. 1.

FIG. 3 is an elevational view of a magnetic core assembly showing the winding arrangement.

FIG. 4 is a circuit diagram of the interceptor transformer.

FIGS. 5 and 6 are charts useful in explaining the invention.

FIG. 7 is a circuit diagram showing a plurality of interceptor transformers arranged as a counting chain.

FIGS. 8 and 9 are views similar to FIG. 3 showing modified forms of core assemblies.

Referring to FIGS. 1–4, there is shown an interceptor transformer **10**, consisting of three annular or toroidal cores **12**, **14** and **16**. Each core may be formed from a single length of nickle-iron alloy wire spirally wound as shown most clearly for core **12** in FIG. 3. The cores may also be composed of a single length of thin magnetic metal tape T instead of wire as shown in FIG. 8, or may be composed of a length of tape FT formed of ferric powder as shown in FIG. 9. The cores are endless magnetic rings which are circular in form and are disposed in three mutually perpendicular planes. They cross each other at diametrally opposed points spaced 90° apart in vertical and horizontal planes as viewed in FIGS. 1–3. The vertical cores **12** and **14**, designated "work cores," carry coils **18**, **20** of electrically conductive insulated wire at their uppermost and lowermost junctions diametrally opposed on the common diameter of the two cores **12**, **14**. Coil **18** is a primary coil for applying alternating or direct current thereto. Coil **20** is a secondary coil. Both coils are so placed that a zero mutual induction condition exists.

On the third core **16**, designated the "bias core," is a coil **22** of insulated wire to which direct current is applied from a battery **24** or other source of direct current to keep this core magnetized with a bias level of magnetism.

Information or data in electrical form is written in by applying an alternating current signal of decreasing amplitude to input terminals **30** of the primary coil **18**. The current flow in coil **18** induces magnetic fields in cores **12** and **14**. As the alternating current signal decreases in energy level through the primary coil **18**, the magnetic field induced in the cores **12**, **14** first leaves the outside portions of larger diameter D2; then leaves the center portions, and lastly leaves the innermost portions of smallest diameter D1. This occurs because the outer portions of larger diameter have lower magnetic permeability while the center portions have higher permeability and while the innermost portions have highest permeability.

In order to recover the stored information in a read out operation, direct current is applied via terminals **41** to input terminals **30** of the primary coil. This gradually increases the magnetization of the core assembly. The portions of the work cores of smallest diameter D1 are magnetized first and magnetization proceeds through the cores until the portions of largest diameter D2 are increased in magnetization. As the magnetizing forces are applied successively through the work cores **12**, **14** they encounter the residual magnetism representing the stored information. As a result, a signal is produced at the output terminals **32** of the secondary coil. This output signal corresponds in varying amplitude to the previously applied alternating current that left the residual magnetizations as it previously gradually lowered in amplitude.

It is significant that this alternating voltage signal is produced while a direct current is being applied to the primary coil. While this D.C. sweeps over all the wire crossings to the outside low permeability core section, thus, the applied direct current pulses or triggers the read out of the device.

FIG. 6 illustrates by hysteresis curves C1 and C2 the magnetic condition of the work cores **12** and **14** just after magnetic variations are stored therein by the applied alternating current of decreasing amplitude, and prior to application of the direct current to read out these magnetic variations.

The application of the direct current effects an equalization of magnetization as seen at the total core through the primary coil **18** so that the device is then ready for application of the next signal to be stored.

The amplitude of the signal read out of the secondary coil has a considerably lower amplitude throughout in comparison to signal input than the applied signal written into the primary. The output of the secondary through a slow rising D.C. in the primary is a "destructive read-out." In other words, it destroys the memory which can be read out only once. If two such transformers are used to read out of, one can be used to rewrite into another in order to read out one information more than once. This may be compensated by applying the output signal to an amplifier **40** connected to the output of transformer **10**, as indicated in the circuit of FIG. 7. The output signal can in turn be applied to the input **30** of a succeeding interceptor transformer **10a**. In order to trigger the read out of the successive transformers, direct curent will be applied via terminals **41** and **42**. This bias current applied to bias coils **22** of the several transformers may be provided by a signal battery **24** connected to the two bias coils in parallel.

There has thus been provided, according to the invention, a means of writing electrical signal data in alternating current form and reading out corresponding alternating current data upon application of a direct current read out signal. The device is useful in digital and electronic computers, automatic controls for electronic equipment and other application.

While I have illustrated and described the preferred embodiments of my invention, it is to be understood that I do not limit myself to the precise construction herein disclosed and that various changes and modifications may be made within the scope of the invention as defined in the appended claims.

Having thus described my invention, what I claim as new, and desire to secure by United States Letters Patent is:

1. An interceptor memory transformer adapted for writing in, storing and reading out information in the form of alternating current signals, comprising three annular magnetic cores crossing each other at diametrally opposed points in three mutually perpendicular planes, a primary coil wound on a first intersection of two of the cores, and a secondary coil wound on a second intersection of said two cores diametrally opposed to the first intersection.

2. An interceptor memory transformer adapted for writing in, storing and reading out information in the form of alternating current signals, comprising three annular magnetic cores crossing each other at diametrally opposed points in three mutually perpendicular planes, a primary coil wound on a first intersection of two of the cores, and a secondary coil wound on a second intersection of said two cores diametrally opposed to the first intersection, there being a bias coil wound around the third one of the cores for maintaining a bias magnetization in the cores.

3. An interceptor memory transformer adapted for writing in, storing and reading out information in the form of alternating current signals, comprising three annular magnetic cores crossing each other at diametrally opposed points in three mutually perpendicular planes, a primary coil wound on a first intersection of two of the cores, and a secondary coil wound on a second intersection of said two cores diametrally opposed to the first intersection, there being a bias coil wound around the third one of the cores for maintaining a bias magnetization in the cores, the magnetic permeability of the cores varying progressively and decreasing from portions of minimum diameter of the cores outwardly to portions of maximum diameter of the cores.

4. An interceptor memory transformer adapted for writing in, storing and reading out information in the form of alternating current signals, comprising three annular magnetic cores crossing each other at diametrally opposed points in three mutually perpendicular planes, a primary coil wound on a first intersection of two of the cores, and a secondary coil wound on a second intersection of said two cores diametrally opposed to the first intersection, there being a bias coil wound around the third one of the cores for maintaining a bias magnetization in the cores, the magnetic permeability of the cores varying progressively and decreasing from portions of minimum diameter of the cores outwardly to portions of maximum diameter of the cores, said primary coil having input terminals for applying an alternating current to the primary coil, said secondary coil having output terminals for deriving an alternating current therefrom upon application of a direct current to said input terminals subsequent to application of the alternating current to the input terminals.

5. A circuit comprising two interceptor memory transformers, each of said transformers including three annular magnetic cores crossing each other at diametrally opposed points in three mutually perpendicular planes, a primary coil wound on a first intersection of two of the cores, and a secondary coil wound on a second intersection of said two cores diametrally opposed to the first intersection; and an amplifier having its input connected to the output terminals of one transformer and its output connected to the input terminals of another transformer.

6. An interceptor memory transformer adapted for writing in, storing and reading out information in the form of alternating current signals, comprising three annular magnetic cores crossing each other at diametrally opposed points in three mutually perpendicular planes, a primary coil wound on a first intersection of two of the cores, and a secondary coil wound on a second intersection of said two cores diametrally opposed to the first intersection, there being a bias coil wound around the third one of the cores for maintaining a bias magnetization in the cores, the magnetic permeability of the cores varying progressively and decreasing from portions of minimum diameter of the cores outwardly to portions of maximum diameter of the cores, each of said cores consisting of a coil of magntic wire wound to form an endless ring, the cores being interwoven at their intersections to form an A.C. output in secondary while a direct current sweeps from a low to a higher energy in the primary.

7. A circuit comprising two interceptor memory transformers, each of said transformers including three annular magnetic cores crossing each other at diametrally opposed points in three mutually perpendicular planes, a primary coil wound on a first intersection of two of the cores, and a secondary coil wound on a second intersection of said two cores diametrally opposed to the first intersection; and an amplifier having its input connected to the output terminals of one transformer and its output connected to the input terminals of another transformer, there being a bias coil wound on the third one of the cores, the bias coil of each transformer being connected to a direct current source, each of said transformers having terminals connected to the primary coil for applying a direct current to the primary and triggering output of an alternating current from the output terminals of the transformer.

8. A circuit comprising two interceptor memory transformers, each of said transformers including three annular magnetic cores crossing each other at diametrally opposed points in three mutually perpendicular planes, a primary coil wound on a first intersection of two of the cores, and a secondary coil wound on a second intersection of said two cores diametrally opposed to the first intersection; and an amplifier having its input connected to the output terminals of one transformer and its output connected to the input terminals of another transformer, there being a bias coil wound on the third one of the cores, the bias coil of each transformer being connected to a direct current source, each of said transformers having terminals connected to the primary coil for applying a direct current to the primary and trigger-

ing output of an alternating current from the output terminals of the transformer, each of the cores in each transformer consisting of a coil of magnetic wire wound to form an endless ring, the cores being interwoven at their intersections to form an A.C. output in secondary while a direct current sweeps from a low to a higher energy in the primary.

9. A circuit comprising two interceptor memory transformers, each of said transformers including three annular magnetic cores crossing each other at diametrally opposed points in three mutually perpendicular planes, a primary coil wound on a first intersection of two of the cores, and a secondary coil wound on a second intersection of said two cores diametrally opposed to the first intersection; and an amplifier having its input connected to the output terminals of one transformer and its output connected to the input terminals of another transformer, there being a bias coil wound on the third one of the cores, the bias coil of each transformer being connected to a direct current source, each of said transformers having terminals connected to the primary coil for applying a direct current to the primary and triggering output of an alternating current from the output terminals of the transformer, each of the cores in each transformer consisting of a coil of magnetic wire wound to form an endless ring, the cores being interwoven at their intersections to form an A.C. output in secondary while a direct current sweeps from a low to a higher energy in the primary, the magnetic permeability of the cores in each transformer varying progressively and decreasing from portions of minimum diameter outwardly to portions of maximum diameter in the assembly.

10. A circuit comprising two interceptor memory transformers, each of said transformers including three annular magnetic cores crossing each other at diametrally opposed points in three mutually perpendicular planes, a primary coil wound on a first intersection of two of the cores, and a secondary coil wound on a second intersection of said two cores diametrally opposed to the first intersection; and an amplifier having its input connected to the output terminals of one transformer and its output connected to the input terminals of another transformer, the magnetic permeability of the cores in each transformer varying progressively and decreasing from portions of minimum diameter outwardly to portions of maximum diameter in the transformer.

11. A circuit comprising two interceptor memory transformers, each of said transformers including three annular magnetic cores crossing each other at diametrally opposed points in three mutually perpendicular planes, a primary coil wound on a first intersection of two of the cores, and a secondary coil wound on a second intersection of said two cores diametrally opposed to the first intersection; and an amplifier having its input connected to the output terminals of one transformer and its output connected to the input terminals of another transformer, each of the cores consisting of a coil of thin magnetic tape wound to form an endless ring, the cores being interwoven at their intersections to form an A.C. output in secondary while a direct current sweeps from a low to a higher energy in the primary.

12. A circuit comprising two interceptor memory transformers, each of said transformers including three annular magnetic cores crossing each other at diametrally opposed points in three mutually perpendicular planes, a primary coil wound on a first intersection of two of the cores, and a secondary coil wound on a second intersection of said two cores diametrally opposed to the first intersection; and an amplifier having its input connected to the output terminals of one transformer and its output connected to the input terminals of another transformer, each of the cores consisting of a coil of thin tape formed of ferric powder to form an endless ring, the cores being interwoven at their intersections to form an A.C. output in secondary while a direct current sweeps from a low to a higher energy in the primary.

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