United States Patent [19]

Pfund

[11] **3,838,218**

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[54] **BIFREQUENCY CONTROLLED ANALOG SHIFT REGISTER SPEECH PROCESSOR**

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[22] Filed: **Mar. 7, 1972**

[21] Appl. No.: **232,495**

[52] **U.S. Cl.** ..... **179/1 SA,** 179/15.55 T

[51] **Int. Cl.** **G10l 1/00**

[58] **Field of Search** ..... 179/15.55 T, 15.55 R, 1 SA

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Primary Examiner—Kathleen H. Claffy

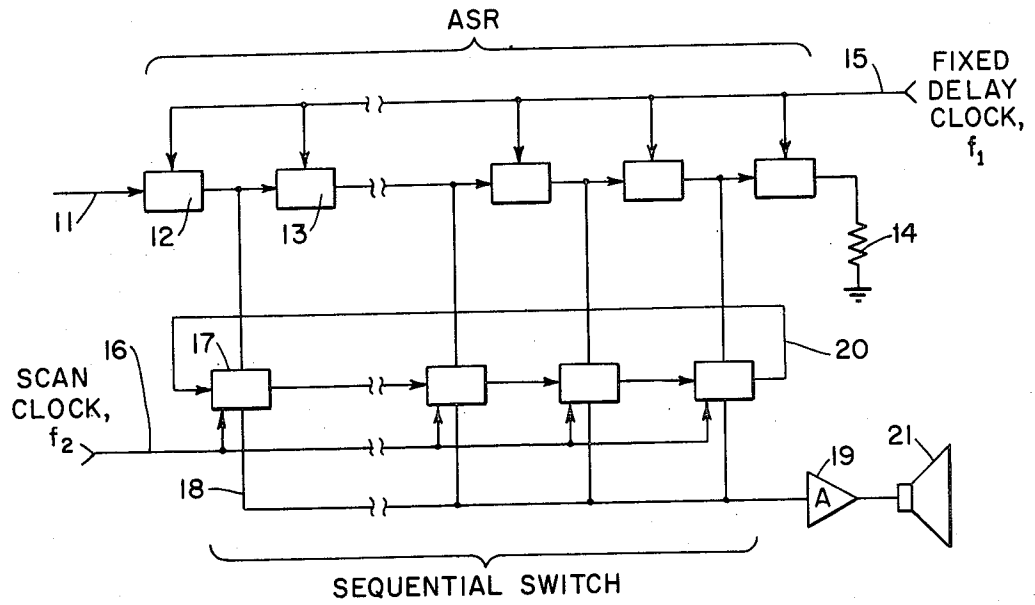
Assistant Examiner—Jon Bradford Leaheey

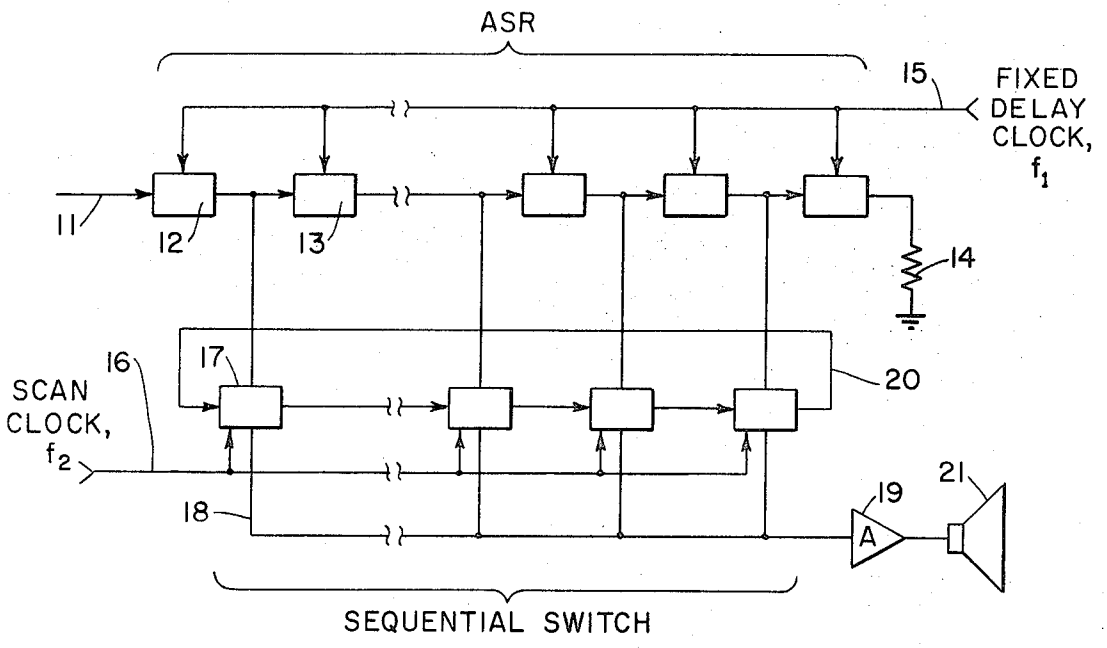
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[57] **ABSTRACT**

A processor for recorded speech and other sounds uses an analog shift register operating at one clock frequency to propogate speech signals through the register while a second clock frequency is used to sequentially shift signal values from each stage of the shift register to a common output where they are combined to operate an audio reproducer. The relative frequencies of the two clocks determines the frequency transformation ratio between the input and output signals.

1 Claim, 1 Drawing Figure




ASR
15
FIXED DELAY CLOCK, f_1
11
12
13
14
16
17
20
SCAN CLOCK, f_2
18
19
21
A
SEQUENTIAL SWITCH

BIFREQUENCY CONTROLLED ANALOG SHIFT REGISTER SPEECH PROCESSOR

BACKGROUND OF THE INVENTION

This invention relates generally to the field of sound signal processors wherein frequency transformation of a sound signal is achieved with or without change in the time duration normally associated with the sound utterance for the purpose of audibly reproducing the sound at its normal or desired pitch or frequency spectrum and in general pertains to the subject matter disclosed in application Ser. No. 171,571 filed Aug. 13, 1971. In that application the processing of sound for the purpose hereinabove stated including the expansion and compression of recorded speech signals is described in connection with various forms of storage delay devices which are capable of control for frequency transformation and which are adapted to accommodate the parameters of human speech.

In the above-referenced patent application, additional prior art is described pertaining to various electro-mechanical and discrete delay line type signal processors for this purpose.

SUMMARY OF THE INVENTION

The present invention provides a speech signal transformation processor of simplified form which permits speech signal inputs to be compressed or expanded in time with the appropriate frequency transformation so that they may be reproduced in audible form with the desired frequency components. For this purpose an analog shift register is used to store an input speech signal train of analog form with a first frequency clock used to shift the sampled version of the input signal stage-by-stage through the shift register at a rate determined by the clock. Associated with the analog shift register is a stage-by-stage readout register which permits sequential, parallel readout of the successive stages of the analog shift register which parallel sequential readouts are combined to form the signal which is applied to an audio reproducer. By controlling the relative clock frequencies for shift through the analog shift register and shift out from the successive stages of the register, frequency transformation, either up or down, is achieved thereby restoring the desired frequency components to the input sound signal as it appears in the output reproducer.

BRIEF DESCRIPTION OF THE DRAWING

The single FIGURE shows a block diagram of an analog shift register signal processor in accordance with the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to the drawing, the signal processor in accordance with the invention is shown to comprise an analog shift register ASR, having an input terminal **11** and successive stages **12, 13** with the output stage terminated in load impedance **14** if desired. The number of stages in the ASR is consistent with the maximum delay for the input speech signal which is desired and the sampling rate for both the input fixed delay clock f_1 and the output scan clock frequency f_2. For this purpose, each stored analog sample in the ASR individual stages is connected to be readout by a sequential switch

comprising gate stages **17** responsive to the clock signal on line **16** and connected to the analog signal sample of respective stages of the ASR which sample values are transferred in succession as the stages **17** are sequentially enabled from left to right in the FIGURE and combined on an output line **18.** The signal on line **18** is amplified in a suitable amplifier **19** and applied to an audio reproducer **21.** As previously stated, the scan clock frequency f_2 which is applied on line **16** will generally be a different frequency than the delay clock f_1 which may or may not be a fixed frequency with the ratio of the frequency transformation between the signal applied at input line **11** and appearing at the output line **18** being determined by the ratio of the frequencies f_1 and f_2. This ratio may be either greater or less than unity for obtaining compression or expansion.

As set forth in the herein referenced application Ser. No. 171,571 the signal on line **11** will generally be the reproduction of a recorded speech signal played back at a speed different than that at which it was recorded so that it occupies a different length of time than the normal speech utterance which was recorded. As is well known, changing the playback speed relative to the recording speed produces a corresponding change in the frequency spectrum of the signal. By selecting the frequencies f_1 and f_2 to have a corresponding ratio, the inverse frequency transformation can be achieved so that the signal on line **18** which is ultimately reproduced in the speaker **21** is restored to the normal frequencies of the original speech utterance.

The invention as disclosed in the present application is particularly suited to integrated circuit techniques where a plurality of stages for the ASR are readily achieved with the interstage gating for the sequential switch also being provided by the integrated circuit technique. The two clock frequencies f_1 and f_2 may be provided by similar simplified and economical circuit construction or may be applied to the integrated circuit frequency transformer as input signals as indicated in the drawing. In either event, the sound signal processor for frequency transformation is readily and economically achieved using the present invention with the usual additional controls, such as the playback speed and input and output filtering required as is well known in the art. For the purpose of output filtering, the amplifier **19** may also include a filter having a suppression characteristic to suppress the scan frequency f_2 without materially reducing adjacent sound signal frequencies.

As indicated in the drawing, it will be understood that the switch stages **17** are sequentially enabled from left to right by the successive pulses in the output scan clock, each stage being enabled for a set period sufficient to allow readout of a signal value from one of the stages of the ASR. The stages **17** are connected in a ring configuration so that when the final right-hand stage is read out, a signal is sent on line **20** to the left end stage and to resume the enabling sequence at the f_2 frequency. Alternately, a series of gates sequentially timed as disclosed in U.S. Pat. No. 3,541,264 can be used. The sequence rate for the sequential switch readout operation can be selected over a wide range in relation to the length of the storage analog shift register and the components of the signals being processed.

Various forms for implementing the present invention and modifications thereof will be apparent from the present disclosure and such modifications are to be

considered as being within the scope of the invention as defined by the appended claims.

I claim:

1. A processor for speech signals or the like comprising:

a single serial analog shift register having a predetermined plurality of stages with a signal input terminal for the first stage;

means for apply to said input terminal a frequency altered speech signal having frequency components altered by a given ratio;

means for clocking said analog shift register at a first clock frequency selected in relation to the number of said stages to provide predetermined maximum delay required for processing said frequency altered speech signal as said input signal values are shifted successively through the stages of said register;

means for clocking signals sequentially from the serial stages of said register at a second clock frequency related to said first clock frequency by said ratio by sampling the signal train stored in the stages of said register, both of said means for clocking operating concurrently on said analog shift register;

means for combining the signals clocked sequentially from the stages of said register to produce a frequency transformed version of the speech signal applied to said input terminal with original frequency components restored; and

means responsive to the combined signals for producing a replica of said speech signal.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 3,838,218

DATED : September 24, 1974

INVENTOR(S) : Charles E. Pfund

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In the legend: "[73] Assignee: Cambridge Research and Development Group, Westport, Conn."

should be -- "[73] Assignees: Cambridge Research and Development Group, Westport, Conn.; Sanford D. Greenberg, Washington, D.C.; DT Liquidating Partnership, New York, N.Y.; Murray M. Schiffman, Westport, Conn. --

Signed and Sealed this

twenty-sixth Day of *August 1975*

[SEAL]

Attest:

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C. MARSHALL DANN
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