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(54) Title: METHODS AND ARRANGEMENTS RELATING TO SEMICONDUCTOR PACKAGES INCLUDING MULTI-MEMORY DIES

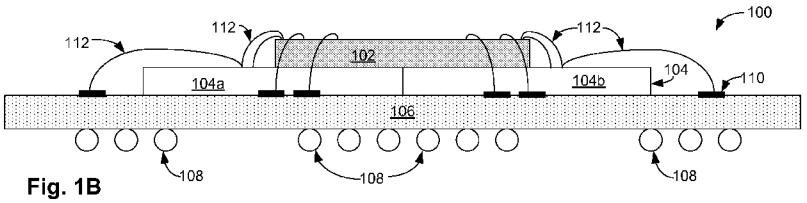

Fig. 1B

(57) Abstract: In an embodiment, there is provided a packaging arrangement comprising a substrate; a multi-memory die coupled to the substrate, wherein the multi-memory die comprises multiple individual memory dies, and each of the multiple individual memory dies is defined as an individual memory die within a wafer of semiconductor material during production of memory dies, and the multi-memory die is created by singulating the wafer of semiconductor material into memory dies, where at least one of the memory dies is the multi-memory die that includes the multiple individual memory dies that are still physically connected together; and a semiconductor die coupled to the multi-memory die and the substrate, wherein the semiconductor die is configured as a system on a chip, wherein at least one of the multi-memory die and the semiconductor die is attached to the substrate.

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METHODS AND ARRANGEMENTS RELATING TO SEMICONDUCTOR PACKAGES INCLUDING MULTI-MEMORY DIES

Cross-References to Related Applications

[0001] The present disclosure claims priority to U.S. Provisional Patent Application No. 61/674,703, filed July 23, 2012, U.S. Provisional Patent Application No. 61/675,626, filed July 25, 2012, and U.S. Non-Provisional Patent Application No. 13/947,936, filed July 22, 2013, the disclosures of which are hereby incorporated by reference. The present disclosure is related to U.S. Patent Application No. 13/532,444, filed June 25, 2012, and U.S. Patent Application No. 13/590,949, filed August 21, 2012, the disclosures of which are hereby incorporated by reference.

Technical Field

[0002] Embodiments of the present disclosure relate to the field of integrated circuits, and more particularly, to techniques, structures, and configurations for semiconductor chip packaging.

Background

[0003] The background description provided herein is for the purpose of generally presenting the context of the disclosure. Work of the presently named inventor(s), to the extent the work is described in this background section, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor impliedly admitted as prior art against the present disclosure.

[0004] Electronic devices utilize packages made up of semiconductor dies where the semiconductor dies are arranged and configured to perform various functions. For example, in a package, one semiconductor die may be configured as a system on a chip (SOC) while

another semiconductor die may be configured as a memory die. The SOC die and the memory die are then interconnected to perform various functions for an electronic device that houses the package. The semiconductor dies in these packages often generate large amounts of heat. Additionally, the semiconductor dies need access to power (VDD) and ground. Thus, in creating and designing such packages, there are many trade-offs including, cost, heat dissipation and access to VDD and ground, as well as interconnectivity among the semiconductor dies within the package.

Summary

[0005] In an embodiment, there is provided a packaging arrangement comprising a substrate; a multi-memory die coupled to the substrate, wherein the multi-memory die comprises multiple individual memory dies, and each of the multiple individual memory dies is defined as an individual memory die within a wafer of semiconductor material during production of memory dies, and the multi-memory die is created by singulating the wafer of semiconductor material into memory dies, where at least one of the memory dies is the multi-memory die that includes the multiple individual memory dies that are still physically connected together; and a semiconductor die coupled to the multi-memory die and the substrate, wherein the semiconductor die is configured as a system on a chip, wherein at least one of the multi-memory die and the semiconductor die is attached to the substrate.

[0006] In an embodiment, there is also provided a method comprising providing a substrate; coupling a multi-memory die to the substrate, wherein the multi-memory die comprises multiple individual memory dies, each of the multiple individual memory dies is defined as an individual memory die within a wafer of semiconductor material during production of memory dies, and the multi-memory die is created by singulating the wafer of

semiconductor material into memory dies, where at least one of the memory dies is the multi-memory die that includes the multiple individual memory dies that are still physically connected together; coupling a semiconductor die to the multi-memory die and the substrate, wherein the semiconductor die is configured as a system on a chip; and attaching at least one of the multi-memory die and the semiconductor die to the substrate.

Brief Description of the Drawings

[0007] Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. Embodiments are illustrated by way of example and not by way of limitation in the figures of the accompanying drawings.

[0008] Fig. 1A schematically illustrates a top view of an example of a packaging arrangement including a multi-memory die that comprises two individual memory dies.

[0009] Fig. 1B schematically illustrates a cross-sectional view of the packaging arrangement illustrated in Fig. 1A.

[0010] Figs. 1C and 1D schematically illustrate a top view and a cross-sectional view, respectively, of an example of a packaging arrangement including a multi-memory die that comprises two individual memory dies.

[0011] Figs. 2-8 schematically illustrate cross-sectional views of various packaging arrangements including a multi-memory die that comprises two individual memory dies.

[0012] Fig. 9 illustrates an example of a method for creating a packaging arrangement that comprises a semiconductor die coupled to a multi-memory die comprising multiple individual memory dies.

Detailed Description

[0013] Fig. 1A illustrates a top view of a semiconductor die 102 configured as a system on a chip (SOC) die stacked on a semiconductor die 104 configured as a memory die. The memory die 104 comprises two separate dies 104a, 104b that were not physically separated from each other when the memory die 104 was manufactured. During manufacturing, a wafer (not illustrated) of semiconductor material that has been configured into a plurality of semiconductor dies for production of semiconductor dies is generally singulated or divided, for example, by cutting with a laser, into individual semiconductor dies in order to provide a plurality of individual semiconductor dies that have been physically separated from each other. Thus, a wafer (not illustrated) that was configured with a plurality of memory dies was cut such that the memory die 104 includes the two memory dies 104a, 104b that are still attached to each other. The memory dies 104a, 104b are generally configured as dynamic random access memory (DRAM), although they can be configured as other types of memory if desired.

[0014] Fig. 1B schematically illustrates a cross-sectional view of the packaging arrangement illustrated in Fig. 1A. Fig. 1B illustrates the SOC die 102 and the memory die 104 stacked on a substrate 106. The S0C die 102 is attached to the memory die 104 via an appropriate epoxy or glue. Likewise, the memory die 104 is attached to the substrate 106 via an appropriate epoxy or glue. The substrate 106 includes solder balls 108 for attaching the resulting packaging arrangement 100 to another substrate such as, for example, a printed circuit board (PCB), another substrate, etc. (not illustrated). Various bonding pads 110 on the SOC die 102, the memory die 104 and the substrate 106 can be coupled to one another with wire bonds 112 via a wire bonding process. The bonding pads 110 can be configured to be utilized for, for example, signals relating to data, commands and/or

addresses, input/output, and access to VDD/ground. Furthermore, wire bonds 112 can be utilized between the SOC die 102 and the substrate 106, and between the memory die 104 and the substrate 106. For example, wire bonds 112 can be utilized to provide access to VDD/ground for the SOC die 102. The packaging arrangement 100 illustrated in Fig. 1B generally provides a reasonable cost but generally does not provide better than average heat dissipation for the SOC die 102 and the memory die 104. Additionally, the packaging arrangement 100 illustrated in Fig. 1A generally provides only minimal VDD/ground access.

[0015] In Figs. 1A and 1B, the bonding pads 110 of the memory die 104a are disposed on or near to a center section of the memory die 104a, and the bonding pads 110 of the memory die 104b are disposed on or near to a center section of the memory die 104b. However, in an embodiment, the bonding pads 110 of each of the memory dies 104a and 104b can be disposed, for example, near an edge of the corresponding memory die. For example, Figs. 1C and 1D schematically illustrate a top view and a cross-sectional view, respectively, of an example of a packaging arrangement including a multi-memory die that comprises two individual memory dies. Figs. 1C and 1D are to an extent similar to Figs. 1A and 1B, respectively. However, unlike Figs. 1A and 1B, in Figs. 1C and 1D, the bonding pads 110 of the memory die 104a are disposed near an edge of the memory die 104a, and the bonding pads 110 of the memory die 104b are disposed near an edge of the memory die 104b. Having the bonding pads 110 disposed near the edges of the memory dies, for example, allows a relatively larger space for the S0C die 102 and consequently, a larger sized SOC die 102 can be used.

[0016] In an embodiment, the memory die 104a is a mirror image of the memory die 104b (e.g., the memory die 104a has components and bonding pad connections that are a mirror image those of the memory die 104b). In another embodiment, the memory die

104a is similar or identical to the memory die 104b (e.g., the memory die 104a has components and bonding pad connections that are similar or identical to those of the memory die 104b, and the memory die 104a is a rotation image of the memory die 104b in the figures). In yet another embodiment, the memory die 104a is different from the memory die 104b (e.g., the memory die 104a has components and bonding pad connections that are different from those of the memory die 104b). In an embodiment, the memory dies 104a and 104b form a dual channel memory. In an example, the memory dies 104a and 104b form a dual channel DRAM.

[0017] Fig. 2A illustrates a packaging arrangement 200a where a hole 214 is defined within a substrate 106. The packaging arrangement 200 includes an SOC die 102 and a memory die 104 that includes two attached memory dies 104a, 104b, as previously described. As can be seen, wire bonds 112 are utilized to provide various connections between the SOC die 102, the memory die 104 and/or the substrate 106. A heat sink 216 is provided and attached to the memory die 104. The heat sink 216 is attached to the memory die 104 via an appropriate epoxy or glue. Solder balls 108 are provided on the substrate 106 so that the packaging arrangement 200 can be attached to another substrate such as, for example, a PCB, another substrate, etc. (not illustrated). The SOC die 102 is attached to the memory die 104 via an appropriate epoxy or glue. As can be seen, when the memory die 104 is attached to the substrate 106 (via an appropriate epoxy or glue), the SOC die 102 extends into the hole 214. The packaging arrangement 200a illustrated in Fig. 2A generally provides good cost benefits, good heat dissipation for the SOC die 102 and very good heat dissipation for the memory die 104 due to the location of the heat sink 216 adjacent to the memory die 104. Additionally, the packaging arrangement 200a provides for improved VDD/ground access.

[0018] Fig. 2B illustrates a packaging arrangement 200b that is similar to the packaging arrangement 200a illustrated in Fig. 2A. In the packaging arrangement 200b, solder balls 218 are provided on the SOC die 102 to provide access to VDD and ground. The packaging arrangement 200b also provides good benefits with respect to cost and heat dissipation for the SOC die 102 and the memory die 104. Additionally, connectivity to VDD and ground is improved by the presence of the solder balls 218 on the SOC die 102 to thereby provide access to VDD and ground when the packaging arrangement 200b is flip chipped onto a substrate such as, for example, a PCB, another substrate, etc. (not illustrated)

[0019] Fig. 3 illustrates a packaging arrangement 300 that is similar to the packaging arrangement 100 illustrated in Fig. 1B. In the packaging arrangement 300, a redistribution layer (RDL) 320 is disposed on the memory die 104. An SOC die 102 is placed on the RDL 320 and is attached to the RDL 320 via an appropriate epoxy or glue. Wire bonds 112 between the SOC die 102 and the RDL 320, as well as wire bonds 112 between the RDL 320 and the substrate 106, allow for routing of various signals such as, for example, data, commands/addresses, and access to VDD and ground. Solder balls 108 are included on the substrate 106 for attaching the packaging arrangement 300 to another substrate such as, for example, a PCB, another substrate, etc. (not illustrated). The packaging arrangement 300 of Fig. 3 has increased costs due to the inclusion of the RDL 320 and provides adequate heat dissipation for the SOC die 102 and the memory die 104, as well as adequate access to VDD and ground via the RDL 320.

[0020] Fig. 4 illustrates a packaging arrangement 400 similar to the packaging arrangement 300 illustrated in Fig. 3. The SOC die 102 however is attached to the RDL 320 via solder balls 418, which thereby provide direct signal access between the SOC die 102 and the RDL 320. As can be seen, the SOC die 102 in the embodiments of both Figs. 3 and 4 can

be larger and can be almost square in comparison to the SOC die 102 that is illustrated in Fig. 1. This is allowable due to the presence of the RDL 320 as opposed to utilizing the bond pads on the memory die 104. A heat sink 416 is also provided in the packaging arrangement 400 and is attached to the SOC die 102 via an appropriate epoxy or glue. Solder balls 108 are provided on the substrate 106 for attaching the packaging arrangement 400 to another substrate such as, for example, a PCB, another substrate, etc. (not illustrated). The packaging arrangement 400 has increased costs and provides improved heat dissipation for the SOC die 102 as well as for the memory die 104 due to the presence of the heat sink 416. Improved access to VDD and ground is provided via the RDL 320.

[0021] Fig. 5 illustrates a packaging arrangement 500 that is configured as a package on package (POP) arrangement. A memory die 104 that includes two attached memory dies 104a, 104b as previously described is attached to a first substrate 106a. The memory die 104 is attached to the substrate 106a via an appropriate epoxy or glue. Holes 514a, 514b are defined within the substrate 106a to allow for wire bonds 112 from the memory die 104 to the substrate 106a. A second substrate 106b is provided that includes the SOC die 102 disposed on the substrate 106b. The SOC die 102 is flip chip attached to the second substrate 106b and thus, the SOC die 102 is attached to the second substrate 106b via solder balls 518 to thereby provide direct signal connectivity between the SOC die 102 and the substrate 106b. The first substrate 106a with the memory die 104 attached thereto is attached to the second substrate 106b via solder balls 108a. Solder balls 108b are provided on the second substrate 106b to attach the POP packaging arrangement 500 to another substrate such as, for example, a PCB, another substrate, etc. (not illustrated). The packaging arrangement 500 generally has average costs associated therewith and provides a fair amount of heat dissipation for the SOC die 102 and the memory die 104. The access to

VDD and ground for the SOC die 102 is very good due to the solder ball connection between the SOC die 102 and the second substrate 106b.

[0022] Fig. 6 illustrates a packaging arrangement 600 wherein a memory die 104 is attached to a heat sink 616. The memory die 104 is attached to the heat sink 616 via an appropriate epoxy or glue. The memory die 104 includes an RDL 320 disposed thereon. An SOC die 102 is flip chip attached via solder balls 618 to the RDL 320 on the memory die 104. Thus, the SOC die 102 has direct signal access to the RDL 320 via the solder balls 618 attaching the SOC die 102 to the RDL 320. The SOC die 102 is also attached to a substrate 106 via an appropriate epoxy or glue. Solder balls 622 are provided between the substrate 106 and the RDL 320 such that when the substrate 106 and SOC die 102 are flip chip attached to the RDL 320 on the memory die 104, direct signal access can be provided between the substrate 106 and the RDL 320. Solder balls 108 are provided on the substrate 106 to attach the packaging arrangement 600 to another substrate such as, for example, a PCB, another substrate, etc. (not illustrated). The packaging arrangement 600 provides improved cost and very good heat dissipation, due to the heat sink 616, for the SOC die 102 and the memory die 104. Additionally, access to the VDD and ground is also very good due to the RDL 320.

[0023] Fig. 7 illustrates a packaging arrangement 700 in which an SOC die 102 is attached to a heat sink 716. The SOC die 102 can be attached to the heat sink 716 via an appropriate epoxy or glue. A memory die 104 is attached to a substrate 106. The memory die 104 can be attached to the substrate 106 via an appropriate epoxy or glue. Holes 714a, 714b are defined within the substrate 106 so that wire bonds 112 can be utilized to couple the memory die 104 to the substrate 106 by routing the wire bonds 112 through the holes 714a, 714b within the substrate 106. The SOC die 102 can be flip chip attached to the

substrate 106 and thus, solder balls 718 provide direct signal access between the substrate 106 and the SOC die 102. Solder balls 108 are provided on the substrate 106 so that the packaging arrangement 700 can be attached to another substrate such as, for example, a PCB, another substrate, etc. (not illustrated). The packaging arrangement 700 provides adequate cost and very good heat dissipation for the SOC die 102 as well as the memory die 104 due to the heat sink 716. Access to VDD and ground is generally adequate.

[0024] Fig. 8 illustrates a packaging arrangement 800 that is similar to the packaging arrangement 700 of Fig. 7. In the packaging arrangement 800 of Fig. 8, the SOC die 102 is wider than the SOC die 102 in the packaging arrangement 700 of Fig. 7. Thus, when the SOC die 102 with the heat sink 716 attached thereto is flip chip attached to the substrate 106, the SOC die 102 can be attached to the substrate 106 beyond the holes 714a, 714b defined within the substrate 106. The packaging arrangement 800 provides adequate cost for the packaging arrangement 800 and very good heat dissipation for the SOC die 102 as well as the memory die 104 due to the heat sink 716. Access to VDD and ground is generally adequate.

[0025] While the various packaging arrangements have been described and illustrated utilizing a memory die 104 that includes two memory dies 104a, 104b that are still attached to each other, it is to be noted that memory dies can be utilized that include only a single memory die. In such embodiments, the memory die will generally be narrower than the memory die 104 described and illustrated in Figs. 1-8. Also, memory dies can be used that include more than two memory dies 104a, 104b that are still attached to each other. In such embodiments, the memory die will generally be wider and/or longer than the memory die 104 described and illustrated in Figs. 1-8. The multi-memory dies 104 can include

arrangements of individual memory dies 104a, 104b of one by two, two by two, two by three, etc. These examples are not meant to be limiting.

[0026] Fig. 9 illustrates an example of a method 900 for creating a packaging arrangement, such as, for example, the packaging arrangements of Figs. 1-8. At 902, a substrate is provided. At 904, a multi-memory die is coupled to the substrate. Each of the multiple individual memory dies is defined as an individual memory die within a wafer of semiconductor material during production of memory dies. The multi-memory die is created by singulating the wafer of semiconductor material into memory dies, where at least one of the memory dies is the multi-memory die that includes the multiple individual memory dies that are still physically connected together. At 906, a semiconductor die is coupled to the multi-memory die and the substrate. The semiconductor die is configured as a system on a chip. At 908, at least one of the multi-memory die and the semiconductor die is attached to the substrate.

[0027] Various operations may have been described as multiple discrete actions or operations in turn, in a manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations may not be performed in the order of presentation. Operations described may be performed in a different order than the described embodiment. Various additional operations may be performed and/or described operations may be omitted in additional embodiments.

[0028] The description may use the terms “embodiment” or “embodiments,” which may each refer to one or more of the same or different embodiments. Furthermore, the terms “comprising,” “including,” “having,” and the like, as used with respect to embodiments, are synonymous.

[0029] Although certain embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that a wide variety of alternate and/or equivalent embodiments or implementations calculated to achieve the same purposes may be substituted for the embodiments illustrated and described without departing from the scope. Those with skill in the art will readily appreciate that embodiments may be implemented in a very wide variety of ways. This application is intended to cover any adaptations or variations of the embodiments discussed herein. Therefore, it is manifestly intended that embodiments be limited only by the claims and the equivalents thereof.

Claims

What is claimed is:

1. A packaging arrangement comprising:

a substrate;

a multi-memory die coupled to the substrate, wherein the multi-memory die comprises multiple individual memory dies and

each of the multiple individual memory dies is defined as an individual memory die within a wafer of semiconductor material during production of memory dies, and

the multi-memory die is created by singulating the wafer of semiconductor material into memory dies, where at least one of the memory dies is the multi-memory die that includes the multiple individual memory dies that are still physically connected together; and

a semiconductor die coupled to the multi-memory die and the substrate, wherein the semiconductor die is configured as a system on a chip,

wherein at least one of the multi-memory die and the semiconductor die is attached to the substrate.

2. The packaging arrangement of claim 1, wherein both the multi-memory die and the semiconductor die are attached to the substrate.

3. The packaging arrangement of claim 2, wherein the semiconductor die is attached to the substrate via a flip chip process.

4. The packaging arrangement of claim 1, wherein the semiconductor die is coupled to the substrate via a wire bonding process.

5. The packaging arrangement of claim 1, further comprising a redistribution layer attached to the multi-memory die.

6. The packaging arrangement of claim 5, wherein the semiconductor die is coupled to the redistribution layer, and thereby the multi-memory die, via a flip chip process.

7. The packaging arrangement of claim 5, wherein the semiconductor die is coupled to the redistribution layer, and thereby the multi-memory die, via a wire bonding process.

8. The packaging arrangement of claim 1, further comprising a heat sink attached to one of the semiconductor die or the multi-memory die.

9. The packaging arrangement of claim 1, wherein the multi-memory die is attached to the substrate via an epoxy or glue.

10. The packaging arrangement of claim 1, wherein the semiconductor die is attached to the substrate via an epoxy or glue.

11. The packaging arrangement of claim 1, wherein the semiconductor die is attached to the multi-memory die via an epoxy or glue.

12. The packaging arrangement of claim 1, wherein the substrate has a hole defined therein and the multi-memory die is coupled to the substrate via a wire bonding process through the hole.

13. The packaging arrangement of claim 12, wherein the multi-memory die is coupled to the semiconductor die via a wire bonding process through the hole.

14. The packaging arrangement of claim 12, wherein:

the substrate is a first substrate;

the packaging arrangement further comprises a second substrate;

the second substrate is coupled to the first substrate via solder balls; and

the semiconductor die is coupled to the second substrate, and thereby the first substrate and the multi-memory die, via a flip-chip process.

15. A method comprising:

providing a substrate;

coupling a multi-memory die to the substrate, wherein

the multi-memory die comprises multiple individual memory dies,

each of the multiple individual memory dies is defined as an individual memory die within a wafer of semiconductor material during production of memory dies, and

the multi-memory die is created by singulating the wafer of semiconductor material into memory dies, where at least one of the memory dies is the multi-memory die that includes the multiple individual memory dies that are still physically connected together;

coupling a semiconductor die to the multi-memory die and the substrate, wherein the semiconductor die is configured as a system on a chip; and

attaching at least one of the multi-memory die and the semiconductor die to the substrate.

16. The method of claim 15, wherein the multi-memory die is coupled to the substrate via one of a flip chip process or a wire bonding process.

17. The method of claim 15, wherein the semiconductor die is coupled to the multi-memory die via one of a flip chip process or a wire bonding process.

18. The method of claim 15, wherein the multi-memory die is coupled to the substrate via one of a flip chip process or a wire bonding process.

19. The method of claim 15, wherein the multi-memory die is attached to the substrate via an epoxy or glue.

20. The method of claim 15, wherein the semiconductor die is attached to the substrate via an epoxy or glue.

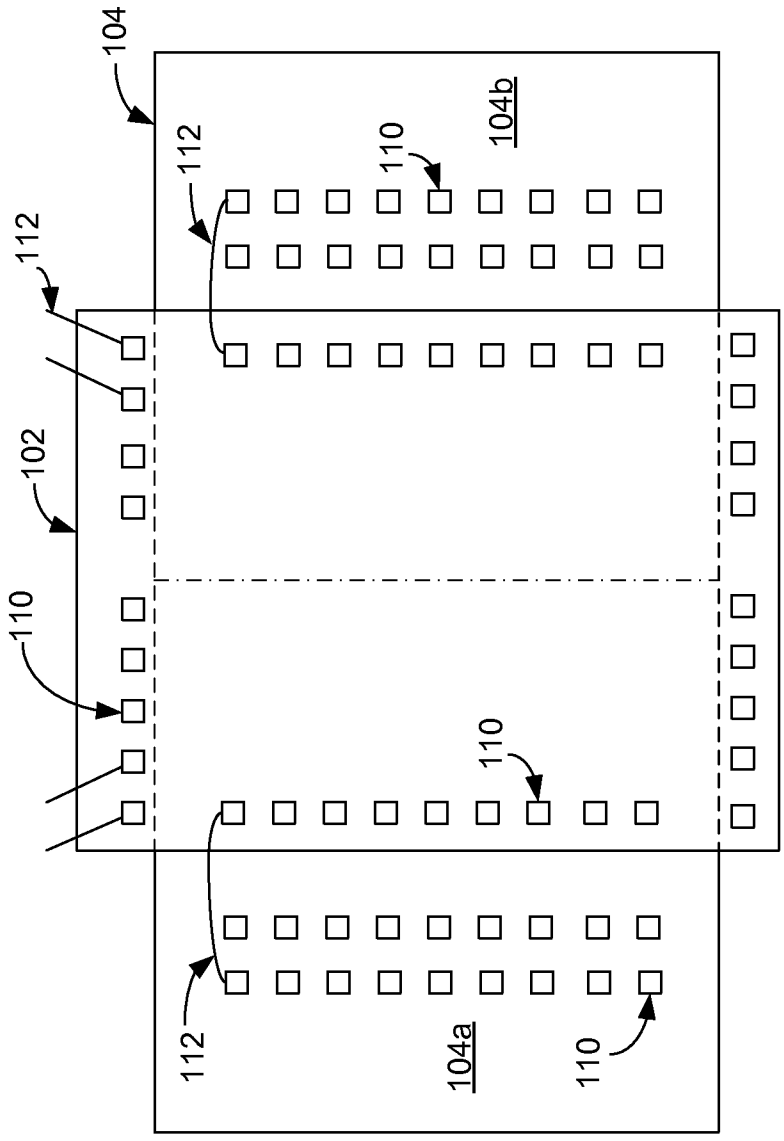
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Fig. 1A

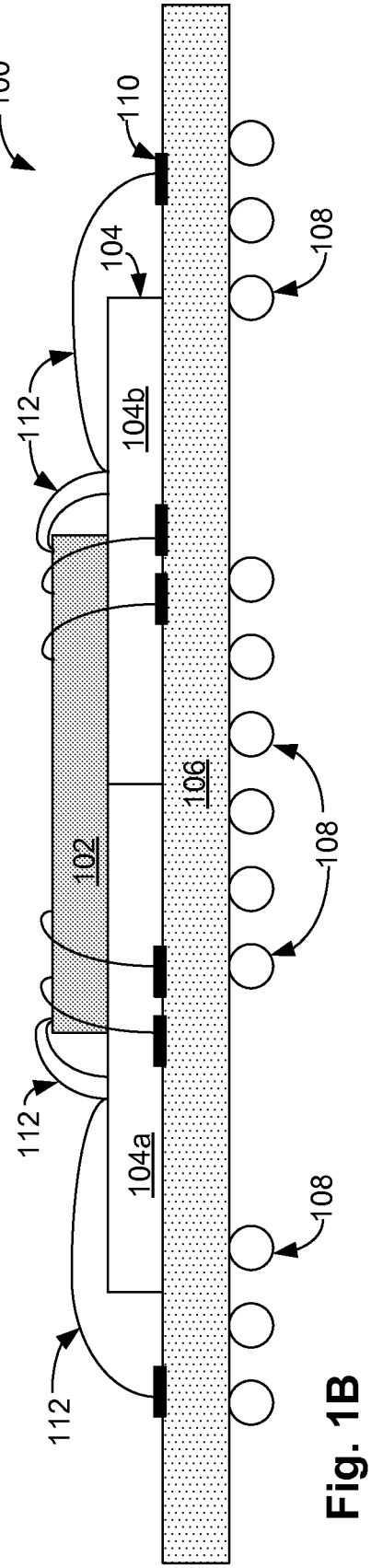
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Fig. 1B

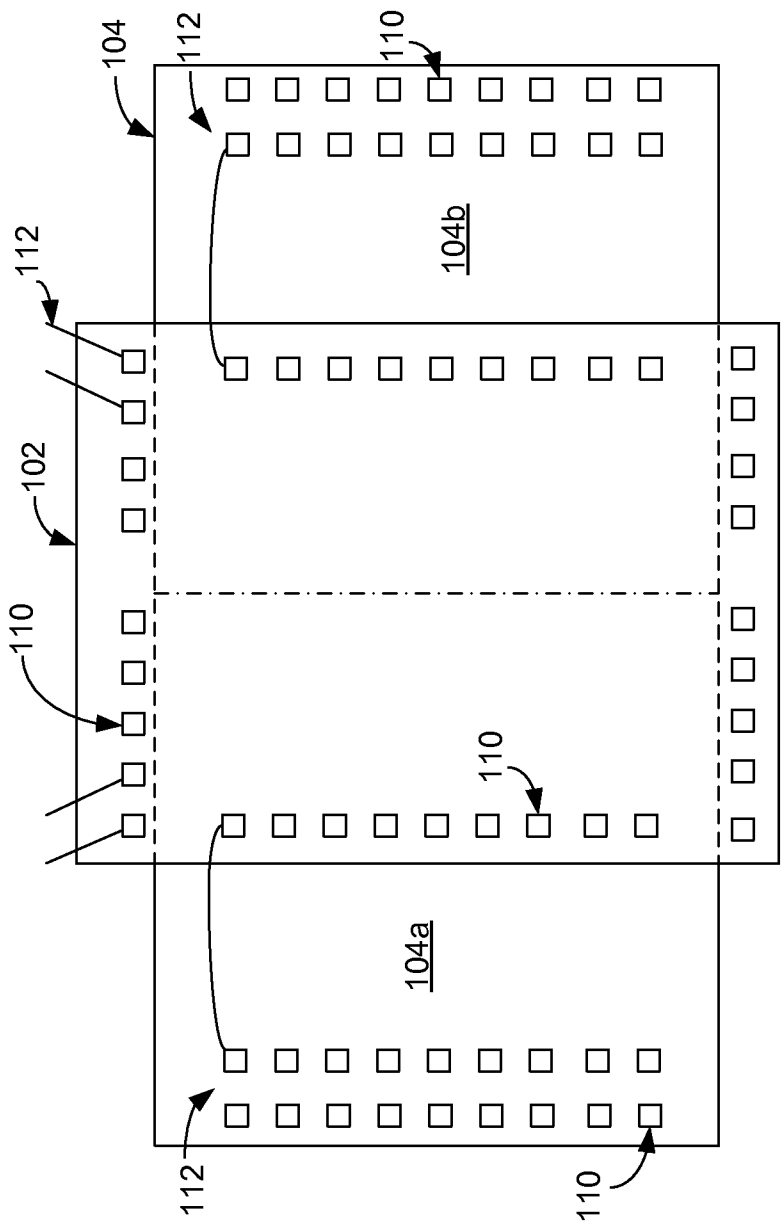
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Fig. 1C

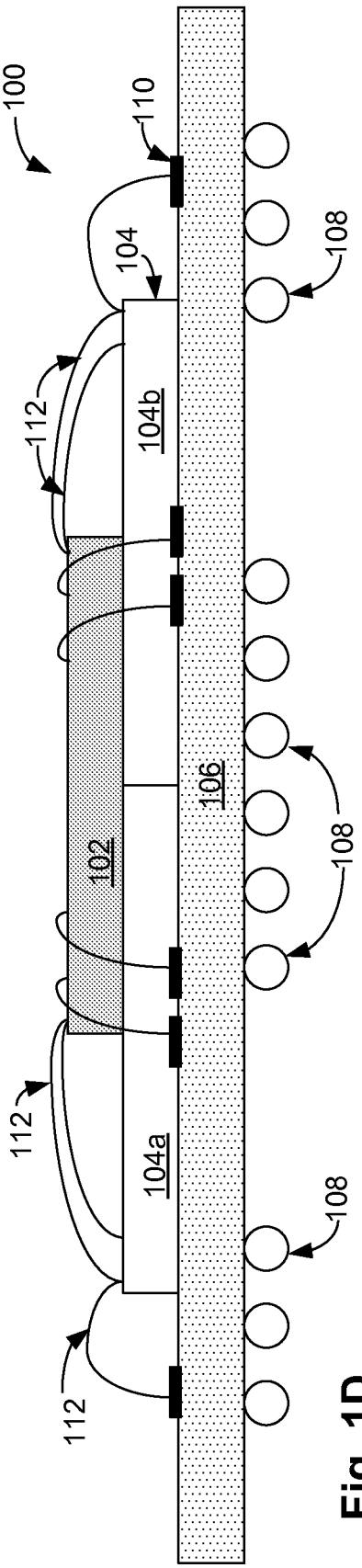
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Fig. 1D

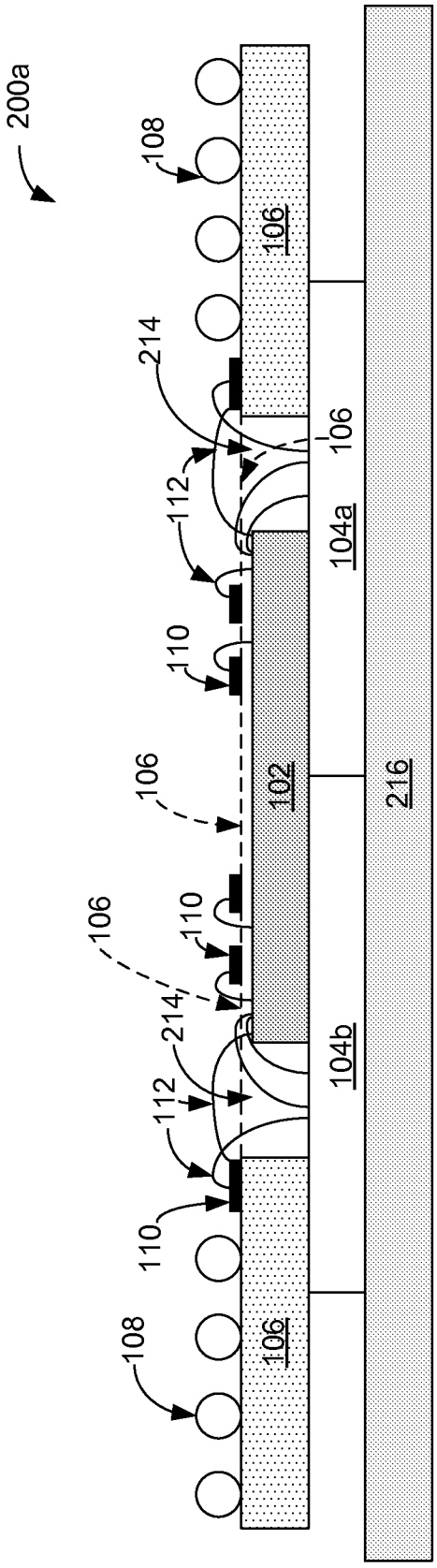
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Fig. 2A

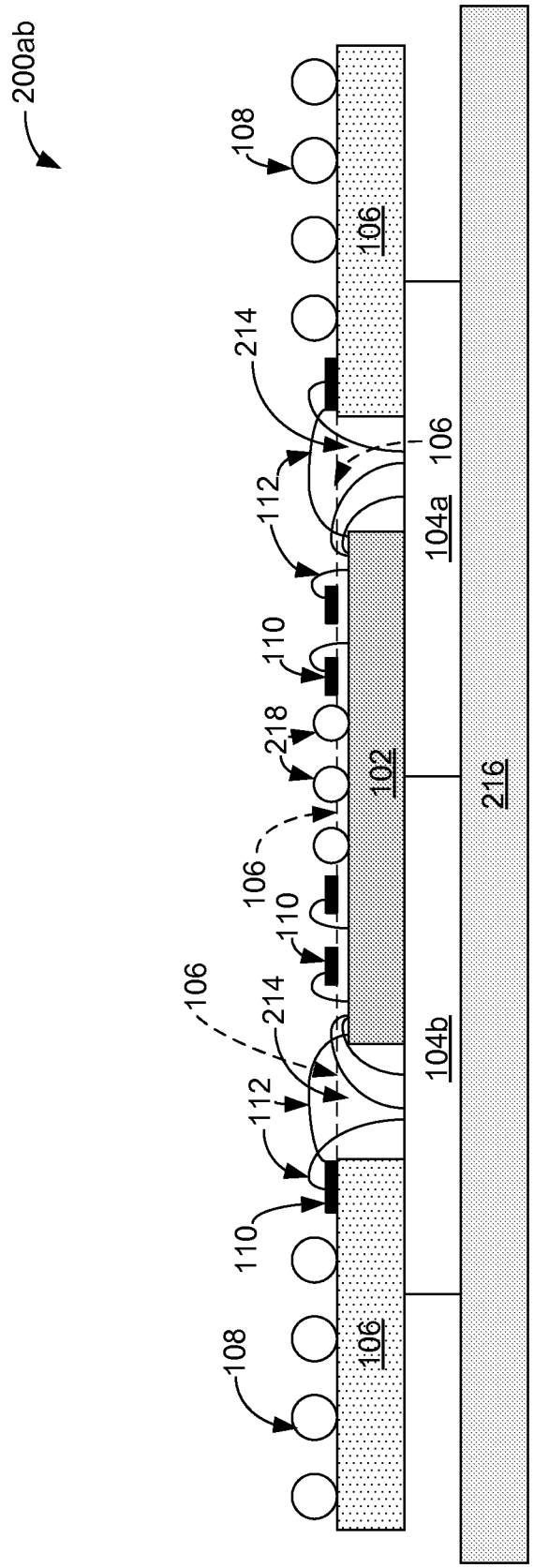
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Fig. 2B

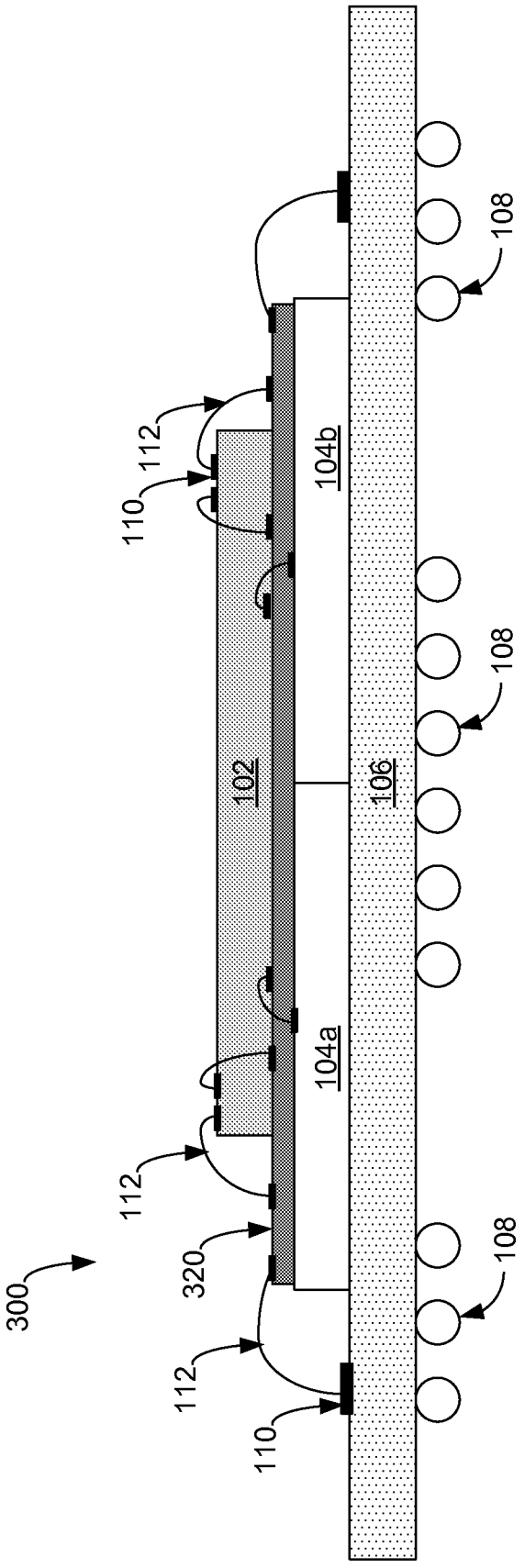

Fig. 3

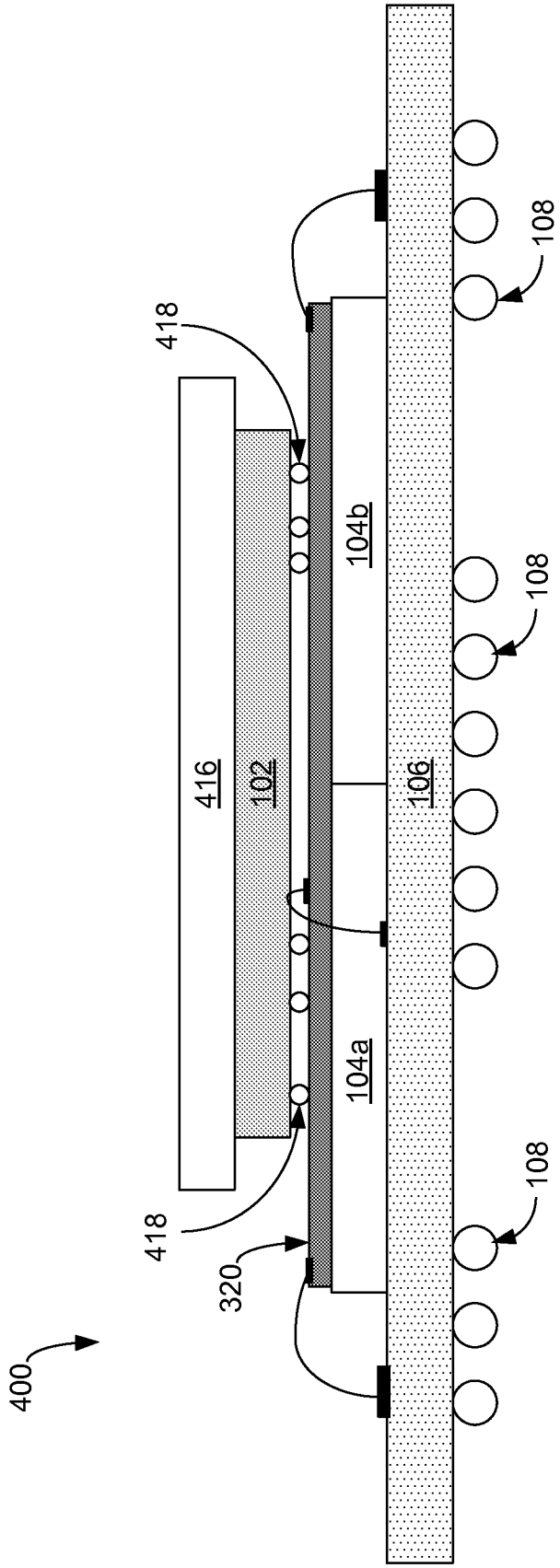

Fig. 4

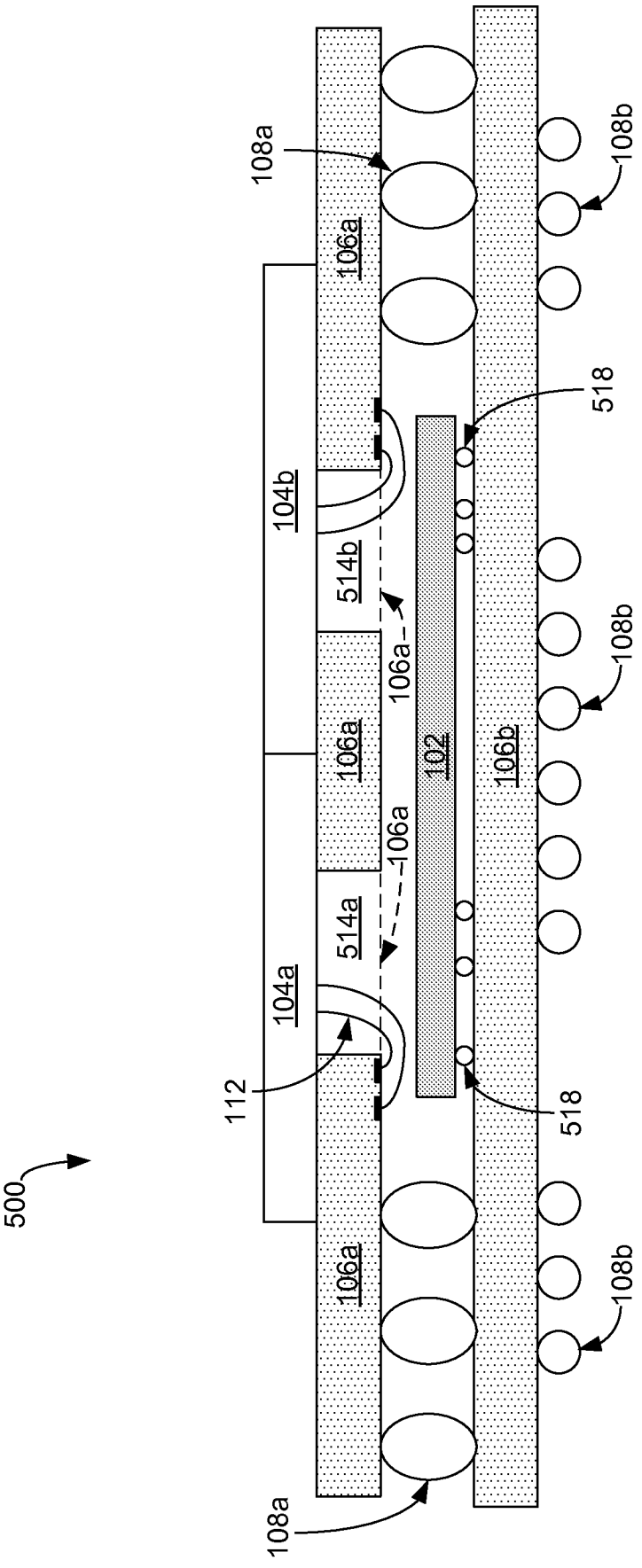
500
108a
106a
104b
514b
106a
106a
102
106b
106a
514a
104a
112
108a
106a
108b
518
108b
518
108b

Fig. 5

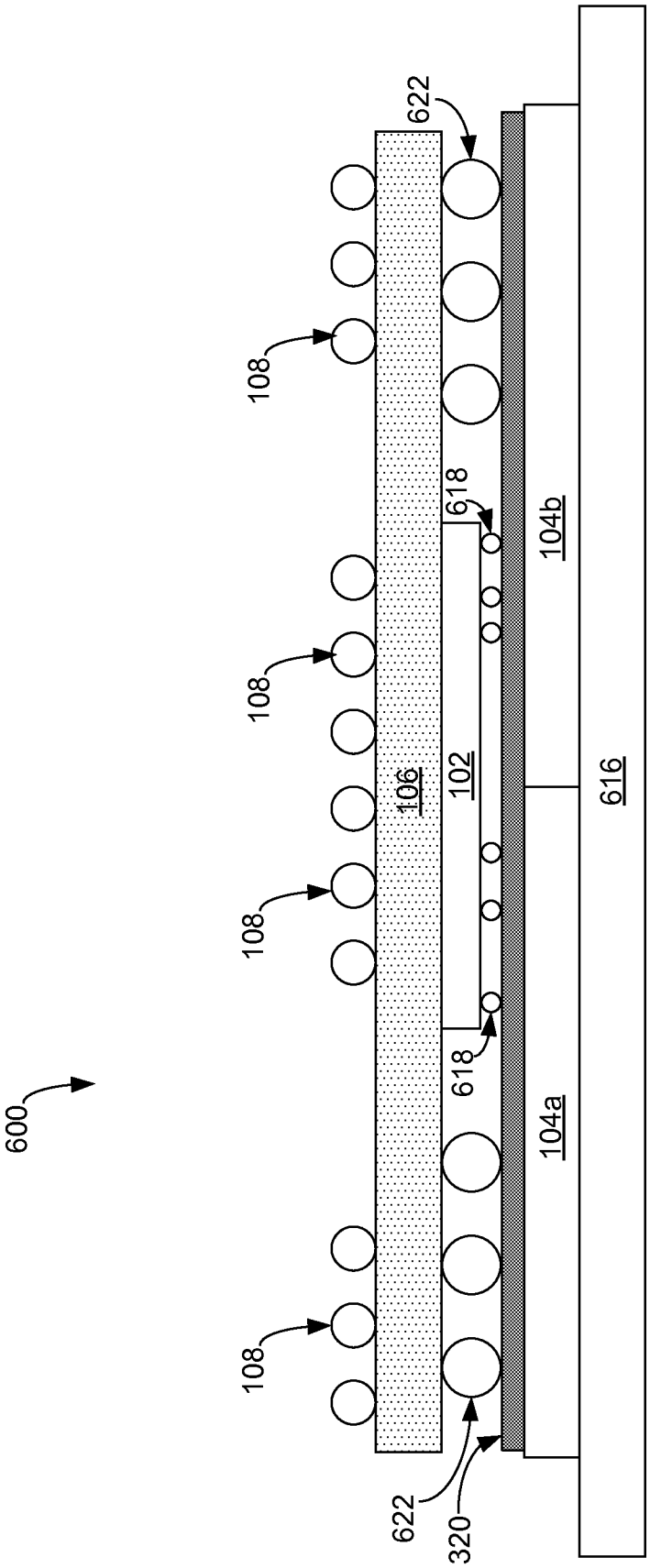

Fig. 6

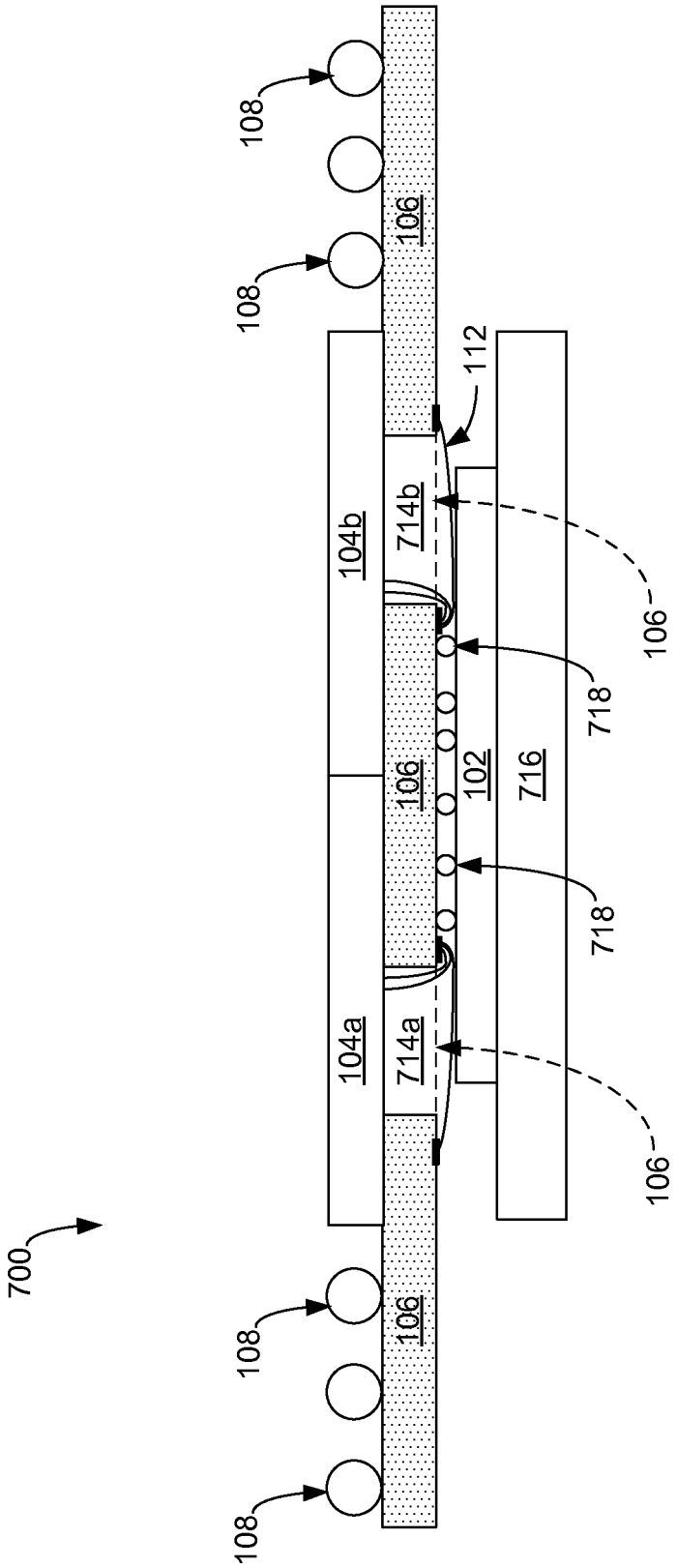
700
108
108
108
106
106
106
106
112
104b
714b
104a
714a
102
716
718
718

Fig. 7

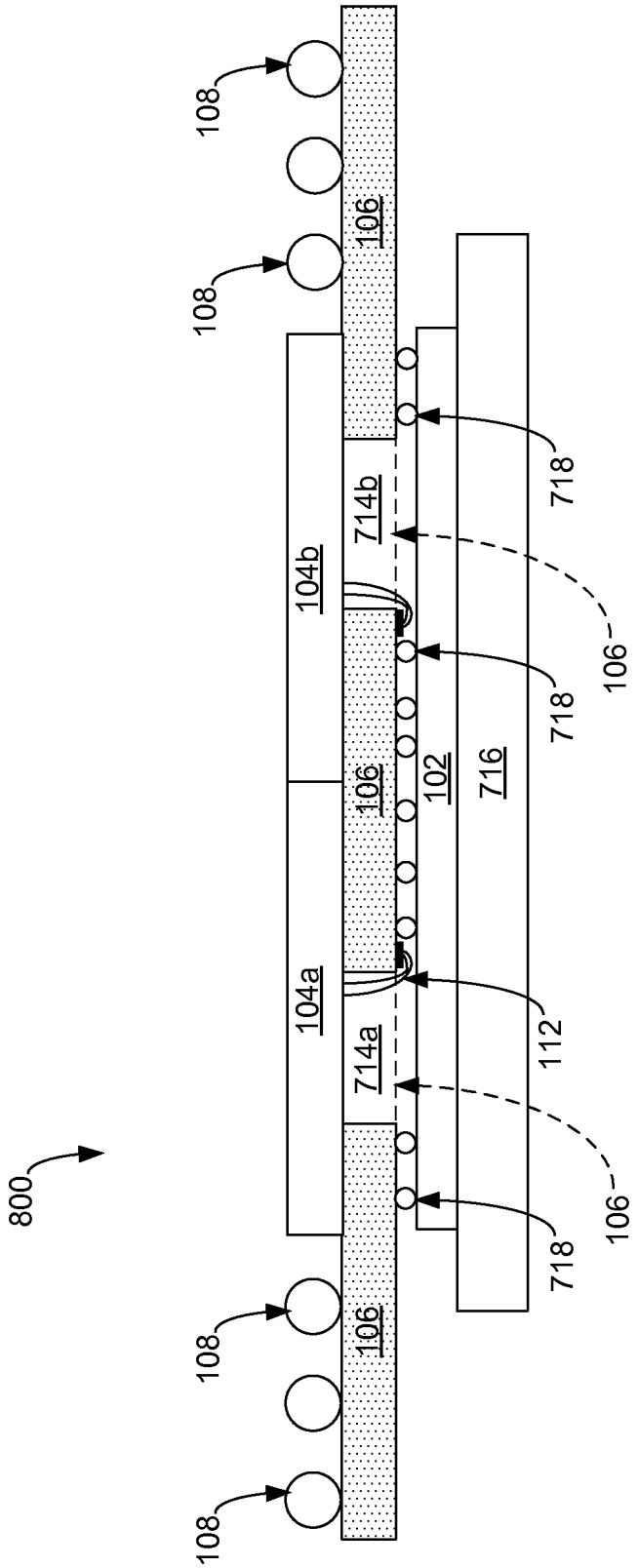
800
108
108
108
106
106
106
104a
104b
714a
714b
102
716
112
718
718
718
106
106

Fig. 8

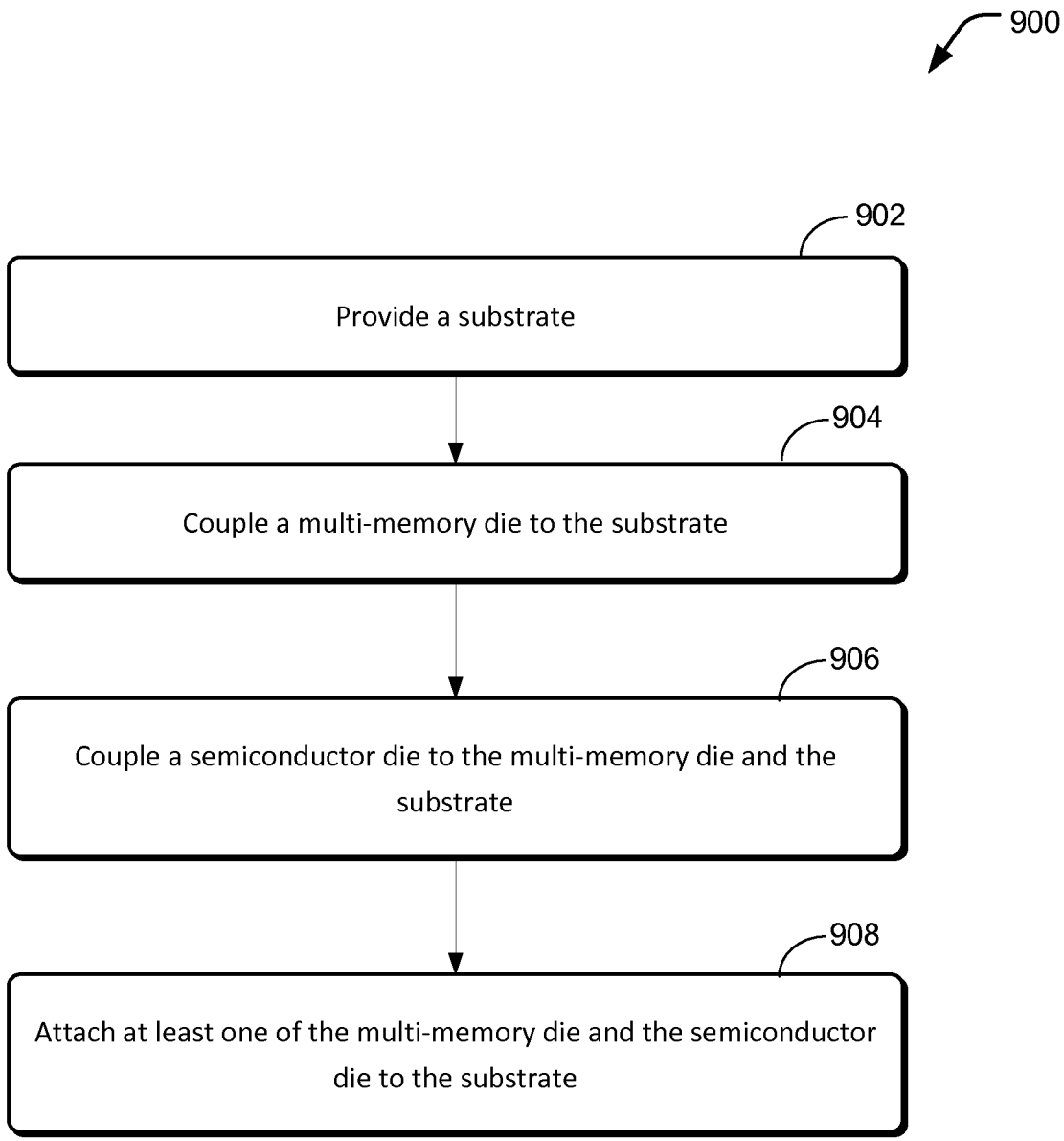
900
902
Provide a substrate
904
Couple a multi-memory die to the substrate
906
Couple a semiconductor die to the multi-memory die and the substrate
908
Attach at least one of the multi-memory die and the semiconductor die to the substrate

Fig. 9

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/051694

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L23/00 H01L25/065 H01L25/10
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2003/015792 A1 (URAKAWA YUKIHIRO [JP]) 23 January 2003 (2003-01-23) paragraphs [0006], [0038], [0120], [0141]; claims 24,33; figures 19,20a -----	1-3,15, 16,18

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
6 September 2013	11/12/2013

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Manook, Rhoda

1

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/051694

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-3, 15, 16, 18

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-3, 15, 16, 18

As all the technical features of independent product claim 1 and corresponding independent method claim 15 are not new, in view of document US2003/0015792 (D1), on which claims 2,4,5,8,9,10,11,12,16-20 directly depend, claims 1 and 15 cannot serve as a single general inventive concept for these dependent claims.
D1 discloses:
A packaging arrangement comprising (fig. 19, claim 24):
a substrate (claim 24; package substrate);
a multi-memory die (claim 24 memory chip; par. 120) coupled to the substrate, wherein the multi-memory die comprises multiple individual memory dies and each of the multiple individual memory dies is defined as an individual memory die within a wafer of semiconductor material during production of memory dies, and the multi-memory die is created by singulating (claim 24 dicing line) the wafer of semiconductor material into memory dies, where at least one of the memory dies is the multi-memory die that includes the multiple individual memory dies that are still physically connected together (claim 24 memory chip); and a semiconductor die (logic chip; claim 24) coupled to the multi-memory die and the substrate, wherein the semiconductor die is configured as a system on a chip (LSI chip is SOC named 'logic chip' (par. 48 and par. 6)), and at least one of the multi-memory die and the semiconductor die is attached to the substrate (fig. 19).
The corresponding method claim 15 is also not new for the same above-mentioned reasoning as claim 1 in view of document D1.
1.1 Hence, the following separate inventions or groups of inventions are not so linked as to form a single general inventive concept.
Group I: directed to the subject matter of claims 1-3 and 15-16 and 18 (c.f claim 2)
(re. claim 2):
D1 also discloses that the multi-memory die (memory chip claim 24) and the semiconductor die (logic chip- claim 24) are attached to the substrate (fig. 19). These features is already known from document D1 and its subject matter therefore cannot form special technical features.
(re. claim 3): D1 also discloses that the semiconductor die (logic chip) is attached to the substrate via a flip chip process (claim 33 and fig. 20a).

1.1. claims: 16, 18

Although the technical features of the dependent claims 16 and 18 are not the same, they could be searched without any effort and are thus included in the first searched group of claims.

claims 16 and 18 directed to the multi-memory die being coupled to the substrate via one of a flip chip process or a wire bonding process.

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2. claims: 5-7

Group II:directed to the subject matter of claims 5-7 (c.f claim 5)
Re. cl. 5 the surplus technical feature with respect to the not novel subject matter of claim 1 is that a redistribution layer is attached to the multi-memory die.
Thus the objective problem of claim 5 to be solved can be construed as: not being limited to connections to the memory die solely by the bond pads of the memory die (see par. 20 of the application).

---

3. claim: 8

Group III:directed to the subject matter of claim 8
Re. cl. 8 the surplus technical feature with respect to the not novel subject matter of claim 1 is that further comprising a heat sink attached to one of the semiconductor die or the multi-memory die.
Thus the objective problem of claim 8 to be solved can be construed as: enabling the package to be optimised for heat dissipation.

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4. claims: 9, 10, 19, 20

Group IV: directed to the subject matter of claims 9,10,19,20
Re. cl. 9 the surplus technical feature with respect to the not novel subject matter of claim 1 is that the multi-memory die is attached to the substrate via an epoxy or glue.
Re. cl. 10 the surplus technical feature with respect to the not novel subject matter of claim 1 is that the semiconductor die is attached to the substrate via an epoxy or glue.
Re. cl. 19 the surplus technical feature with respect to the not novel subject matter of claim 15 is that the multi-memory die is attached to the substrate via an epoxy or glue.
Re. cl. 20 the surplus technical feature with respect to the not novel subject matter of claim 15 is that the semiconductor die is attached to the substrate via an epoxy or glue.
Thus the objective problem of claims 9-10 and 19-20 to be solved can be construed as: method of attaching the chips (semiconductor die or multi-memory die) such that the chips are stably/mechanically fixed to the substrate.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

5. claims: 11, 17

Group V:directed to the subject matter of claims 11 and 17
Re. cl. 11 the surplus technical feature with respect to the not novel subject matter of claim 1 is that the semiconductor die is attached to the multi-memory die via an epoxy or glue.
Re. cl. 17 the surplus technical feature with respect to the not novel subject matter of claim 15 is that the semiconductor die is coupled to the multi- memory die via one of a flip chip process or a wire bonding process.
Thus the objective problem of claim 11 and 17 to be solved can be construed as: enabling the footprint of the assembly to be minimised, whilst increasing the density of the package.

---

6. claims: 12-14

Group VI: directed to the subject matter of claim s 12-14 (c.f. claim 12)
Re. cl. 12 the surplus technical feature with respect to the not novel subject matter of claim 1 is that the substrate has a hole defined therein and the multi-memory die is coupled to the substrate via a wire bonding process through the hole.
Thus the objective problem of claim 12 to be solved can be construed as: Minimising the height of the packaged assembly.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2013/051694

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2003015792 A1	23-01-2003	CN 1463036 A	24-12-2003
		JP 2003023138 A	24-01-2003
		KR 20030007076 A	23-01-2003
		TW 571392 B	11-01-2004
		US 2003015792 A1	23-01-2003
		US 2004164425 A1	26-08-2004
		US 2006148130 A1	06-07-2006