

(43) International Publication Date
12 January 2017 (12.01.2017)

(51) International Patent Classification:

H03H 7/01 (2006.01) H02H 9/00 (2006.01)
H02M 1/12 (2006.01)

(21) International Application Number:

PCT/EP2016/063630

(22) International Filing Date:

14 June 2016 (14.06.2016)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

15175302.7 3 July 2015 (03.07.2015) EP

(71) Applicant: EPCOS AG [DE/DE]; St.-Martin-Strasse 53,
81669 München (DE).(72) Inventor: TUCKER, Andrew; Untere Sternengasse 12,
4500 Solothurn (CH).(74) Agent: EPPING HERMANN FISCHER PATENTAN-
WALTSGESELLSCHAFT MBH; Schlossschmidstr. 5,
80639 München (DE).(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY,
BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM,
DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,
HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR,
KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG,
MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM,
PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC,
SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN,
TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.(84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, GH,
GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ,
TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU,
TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE,
DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU,
LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,
SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ,
GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

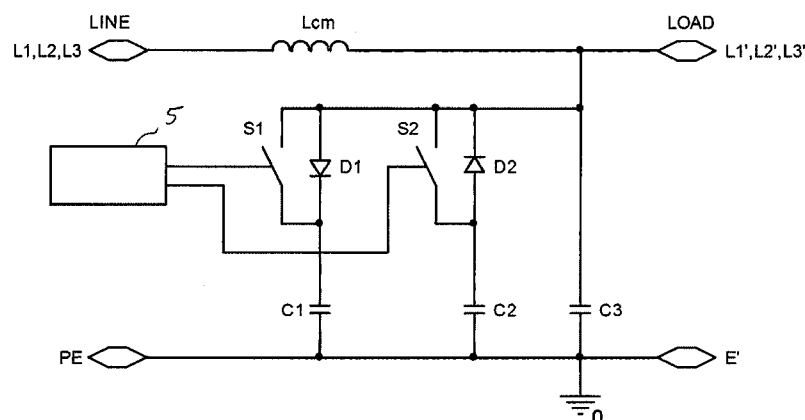
(54) Title: ELECTRONIC DEVICES AND METHODS FOR FILTERING COMMON MODE DISTURBANCES FROM POWER
ELECTRONIC DEVICES

Figure 5

(57) Abstract: An electronic device comprises: a first capacitor (C1) being coupled in series to a first one-way conductor (D1), that allows current flow in one direction, and the first one-way conductor (D1) and the first capacitor (C1) being coupled between a load node (LOAD) and a reference potential (0), and a second capacitor (C2) being coupled in series to a second one-way conductor (D2), that allows current flow in the opposite direction, the second one-way conductor (D2) and the second capacitor (C2) being coupled between the load node (LOAD) and the reference potential (0), and a third capacitor (C3) being coupled between the load node (LOAD) and the reference potential (0), and a first switch (S1) bypassing the first one-way conductor (D1), and a second switch (S2) bypassing the second one-way conductor (D2).

Description

Electronic devices and methods for filtering common mode disturbances from power electronic devices

5

The invention concerns a method for filtering common mode disturbances from power electronic devices that may serve as a line filter or as part thereof.

10 In an electrical installation it is usual to interpose a low-pass power line filter at the input of an electrical appliance to help prevent high frequency signals from passing between a load appliance and supply, thus improving the electromagnetic compatibility (EMC) of the system. A typical low-pass passive
15 power line filter may comprise series inductive and shunt capacitive interconnected components.

Pulse width modulation (PWM) power electronic loads, such as variable speed motor drives, generate parasitic common mode
20 currents. This is due to the high voltage slew rate of their switches imposed on the stray earth capacitance in the system. This common mode current constitutes an Electromagnetic Interference (EMI) which manifests itself as common mode (CM) conducted emissions and earth leakage current, phenomena in
25 the field of Electromagnetic Compatibility (EMC).

The low pass power line filter provides a degree of common mode (CM) attenuation which effectively reduces the amplitude and bandwidth of common mode current allowed to flow on the
30 supply line. However the size and cost of the filter can be prohibitively high especially when the common mode currents are high or when significant attenuation of such current is required at or near to the drive switching frequency.

It is the aim of this invention to provide an alternative method for filtering CM disturbances from switched power electronic systems having the benefit of reduced size and cost compared to a conventional passive filter.

5

A low pass power line filter may consist of one or more series inductive elements which have relatively low impedance at power frequencies which allows the relatively free conduction of power current and which have relatively high impedance at radio frequencies which restricts the flow of interference currents. In addition a low pass power line filter may consist of one or more shunt capacitive elements which have relatively high impedance at power frequencies which serves to isolate the power line voltages and which have relatively low impedance at radio frequencies which allows the flow of interference currents.

15

In its simplest form, an equivalent circuit of the common mode parameters of a low pass power line filter may comprise a series common mode inductance inserted between a line load and a load node and a shunt common mode capacitance inserted between the load node and the reference potential.

20

This invention is realized in a variety of embodiments all of which essentially replace the shunt common mode capacitance connected between the load node and the reference potential. The circuits of these embodiments provide for the reduction of load node voltage so that it remains close to the reference potential for as much time as possible. By doing so, the time integral of load node voltage is reduced. The load node voltage is essentially imposed over the series common mode inductance and the current made to flow in this inductance is proportional to the time integral of the load node voltage.

25

30

Thus the circuit means described in this invention serve to reduce the current in the series common mode inductance.

The invention concerns electronic devices and corresponding methods that reduce the node load voltage by switches or by

5 means of an amplifier, which are alternative means for achieving the same goal.

In one embodiment, an electronic device comprises a first capacitive element being coupled in series to a first one-way
10 conductor that allows current flow in one direction. The first one-way conductor and the first capacitive element are coupled between a load node and a reference potential. The current flow may be allowed in the direction from the load node to the reference potential, which may be defined as one direction.

15

A second capacitive element is coupled in series to a further one-way conductor that allows current flow in the opposite direction. The further one-way conductor and the second capacitive element are coupled between the load node and the
20 reference potential. The current flow may be allowed in the direction from the reference potential to the load node, which may be defined as the opposite direction. The one-way conductor may be diodes.

25

A capacitive means is coupled between the load node and the reference potential. The capacitive means may comprise one or more capacitors. A first switch connects between a potential node, that is between the first one-way conductor and the first capacitive element, and the load node. A second switch

30

connects between a further potential node, that is between the further one-way conductor and the second capacitive element, and the load node. The switches may be switched by means of a switch control, for example, between a conducting state

allowing current flow and a non-conducting state with no current flow.

The one-way conductors, which may be diodes, are connected to the load node and the capacitive elements are connected to the reference node. Alternatively the complete circuit arrangement can be inverted in relation to load and reference nodes.

The method for filtering common mode disturbances by such an electronic device comprises:

- applying alternating positive and negative voltage transitions at the load node;
- charging the first capacitive element and the capacitive means positive by one positive voltage transition of the load node, transferring energy to the first capacitive element and the capacitive means,
- discharging the capacitive means and the second capacitive element, the latter having been charged negative by a previous negative voltage transition at the load node, when the second switch is switched to the conducting state, then switching it to the non-conducting state,
- charging the second capacitive element and the capacitive means negative by one negative voltage transition of the load node, transferring energy to the second capacitive element and the capacitive means,
- discharging the capacitive means and the first capacitive element, the latter having been charged positive by a previous positive voltage transition at the load node, when the first switch is switched to the conducting state, then switching it to the non-conducting state.

In one embodiment, the electronic device comprises a first capacitor being coupled in series to a first one-way conductor, the first one-way conductor and the first capacitor

being coupled between the load node and the reference potential, and a second capacitor being coupled in series to a second one-way conductor, the second one-way conductor and the second capacitor being coupled between the load node and the reference potential, and a third capacitor being coupled in series to a third one-way conductor, the third one-way conductor and the third capacitor being coupled between the load node and the reference potential, and a fourth capacitor being coupled in series to a fourth one-way conductor, the fourth one-way conductor and the fourth capacitor being coupled between the load node and the reference potential. The first and third one-way conductors allow current flow in one direction; the second and fourth one-way conductors allow current flow in the opposite direction. The first switch connects between a first potential node, that is between the first capacitor and the first one-way conductor, and a second potential node, that is between the second capacitor and the second one-way conductor. The second switch connects between a third potential node, that is between the third capacitor and the third one-way conductor, and a fourth potential node, that is between the fourth capacitor and the fourth one-way conductor.

Preferably, the one-way conductors, which may be diodes, are connected to the load node and the capacitive elements are connected to the reference node. Alternatively the load and reference node connections may be reversed. The switches may be switched by means of a switch control, for example, between a conducting state allowing current flow and a non-conducting state with no current flow.

A method for filtering common mode disturbances by an electronic device as mentioned above comprises:

- applying alternating positive and negative voltage transitions at the load node;
- charging the first capacitor and the third capacitor positive by one positive voltage transition of the load node,
5 where the first one-way conductor and the third one-way conductors are in the conduction state, transferring energy to the first capacitor and the third capacitor;
- discharging the first capacitor and the second capacitor, the latter having been charged negative by a previous negative
10 voltage transition at the load node, when the first switch is switched to the conducting state;
- switching the first switch to the non-conducting state;
- charging the second capacitor and the fourth capacitor negative by one negative voltage transition of the load node,
15 where the second one-way conductor and the fourth one-way conductors are in the conduction state, transferring energy to the second capacitor and the fourth capacitor;
- discharging the third capacitor and the fourth capacitor, the former having been charged positive by the previous
20 positive voltage transition at the load node, when the second switch is switched to the conducting state;
- switching the second switch to the non-conducting state.

In one embodiment, the electronic device comprises a first
25 capacitor being coupled in series to the first one-way conductor, the first capacitor and the first one-way conductor being coupled between the load node and the reference potential, and a second capacitor being coupled in series to the second one-way conductor, the second capacitor and the
30 second one-way conductor being coupled between the load node and the reference potential, and a third capacitor being coupled between the load node and the reference potential. A first switch is connected in parallel with the first one-way conductor and a second switch is connected in parallel with

the second one-way conductor. Preferably, the one-way conductors, which may be diodes, are connected to the load node and the capacitive elements are connected to the reference node. Alternatively the load and reference node connections may be reversed. The switches may be switched by means of a switch control, for example, between a conducting state allowing current flow and a non-conducting state with no current flow.

10 The method for filtering common mode disturbances by such an electronic device comprises:

- applying alternating positive and negative voltage transitions at the load node;

- charging the first capacitor and the third capacitor positive by one positive voltage transition of the load node, where the first one-way conductor is in the conduction state, transferring energy to the first capacitor and the third capacitor;

- discharging the second capacitor and the third capacitor, the former having been charged negative by a previous negative voltage transition at the load node, when the second switch is switched to the conducting state;

- switching the second switch to the non-conducting state;
- charging the second capacitor and the third capacitor

- negative by one negative voltage transition of the load node, where the second one-way conductor is in the conduction state, transferring energy to the second capacitor and the third capacitor;

- discharging the first capacitor and third capacitor, the former having been charged positive by a previous positive voltage transition at the load node, when the first switch is switched to the conducting state;

- switching the first switch to the non-conducting state.

The first switch connected in parallel with the first one-way conductor or the second switch connected in parallel with the second one-way conductor may be embodied as a MOSFET with body diode or an insulated-gate bipolar transistor with a

5 freewheeling diode or a bipolar junction transistor with a freewheeling diode or a silicon-controlled rectifier (SCR) with a reverse connected diode in parallel.

In one embodiment, a method concerns a device wherein a first
10 capacitor is connected in series with a first one-way conductor, a second capacitor is connected in series with a second one-way conductor, a third capacitor is connected in series with a third one-way conductor, and a fourth capacitor is connected in series with a forth one-way conductor. These
15 series connections are all connected in parallel between the load node and the reference potential. The one-way conductors are polarized such that the first and third capacitors charge positive and the second and fourth capacitors charge negative in relation to the reference potential, as a result of
20 positive and negative voltage excursions of the load node respectively. A first switch bridges between the first and second capacitors and a second switch bridges between the third and fourth capacitors.

25 The method further comprises:

- charging the first and third capacitors positively by a positive voltage transition at the load node, while the first switch is in the non-conducting state;
- discharging the first and second capacitors, the latter
30 having been charged negatively by a previous negative voltage transition of the load node, when the first switch is switched to the conducting state;
- switching the first switch to the non-conducting state;

- charging the second and fourth capacitors negatively by a negative voltage transition at the load node, while the second switch is in the non-conducting state;

- discharging the third and fourth capacitors, the former

5 having been charged positively by a previous positive voltage transition of the load node, when the second switch is switched to the conducting state;

- switching the second switch to the non-conducting state;

10 In the above-mentioned method, the second and third capacitors serve as charge reservoirs that allow discharging the first and fourth capacitors.

An alternating impulsive current generated by a load (i.e. a variable speed motor drive) is rectified into the array of

15 four equal valued capacitors. Two capacitors can be charged positively and two negatively. Immediately after each

impulsive event, the energy in one capacitor is discharged, via a suitable switch, with the energy in another capacitor of opposite polarity. The energy in one capacitor is always

20 stored and held until the subsequent impulse event so that energy of opposite polarity is available for the next

discharge. In this way the energy and associated voltage at the load node is reduced near to the reference potential during most of the time and consequently the common mode

25 current generated in the filter common mode inductor, which is proportional to the time integral of load node voltage, is reduced considerably.

In another embodiment, a first capacitor connects in series to
30 the drain of a first MOSFET and a second capacitor connects in series to the source of a second MOSFET. These series legs are further connected in parallel between the load node and the reference potential, where the source of the first MOSFET and the drain of the second MOSFET connect to the load node and

the first and second capacitors connect to the reference potential. A third capacitor connects between the load node and the reference potential. The MOSFETs may be both n-channel type with integrated body diodes.

5

The method further comprises:

- charging the first and third capacitors positively by a positive voltage transition at the load node, while the first and second MOSFETs are in the non-conducting state and the body diode of the first MOSFET is forward biased;
 - discharging the second and third capacitors, the former having been charged negatively by a previous negative voltage transition of the load node, when the second MOSFET is switched to the conducting state;
 - switching the second MOSFET to the non-conducting state;
 - charging the second and third capacitors negatively by a negative voltage transition at the load node, while the first and second MOSFETs are in the non-conducting state and the body diode of the second MOSFET is forward biased;
 - discharging the first and third capacitors, the former having been charged positively by a previous positive voltage transition of the load node, when the first MOSFET is switched to the conducting state;
 - switching the first MOSFET to the non-conducting state;
- In the above-mentioned method, the first and second capacitors serve as charge reservoirs that allow discharging the third capacitor. The first and second capacitors may be chosen to be larger than the third capacitor wherein the third capacitor may be fully discharged or discharged beyond the reference potential while the first and second capacitors may be only partially discharged.

An alternating impulsive current generated by a load (i.e. a variable speed motor drive) is rectified into the array of

three capacitors. One capacitor is charged positively, a second capacitor is charged negatively and a third capacitor is charged both positively and negatively as a result of positive and negative voltage transitions of the load node.

- 5 Immediately after each impulsive event, the energy in the bipolar capacitor is discharged, via a suitable switch, with the energy, or part thereof, in the polarized capacitor of opposite polarity. The energy in one polarized capacitor is always stored and held until the subsequent impulse event so
- 10 that energy of opposite polarity is available for the next discharge. In this way the energy and associated voltage at the load node is reduced near to the reference potential during most of the time and consequently the common mode current generated in the filter common mode inductor, which is
- 15 proportional to the time integral of load node voltage, is reduced considerably.

- In one embodiment, the electronic device comprises a first capacitor being coupled in series to a first one-way
- 20 conductor, that allows current flow in one direction, the first one-way conductor and the first capacitor being coupled between a load node and a reference potential. A second capacitor is coupled in series to a second one-way conductor, that allows current flow in the opposite direction, the second
- 25 one-way conductor and the second capacitor being coupled between the load node and the reference potential. A third capacitor is coupled between the load node and the reference potential. The device comprises an amplifier having an output terminal, and positive and negative supply rail terminals. The
- 30 output terminal is coupled to the load node. The positive supply rail terminal is coupled to a first potential node, that is between the first capacitor and the first one-way conductor. The negative supply rail terminal is coupled to the

a second potential node, that is between the second capacitor and the second one-way conductor.

The one-way conductors which may be diodes are connected to the load node and the capacitive elements are connected to the reference node. "Coupling" two components includes a direct connection between the components and coupling further components between the two components. Preferably, further components are coupled between the output terminal and the load node.

The method for filtering common mode disturbances by such an electronic device comprises:

- applying positive and negative voltage transitions at the load node,
- charging the first capacitor positive by positive voltage transitions of the load node, where the first one-way conductor is in conduction state, transferring energy to the first capacitor,
- charging the second capacitor negative by negative voltage transitions of the load node, where the second one-way conductor is in conduction state, transferring energy to the second capacitor,
- charging the third capacitor positive when a positive transition is applied and negative when a negative transition is applied,
- discharging the third capacitor to a voltage near to reference potential into the output terminal of the amplifier,
- at least partially discharging the first capacitor via the positive supply rail terminal of the voltage buffer amplifier,
- at least partially discharging the second capacitor via the negative supply rail terminal of the voltage buffer amplifier.

In yet another embodiment, a bypass inductor and discharge resistor are connected in parallel and which are further connected in series with, and on the load-side of, the common mode inductance. A voltage buffer amplifier having an input terminal connected via a capacitance to the reference potential, an output terminal connected to the series junction of the common mode inductance and the bypass inductor, a positive supply terminal which is connected via a first diode to the load node and a negative supply terminal which is connected via a second diode to the load node. The diodes are orientated such that the positive supply terminal is charged positively and the negative supply terminal is charged negatively as a result of positive and negative voltage excursions of the load node respectively. A first capacitor is connected between the positive supply terminal and the reference potential and a second capacitor is connected between the negative supply terminal and the reference potential. A third capacitor connects between the load node and the reference potential.

The method further comprises:

- charging the first and third capacitors positively by a positive voltage transition at the load node, while the first diode is forward biased.

- discharging the second and third capacitors, the former having been charged negatively by a previous negative voltage transition of the load node, via the discharge resistor, the output terminal and the negative supply terminal.

- charging the second and third capacitors negatively by a negative voltage transition at the load node, while the second diode is forward biased.

- discharging the first and third capacitors, the former having been charged positively by a previous positive voltage

transition of the load node, via the discharge resistor, the output terminal and the positive supply terminal.

In the above-mentioned method, the first and second capacitors serve as charge reservoirs that allow discharging the third capacitor. The voltage buffer amplifier serves to keep the load side of the common mode inductor near to the reference potential.

An alternating impulsive current generated by a load (i.e. a variable speed motor drive) is passed into the array of three capacitors. A first capacitor is charged positively, a second capacitor is charged negatively and a third follows the load node potential. The third capacitor is discharged continuously via a discharge resistor and a voltage buffer amplifier which serves to distribute the discharge current via its supply terminals to the polarized capacitors. The discharge current amplitude is controlled by the value of the discharge resistor. At motor drive carrier frequencies the output terminal voltage, which is connected to the load-side of the common mode inductor, is held close to the reference potential. In this way the energy and associated voltage at the load-side of the common mode inductor is reduced near to the reference potential during most of the time and consequently the common mode current generated in the common mode inductor, which is proportional to the time integral of the voltage imposed on it, is reduced considerably.

In one embodiment, a method for filtering common mode disturbances concerns an electronic device comprising:

- a first capacitor being coupled in series to a first one-way conductor, the first capacitor and the first one-way conductor being coupled between a load node and a reference potential, and

- a second capacitor being coupled in series to a second one-way conductor, the second capacitor and the second one-way conductor being coupled between the load node and the reference potential;
- 5 - a third capacitor being coupled between load node and the reference potential;
- a first inductor being coupled in series to second inductor, the first inductor and the second inductor being coupled between the line node and the load node with first inductor on
- 10 the line-side and second inductor (L2) on the load-side;
- a resistor being coupled in parallel with the second inductor;
- a voltage buffer amplifier with its output terminal being coupled to the series junction between the first inductor and
- 15 the second inductor, its positive supply rail terminal being coupled to the first capacitor and its negative supply rail terminal being coupled to the second capacitor and its input terminal coupled at drive carrier frequencies via a fourth capacitor which is connected to the reference potential.
- 20 Positive and negative voltage transitions are present at the load node.

The method comprises:

- charging the first capacitor positive by positive voltage
- 25 transitions of the load node, where the first one-way conductor in conduction state, transferring energy to the first capacitor,
- charging the second capacitor negative by negative voltage transitions of the load node, where the second one-way
- 30 conductor in conduction state, transferring energy to the second capacitor,
- charging the third capacitor to the load node potential, varying over time sometimes positive and sometimes negative,

- discharging the third capacitor via the resistor to a voltage near to reference potential into the output terminal of the voltage buffer amplifier,
- partially discharging the first capacitor via the positive
5 supply rail terminal of the voltage buffer amplifier,
- partially discharging the second capacitor via the negative supply rail terminal of the voltage buffer amplifier,
- holding the series junction of the first inductor and the
10 second inductor by the output terminal of the voltage buffer amplifier, where the input terminal of the voltage buffer amplifier is referenced at drive carrier frequencies to the reference potential by a fourth capacitor.

The parallel resistor, which serves to dissipate energy and
15 control discharge current, can be replaced with a voltage boost device, wherein the input to the voltage boost device is coupled to the second inductor via an auxiliary winding, the output of the voltage boost device is coupled to an external power sink, such as the dc link of the variable speed motor
20 drive, where the removed energy can be used efficiently.

A linear voltage amplifier may be connected in closed loop to provide the same function as the voltage buffer amplifier. The linear voltage amplifier can be replaced with a D Class
25 voltage amplifier to improve efficiency of the amplifier.

The capacitor connected to the input terminal of the voltage buffer amplifier is replaced by a high pass filter to improve the rejection of power frequency common mode voltages.
30 Several interface networks of capacitors and resistors are included to provide effective filtering of a 3 phase supply. A star network of capacitors and series resistor can couple the 3 phases to the output terminal of the linear voltage amplifier. A star network of capacitors can couple the three

phase load node to the one-way conductors and the third capacitor. A star network of high impedance components such as resistors can couple the 3 phases to the inverting input terminal of the linear voltage amplifier.

5

Features that are described herein above and below in conjunction with the different aspects and embodiments presented may also apply to other aspects and embodiments. Further features and advantageous embodiments of the subject-

10 matter of the disclosure will become apparent from the following description of the exemplary embodiments in conjunction with the figures, in which:

15

Figure 1 shows a common mode equivalent circuit of a variable speed drive system.

Figure 2 shows a common mode equivalent circuit of a low pass power line filter and terminating networks.

20

Figure 3 shows a common mode equivalent circuit of a low pass power line filter, including a switch over the capacitor, which is for demonstration purposes only.

25

Figure 4 shows a common mode equivalent circuit of one embodiment of the invention involving four capacitors, four diodes and two switches.

30

Figure 5 shows a common mode equivalent circuit of one embodiment of the invention involving three capacitors and two diodes and two switches.

Figure 6 shows a common mode equivalent circuit of one embodiment of the invention involving three capacitors, two

diodes, a voltage buffer amplifier, a bypass inductor and a discharge resistor.

Figure 7 shows an equivalent circuit of a three phase embodiment of the circuit in Figure 6.

Figure 8 shows a common mode equivalent circuit of the circuit in Figure 6 with D class amplifier and voltage boost device to replace the discharge resistor.

Figure 1 shows a single line common mode equivalent circuit of a variable speed motor drive system connected to a TN supply where the supply is connected to the reference potential, in this case the supply earth. Voltage V_s represents a common mode voltage which results from a voltage imbalance relative to the reference potential. On balanced three phase supply V_s may be quite small while for single phase or corner earthed three phase supplies it may be larger. The supply is connected via a low pass power line filter 1 to a variable speed motor drive 2 and then to a screened motor cable 4 and to a motor 3. The system may contain one or more motor drives 2 and one or more motors 3. The motor drive 2 may be regenerative or non-regenerative type.

All parts of the power train may effect capacitive coupling to the reference potential, which may be stray (parasitic) or intentional. The screened motor cable may form a large stray capacitive component especially where the motor cable is long. This capacitance is represented collectively by C_s . The high slew rate voltage transitions from the switches in the variable speed motor drive 2 cause impulsive common mode current to flow in loops along the power conductors and earth connections.

The low pass power line filter works to contain these impulsive common mode currents to its load-side and to limit the amplitude and frequency bandwidth of common mode interference current I_{cm} allowed to flow in the supply line.

5

The common mode equivalent circuit of a low pass line filter and terminating networks is shown in Figure 2. A common mode inductance L_{cm} is connected between the line node LINE and the load node LOAD. A common mode capacitance C_y is connected

10

between the load node LOAD and the reference potential 0. L_{cm} and C_y represent the common mode parameters of the low pass power line filter. The power line filter is terminated on the line-side by a short circuit to the reference potential where a common mode interference current I_{cm} may flow. For

15

simplicity common mode power line voltage V_s , from Figure 1, is assumed to be zero. The power line filter is terminated on the load-side with the reference coupled capacitance C_s connected in series with a voltage source V_n which represents the switching transitions of the variable speed motor drive

20

switches. Impulsive currents resulting from the switch transitions in the load impinge on the load-side of the filter. The series inductance and shunt capacitance are selected to give relative impedances such that the impulsive current passes mainly through the common mode capacitance C_y .

25

The current allowed to flow in the common mode inductor L_{cm} , and therefore the current I_{cm} allowed to flow on the supply line, is proportional to the time integral of the resultant voltage across the common mode capacitance C_y .

30

Significant problems can result in the filter when the common mode inductance and common mode capacitance self-resonate wherein the common mode current in the inductor and therefore the current on the supply line I_{cm} , may become very large.

This may result in high system losses and may result in magnetic saturation of the common mode inductor Lcm core.

Figure 3 shows one principle of operation of the invention where a switch S is imposed in parallel with the common mode capacitor Cy.

The switch S, which is normally open, may be closed momentarily immediately after the common mode capacitor Cy has been charged by a voltage transition of the load node LOAD. When the common mode capacitor Cy is discharged and its energy mostly dissipated, there is little energy available to energize the common mode inductance Lcm. The current in the common mode inductor Lcm, which is proportional to the time integral of the voltage over the common mode capacitance Cy, is reduced when the voltage across the common mode capacitance Cy is held near to the reference potential for as much time as possible.

The imposition of the switch S in parallel with the common mode capacitor Cy is for demonstration purposes only. Such a configuration cannot be used in a power line filter because the switch S will compromise the voltage isolation provided by the common mode capacitor Cy between the power line voltages and the reference potential.

The dissipation of energy from the common mode capacitance Cy by switch S serves to avoid self-resonate between the common mode inductance Lcm and the common mode capacitance Cy.

Figure 4 shows an embodiment of the invention where the common mode capacitance Cy of Figure 2 is replaced by a network of four capacitors C1, C2, C3 and C4, four diodes D1, D2, D3 and D4 and two switches S1 and S2. The diodes work as rectifiers

such that capacitors C1 and C3 charge positive and capacitors C2 and C4 are charge negative in relation to the reference potential 0. Switch S1 bridges between capacitors C1 and C2 and switch S2 bridges between capacitors C3 and C4. The
5 switches S1 and S2 are controlled by a control circuit 5 serving as switch control.

The circuit works as follows: Switches S1 and S2 are normally in the non-conducting state. Capacitors C1 and C3 are charged
10 positive due to a positive impulsive current entering the load node. Immediately after this event switch S1 is momentarily closed, whereby the charge in C1 is discharged with the charge in C2 which has been charged negative by a previous negative impulsive current entering the load node. Capacitors C2 and C4
15 are charged negative due to a negative impulsive current entering the load node. Immediately after this event switch S2 is momentarily closed, whereby the charge in C4 is discharged with the charge in C3 which has been charged positive by a previous positive impulsive current entering the load node.

20 An alternating impulsive common mode current impinging on the load node is allowed to charge a capacitor pair, immediately after which the one of these capacitors is discharged with one of the capacitors which was previously charged to the opposite
25 polarity.

The voltage isolation integrity provided by capacitors C1, C2, C3 and C4 is maintained because the switches S1 and S2 are connected between the capacitors and are not connected to the
30 reference potential.

The voltage at the load node is reduced near to the reference potential during most of the time and consequently the common mode current generated in the filter common mode inductor,

which is proportional to the time integral of load node voltage, is reduced considerably.

In the above-mentioned method, capacitors C2 and C3 serve as
5 charge reservoirs that allow the discharging of capacitors C1 and C4.

Figure 5 shows an embodiment of the invention where the common mode capacitance C_y of Figure 2 is replaced by a network of
10 three capacitors C1, C2 and C3, two diodes D1 and D2 and two switches S1 and S2. The diodes work as rectifiers such that capacitor C1 charges positive and capacitor C2 charges negative in relation to the reference potential 0. Switch S1 connects in parallel with diode D1 and switch S2 connects in
15 parallel with between diode D2. When the switches are closed the diodes are bypassed. Capacitor C3 follows the load node voltage. The switches S1 and S2 are controlled by a control circuit 5 serving as switch control.

20 The circuit works as follows: Switches S1 and S2 are normally in the non-conducting state. Capacitors C1 and C3 are charged positive due to a positive impulsive current entering the load node. Immediately after this event switch S2 is momentarily closed, whereby the charge in C3 is discharged with the charge
25 in C2 which has been charged negative by a previous negative impulsive current entering the load node. Capacitors C2 and C3 are charged negative due to a negative impulsive current entering the load node. Immediately after this event switch S1 is momentarily closed, whereby the charge in C3 is discharged
30 with the charge in C1 which has been charged positive by a previous positive impulsive current entering the load node. An alternating impulsive common mode current impinging on the load node is allowed to charge a capacitor pair, immediately after which the capacitor C3 is discharged with the capacitor

C1 or C2 which was previously charged to the opposite polarity.

The voltage isolation integrity provided by capacitors C1, C2 and C3 is maintained because the switches S1 and S2 are connected across the diodes and are not connected to the reference potential.

The voltage at the load node is reduced near to the reference potential during most of the time and consequently the common mode current generated in the filter common mode inductor, which is proportional to the time integral of load node voltage, is reduced considerably.

In the above-mentioned method, capacitors C1 and C2 serve as charge reservoirs that allow discharging capacitor C3. Capacitors C1 and C2 may be chosen to be larger than capacitor C3 wherein the capacitor C3 may be fully discharged or discharged beyond the reference potential while capacitors C1 and C2 may be only partially discharged.

Figure 6 shows an embodiment of the invention where the common mode capacitance C_y of Figure 2 is replaced by a network of four capacitors C1, C2, C3 and C4, two diodes D1 and D2, a voltage buffer amplifier U1, a bypass inductor L2 and a discharge resistor R2. The diodes work as rectifiers such that capacitor C1 charges positive and capacitor C2 charges negative in relation to the reference potential 0. The input of the voltage buffer amplifier is reference to the reference potential via capacitor C4. The buffer amplifier output voltage, which follows the reference potential at radio frequencies, is connected to the line-side of bypass inductor L2.

The circuit works as follows: Capacitors C1 is charged positive due to positive impulsive current entering the load node and capacitor C2 is charged negative due negative impulsive current entering the load node. Capacitor C3 follows the load node voltage. The output terminal of U1 is constantly maintained at the reference potential such that capacitor C3 is constantly discharged via discharge resistor R2 which controls the amplitude of discharge current. The aim is to maintain the voltage across capacitor C3 as near to the reference potential for as much time as possible. The discharge current taken from capacitor C3 is fed via the supply terminals of U1 to capacitors C1 and C2 which are partially discharged.

15 An alternating impulsive common mode current impinging on the load node is allowed to charge a capacitor pair, immediately after which the capacitor C3 is discharged with the capacitor C1 or C2 which was previously charged to the opposite polarity. Voltage isolation integrity is provided by

20 capacitors C1, C2, C3 and C4.

The voltage on the load-side of the common mode inductor Lcm is reduced near to the reference potential during most of the time and consequently the common mode current generated in the filter common mode inductor Lcm, which is proportional to the time integral of the voltage across the common mode inductor Lcm, is reduced considerably.

In the above-mentioned method, capacitors C1 and C2 serve as charge reservoirs that allow discharging capacitor C3. Capacitors C1 and C2 also serve as power supply reservoir capacitors feeding voltage buffer amplifier U1. Capacitors C1 and C2 may be chosen to be larger than capacitor C3 wherein the capacitor C3 may be fully discharged while capacitors C1

and C2 may be only partially discharged. The output of the voltage buffer amplifier serves to maintain near reference potential on the load-side of common mode inductor Lcm.

5 Figure 7 shows a three phase embodiment of the embodiment shown in Figure 6. The voltage buffer amplifier is replaced with a voltage amplifier U1 with differential inputs. The voltage amplifier output is connected to the three phase line via a resistance in series with a capacitor star network. The
10 voltage amplifier is connected in a closed loop where the inverting input of the voltage amplifier is maintained at the common mode voltage of the line via a resistor star network. The voltage amplifier non-inverting input is maintained at the reference potential via capacitor C4. Thus the three phase
15 line at the load-side of the common mode inductance Lcm is held near to the reference potential. Capacitors C1, C2 and C3 and diodes D1 and D2 are connected to the three phase load node via a capacitor star network. The discharge resistor R2 is inductively coupled to the bypass inductor L2 via and
20 auxiliary winding on L2.

The circuit works in the same way as described for Figure 6. The star point of the two additional capacitor networks and the additional resistor network serve as the common mode
25 points of the three phase line. Voltage isolation integrity is provided by capacitors C1, C2, C3 and C4.

The voltage on the load-side of the common mode inductor Lcm is reduced near to the reference potential during most of the
30 time and consequently the common mode current generated in the filter common mode inductor Lcm, which is proportional to the time integral of the voltage across the common mode inductor Lcm, is reduced considerably.

In the above-mentioned method, capacitors C1 and C2 serve as charge reservoirs that allow discharging capacitor C3.

Capacitors C1 and C2 also serve as power supply reservoir capacitors feeding voltage amplifier U1. Capacitors C1 and C2

5 may be chosen to be larger than capacitor C3 wherein the capacitor C3 may be fully discharged while capacitors C1 and C2 may be only partially discharged. The output of the voltage buffer amplifier serves maintain near reference potential on the load-side of common mode inductor Lcm.

10

Figure 8 shows an embodiment of the invention where the efficiency of the embodiment shown in Figure 6 is improved.

The voltage buffer amplifier is replaced with a D class voltage amplifier U1 with differential inputs which is

15 connected in closed loop whereby the load-side of common mode inductance Lcm is maintained near the reference potential by the error signal between non-inverting and inverting inputs. The function of capacitors C1, C2, C3 and C4 and diodes D1 and D2 remains the same. The discharge resistor is replaced by a
20 voltage boost device which moves energy to a voltage supply within the motor drive system, i.e. the dc link, where the energy can be used efficiently. The input to the voltage boost may be made to be equivalent to the characteristics of the discharge resistor.

25

The circuit works in the same way as described for Figure 6. Voltage isolation integrity is provided by capacitors C1, C2, C3 and C4.

30 The voltage on the load-side of the common mode inductor Lcm is reduced near to the reference potential during most of the time and consequently the common mode current generated in the filter common mode inductor Lcm, which is proportional to the

time integral of the voltage across the common mode inductor L_{cm} , is reduced considerably.

In the above-mentioned method, capacitors C1 and C2 serve as
5 charge reservoirs that allow discharging capacitor C3.
Capacitors C1 and C2 also serve as power supply reservoir
capacitors feeding voltage amplifier U1. Capacitors C1 and C2
may be chosen to be larger than capacitor C3 wherein the
capacitor C3 may be fully discharged while capacitors C1 and
10 C2 may be only partially discharged. The output of the D class
voltage amplifier serves to maintain near reference potential
on the load-side of common mode inductor L_{cm} .

Claims

1. An electronic device comprising

- a first capacitor (C1) being coupled in series to a first
5 one-way conductor (D1), that allows current flow in one
direction, and the first one-way conductor (D1) and the first
capacitor (C1) being coupled between a load node (LOAD) and a
reference potential (0), and

- a second capacitor (C2) being coupled in series to a second
10 one-way conductor (D2), that allows current flow in the
opposite direction, the second one-way conductor (D2) and the
second capacitor (C2) being coupled between the load node
(LOAD) and the reference potential (0), and

- a third capacitor (C3) being coupled between the load node
15 (LOAD) and the reference potential (0), and

- a first switch (S1) bypassing the first one-way conductor
(D1), and

- a second switch (S2) bypassing the second one-way conductor
(D2).

2. An electronic device comprising

- a first capacitor (C1) being coupled in series to a first
one-way conductor (D1), the first one-way conductor (D1) and
the first capacitor (C1) being coupled between a load node
25 (LOAD) and a reference potential (0), and

- a second capacitor (C2) being coupled in series to a second
one-way conductor (D2), the second one-way conductor (D2) and
the second capacitor (C2) being coupled between the load node
(LOAD) and the reference potential (0), and

- a third capacitor (C3) being coupled in series to a third
30 one-way conductor (D3), the third one-way conductor (D3) and
the third capacitor (C3) being coupled between the load node
(LOAD) and the reference potential (0), and

- a fourth capacitor (C4) being coupled in series to a fourth one-way conductor (D4), the fourth one-way conductor (D4) and the fourth capacitor (C4) being coupled between the load node (LOAD) and the reference potential (0),
 - 5 - the first and third one-way conductors (D1, D3) allowing current flow in one direction, the second and fourth one-way conductors (D2, D4) allowing current flow in the opposite direction,
 - a first switch (S1) coupled between a first potential node, that is between the first capacitor (C1) and the first one-way conductor (D1), and a second potential node, that is between the second capacitor (C2) and the second one-way conductor (D2),
 - 10 - a second switch (S2) coupled between a third potential node, that is between the third capacitor (C3) and the third one-way conductor (D3), and a fourth potential node, that is between the fourth capacitor (C4) and the fourth one-way conductor (D4).
- 20 3. The electronic device according to claim 1, wherein the first switch (S1) is coupled between a potential node, that is between the first one-way conductor (D1) and the first capacitor (C1), and the load node (LOAD), and the second switch (S2) is coupled between a further potential
- 25 node, that is between the second one-way conductor (D2) and the second capacitor (C2), and the load node (LOAD).
4. The electronic device according to claim 1 or 3, wherein the first switch (S1) connected in parallel with the first
- 30 one-way conductor (D1) or the second switch (S2) connected in parallel with the second one-way conductor (D2) is embodied as a MOSFET with body diode or an insulated-gate bipolar transistor with a freewheeling diode or a bipolar junction

transistor with a freewheeling diode or a silicon-controlled rectifier with a reverse connected diode in parallel.

5. The electronic device according to any of the previous claims further comprising a switch control (5) for switching the switches (S1, S2, S3, S4) between a conducting state allowing current flow and a non-conducting state with no current flow.

- 10 6. An electronic device comprising
- a first capacitor (C1) being coupled in series to a first one-way conductor (D1), that allows current flow in one direction, the first one-way conductor (D1) and the first capacitor (C1) being coupled between a load node (LOAD) and a
 - 15 reference potential (0), and
 - a second capacitor (C2) being coupled in series to a second one-way conductor (D2), that allows current flow in the opposite direction, the second one-way conductor (D2) and the second capacitor (C2) being coupled between the load node
 - 20 (LOAD) and the reference potential (0),
 - a third capacitor (C3) being coupled between the load node (LOAD) and the reference potential (0),
 - an amplifier (U1) having an output terminal, and positive and negative supply rail terminals, the output terminal being
 - 25 coupled to the load node (LOAD), the positive supply rail terminal being coupled to a first potential node, that is between the first capacitor (C1) and the first one-way conductor (D1), and the negative supply rail terminal being coupled to the a second potential node, that is between the
 - 30 second capacitor (C2) and the second one-way conductor (D2).

7. The electronic device according to claim 6, wherein the amplifier (U1) is embodied as a voltage buffer amplifier or a linear voltage amplifier or a D class voltage amplifier.

8. The electronic device according to claim 6 or 7, wherein an input of the amplifier is coupled via a capacitor (C4) or a high-pass filter to the reference potential (0).

5 9. The electronic device according to claim 6, 7 or 8 wherein a resistor (R2) and a inductor (L2), that are coupled in parallel, are coupled between the output terminal of the amplifier (U1) and the load node (LOAD) or wherein an inductor is coupled between the output terminal of the amplifier (U1)
10 and the load node (LOAD), a voltage boost device being coupled to the inductor via an auxiliary winding.

10. The electronic device according to claim 6, 7, 8 or 9, that can be coupled to a 3 phase supply, the device further
15 comprising
- a star network of capacitors and a series resistor (R3) to couple the 3 phases to the output terminal of the linear voltage amplifier (U1),
- a star network of capacitors to couple the 3 phases to the
20 one-way conductors (D1, D2) and the third capacitor (C3),
- a star network of components to couple the 3 phases to the inverting input terminal of the amplifier (U1).

11. Method for filtering common mode disturbances by an
25 electronic device, that comprises:
- a first capacitor (C1) being coupled in series to a first one-way conductor (D1), the first capacitor (C1) and the first one-way conductor (D1) being coupled between a load node (LOAD) and a reference potential (0), and
30 - a second capacitor (C2) being coupled in series to a second one-way conductor (D2), the second capacitor (C2) and the second one-way conductor (D2) being coupled between the load node (LOAD) and the reference potential (0), and

- a third capacitor (C3) being coupled between the load node (LOAD) and the reference potential (0),
- a first switch (S1) coupled in parallel with the first one way conductor (D1) and a second switch (S2) coupled in parallel with the second one way conductor (D2),
- 5 the method comprising:
 - applying alternating positive and negative voltage transitions at the load node (LOAD),
 - charging the first capacitor (C1) and the third capacitor (C3) positive by one positive voltage transition of the load node (LOAD), where the first one-way conductor (D1) is in the conduction state, transferring energy to the first capacitor (C1) and the third capacitor (C3),
 - 10 - discharging the second capacitor (C2) and the third capacitor (C3), the former (C2) having been charged negative by a previous negative voltage transition at the load node (LOAD), when the second switch (S2) is switched to the conducting state,
 - 15 - switching the second switch (S2) to the non-conducting state,
 - 20 - charging the second capacitor (C2) and the third capacitor (C3) negative by one negative voltage transition of the load node (LOAD), where the second one-way conductor (D2) is in the conduction state, transferring energy to the second capacitor (C2) and the third capacitor (C3),
 - 25 - discharging the first capacitor (C1) and third capacitor (C3), the former (C1) having been charged positive by a previous positive voltage transition at the load node (LOAD), when the first switch (S1) is switched to the conducting state,
 - 30 - switching the first switch (S1) to the non-conducting state.

12. Method for filtering common mode disturbances by an electronic device, that comprises:

- a first capacitor (C1) being coupled in series to a first one-way conductor (D1), the first capacitor (C1) and the first one-way conductor (D1) being coupled between a load node (LOAD) and a reference potential (0), and
 - 5 - a second capacitor (C2) being coupled in series to a second one-way conductor (D2), the second capacitor (C2) and the second one-way conductor (D2) being coupled between the load node (LOAD) and the reference potential (0), and
 - a third capacitor (C3) being coupled in series to a third
 - 10 one-way conductor (D3), the third capacitor (C3) and the third one-way conductor (D3) being coupled between the load node (LOAD) and the reference potential (0), and
 - a fourth capacitor (C4) being coupled in series to a fourth one-way conductor (D4), the fourth capacitor (C4) and the
 - 15 fourth one-way conductor (D4) being coupled between the load node (LOAD) and the reference potential (0),
 - a first switch (S1) coupled between a first potential node, that is between the first capacitor (C1) and the first one-way conductor (D1), and a second potential node, that is between
 - 20 the second capacitor (C2) and the second one-way conductor (D2),
 - a second switch (S2) coupled between a third potential node, that is between the third capacitor (C3) and the third one-way conductor (D3), and a fourth potential node, that is between
 - 25 the fourth capacitor (C4) and the fourth one-way conductor (D4);
- the method comprising:
- applying alternating positive and negative voltage transitions at the load node (LOAD),
 - 30 - charging the first capacitor (C1) and the third capacitor (C3) positive by one positive voltage transition of the load node (LOAD), where the first one-way conductor (D1) and the third one-way conductor (D3) are in the conduction state,

transferring energy to the first capacitor (C1) and the third capacitor (C3),

- discharging the first capacitor (C1) and the second capacitor (C2), the latter (C2) having been charged negative by a previous negative voltage transition at the load node (LOAD), when the first switch (S1) is switched to the conducting state,

- switching the first switch (S1) to the non-conducting state,
- charging the second capacitor (C2) and the fourth capacitor (C4) negative by one negative voltage transition of the load node (LOAD), where the second one-way conductor (D2) and the fourth one-way conductor (D4) are in the conduction state, transferring energy to the second capacitor (C2) and the fourth capacitor (C4),

- discharging the third capacitor (C3) and the fourth capacitor (C4), the former (C3) having been charged positive by the previous positive voltage transition at the load node (LOAD), when the second switch (S2) is switched to the conducting state,

- switching the second switch (S2) to the non-conducting state.

13. Method according to claim 11, wherein the first switch (S1) in parallel with the first one-way conductor (D1) or the second switch (S2) in parallel with the second one-way conductor (D2) is embodied as a MOSFET with body diode or an insulated-gate bipolar transistor with freewheeling diode or a bipolar junction transistor with freewheeling diode or a silicon-controlled rectifier with a reverse connected diode in parallel.

14. Method for filtering common mode disturbances by an electronic device, that comprises:

- a first capacitor (C1) being coupled in series to a first one-way conductor (D1), the first capacitor (C1) and the first one-way conductor (D1) being coupled between a load node (LOAD) and a reference potential (0), and
- 5 - a second capacitor (C2) being coupled in series to a second one-way conductor (D2), the second capacitor (C2) and the second one-way conductor (D2) being coupled between the load node (LOAD) and the reference potential (0),
- a third capacitor (C3) being coupled between load node
- 10 (LOAD) and the reference potential (0),
- an amplifier (U1) having an output terminal, and positive and negative supply rail terminals, the output terminal being coupled to the load node (LOAD) , the positive supply rail terminal being coupled to the first capacitor (C1) and the
- 15 negative supply rail terminal being coupled to the second capacitor (C2),
- the method comprising:
- applying positive and negative voltage transitions at the load node (LOAD),
- 20 - charging the first capacitor (C1) positive by positive voltage transitions of the load node (LOAD), where the first one-way conductor (D1) in conduction state, transferring energy to the first capacitor (C1),
- charging the second capacitor (C2) negative by negative
- 25 voltage transitions of the load node (LOAD), where the second one-way conductor (D2) in conduction state, transferring energy to the second capacitor (C2),
- charging the third capacitor (C3) positive when a positive transition is applied and negative when a negative transition
- 30 is applied,
- discharging the third capacitor (C3) to a voltage near to reference potential (0) into the output terminal of the amplifier (U1),

- at least partially discharging the first capacitor (C1) via the positive supply rail terminal of the voltage buffer amplifier (U1),

5 - at least partially discharging the second capacitor (C2) via the negative supply rail terminal of the voltage buffer amplifier (U1).

15. Method according to claim 14, wherein the amplifier (U1) is embodied as a linear voltage amplifier (U1) being connected in closed loop or as a voltage buffer amplifier (U1) or as D Class voltage amplifier (U1).

16. Method according to claim 14 or 15, wherein

- a first inductor (Lcm) being coupled in series to second inductor (L2), the first inductor (Lcm) and the second inductor (L2) being coupled between a line node (LINE) and the load node (LOAD) with the first inductor (Lcm) on the line-side and the second inductor (L2) on the load-side,
- a resistor (R2) being coupled in parallel with the second inductor (L2),

20 the third capacitor (C3) being discharged via the resistor (R2).

17. Method according to claims 14 or 15, wherein

- 25 - a first inductor (Lcm) being coupled in series to second inductor (L2), the first inductor (Lcm) and the second inductor (L2) being coupled between a line node (LINE) and the load node (LOAD) with the first inductor (Lcm) on the line-side and the second inductor (L2) on the load-side,
- 30 - the input to a voltage boost device is coupled to the second inductor (L2) via an auxiliary winding; the third capacitor (C3) being discharged via the second inductor (L2); where the energy stored in the third capacitor (C3) is transferred from

the auxiliary winding into the input of the voltage boost device,

- the output of the voltage boost device is coupled to an external power sink; where the energy removed from the third capacitor (C3) is deposited.

18. Method according to claim 14, 15, 16 or 17 wherein an input of the amplifier (U1) is coupled via a capacitor (C4) or a high-pass filter to the reference potential (0).

10

19. Method according to claim 14, wherein

- a star network of capacitors and a series resistor (R3) are coupled between a line side of a 3 phase supply and the output terminal of the amplifier (U1),
- 15 - a star network of capacitors is coupled between the load side of the 3 phase supply and the one-way conductors (D1, D2) and the third capacitor (C3),
- a star network of impedance components is coupled between the 3 phases of the 3 phase supply and the inverting input
- 20 terminal of the amplifier (U1).

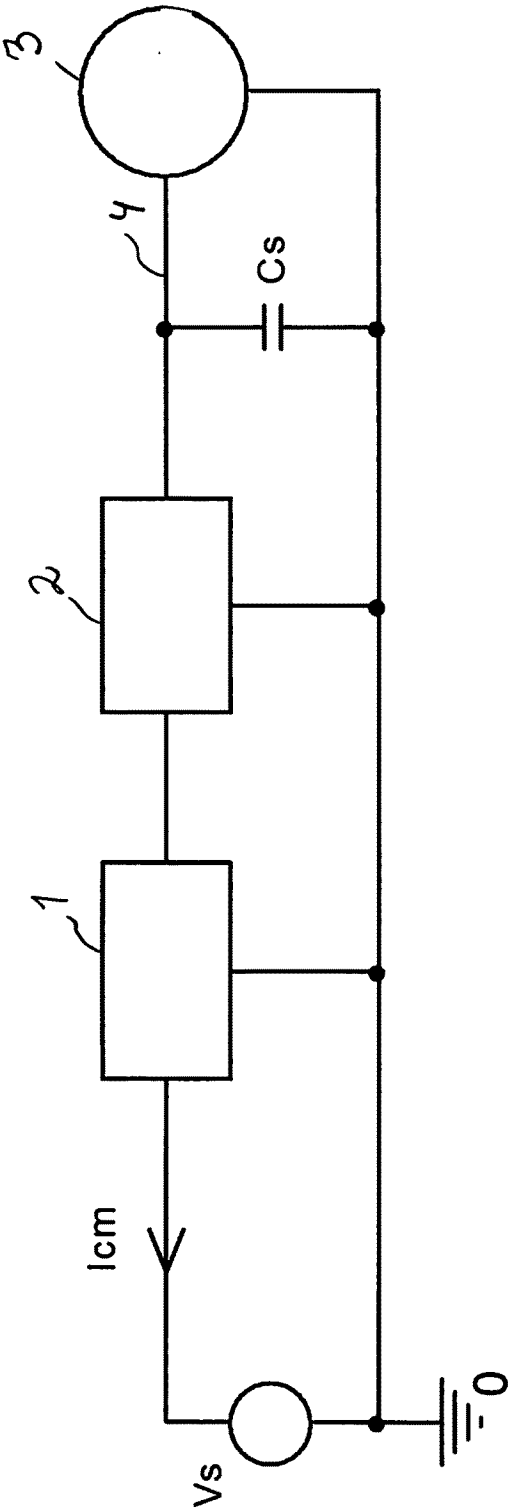


Figure 1

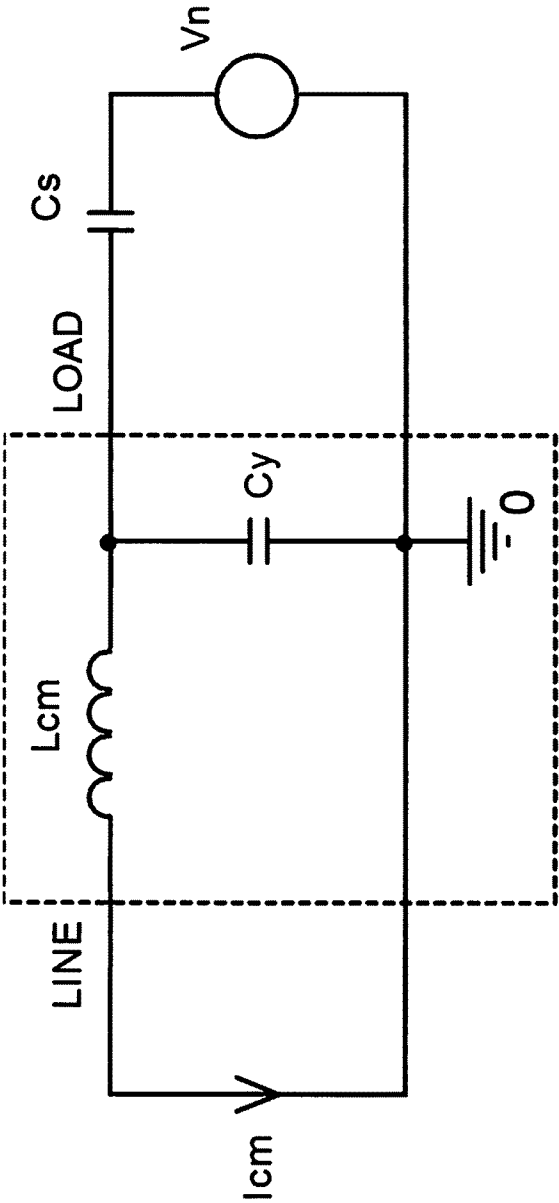


Figure 2

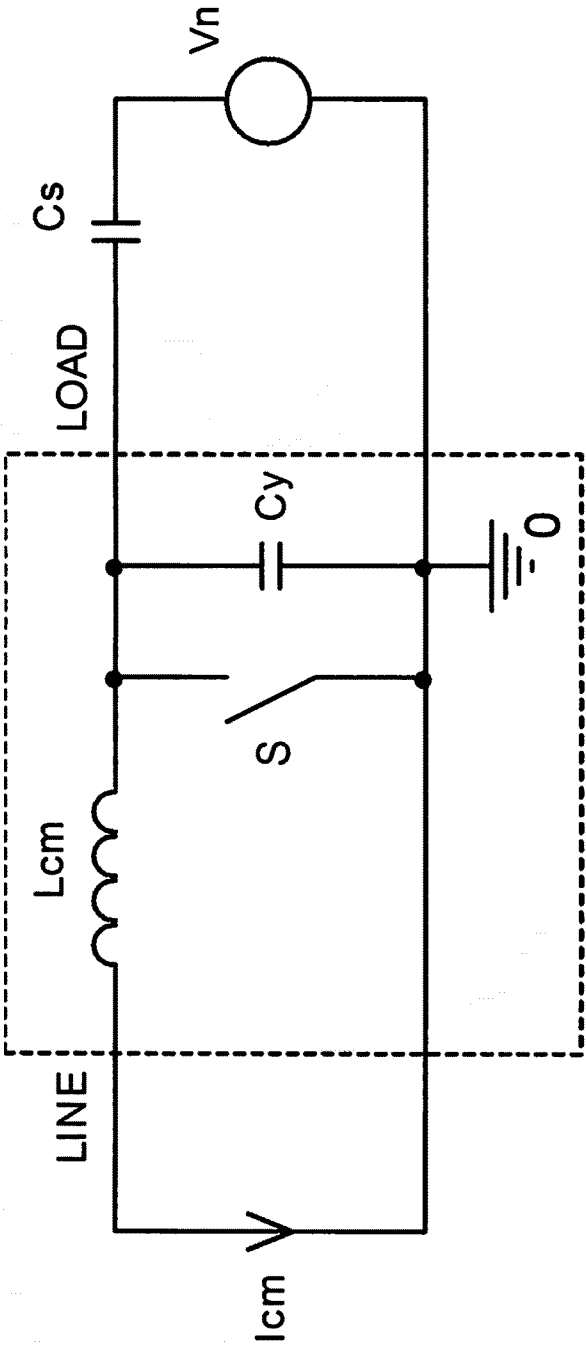


Figure 3

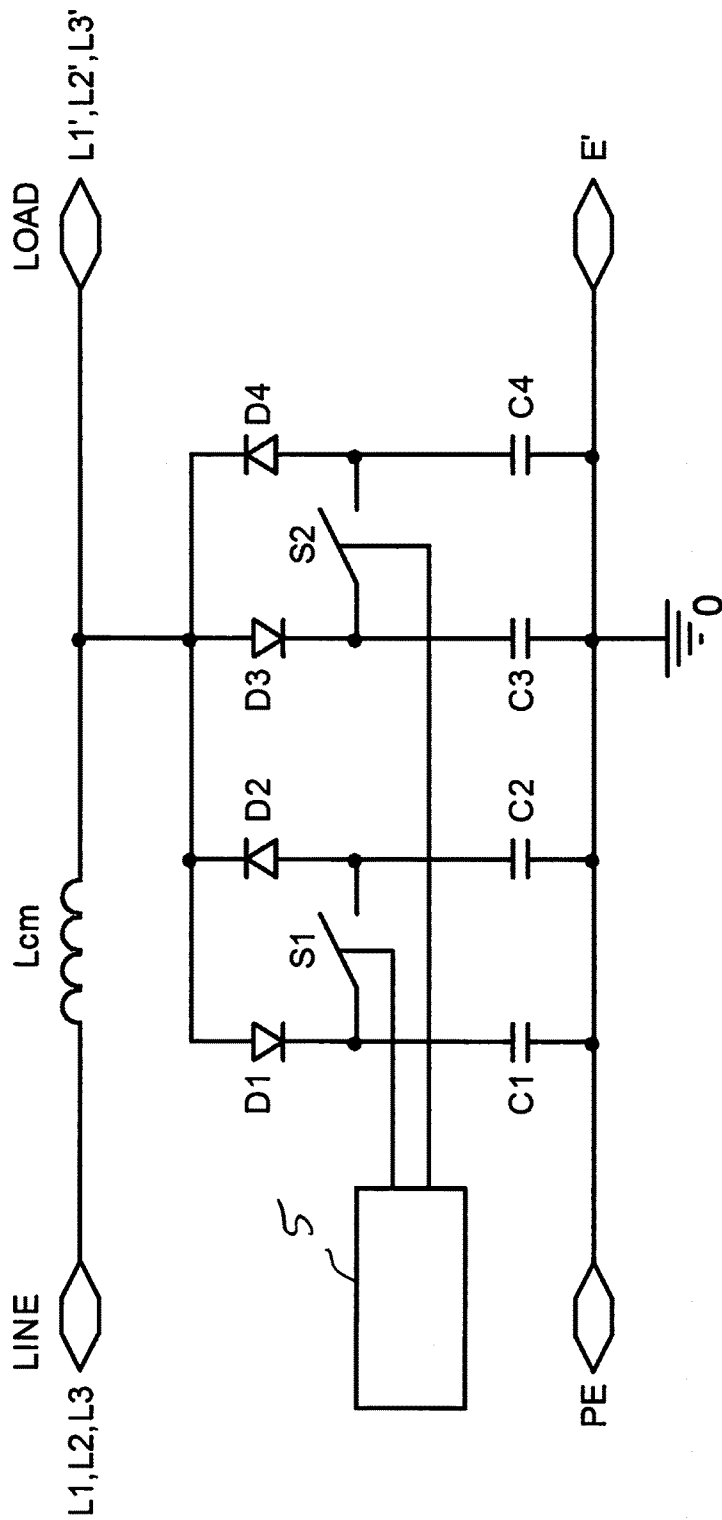


Figure 4

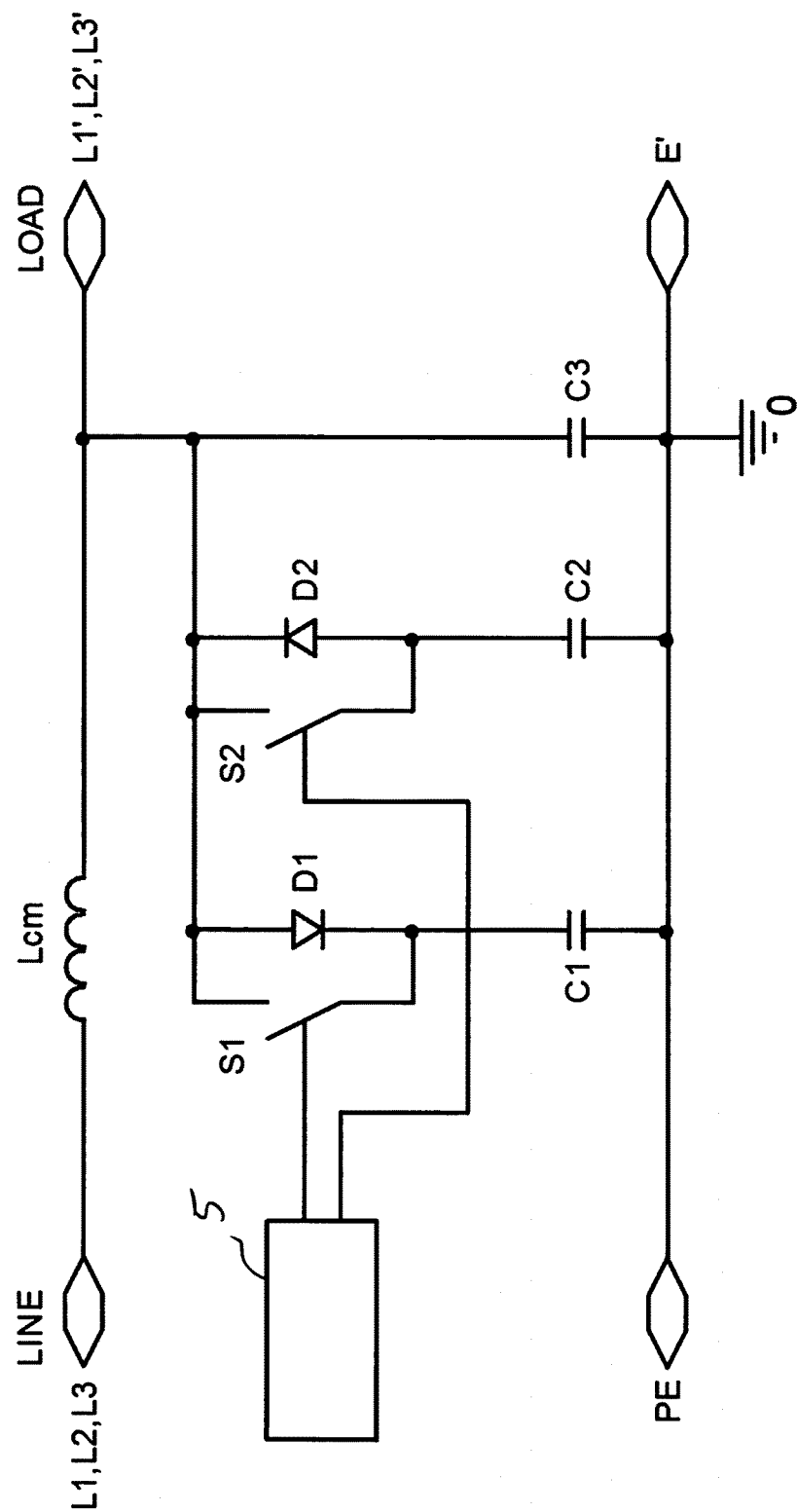


Figure 5

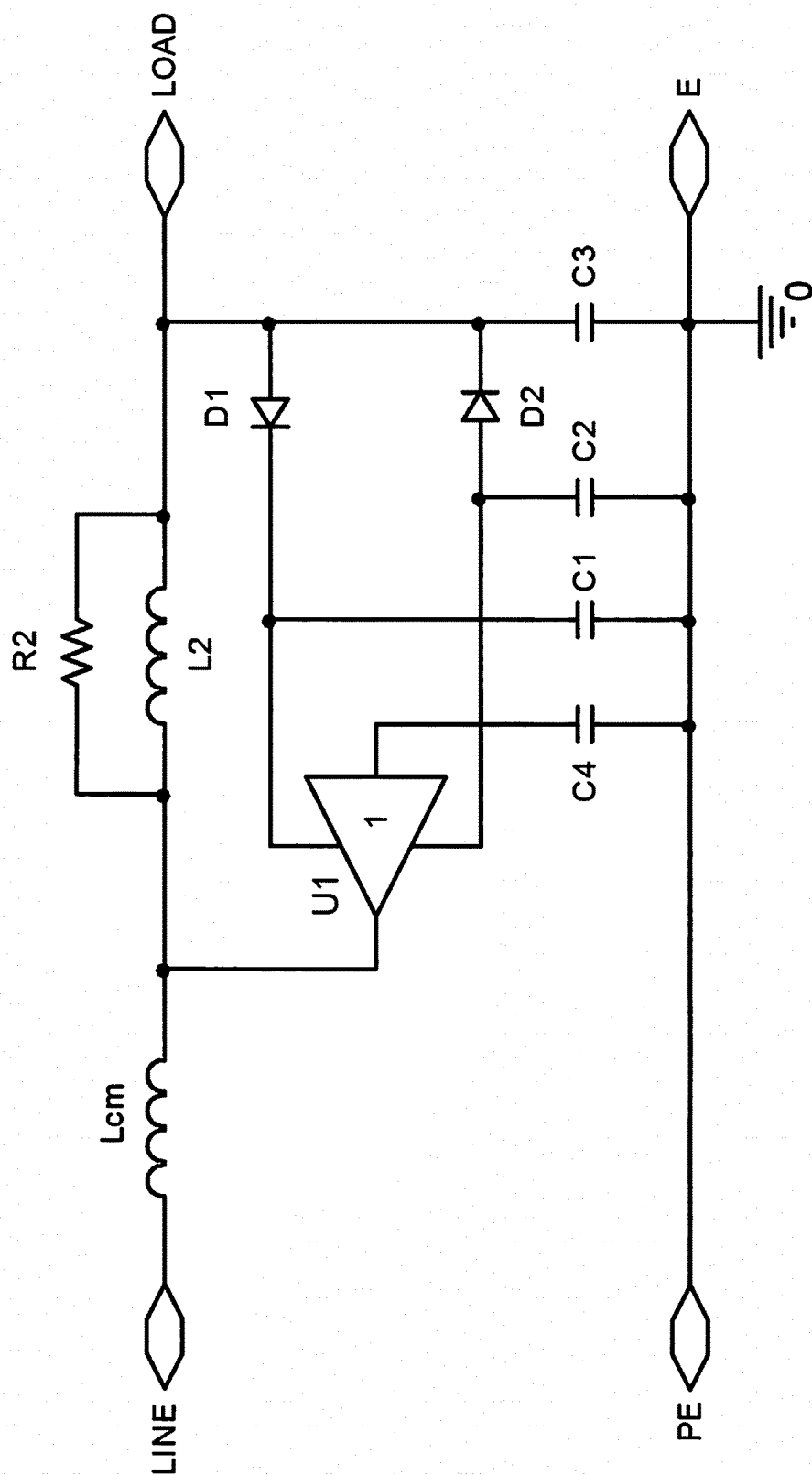


Figure 6

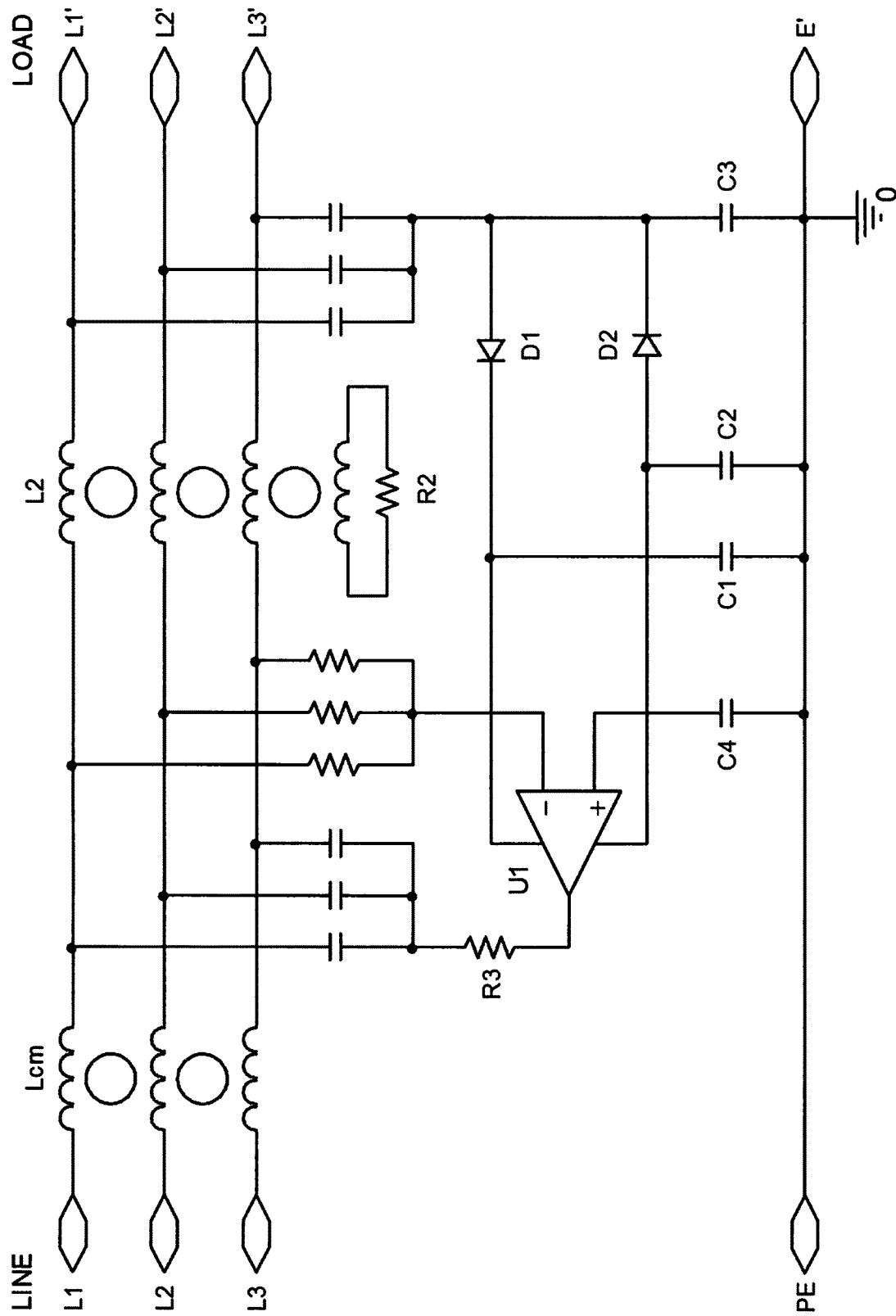


Figure 7

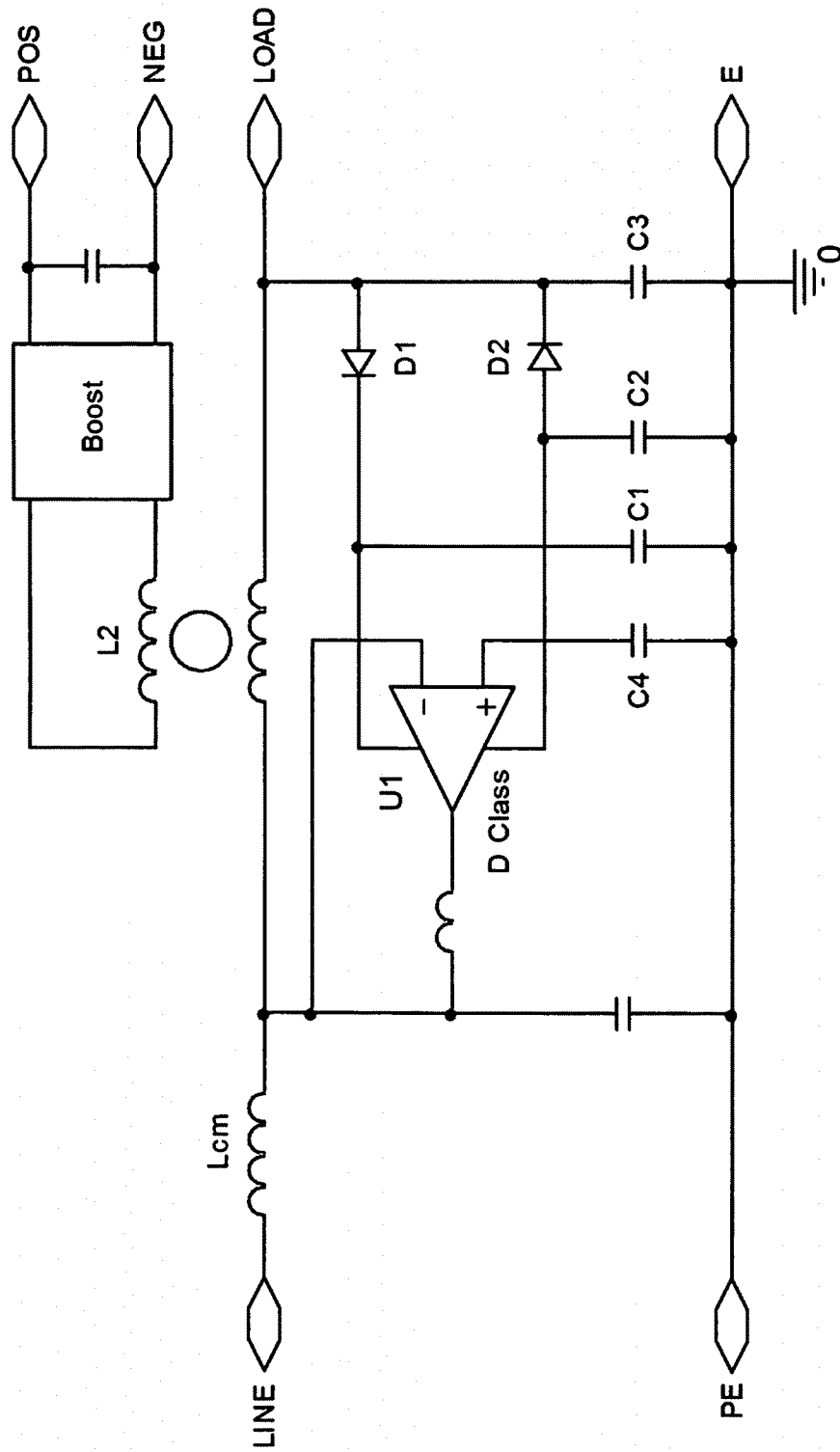


Figure 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2016/063630

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03H7/01 H02M1/12
ADD. H02H9/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03H H02M H02J H02H H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data, COMPENDEX, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2002/105233 A1 (VICE MICHAEL WENDELL [US]) 8 August 2002 (2002-08-08) figures 18-24 -----	1-19
A	EP 1 404 013 A1 (SIEMENS AG [DE]) 31 March 2004 (2004-03-31) figure 3 -----	1-19
A	FR 2 675 320 A1 (ALCATEL CABLE [FR]) 16 October 1992 (1992-10-16) figure 1 -----	1-19
A	US 4 434 396 A (MONTAGUE HERBERT R [US]) 28 February 1984 (1984-02-28) figures 1,2 -----	1-19



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

2 September 2016

Date of mailing of the international search report

12/09/2016

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Radomirescu, B-M

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2016/063630

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2002105233	A1	08-08-2002	NONE
EP 1404013	A1	31-03-2004	NONE
FR 2675320	A1	16-10-1992	NONE
US 4434396	A	28-02-1984	NONE