

(43) International Publication Date  
7 November 2013 (07.11.2013)

- (51) **International Patent Classification:**  
*H01F 27/28* (2006.01) *H01F 17/00* (2006.01)
- (21) **International Application Number:**  
PCT/US2013/037173
- (22) **International Filing Date:**  
18 April 2013 (18.04.2013)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**  
13/463,257 3 May 2012 (03.05.2012) US
- (71) **Applicant:** QUALCOMM MEMS TECHNOLOGIES, INC. [US/US]; ATTN: International IP Administration, 5775 Morehouse Drive, San Diego, California 92121-1714 (US).
- (72) **Inventors:** LO, Chi Shun; 5775 Morehouse Drive, San Diego, California 92121 (US). KIM, Jonghae; 5775 Morehouse Drive, San Diego, California 92121 (US). ZUO, Chengjie; 5775 Morehouse Drive, San Diego, California 92121 (US). YUN, Changhan Hobie; 5775 Morehouse Drive, San Diego, California 92121 (US).
- (74) **Agents:** DONNELLY, Kevin M. et al.; Weaver Austin Villeneuve & Sampson LLP, P. O. Box 70250, Oakland, California 94612-0250 (US).
- (81) **Designated States** (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM,

AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

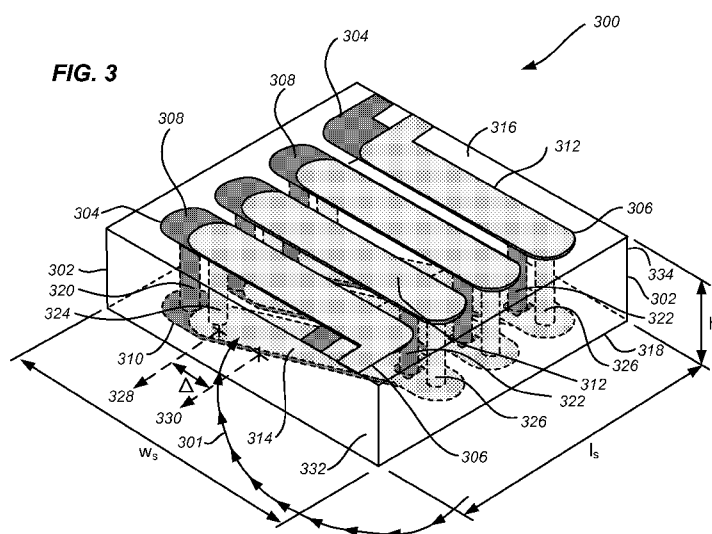
- (84) **Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**Declarations under Rule 4.17:**

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

**Published:**

- *with international search report (Art. 21(3))*

(54) **Title:** THREE-DIMENSIONAL MULTILAYER SOLENOID TRANSFORMER

(57) **Abstract:** This disclosure provides implementations of inductors, transformers, and related processes. In one aspect, a device includes a substrate having first and second surfaces. A first inducting arrangement includes a first set of vias, a second set of vias, a first set of traces arranged over the first surface connecting the first and second vias, and a second set of traces arranged over the second surface connecting the first and second vias. A second inducting arrangement is inductively-coupled and interleaved with the first inducting arrangement and includes a third set of vias, a fourth set of vias, a third set of traces arranged over the first surface connecting the third and fourth vias, and a fourth set of traces arranged over the second surface connecting the third and fourth vias. One or more sets of dielectric layers insulate portions of the traces from one another.

# THREE-DIMENSIONAL MULTILAYER SOLENOID TRANSFORMER

## RELATED APPLICATIONS

5     **[0001]**     This disclosure claims the benefit of priority of co-pending U.S. Patent Application No. 13/463,257, entitled “THREE-DIMENSIONAL MULTILAYER SOLENOID TRANSFORMER”, by Lo et al., filed on May 3, 2012 (Attorney Docket No. 112986/QUALP119), which is hereby incorporated by reference in its entirety and for all purposes.

## 10 TECHNICAL FIELD

**[0002]** The described technology relates generally to inductors and transformers, and more specifically to a three-dimensional solenoid transformer that includes a multilayer interleaving scheme.

## DESCRIPTION OF THE RELATED TECHNOLOGY

15    **[0003]**    Electromechanical systems (EMS) include devices having electrical and  
mechanical elements, transducers such as actuators and sensors, optical components  
(including mirrors), and electronics. EMS can be manufactured at a variety of scales  
including, but not limited to, microscales and nanoscales. For example,  
microelectromechanical systems (MEMS) devices can include structures having sizes  
20    ranging from about one micron to hundreds of microns or more.

Nanoelectromechanical systems (NEMS) devices can include structures having sizes smaller than one micron including, for example, sizes smaller than several hundred nanometers. Electromechanical elements may be created using deposition, etching, lithography, or other micromachining processes that etch away parts of substrates or deposited material layers, or that add layers to form electrical, mechanical, and electromechanical devices.

**[0004]** One type of EMS device is called an interferometric modulator (IMOD). As used herein, the term IMOD or interferometric light modulator refers to a device that selectively absorbs or reflects light using the principles of optical interference. In some implementations, an IMOD may include a pair of conductive plates, one or both

of which may be transparent or reflective, wholly or in part, and capable of relative motion upon application of an appropriate electrical signal. In an implementation, one plate may include a stationary layer deposited on a substrate and the other plate may include a reflective membrane separated from the stationary layer by an air gap.

- 5 The position of one plate in relation to another can change the optical interference of light incident on the IMOD. IMOD devices have a wide range of applications, and are anticipated to be used in improving existing products and creating new products, especially those with display capabilities.

- [0005] Various electronic circuit components can be implemented at the EMS  
10 level, including inductors and transformers. Such circuit components may be suitable for use in various types of electronic devices, such as integrated circuits (ICs), integrated passive devices, printed circuit boards (PCBs), or low temperature co-fired ceramic (LTCC) devices. A transformer can transfer electrical energy from one circuit to another through inductively-coupled coils or windings. For example, in a  
15 traditional design, a varying current,  $I_p$ , in a primary coil induces a voltage,  $V_s$ , in a secondary coil. When a load is connected to the secondary coil, electrical energy can be transferred through the coils to the load. The induced voltage,  $V_s$ , in the second coil is generally proportional to a voltage,  $V_p$ , delivered to the first coil and is given by the ratio of the number of turns (windings) in the second coil,  $N_s$ , to the number of  
20 turns in the first coil,  $N_p$ . This transformation ratio is generally defined as follows:

$$V_s/V_p = N_s/N_p$$

- [0006] In some modern circuits, small form factor transformers are specified. Conventional transformers made of relatively large metal spiral inductors often do not meet such specifications, especially as devices become increasingly smaller and  
25 power requirements become increasingly important. Transformers suitable for use in some IC devices may be implemented using high-resistivity substrates, such as glass substrates. Generally, transformers incorporating such substrates can be implemented as planar transformers or as solenoid transformers. Traditional solenoid transformers generally have higher quality (Q) factors than planar transformers, but traditional  
30 solenoid transformers may have coupling coefficients ( $k$ ) not suitable for use in modern circuits. While planar transformers generally have higher  $k$  values than solenoid transformers, planar transformers may have Q factors not suitable for use in

modern circuits. Additionally, a fundamental bottleneck exists when attempting to increase the  $k$  value —the pitch of the through-glass-via (TGV).

### SUMMARY

[0007] The structures, devices, apparatus, systems, and processes of the disclosure each have several innovative aspects, no single one of which is solely responsible for the desirable attributes disclosed herein.

[0008] Disclosed are example implementations of inductors, transformers, devices, apparatus, systems, and related fabrication processes.

[0009] According to one innovative aspect of the subject matter described in this disclosure, a device includes a substrate having a first surface and a second surface. The device includes a first inducting arrangement including a plurality of first conductive pathways that together form a first conductive path. The first conductive path has a first axis of revolution. In some implementations, the plurality of first conductive pathways includes a first set of vias extending at least from the first surface to the second surface, a second set of vias extending at least from the first surface to the second surface, a first set of traces arranged over the first surface that connect the first set of vias with the second set of vias, and a second set of traces arranged over the second surface that connect the first set of vias with the second set of vias. The device also includes a second inducting arrangement inductively-coupled with and interleaved with the first inducting arrangement and including a plurality of second conductive pathways that together form a second conductive path. The second conductive path has a second axis of revolution, at least part of the first axis of revolution being inside the second inducting arrangement, the second axis of revolution being inside the first inducting arrangement. In some implementations, the plurality of second conductive pathways includes a third set of vias extending at least from the first surface to the second surface, a fourth set of vias extending at least from the first surface to the second surface, a third set of traces arranged over the first surface that connect the third set of vias with the fourth set of vias, and a fourth set of traces arranged over the second surface that connect the third set of vias with the fourth set of vias. The device also includes a first set of one or more dielectric layers that insulate portions of the first traces from portions of the third traces, and a second set of one or more dielectric layers that insulate portions of the second traces from portions of the fourth traces.

[0010] In some implementations, the first set of vias are arranged along a first row and the second set of vias are arranged along a second row, each of the first set of traces connecting a via from the first row with a via from the second row over the first surface, each of the second set of traces connecting a via from the first row with a via from the second row over the second surface. In some implementations, the third set of vias are arranged along a third row and the fourth set of vias are arranged along a fourth row, each of the third set of traces connecting a via from the third row with a via from the fourth row over the third surface, each of the fourth set of traces connecting a via from the third row with a via from the fourth row over the second surface.

[0011] In some implementations, the first set of traces are formed from a first conductive layer deposited and patterned on the first surface and the first set of one or more dielectric layers that insulate portions of the first set of traces from portions of the third set of traces include a first dielectric layer deposited and patterned over the first surface so as to cover portions of the first set of traces. In some implementations, the third set of traces are formed from a third conductive layer deposited and patterned over the first dielectric layer. In some implementations, the second set of traces are formed from a second conductive layer deposited and patterned on the second surface and the second set of one or more dielectric layers that insulate portions of the second set of traces from portions of the fourth set of traces include a second dielectric layer deposited and patterned over the second surface so as to cover portions of the second set of traces. In some implementations, the fourth set of traces are formed from a fourth conductive layer deposited and patterned over the second dielectric layer.

[0012] In some implementations, the first set of traces are formed from a first conductive layer deposited and patterned on the first surface and the one or more dielectric layers that insulate portions of the first traces from portions of the third traces include a first dielectric layer deposited and patterned over the first surface so as to cover portions of the first set of traces. In some implementations, the third set of traces are formed from a third conductive layer deposited and patterned over the first dielectric layer. In some implementations, the fourth set of traces are formed from a fourth conductive layer deposited and patterned on the second surface and the one or more dielectric layers that insulate portions of the second traces from portions of the

fourth traces include a second dielectric layer deposited and patterned over the second surface so as to cover portions of the fourth set of traces. In some implementations, the second set of traces are formed from a second conductive layer deposited and patterned over the second dielectric layer.

5    **[0013]**     In some implementations, the plurality of first conductive pathways are arranged entirely within a region that is within the plurality of second conductive pathways. In some implementations, the first axis of revolution is laterally offset from the second axis of revolution. In some implementations, an effective number of turns of the first conductive pathways and an effective number of turns of the second  
10   conductive pathways are substantially equal as a result of the lateral offset such that the first inducting arrangement is inductively-coupled with the second inducting arrangement with a transformation ratio of substantially 1:1.

**[0014]**     According to another innovative aspect of the subject matter described in this disclosure, a method includes providing a substrate; forming a plurality of vias in  
15   the substrate that each extend through the substrate from a first surface of the substrate to a second surface of the substrate, the plurality of vias including a first set of vias, a second set of vias, a third set of vias, and a fourth set of vias; depositing a first conductive layer over the first surface of the substrate to form a first set of traces that each connect a via from the first set of vias with a via from the second set of vias;  
20   depositing one or more first dielectric layers over portions of the first traces; depositing a third conductive layer over the first dielectric layers to form a third set of traces that each connect a via from the third set of vias with a via from the fourth set of vias; depositing a fourth conductive layer over the second surface of the substrate to form a fourth set of traces that each connect a via from the third set of vias with a  
25   via from the fourth set of vias; depositing one or more second dielectric layers over portions of the fourth traces; and depositing a second conductive layer over the second dielectric layers to form a second set of traces that each connect a via from the first set of vias with a via from the second set of vias.

**[0015]**     In some implementations, the first set of vias, the second set of vias, the  
30   first set of traces, and the second set of traces form at least a portion of a first inducting arrangement including a plurality of first conductive pathways that together form a first conductive path, the first conductive path having a first axis of revolution. In some implementations, the third set of vias, the fourth set of vias, the third set of

traces, and the fourth set of traces form at least a portion of a second inducting arrangement including a plurality of second conductive pathways that together form a second conductive path, the second conductive path having a second axis of revolution. In some implementations, the second inducting arrangement is inductively-coupled with and interleaved with the first inducting arrangement. In some implementations, the first axis of revolution is inside the second inducting arrangement and the second axis of revolution is inside the first inducting arrangement. In some implementations, the first axis of revolution is laterally offset from the second axis of revolution. In some implementations, an effective number of turns of the first conductive pathways and an effective number of turns of the second conductive pathways are substantially equal as a result of the lateral offset such that the first inducting arrangement is inductively-coupled with the second inducting arrangement with a transformation ratio of substantially 1:1.

**[0016]** According to another innovative aspect of the subject matter described in this disclosure, a device includes a substrate having a first surface and a second surface. The device includes a first inducting means including a plurality of first conductive pathways that together form a first conductive path, the first conductive path having a first axis of revolution. The plurality of first conductive pathways includes a first set of via means extending at least from the first surface to the second surface, a second set of via means extending at least from the first surface to the second surface, a first set of conductive means arranged over the first surface that connect the first set of via means with the second set of via means, and a second set of conductive means arranged over the second surface that connect the first set of via means with the second set of via means. The device also includes a second inducting means inductively-coupled with and interleaved with the first inducting means and including a plurality of second conductive pathways that together form a second conductive path, the second conductive path having a second axis of revolution. In some implementations, at least part of the first axis of revolution is inside the second inducting means, and the second axis of revolution is inside the first inducting means. The plurality of second conductive pathways includes a third set of via means extending at least from the first surface to the second surface, a fourth set of via means extending at least from the first surface to the second surface, a third set of conductive means arranged over the first surface that connect the third set of via

means with the fourth set of via means, and a fourth set of conductive means arranged over the second surface that connect the third set of via means with the fourth set of via means. The device also includes a first set of one or more dielectric means that insulate portions of the first conductive means from portions of the third conductive means, and a second set of one or more dielectric means that insulate portions of the second conductive means from portions of the fourth conductive means.

### BRIEF DESCRIPTION OF THE DRAWINGS

[0017] Figure 1 shows an axonometric view of a planar transformer design in which the windings of the first inductor are interleaved with the windings of the second inductor on a surface of a substrate.

[0018] Figure 2 shows an axonometric view, including hidden lines, of a solenoid transformer design in which the windings of the first inductor are interleaved with the windings of the second inductor within and on a substrate.

[0019] Figure 3 shows an axonometric view, including hidden lines, of an example solenoid transformer design in which the windings of the first inductor are three-dimensionally interleaved with the windings of the second inductor.

[0020] Figure 4A shows a top view, including hidden lines, of a first inductor of the example solenoid transformer design of Figure 3.

[0021] Figure 4B shows a top view, including hidden lines, of a second inductor of the example solenoid transformer design of Figure 3.

[0022] Figure 5 shows a cross-sectional side view depiction of an example solenoid transformer design, such as the transformer design of Figure 3, in which one or more dielectric layers insulate the first inductor from the second inductor.

[0023] Figure 6 shows plots of the coupling coefficient  $k$  as a function of an applied frequency in GHz obtained from simulations using the transformer designs shown in Figures 1, 2, and 3.

[0024] Figure 7 shows plots of the Q factor as a function of an applied frequency in GHz obtained from simulations using the transformer designs shown in Figures 1, 2, and 3.

[0025] Figure 8 shows an axonometric view, including hidden lines, of an example solenoid transformer design in which the windings of the first inductor are three-dimensionally interleaved with and arranged within the windings of the second inductor.



[0026] Figure 9A shows a top view, including hidden lines, of a first inductor of the example solenoid transformer design of Figure 8.

[0027] Figure 9B shows a top view, including hidden lines, of a second inductor of the example solenoid transformer design of Figure 8.

5 [0028] Figure 10 shows a cross-sectional side view depiction of an example solenoid transformer design, such as the transformer design of Figure 8, in which one or more dielectric layers insulate the first inductor from the second inductor.

[0029] Figure 11A shows a top view, including hidden lines, of a first inductor of another example solenoid transformer design in which the first inductor is three-  
10 dimensionally interleaved with and arranged within the second inductor.

[0030] Figure 11B shows a top view, including hidden lines, of the second inductor of the example solenoid transformer design of Figure 11A.

[0031] Figure 12 is a flow diagram depicting an example process for forming a transformer such as the transformer of Figure 3.

15 [0032] Figure 13 is a flow diagram depicting an example process for forming a transformer such as the transformer of Figure 8.

[0033] Figure 14A shows an isometric view depicting two adjacent example pixels in a series of pixels of an example IMOD display device.

[0034] Figure 14B shows an example system block diagram depicting an example  
20 electronic device incorporating an IMOD display.

[0035] Figures 15A and 15B show examples of system block diagrams depicting an example display device that includes a plurality of IMODs.

[0036] Like reference numbers and designations in the various drawings indicate like elements.

25

## DETAILED DESCRIPTION

[0037] The following detailed description is directed to certain implementations for the purposes of describing the innovative aspects. However, the teachings herein can be applied and implemented in a multitude of different ways.

[0038] The disclosed implementations include examples of inducting  
30 arrangements (hereinafter simply “inductors”) and transforming arrangements (hereinafter simply “transformers”) that achieve both high  $Q$  factors and high  $k$

values. Related apparatus, systems, and fabrication processes and techniques are also disclosed.

[0039] Transformers with high  $Q$  factors and high  $k$  are desirable for many applications, such as those involving impedance matching, and for many devices, such as baluns, filters, and duplexers. Some planar and solenoid transformer designs achieve higher  $k$  by interleaving the conductive windings of a first inductor of the transformer with the conductive windings of a second inductor of the transformer. Figure 1 shows an axonometric view of a planar transformer design 100 in which the windings of the first inductor 104 are interleaved with the windings of the second inductor 106 on a surface of a substrate 102. The windings of the first inductor 104 are formed with first conductive traces 108. The windings of the second inductor 106 are formed with second conductive traces 110. Both the first traces 108 and the second traces 110 are patterned or arranged over a single upper surface 116 of the underlying substrate 102. Arrows 101 indicate magnetic ( $H$ ) field lines; that is, a direction of the  $H$  field by and through the inductors 104 and 106.

[0040] Figure 2 shows an axonometric view, including hidden lines, of a solenoid transformer design 200 in which the windings of the first inductor 204 are interleaved with the windings of the second inductor 206 within and on a substrate 202. The substrate 202 has a first surface 216 and a second surface 218 opposite the first surface 216. The first inductor 204 includes a plurality of first conductive pathways or windings that together form a first conductive path. The plurality of first conductive pathways includes a first set of vias 220 extending from the first surface 216 to the second surface 218 and a second set of vias 222 extending from the first surface 216 to the second surface 218. The plurality of first conductive pathways includes a first set of traces 208 arranged over the first surface 216 that connect the first set of vias 220 with the second set of vias 222. The plurality of first conductive pathways further includes second set of traces 210 arranged over the second surface 218 that connect the first set of vias 220 with the second set of vias 222.

[0041] Similarly the second inductor 206 includes a plurality of second conductive pathways or windings that together form a second conductive path. The plurality of second conductive pathways includes a third set of vias 224 extending from the first surface 216 to the second surface 218 and a fourth set of vias 226 extending from the first surface 216 to the second surface 218. The plurality of

second conductive pathways includes a third set of traces 212 arranged over the first surface 216 that connect the third set of vias 224 with the fourth set of vias 226. The plurality of second conductive pathways further includes a fourth set of traces 214 arranged over the second surface 218 that connect the third set of vias 224 with the fourth set of vias 226.

[0042] As shown, the first conductive pathways or windings are interleaved with the second conductive pathways or windings. More specifically, the first set of vias 220 and the third set of vias 224 are arranged in a first row while the second set of vias 222 and the fourth set of vias 226 are arranged in a second row parallel to the first row. The first, second, third, and fourth sets of vias 220, 222, 224, and 226, respectively, are positioned to enable the first set of traces 208 to be two-dimensionally interleaved with the third set of traces 212 such that the first set of traces 208 and the third set of traces 212 are arranged in alternating fashion along the first surface 216. Similarly, the first, second, third, and fourth sets of vias 220, 222, 224, and 226, respectively, are positioned to enable the second set of traces 210 to be two-dimensionally interleaved with the fourth set of traces 214 such that the second set of traces 210 and the fourth set of traces 214 are arranged in alternating fashion along the second surface 218. In such a design, the first conductive pathways and the second conductive pathways share an axis of revolution 228 that passes through first and second side surfaces 232 and 234. Arrows 201 indicate an H field line; that is, a direction of the H field by and through the inductors 204 and 206.

[0043] Figure 3 shows an axonometric view, including hidden lines, of an example solenoid transformer design 300 in which the windings of the first inductor 304 are three-dimensionally interleaved with the windings of the second inductor 306. Figure 4A shows a top view, including hidden lines, of a first inductor of the example solenoid transformer design of Figure 3. Figure 4B shows a top view, including hidden lines, of a second inductor of the example solenoid transformer design of Figure 3. Arrows 301 indicate the H field lines; that is, the direction of the H field by and through the inductors 304 and 306. The substrate 302 has a first surface 316 and a second surface 318 opposite the first surface 316. The first inductor 304 includes a plurality of first conductive pathways that together form a first conductive path. The plurality of first conductive pathways includes a first set of vias 320 extending from at least the first surface 316 to at least the second surface 318 and a second set of vias

322 extending from at least the first surface 316 to at least the second surface 318.

The plurality of first conductive pathways includes a first set of traces 308 arranged over the first surface 316 that connect the first set of vias 320 with the second set of vias 322. The plurality of first conductive pathways further includes a second set of traces 310 arranged over the second surface 318 that connect the first set of vias 320 with the second set of vias 322.

[0044] Similarly, the second inductor 306 includes a plurality of second conductive pathways that together form a second conductive path. The plurality of second conductive pathways includes a third set of vias 324 extending from at least the first surface 316 to at least the second surface 318 and a fourth set of vias 326 extending from at least the first surface 316 to at least the second surface 318. The plurality of second conductive pathways includes a third set of traces 312 arranged over the first surface 316 that connect the third set of vias 324 with the fourth set of vias 326. The plurality of second conductive pathways further includes a fourth set of traces 314 arranged over the second surface 318 that connect the third set of vias 324 with the fourth set of vias 326.

[0045] There is an angle  $\theta$  between the first traces 308 and the second traces 310. In some implementations, the same angle or a different angle  $\theta$  also can be between the third traces 312 and the fourth traces 314. The angle  $\theta$  can be any suitable angle to achieve the desired inductance or other electrical characteristics. In some implementations, the angle  $\theta$  can be as small as the pitch of the traces or process flows permits. The first, second, third, and fourth sets of vias 320, 322, 324, and 326, respectively, are positioned to enable the first set of traces 308 and the third set of traces 312 to be arranged in an overlying but electrically isolated fashion along the first surface 316 and to enable the second set of traces 310 and the fourth set of traces 314 to be arranged in an overlying but electrically isolated fashion along the second surface 318.

[0046] Figure 5 shows a cross-sectional side view depiction of an example solenoid transformer design, such as the transformer design 300 of Figure 3, in which one or more dielectric layers insulate the first inductor 304 from the second inductor 306. More specifically, one or more dielectric layers 336 insulate portions of the first traces 308 from portions of the third traces 312 over the first surface 316. Similarly, one or more second dielectric layers 338 insulate portions of the second traces 310

from portions of the fourth traces 314 over the second surface 318, as Figure 5 shows. The dielectric layers 336 enable the third traces 312 to overlay—but be insulated from—the first traces 308 over the first surface 316, while the dielectric layers 338 enable the second traces 310 to overlie—but be insulated from—the fourth traces 314 over the second surface 318, as Figure 5 shows. An advantageous result of such an implementation is that the pitch of the vias and traces can be doubled.

[0047] As shown in Figures 3–5, the first conductive pathways are three-dimensionally interleaved with the second conductive pathways. In some implementations, the first set of vias 320 is arranged in a first row and the second set of vias 322 is arranged in a second row. In some implementations, the first row of vias 320 is parallel to the second row of vias 322. In some implementations, the third set of vias 324 is arranged in a third row and the fourth set of vias 326 is arranged in a fourth row. In some implementations, the third row of vias 324 is approximately parallel to the fourth row of vias 326. In some implementations, the first row of vias 320 is approximately parallel to the third row of vias 324, and the second row of vias 322 is approximately parallel to the fourth row of vias 326.

[0048] In some implementations, the first conductive pathways can have a first axis of revolution 328 that passes through the first and second side surfaces 332 and 334. The second conductive pathways can have a second axis of revolution 330 that passes through the first and second side surfaces 332 and 334. In some implementations, the first axis of revolution 328 is laterally offset from the second axis of revolution 330. For example, the lateral offset  $\Delta$  can be any suitable length to achieve the desired inductance or other electrical characteristics. In some implementations, the lateral offset can approximately match the pitch of the traces or the combined distance of the width of a trace and the width of the dielectric between the trace and the immediately neighboring trace. One or more of these distances also can be as small as process flows permit.

[0049] In some implementations, when the length of each first conductive pathway—the sum of the lengths of a first trace 308, a second trace 310, a first via 320, and a second via 322—is substantially equal to the length of each second conductive pathway—the sum of the lengths of a third trace 312, a fourth trace 314, a third via 324, and a fourth via 326—a ratio of the number of first conductive pathways to the number of second conductive pathways can characterize a

transformation ratio of the transformer 300. That is, in some implementations, a ratio of the number of first conductive pathways—an effective number of turns of the first inductor—to the number of second conductive pathways—an effective number of turns of the second inductor—can characterize a transformation ratio of the

5 transformer 300. The lateral offset  $\Delta$  can enable a transformation ratio of 1:1 because the offset is also reflected in an offset in the first and third rows of vias and an offset in the second and fourth rows of vias. These offsets enable the length of each first conductive pathway to be equal to the length of each second conductive pathway.

[0050] In some other implementations, the first conductive pathways can have  
10 lengths different than the lengths of the second conductive pathways enabling a different transformation ratio. In some other implementations, the number of first conductive pathways can be different than the number of second conductive pathways enabling a different transformation ratio. For example, in some implementations, the number of first conductive pathways—an effective number of turns of the first  
15 inductor—can be in the range of one to ten or more. Similarly, the number of second conductive pathways—an effective number of turns of the second inductor—can be in the range of one to ten or more.

[0051] In such a three-dimensional implementation, because the first traces 308 and the third traces 312 are patterned in different respective layers of a multilayer  
20 structure over the first surface 316, and because the second traces 310 and the fourth traces 314 are patterned in different respective layers of a multilayer structure over the opposing second surface 318, each of the inductively-coupled first and second conductive paths of the first and second inductors 304 and 306, respectively, can occupy substantially the same footprint or area (save for the width between the first  
25 and third rows of vias 320 and 324 and the width between the second and fourth sets of vias 322 and 326). Because the windings of each of the first and second conductors 304 and 306 can occupy substantially the same footprint, the length of the device from surface 332 to 334 can be reduced by a factor of two. As a result, the total footprint required by the transformer 300 can potentially be reduced by  
30 approximately a factor of 2 as compared with, for example, the transformer 200 of figure 2.

[0052] Furthermore, the coupling coefficient  $k$  of the transformer 300 can be increased over that of, for example, transformers 100 and 200 of Figures 1 and 2,

respectively. Figure 6 shows plots  $k_1$ ,  $k_2$ , and  $k_3$  of the coupling coefficient  $k$  as a function of an applied frequency in GHz obtained from simulations using the transformer designs 100, 200, and 300, respectively, shown in Figures 1, 2, and 3, respectively. In some implementations, the transformer design 300 achieves a value of  $k$  in the range of approximately 0.6 to approximately 0.8. Figure 7 shows plots Q1, Q2, and Q3 of the Q factor as a function of an applied frequency in GHz obtained from simulations using the transformer designs 100, 200, and 300, respectively, shown in Figures 1, 2, and 3, respectively. In some implementations, the transformer design 300 achieves a Q factor in the range of approximately 60 to approximately 100. In some implementations, the transformer design 300 can achieve these  $k$  and Q factor values in half the footprint surface area of a transformer design 100 that only achieves a  $k$  value in the range of approximately 0.4 to 0.5 and a Q factor in the range of approximately 5 to approximately 20. In some implementations, the transformer design 300 can achieve these  $k$  and Q factor values with half the footprint surface area of a transformer design 200 that only achieves a  $k$  value in the range of approximately 0.4 to 0.5 and a Q factor in the range of approximately 60 to approximately 100.

**[0053]** Figure 8 shows an axonometric view, including hidden lines, of an example solenoid transformer 800 design in which the windings of the first inductor 804 are three-dimensionally interleaved with and arranged within the windings of the second inductor 806. In particular, the entire first conductive path of the first inductor 804 is arranged within a region around which is arranged the second conductive path of the second conductor 806. Arrows 1001 indicate the H field lines; that is, the direction of the H field by and through the inductors 804 and 806.

**[0054]** The substrate 802 has a first surface 816 and a second surface 818 opposite the first surface 816. The first inductor 804 includes a plurality of first conductive pathways that together form a first conductive path. The plurality of first conductive pathways includes a first set of vias 820 extending from at least the first surface 816 to at least the second surface 818 and a second set of vias 822 extending from at least the first surface 816 to at least the second surface 818. The plurality of first conductive pathways includes a first set of traces 808 arranged over the first surface 816 that connect the first set of vias 820 with the second set of vias 822. The plurality of first conductive pathways further includes a second set of traces 810 arranged over

the second surface 818 that connect the first set of vias 820 with the second set of vias 822.

[0055] Similarly, the second inductor 806 includes a plurality of second conductive pathways that together form a second conductive path. The plurality of second conductive pathways includes a third set of vias 824 extending from at least the first surface 816 to at least the second surface 818 and a fourth set of vias 826 extending from at least the first surface 816 to at least the second surface 818. The plurality of second conductive pathways includes a third set of traces 812 arranged over the first surface 816 that connect the third set of vias 824 with the fourth set of vias 826. The plurality of second conductive pathways further includes a fourth set of traces 814 arranged over the second surface 818 that connect the third set of vias 824 with the fourth set of vias 826.

[0056] There is an angle  $\theta$  between the first traces 808 and the second traces 810. In some implementations, the same angle or a different angle  $\theta$  also can be between the third traces 812 and the fourth traces 814. The angle  $\theta$  can be any suitable angle to achieve the desired inductance or other electrical characteristics. In some implementations, the angle  $\theta$  can be as small as the pitch of the traces or process flows permits. The first, second, third, and fourth sets of vias 820, 822, 824, and 826, respectively, are positioned to enable the first set of traces 808 and the third set of traces 812 to be arranged in an overlying fashion along the first surface 816 and to enable the second set of traces 810 and the fourth set of traces 834 to be arranged in an overlying fashion along the second surface 818. Figure 9A shows a top view, including hidden lines, of the first inductor 804 of the example solenoid transformer design 800 of Figure 10. Figure 9B shows a top view, including hidden lines, of the second inductor 806 of the example solenoid transformer design 800 of Figure 8.

[0057] Figure 10 shows a cross-sectional side view depiction of an example solenoid transformer design, such as the transformer design 800 of Figure 8, in which one or more dielectric layers insulate the first inductor from the second inductor. More specifically, one or more dielectric layers 836 insulate portions of the first traces 808 from portions of the third traces 812 over the first surface 816. Similarly, one or more second dielectric layers 838 insulate portions of the second traces 810 from portions of the fourth traces 814 over the second surface 818. The dielectric layers 836 enable the third traces 812 to overlie—but be insulated from—the first traces 808



over the first surface 816, while the dielectric layers 838 enable the fourth traces 814 to overly—but be insulated from—the second traces 810 over the second surface 818.

[0058] In some implementations, the first conductive pathways can have a first axis of revolution 828 that passes through the first and second side surfaces 832 and 834. The second conductive pathways can have a second axis of revolution 830 that passes through the first and second side surfaces 832 and 834. In some implementations, the first axis of revolution 828 is collinear with the second axis of revolution 830. In some other implementations, the first axis of revolution 828 can be laterally offset from the second axis of revolution 830.

[0059] Figure 11A shows a top view, including hidden lines, of a first inductor 1104 of another example solenoid transformer design in which the first inductor 1104 is three-dimensionally interleaved with and arranged within the second inductor 1106. Figure 11B shows a top view, including hidden lines, of the second inductor 1106 of the example solenoid transformer design of Figure 11A. In Figures 11A and 11B, the first, second, third, and fourth traces 1108, 1110, 1112, and 1114, respectively, and the respective connecting vias can be arranged to enable a smaller angle  $\theta$  between the first traces 1108 and the second traces 1110 (the same angle  $\theta$  or a different angle  $\theta$  also can be between the third traces 1112 and the fourth traces 1114 in some implementations) which can result in more overlap of all the traces. For example, the first and second traces 1108 and 1110 can be rotated (as compared to first and second traces 808 and 810) by an angle  $\phi$  while third traces and fourth traces 1112 and 1114 can be rotated (as compared to third and fourth traces 1312 and 1314) by an angle  $\gamma$  (Similar modifications, although not illustrated, can be made to the design of Figure 3, for example, to enable more overlap).

[0060] Figure 12 is a flow diagram depicting an example process 1200 for forming a transformer such as the transformer design 300 of Figure 3. In some implementations, process 1200 begins in block 1202 with providing a substrate, such as substrate 302. In some implementations, first, second, third, and fourth rows of vias are formed in block 1204 through the substrate, such as vias 320, 322, 324, and 326. The vias can be plated or filled in block 1206 with a conductive layer to enable electrical conduction through the vias. In some implementations, a first conductive layer is then deposited or patterned in block 1208 on a first surface of the substrate so as to form first traces, such as first traces 308. For example, the traces can be formed

by physical vapor deposition (PVD) including thermal evaporation one or more metals or metallic alloys or sputtering one or more targets of one or more metals or metallic alloys followed by one or more lithographic techniques including, for example, photoresist patterning, etching, and photoresist, cleaning. The traces also  
5 can be formed by seed layer deposition followed by, for example, photoresist patterning, electro- or electroless-plating, photoresist cleaning, and seed layer removal.

[0061] In some implementations, process 1200 proceeds in block 1210 with depositing one or more dielectric layers over and around the first traces, such as  
10 dielectric layers 336. For example, the dielectric layers can be formed by one or more chemical vapor deposition (CVD) processes including, for example, low-pressure CVD (LPCVD) and plasma-enhanced CVD (PECVD). The deposited dielectric material (e.g., mostly oxide) can then be patterned to provide insulation where indicated and to allow for electrical connection to vias where indicated. In some  
15 implementations, process 1200 proceeds in block 1212 with depositing or patterning another conductive layer to form additional traces over the first traces, such as third traces 312. For example, the traces can be formed by any of the processes described above for forming the traces. In some implementations, additional dielectric or other layers also can be deposited over the additional traces (such as over the third traces  
20 312).

[0062] In some implementations, another conductive layer is then deposited or patterned in block 1214 on a second surface of the substrate opposite the first surface so as to form additional traces on the second surface, such as fourth traces 314. For example, the traces can be formed by any of the processes described above for  
25 forming the traces.

[0063] In some implementations, process 1200 proceeds in block 1216 with depositing one or more dielectric layers over and around these traces, such as dielectric layers 338. For example, the dielectric layers can be formed by any of the processes described above for forming dielectric layers. In some implementations,  
30 process 1200 proceeds in block 1218 with depositing or patterning another conductive layer to form additional traces over the traces previously patterned over the second surface, such as second traces 310. For example, the traces can be formed by any of the processes described above for forming traces. In some implementations,

additional dielectric or other layers also can be deposited over the additional traces (such as over the second traces 310).

[0064] Figure 13 is a flow diagram depicting an example process 1300 for forming a transformer such as the transformer design 800 of Figure 10. In some implementations, process 1300 begins in block 1302 with providing a substrate, such as substrate 802. In some implementations, first, second, third, and fourth rows of vias are formed in block 1304 through the substrate, such as vias 820, 822, 824, and 826. The vias can be plated or filled in block 1306 with a conductive layer to enable electrical conduction through the vias. In some implementations, a first conductive layer is then deposited or patterned in block 1308 on a first surface of the substrate so as to form first traces, such as first traces 808. For example, the traces can be formed by any of the processes described above for forming traces.

[0065] In some implementations, process 1300 proceeds in block 1310 with depositing one or more dielectric layers over and around the first traces, such as dielectric layers 836. For example, the dielectric layers can be formed by any of the processes described above for forming dielectric layers. In some implementations, process 1300 proceeds in block 1312 with depositing or patterning another conductive layer to form additional traces over the first traces, such as third traces 812. For example, the traces can be formed by any of the processes described above for forming traces. In some implementations, additional dielectric or other layers also can be deposited over the additional traces (such as over the third traces 812).

[0066] In some implementations, a second conductive layer is then deposited or patterned in block 1314 on a second surface of the substrate opposite the first surface so as to form additional traces on the second surface, such as second traces 814. For example, the traces can be formed by any of the processes described above for forming traces.

[0067] In some implementations, process 1300 proceeds in block 1316 with depositing one or more dielectric layers over and around these traces, such as dielectric layers 838. For example, the dielectric layers can be formed by any of the processes described above for forming dielectric layers. In some implementations, process 1300 proceeds in block 1318 with depositing or patterning another conductive layer to form additional traces over the second traces previously patterned over the second surface, such as fourth traces 814. For example, the traces can be formed by

any of the processes described above for forming traces. In some implementations, additional dielectric or other layers also can be deposited over the additional traces (such as over the fourth traces 814).

[0068] In some implementations, any of the substrates described above can be a high-resistivity semiconducting substrate. In some implementations, the substrate can have a length  $l_s$  in the range of approximately 100  $\mu\text{m}$  to approximately 5000  $\mu\text{m}$ , a width  $w_s$  in the range of approximately 100  $\mu\text{m}$  to approximately 5000  $\mu\text{m}$ , and a height or thickness  $h$  in the range of approximately 100  $\mu\text{m}$  to approximately 800  $\mu\text{m}$ .

[0069] In some implementations, the substrate can be made of display-grade glass (such as alkaline earth boro-aluminosilicate) or soda lime glass. Other suitable insulating materials include silicate glasses, such as alkaline earth aluminosilicate, borosilicate, or modified borosilicate. Also, ceramic materials such as aluminum oxide (AlOx), yttrium oxide (Y<sub>2</sub>O<sub>3</sub>), boron nitride (BN), silicon carbide (SiC), aluminum nitride (AlN), and gallium nitride (GaN<sub>x</sub>) also can be used in some implementations. In some other implementations, high-resistivity Si can be used. In some implementations, silicon on insulator (SOI) substrates, gallium arsenide (GaAs) substrates, indium phosphide (InP) substrates, and plastic (polyethylene naphthalate or polyethylene terephthalate) substrates, e.g., associated with flexible electronics, also can be used.

[0070] In some implementations, any of the vias described above can be produced by etching through the respective substrate. In some other implementations, the vias can be produced by micro-machining, drilling, or by other suitable means. In some implementations, one or more conductive layers are then plated or otherwise deposited on the surfaces of the vias such that the vias can conduct electric current from the respective ones of the traces on or over the first surface of the substrate to the respective ones of the traces on or over the second surface of the substrate. For example, in some implementations, the vias are plated with a conductive metal or metallic alloy. For example, the vias can be plated with nickel (Ni), aluminum (Al), copper (Cu), titanium (Ti), aluminum nitride (AlN), titanium nitride (TiN), aluminum copper (AlCu), molybdenum (Mo), aluminum silicon (AlSi), platinum (Pt), tungsten (W), ruthenium (Ru), or other appropriate or suitable materials or combinations thereof. In some implementations, the vias can have widths or diameters in the range of approximately 20  $\mu\text{m}$  to approximately 200  $\mu\text{m}$ , while the conductive layers within

the vias can have a thickness in the range of approximately 1  $\mu\text{m}$  to approximately 30  $\mu\text{m}$  or even fill the volume of the via entirely.

[0071] In some implementations, any of the traces described above can be produced by masking and sputtering or otherwise patterning and depositing one or more conductive layers. For example, in some implementations, the traces can be plated with or otherwise formed from nickel (Ni), aluminum (Al), copper (Cu), titanium (Ti), aluminum nitride (AlN), titanium nitride (TiN), aluminum copper (AlCu), molybdenum (Mo), aluminum silicon (AlSi), platinum (Pt), tungsten (W), ruthenium (Ru), or other appropriate or suitable materials or combinations thereof. In some implementations, the traces can have a length in the range of approximately 100  $\mu\text{m}$  to approximately 2000  $\mu\text{m}$ , a width in the range of approximately 20  $\mu\text{m}$  to approximately 300  $\mu\text{m}$ , and a thickness in the range of approximately 1  $\mu\text{m}$  to approximately 30  $\mu\text{m}$ .

[0072] In some implementations, any of the dielectric layers described above can be produced by masking, patterning, etching, or through other lithographic techniques. For example, in some implementations, the dielectric layers can be formed from silicon oxide ( $\text{SiO}_x$ ), silicon nitride ( $\text{SiN}_x$ ), or silicon oxy-nitride ( $\text{SiON}$ ). In some other implementations, the dielectric layers can be formed of polyimide or benzocyclobutene (BCB) or similar materials, which can be desirable as they don't require photoresists because they are already photo-patternable. In some implementations, the dielectric layers can have a thickness that is greater than or equal to the thickness of the adjacent traces.

[0073] The description herein is directed to certain implementations for the purposes of describing the innovative aspects of this disclosure. However, a person having ordinary skill in the art will readily recognize that the teachings herein can be applied in a multitude of different ways. The described implementations may be implemented in any device or system that can be configured to display an image, whether in motion (e.g., video) or stationary (e.g., still image), and whether textual, graphical or pictorial. More particularly, it is contemplated that the described implementations may be included in or associated with a variety of electronic devices such as, but not limited to: mobile telephones, multimedia Internet enabled cellular telephones, mobile television receivers, wireless devices, smartphones, Bluetooth® devices, personal data assistants (PDAs), wireless electronic mail receivers, hand-held

or portable computers, netbooks, notebooks, smartbooks, tablets, printers, copiers, scanners, facsimile devices, GPS receivers/navigators, cameras, MP3 players, camcorders, game consoles, wrist watches, clocks, calculators, television monitors, flat panel displays, electronic reading devices (i.e., e-readers), computer monitors, auto displays (including odometer and speedometer displays, etc.), cockpit controls and/or displays, camera view displays (such as the display of a rear view camera in a vehicle), electronic photographs, electronic billboards or signs, projectors, architectural structures, microwaves, refrigerators, stereo systems, cassette recorders or players, DVD players, CD players, VCRs, radios, portable memory chips, washers, dryers, washer/dryers, parking meters, packaging (such as in electromechanical systems (EMS), microelectromechanical systems (MEMS) and non-MEMS applications), aesthetic structures (e.g., display of images on a piece of jewelry) and a variety of EMS devices. The teachings herein also can be used in non-display applications such as, but not limited to, electronic switching devices, radio frequency filters, sensors, accelerometers, gyroscopes, motion-sensing devices, magnetometers, inertial components for consumer electronics, parts of consumer electronics products, varactors, liquid crystal devices, electrophoretic devices, drive schemes, manufacturing processes and electronic test equipment. Thus, the teachings are not intended to be limited to the implementations depicted solely in the Figures, but instead have wide applicability as will be readily apparent to one having ordinary skill in the art.

**[0074]** An example of a suitable EMS or MEMS device, to which the described implementations may apply, is a reflective display device. Reflective display devices can incorporate interferometric modulators (IMODs) to selectively absorb and/or reflect light incident thereon using principles of optical interference. IMODs can include an absorber, a reflector that is movable with respect to the absorber, and an optical resonant cavity defined between the absorber and the reflector. The reflector can be moved to two or more different positions, which can change the size of the optical resonant cavity and thereby affect the reflectance of the IMOD. The reflectance spectrums of IMODs can create fairly broad spectral bands which can be shifted across the visible wavelengths to generate different colors. The position of the spectral band can be adjusted by changing the thickness of the optical resonant cavity, i.e., by changing the position of the reflector.

[0075] Figure 14A shows an example of an isometric view depicting two adjacent pixels in a series of pixels of an IMOD display device. The IMOD display device includes one or more interferometric MEMS display elements. In these devices, the pixels of the MEMS display elements can be in either a bright or dark state. In the bright (“relaxed,” “open” or “on”) state, the display element reflects a large portion of incident visible light, e.g., to a user. Conversely, in the dark (“actuated,” “closed” or “off”) state, the display element reflects little incident visible light. In some implementations, the light reflectance properties of the on and off states may be reversed. MEMS pixels can be configured to reflect predominantly at particular wavelengths allowing for a color display in addition to black and white.

[0076] The IMOD display device can include a row/column array of IMODs. Each IMOD can include a pair of reflective layers, i.e., a movable reflective layer and a fixed partially reflective layer, positioned at a variable and controllable distance from each other to form an air gap (also referred to as an optical gap or cavity). The movable reflective layer may be moved between at least two positions. In a first position, i.e., a relaxed position, the movable reflective layer can be positioned at a relatively large distance from the fixed partially reflective layer. In a second position, i.e., an actuated position, the movable reflective layer can be positioned more closely to the partially reflective layer. Incident light that reflects from the two layers can interfere constructively or destructively depending on the position of the movable reflective layer, producing either an overall reflective or non-reflective state for each pixel. In some implementations, the IMOD may be in a reflective state when unactuated, reflecting light within the visible spectrum, and may be in a dark state when unactuated, reflecting light outside of the visible range (such as infrared light). In some other implementations, however, an IMOD may be in a dark state when unactuated, and in a reflective state when actuated. In some implementations, the introduction of an applied voltage can drive the pixels to change states. In some other implementations, an applied charge can drive the pixels to change states.

[0077] The depicted portion of the pixel array in Figure 14A includes two adjacent IMODs 12. In the IMOD 12 on the left (as illustrated), a movable reflective layer 14 is illustrated in a relaxed position at a predetermined distance from an optical stack 16, which includes a partially reflective layer. The voltage V0 applied across the IMOD 12 on the left is insufficient to cause actuation of the movable reflective

layer 14. In the IMOD 12 on the right, the movable reflective layer 14 is illustrated in an actuated position near or adjacent the optical stack 16. The voltage  $V_{bias}$  applied across the IMOD 12 on the right is sufficient to maintain the movable reflective layer 14 in the actuated position.

5 [0078] In Figure 14A, the reflective properties of pixels 12 are generally illustrated with arrows 13 indicating light incident upon the pixels 12, and light 15 reflecting from the IMOD 12 on the left. Although not illustrated in detail, it will be understood by one having ordinary skill in the art that most of the light 13 incident upon the pixels 12 will be transmitted through the transparent substrate 20, toward the  
10 optical stack 16. A portion of the light incident upon the optical stack 16 will be transmitted through the partially reflective layer of the optical stack 16, and a portion will be reflected back through the transparent substrate 20. The portion of light 13 that is transmitted through the optical stack 16 will be reflected at the movable reflective layer 14, back toward (and through) the transparent substrate 20.  
15 Interference (constructive or destructive) between the light reflected from the partially reflective layer of the optical stack 16 and the light reflected from the movable reflective layer 14 will determine the wavelength(s) of light 15 reflected from the IMOD 12.

[0079] The optical stack 16 can include a single layer or several layers. The  
20 layer(s) can include one or more of an electrode layer, a partially reflective and partially transmissive layer and a transparent dielectric layer. In some implementations, the optical stack 16 is electrically conductive, partially transparent and partially reflective, and may be fabricated, for example, by depositing one or more of the above layers onto a transparent substrate 20. The electrode layer can be  
25 formed from a variety of materials, such as various metals, for example indium tin oxide (ITO). The partially reflective layer can be formed from a variety of materials that are partially reflective, such as various metals, e.g., chromium (Cr), semiconductors, and dielectrics. The partially reflective layer can be formed of one or more layers of materials, and each of the layers can be formed of a single material or a  
30 combination of materials. In some implementations, the optical stack 16 can include a single semi-transparent thickness of metal or semiconductor which serves as both an optical absorber and conductor, while different, more conductive layers or portions (e.g., of the optical stack 16 or of other structures of the IMOD) can serve to bus



signals between IMOD pixels. The optical stack 16 also can include one or more insulating or dielectric layers covering one or more conductive layers or a conductive/absorptive layer.

[0080] In some implementations, the layer(s) of the optical stack 16 can be patterned into parallel strips, and may form row electrodes in a display device as described further below. As will be understood by one having skill in the art, the term “patterned” is used herein to refer to masking as well as etching processes. In some implementations, a highly conductive and reflective material, such as aluminum (Al), may be used for the movable reflective layer 14, and these strips may form column electrodes in a display device. The movable reflective layer 14 may be formed as a series of parallel strips of a deposited metal layer or layers (orthogonal to the row electrodes of the optical stack 16) to form columns deposited on top of posts 18 and an intervening sacrificial material deposited between the posts 18. When the sacrificial material is etched away, a defined gap 19, or optical cavity, can be formed between the movable reflective layer 14 and the optical stack 16. In some implementations, the separation between posts 18 may be approximately 1–800  $\mu\text{m}$ , while the gap 19 may be less than 10,000 Angstroms ( $\text{\AA}$ ).

[0081] In some implementations, each pixel of the IMOD, whether in the actuated or relaxed state, is essentially a capacitor formed by the fixed and moving reflective layers. When no voltage is applied, the movable reflective layer 14 remains in a mechanically relaxed state, as illustrated by the IMOD 12 on the left in Figure 14A, with the gap 19 between the movable reflective layer 14 and optical stack 16. However, when a potential difference, e.g., voltage, is applied to at least one of a selected row and column, the capacitor formed at the intersection of the row and column electrodes at the corresponding pixel becomes charged, and electrostatic forces pull the electrodes together. If the applied voltage exceeds a threshold, the movable reflective layer 14 can deform and move near or against the optical stack 16. A dielectric layer (not shown) within the optical stack 16 may prevent shorting and control the separation distance between the layers 14 and 16, as illustrated by the actuated IMOD 12 on the right in Figure 14A. The behavior is the same regardless of the polarity of the applied potential difference. Though a series of pixels in an array may be referred to in some instances as “rows” or “columns,” a person having ordinary skill in the art will readily understand that referring to one direction as a

“row” and another as a “column” is arbitrary. Restated, in some orientations, the rows can be considered columns, and the columns considered to be rows.

Furthermore, the display elements may be evenly arranged in orthogonal rows and columns (an “array”), or arranged in non-linear configurations, for example, having certain positional offsets with respect to one another (a “mosaic”). The terms “array” and “mosaic” may refer to either configuration. Thus, although the display is referred to as including an “array” or “mosaic,” the elements themselves need not be arranged orthogonally to one another, or disposed in an even distribution, in any instance, but may include arrangements having asymmetric shapes and unevenly distributed elements.

**[0082]** Figure 14B shows an example of a system block diagram depicting an electronic device incorporating a 3x3 IMOD display. The electronic device depicted in Figure 14B represents one implementation in which a piezoelectric resonator transformer constructed in accordance with the implementations described above with respect to Figures 1–13 can be incorporated. The electronic device in which device 11 is incorporated may, for example, form part or all of any of the variety of electrical devices and electromechanical systems devices set forth above, including both display and non-display applications.

**[0083]** Here, the electronic device includes a controller 21, which may include one or more general purpose single- or multi-chip microprocessors such as an ARM®, Pentium®, 8051, MIPS®, Power PC®, or ALPHA®, or special purpose microprocessors such as a digital signal processor, microcontroller, or a programmable gate array. Controller 21 may be configured to execute one or more software modules. In addition to executing an operating system, the controller 21 may be configured to execute one or more software applications, including a web browser, a telephone application, an email program, or any other software application.

**[0084]** The controller 21 is configured to communicate with device 11. The controller 21 also can be configured to communicate with an array driver 22. The array driver 22 can include a row driver circuit 24 and a column driver circuit 26 that provide signals to, e.g., a display array or panel 30. Although Figure 14B shows a 3x3 array of IMODs for the sake of clarity, the display array 30 may contain a very large number of IMODs, and may have a different number of IMODs in rows than in

columns, and vice versa. Controller 21 and array driver 22 may sometimes be referred to herein as being “logic devices” and/or part of a “logic system.”

[0085] Figures 15A and 15B show examples of system block diagrams depicting a display device 40 that includes a plurality of IMODs. The display device 40 can be, for example, a smart phone, a cellular or mobile telephone. However, the same components of the display device 40 or slight variations thereof are also illustrative of various types of display devices such as televisions, tablets, e-readers, hand-held devices and portable media players.

[0086] The display device 40 includes a housing 41, a display 30, an antenna 43, a speaker 45, an input device 48 and a microphone 46. The housing 41 can be formed from any of a variety of manufacturing processes, including injection molding, and vacuum forming. In addition, the housing 41 may be made from any of a variety of materials, including, but not limited to: plastic, metal, glass, rubber and ceramic, or a combination thereof. The housing 41 can include removable portions (not shown) that may be interchanged with other removable portions of different color, or containing different logos, pictures, or symbols.

[0087] The display 30 may be any of a variety of displays, including a bi-stable or analog display, as described herein. The display 30 also can be configured to include a flat-panel display, such as plasma, EL, OLED, STN LCD, or TFT LCD, or a non-flat-panel display, such as a CRT or other tube device. In addition, the display 30 can include an IMOD display, as described herein.

[0088] The components of the display device 40 are schematically illustrated in Figure 15B. The display device 40 includes a housing 41 and can include additional components at least partially enclosed therein. For example, the display device 40 includes a network interface 27 that includes an antenna 43 which is coupled to a transceiver 47. The transceiver 47 is connected to a processor 21, which is connected to conditioning hardware 52. The conditioning hardware 52 may be configured to condition a signal (e.g., filter a signal). The conditioning hardware 52 is connected to a speaker 45 and a microphone 46. The processor 21 is also connected to an input device 48 and a driver controller 29. The driver controller 29 is coupled to a frame buffer 28, and to an array driver 22, which in turn is coupled to a display array 30. In some implementations, a power supply 50 can provide power to substantially all components in the particular display device 40 design.

[0089] The network interface 27 includes the antenna 43 and the transceiver 47 so that the display device 40 can communicate with one or more devices over a network. The network interface 27 also may have some processing capabilities to relieve, for example, data processing requirements of the processor 21. The antenna 43 can  
5 transmit and receive signals. In some implementations, the antenna 43 transmits and receives RF signals according to the IEEE 16.11 standard, including IEEE 16.11(a), (b), or (g), or the IEEE 802.11 standard, including IEEE 802.11a, b, g, n, and further implementations thereof. In some other implementations, the antenna 43 transmits and receives RF signals according to the BLUETOOTH standard. In the case of a  
10 cellular telephone, the antenna 43 is designed to receive code division multiple access (CDMA), frequency division multiple access (FDMA), time division multiple access (TDMA), Global System for Mobile communications (GSM), GSM/General Packet Radio Service (GPRS), Enhanced Data GSM Environment (EDGE), Terrestrial Trunked Radio (TETRA), Wideband-CDMA (W-CDMA), Evolution Data Optimized  
15 (EV-DO), 1xEV-DO, EV-DO Rev A, EV-DO Rev B, High Speed Packet Access (HSPA), High Speed Downlink Packet Access (HSDPA), High Speed Uplink Packet Access (HSUPA), Evolved High Speed Packet Access (HSPA+), Long Term Evolution (LTE), AMPS, or other known signals that are used to communicate within a wireless network, such as a system utilizing 3G or 4G technology. The transceiver  
20 47 can pre-process the signals received from the antenna 43 so that they may be received by and further manipulated by the processor 21. The transceiver 47 also can process signals received from the processor 21 so that they may be transmitted from the display device 40 via the antenna 43.

[0090] In some implementations, the transceiver 47 can be replaced by a receiver. In addition, in some implementations, the network interface 27 can be replaced by an  
25 image source, which can store or generate image data to be sent to the processor 21. The processor 21 can control the overall operation of the display device 40. The processor 21 receives data, such as compressed image data from the network interface 27 or an image source, and processes the data into raw image data or into a format  
30 that is readily processed into raw image data. The processor 21 can send the processed data to the driver controller 29 or to the frame buffer 28 for storage. Raw data typically refers to the information that identifies the image characteristics at each

location within an image. For example, such image characteristics can include color, saturation and gray-scale level.

[0091] The processor 21 can include a microcontroller, CPU, or logic unit to control operation of the display device 40. The conditioning hardware 52 may include amplifiers and filters for transmitting signals to the speaker 45, and for receiving signals from the microphone 46. The conditioning hardware 52 may be discrete components within the display device 40, or may be incorporated within the processor 21 or other components.

[0092] The driver controller 29 can take the raw image data generated by the processor 21 either directly from the processor 21 or from the frame buffer 28 and can re-format the raw image data appropriately for high speed transmission to the array driver 22. In some implementations, the driver controller 29 can re-format the raw image data into a data flow having a raster-like format, such that it has a time order suitable for scanning across the display array 30. Then the driver controller 29 sends the formatted information to the array driver 22. Although a driver controller 29, such as an LCD controller, is often associated with the system processor 21 as a stand-alone Integrated Circuit (IC), such controllers may be implemented in many ways. For example, controllers may be embedded in the processor 21 as hardware, embedded in the processor 21 as software, or fully integrated in hardware with the array driver 22.

[0093] The array driver 22 can receive the formatted information from the driver controller 29 and can re-format the video data into a parallel set of waveforms that are applied many times per second to the hundreds, and sometimes thousands (or more), of leads coming from the display's x-y matrix of pixels.

[0094] In some implementations, the driver controller 29, the array driver 22, and the display array 30 are appropriate for any of the types of displays described herein. For example, the driver controller 29 can be a conventional display controller or a bi-stable display controller (such as an IMOD controller). Additionally, the array driver 22 can be a conventional driver or a bi-stable display driver (such as an IMOD display driver). Moreover, the display array 30 can be a conventional display array or a bi-stable display array (such as a display including an array of IMODs). In some implementations, the driver controller 29 can be integrated with the array driver 22.

Such an implementation can be useful in highly integrated systems, for example, mobile phones, portable-electronic devices, watches or small-area displays.

[0095] In some implementations, the input device 48 can be configured to allow, for example, a user to control the operation of the display device 40. The input device 5 48 can include a keypad, such as a QWERTY keyboard or a telephone keypad, a button, a switch, a rocker, a touch-sensitive screen, a touch-sensitive screen integrated with the display array 30, or a pressure- or heat-sensitive membrane. The microphone 46 can be configured as an input device for the display device 40. In some implementations, voice commands through the microphone 46 can be used for 10 controlling operations of the display device 40.

[0096] The power supply 50 can include a variety of energy storage devices. For example, the power supply 50 can be a rechargeable battery, such as a nickel-cadmium battery or a lithium-ion battery. In implementations using a rechargeable battery, the rechargeable battery may be chargeable using power coming from, for 15 example, a wall socket or a photovoltaic device or array. Alternatively, the rechargeable battery can be wirelessly chargeable. The power supply 50 also can be a renewable energy source, a capacitor, or a solar cell, including a plastic solar cell or solar-cell paint. The power supply 50 also can be configured to receive power from a wall outlet.

[0097] In some implementations, control programmability resides in the driver 20 controller 29 which can be located in several places in the electronic display system. In some other implementations, control programmability resides in the array driver 22. The above-described optimization may be implemented in any number of hardware and/or software components and in various configurations.

[0098] The various illustrative logics, logical blocks, modules, circuits and 25 algorithm steps described in connection with the implementations disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. The interchangeability of hardware and software has been described generally, in terms of functionality, and illustrated in the various illustrative components, blocks, 30 modules, circuits and steps described above. Whether such functionality is implemented in hardware or software depends upon the particular application and design constraints imposed on the overall system.

[0099] The hardware and data processing apparatus used to implement the various illustrative logics, logical blocks, modules and circuits described in connection with the aspects disclosed herein may be implemented or performed with a general purpose single- or multi-chip processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor may be a microprocessor, or, any conventional processor, controller, microcontroller, or state machine. A processor also may be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration. In some implementations, particular steps and methods may be performed by circuitry that is specific to a given function.

[00100] In one or more aspects, the functions described may be implemented in hardware, digital electronic circuitry, computer software, firmware, including the structures disclosed in this specification and their structural equivalents thereof, or in any combination thereof. Implementations of the subject matter described in this specification also can be implemented as one or more computer programs, i.e., one or more modules of computer program instructions, encoded on a computer storage media for execution by, or to control the operation of, data processing apparatus.

[00101] Various modifications to the implementations described in this disclosure may be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other implementations without departing from the spirit or scope of this disclosure. Thus, the claims are not intended to be limited to the implementations shown herein, but are to be accorded the widest scope consistent with this disclosure, the principles and the novel features disclosed herein. Additionally, a person having ordinary skill in the art will readily appreciate, the terms “upper” and “lower” are sometimes used for ease of describing the figures, and indicate relative positions corresponding to the orientation of the figure on a properly oriented page, and may not reflect the proper orientation of the IMOD as implemented.

**[00102]** Certain features that are described in this specification in the context of separate implementations also can be implemented in combination in a single implementation. Conversely, various features that are described in the context of a single implementation also can be implemented in multiple implementations

5 separately or in any suitable subcombination. Moreover, although features may be described above as acting in certain combinations and even initially claimed as such, one or more features from a claimed combination can in some cases be excised from the combination, and the claimed combination may be directed to a subcombination or variation of a subcombination.

10 **[00103]** Similarly, while operations are depicted in the drawings in a particular order, this should not be understood as requiring that such operations be performed in the particular order shown or in sequential order, or that all illustrated operations be performed, to achieve desirable results. Further, the drawings may schematically depict one more example processes in the form of a flow diagram. However, other

15 operations that are not depicted can be incorporated in the example processes that are schematically illustrated. For example, one or more additional operations can be performed before, after, simultaneously, or between any of the illustrated operations. In certain circumstances, multitasking and parallel processing may be advantageous. Moreover, the separation of various system components in the implementations

20 described above should not be understood as requiring such separation in all implementations, and it should be understood that the described program components and systems can generally be integrated together in a single software product or packaged into multiple software products. Additionally, other implementations are within the scope of the following claims. In some cases, the actions recited in the

25 claims can be performed in a different order and still achieve desirable results.



## CLAIMS

What is claimed is:

1. A device comprising:

a substrate having a first surface and a second surface;

5 a first inducting arrangement including a plurality of first conductive pathways that together form a first conductive path, the first conductive path having a first axis of revolution, the plurality of first conductive pathways including a first set of vias extending at least from the first surface to the second surface, a second set of vias extending at least from the first surface to the second surface, a first set of traces arranged over the first surface that connect the first set of vias with the second set of vias, and a second set of traces arranged over the second surface that connect the first set of vias with the second set of vias;

a second inducting arrangement inductively-coupled with and  
15 interleaved with the first inducting arrangement and including a plurality of second conductive pathways that together form a second conductive path, the second conductive path having a second axis of revolution, at least part of the first axis of revolution extending within the second inducting arrangement, at least part of the second axis of revolution extending within the first inducting arrangement, the plurality of second conductive pathways including a third set of vias extending at least from the first surface to the second surface, a fourth set of vias extending at least from the first surface to the second surface, a third set of traces arranged over the first surface that connect the third set of vias with the fourth set of vias, and a fourth set of traces arranged over the second surface that connect the third set of vias with the fourth set of vias;

20 a first set of one or more dielectric layers that insulate portions of the first set of traces from portions of the third set of traces; and

a second set of one or more dielectric layers that insulate portions of the second set of traces from portions of the fourth set of traces.

30

2. The device of claim 1, wherein:

the first set of vias are arranged along a first row and the second set of vias are arranged along a second row, each of the first set of traces connecting

a via from the first row with a via from the second row over the first surface, each of the second set of traces connecting a via from the first row with a via from the second row over the second surface; and

the third set of vias are arranged along a third row and the fourth set of vias  
5 are arranged along a fourth row, each of the third set of traces connecting a via from the third row with a via from the fourth row over the third surface, each of the fourth set of traces connecting a via from the third row with a via from the fourth row over the second surface.

10 3. The device of claim 2, wherein:  
the first row is substantially parallel with the second row; and  
the third row is substantially parallel with the fourth row.

4. The device of claims 2 or 3, wherein:  
15 the first row is substantially parallel with the third row; and  
the second row is substantially parallel with the fourth row.

5. The device of any preceding claim, wherein:  
the first set of traces are formed from a first conductive layer deposited and  
20 patterned on the first surface;

the first set of one or more dielectric layers that insulate portions of the first traces from portions of the third traces include a first dielectric layer deposited and patterned over the first surface so as to cover portions of the first set of traces;

the third set of traces are formed from a third conductive layer deposited and  
25 patterned over the first dielectric layer;

the second set of traces are formed from a second conductive layer deposited and patterned on the second surface;

the second set of one or more dielectric layers that insulate portions of the second traces from portions of the fourth traces include a second dielectric layer  
30 deposited and patterned over the second surface so as to cover portions of the second set of traces; and

the fourth set of traces are formed from a fourth conductive layer deposited and patterned over the second dielectric layer.

6. The device of any preceding claim, wherein the plurality of first conductive pathways are arranged entirely within a region that is within the plurality of second conductive pathways.

5

7. The device of any of claims 1 to 4, wherein:

the first set of traces are formed from a first conductive layer deposited and patterned on the first surface;

the one or more dielectric layers that insulate portions of the first traces from portions of the third traces include a first dielectric layer deposited and patterned over the first surface so as to cover portions of the first set of traces;

the third set of traces are formed from a third conductive layer deposited and patterned over the first dielectric layer;

the fourth set of traces are formed from a fourth conductive layer deposited and patterned on the second surface;

the one or more dielectric layers that insulate portions of the second traces from portions of the fourth traces include a second dielectric layer deposited and patterned over the second surface so as to cover portions of the fourth set of traces; and

the second set of traces are formed from a second conductive layer deposited and patterned over the second dielectric layer.

8. The device of any claim 7, wherein the first axis of revolution is laterally offset from the second axis of revolution.

25

9. The device of claim 8, wherein the first axis of revolution is parallel to the second axis of revolution.

10. The device of claims 8 or 9, wherein an effective number of turns of the first conductive pathways and an effective number of turns of the second conductive pathways are substantially equal as a result of the lateral offset such that the first inducting arrangement is inductively-coupled with the second inducting arrangement with a transformation ratio of substantially 1:1.

30

11. The device of any preceding claim, wherein the substrate is formed from glass, sapphire, or quartz.

5 12. The device of any preceding claim, wherein;  
magnetic field lines within the substrate within the region of the substrate within both the first and the second inducting arrangements are parallel with the first and the second surfaces.

10 13. A method comprising:  
providing a substrate;  
forming a plurality of vias in the substrate that each extend through the substrate from a first surface of the substrate to a second surface of the substrate, the plurality of vias including a first set of vias, a second set of vias, a third set of vias,  
15 and a fourth set of vias;

depositing a first conductive layer over the first surface of the substrate to form a first set of traces that each connect a via from the first set of vias with a via from the second set of vias;

depositing one or more first dielectric layers over portions of the first traces;

20 depositing a third conductive layer over the first dielectric layers to form a third set of traces that each connect a via from the third set of vias with a via from the fourth set of vias;

depositing a fourth conductive layer over the second surface of the substrate to form a fourth set of traces that each connect a via from the third set of vias with a via  
25 from the fourth set of vias;

depositing one or more second dielectric layers over portions of the fourth traces; and

depositing a second conductive layer over the second dielectric layers to form a second set of traces that each connect a via from the first set of vias with a via from  
30 the second set of vias.

14. The method of claim 13, further comprising plating or filling the plurality of vias with a conductive material.

15. The method of claim 14, wherein:

the first set of vias, the second set of vias, the first set of traces, and the second set of traces form at least a portion of a first inducting arrangement including a plurality of first conductive pathways that together form a first  
5 conductive path, the first conductive path having a first axis of revolution;

the third set of vias, the fourth set of vias, the third set of traces, and the fourth set of traces form at least a portion of a second inducting arrangement including a plurality of second conductive pathways that together  
10 form a second conductive path, the second conductive path having a second axis of revolution that is laterally offset from the first axis of revolution; and

the second inducting arrangement is inductively-coupled with and interleaved with the first inducting arrangement.

16. The method of claim 15, wherein:

the first axis of revolution extends within the second inducting arrangement; and

the second axis of revolution extends within the first inducting arrangement.

17. The method of claims 15 or 16, wherein an effective number of turns of the first conductive pathways and an effective number of turns of the second conductive pathways are substantially equal as a result of the lateral offset such that the first inducting arrangement is inductively-coupled with the  
25 second inducting arrangement with a transformation ratio of substantially 1:1.

18. A device comprising:

a substrate having a first surface and a second surface;

a first inducting means including a plurality of first conductive pathways that together form a first conductive path, the first conductive path having a first axis of revolution, the plurality of first conductive pathways including a first set of via means extending at least from the first surface to the second surface, a second set of via means extending at least from the first  
30

surface to the second surface, a first set of conductive means arranged over the first surface that connect the first set of via means with the second set of via means, and a second set of conductive means arranged over the second surface that connect the first set of via means with the second set of via means;

5           a second inducting means inductively-coupled with and interleaved with the first inducting means and including a plurality of second conductive pathways that together form a second conductive path, the second conductive path having a second axis of revolution, at least part of the first axis of revolution being inside the second inducting means, the second axis of revolution being inside the first inducting means,  
10       the plurality of second conductive pathways including a third set of via means extending at least from the first surface to the second surface, a fourth set of via means extending at least from the first surface to the second surface, a third set of conductive means arranged over the first surface that connect the third set of via means with the fourth set of via means, and a fourth set of conductive means arranged  
15       over the second surface that connect the third set of via means with the fourth set of via means;

          a first set of one or more dielectric means that insulate portions of the first conductive means from portions of the third conductive means; and

          a second set of one or more dielectric means that insulate portions of the  
20       second conductive means from portions of the fourth conductive means.

19.       The device of claim 18, wherein the plurality of first conductive pathways are arranged entirely within a region that is within the plurality of second conductive pathways.

25

20.       The device of claims 18, wherein the first axis of revolution is laterally offset from the second axis of revolution.

21.       The device of claim 20, wherein an effective number of turns of the  
30       first conductive pathways and an effective number of turns of the second conductive pathways are substantially equal as a result of the lateral offset such that the first inducting means is inductively-coupled with the second inducting means with a transformation ratio of substantially 1:1.

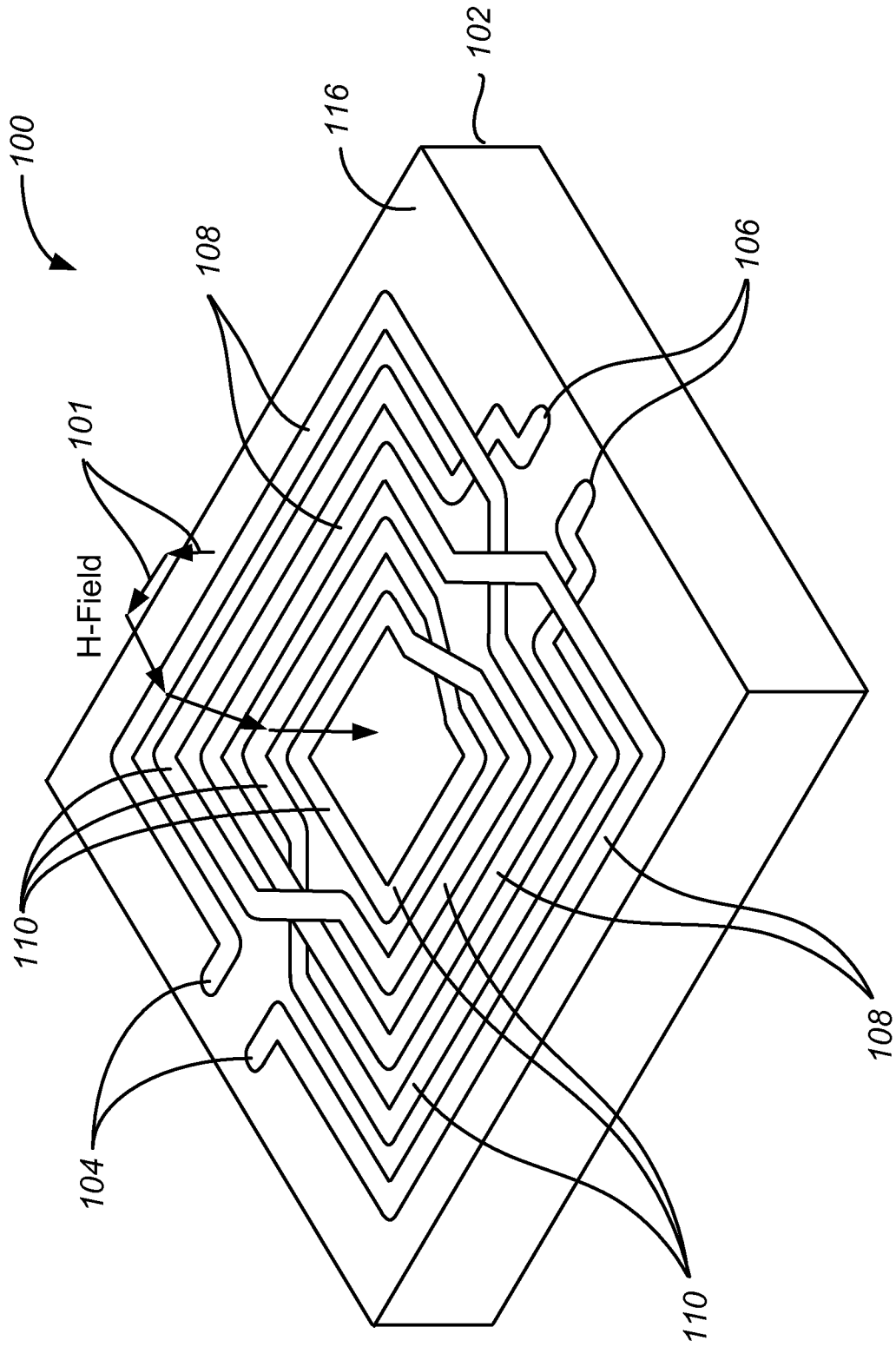


FIG. 1

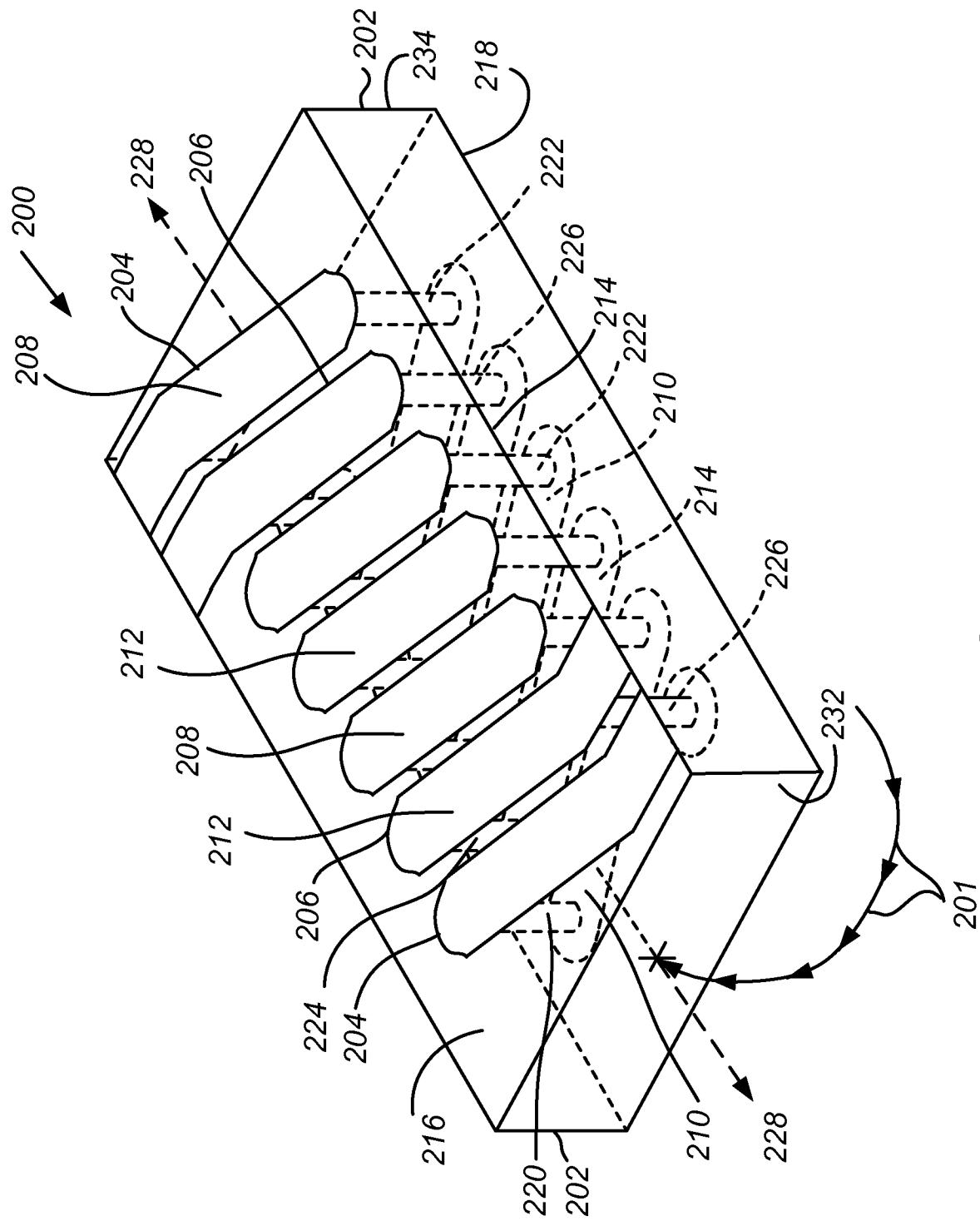
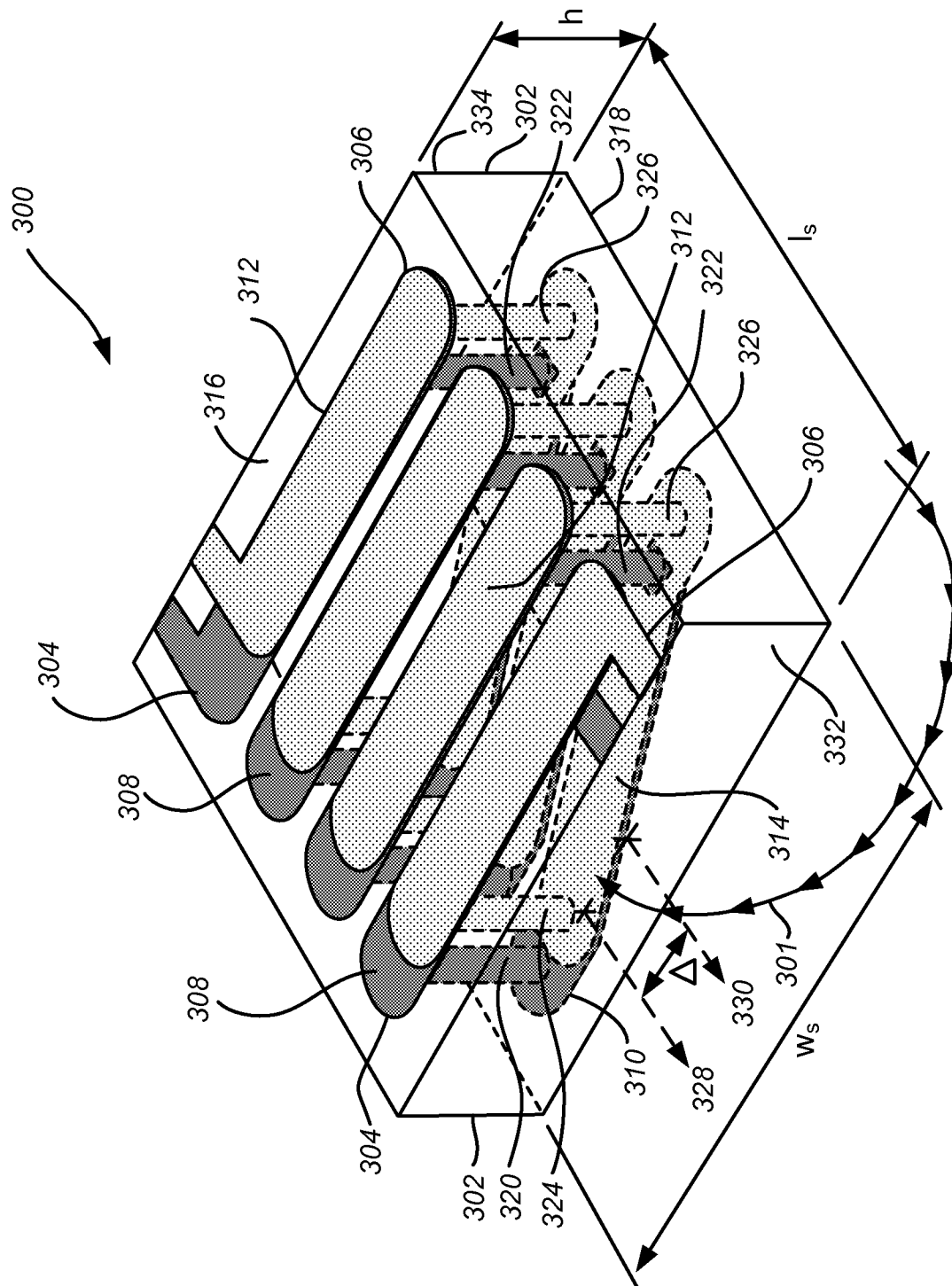


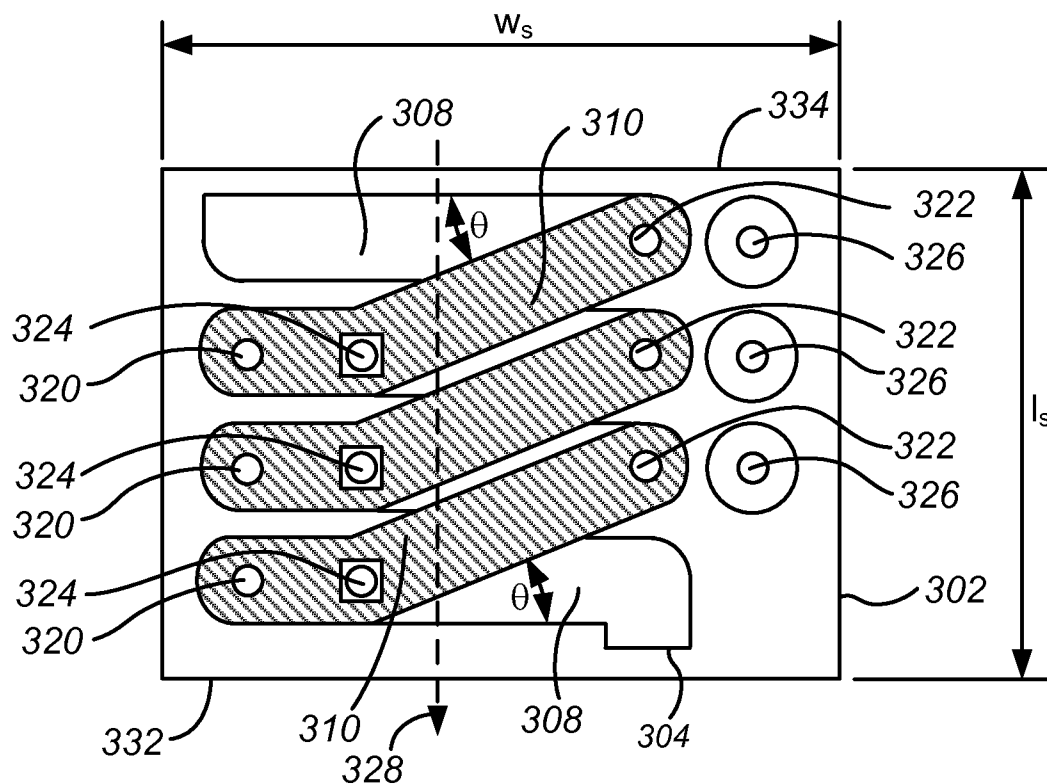
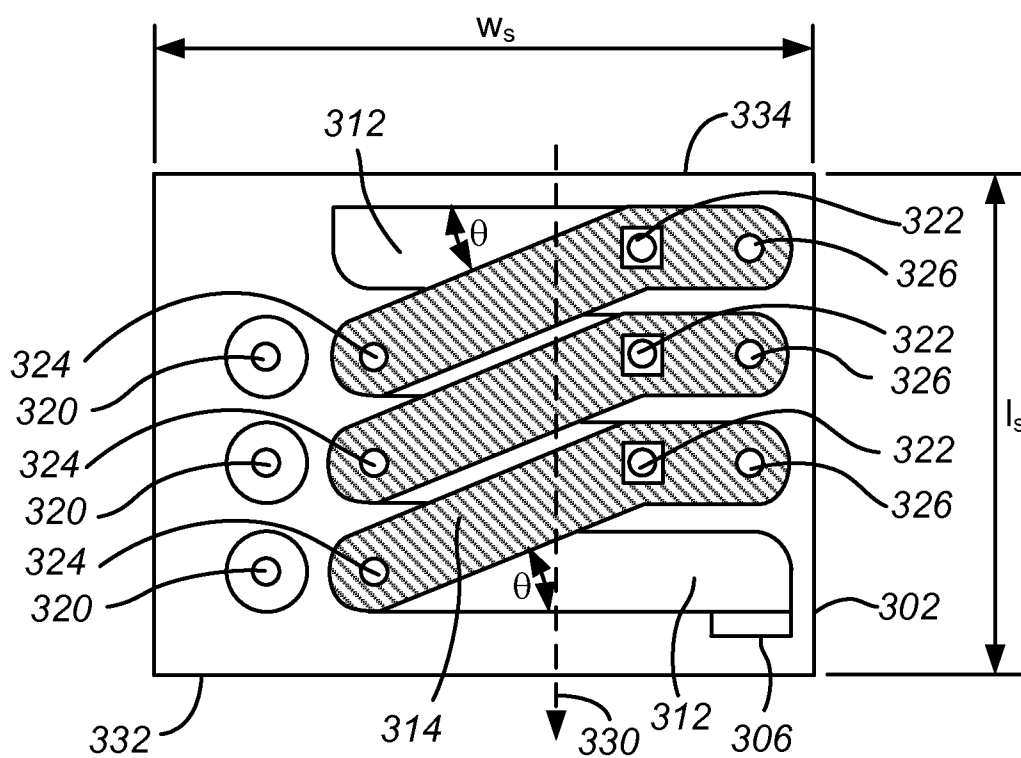
FIG. 2

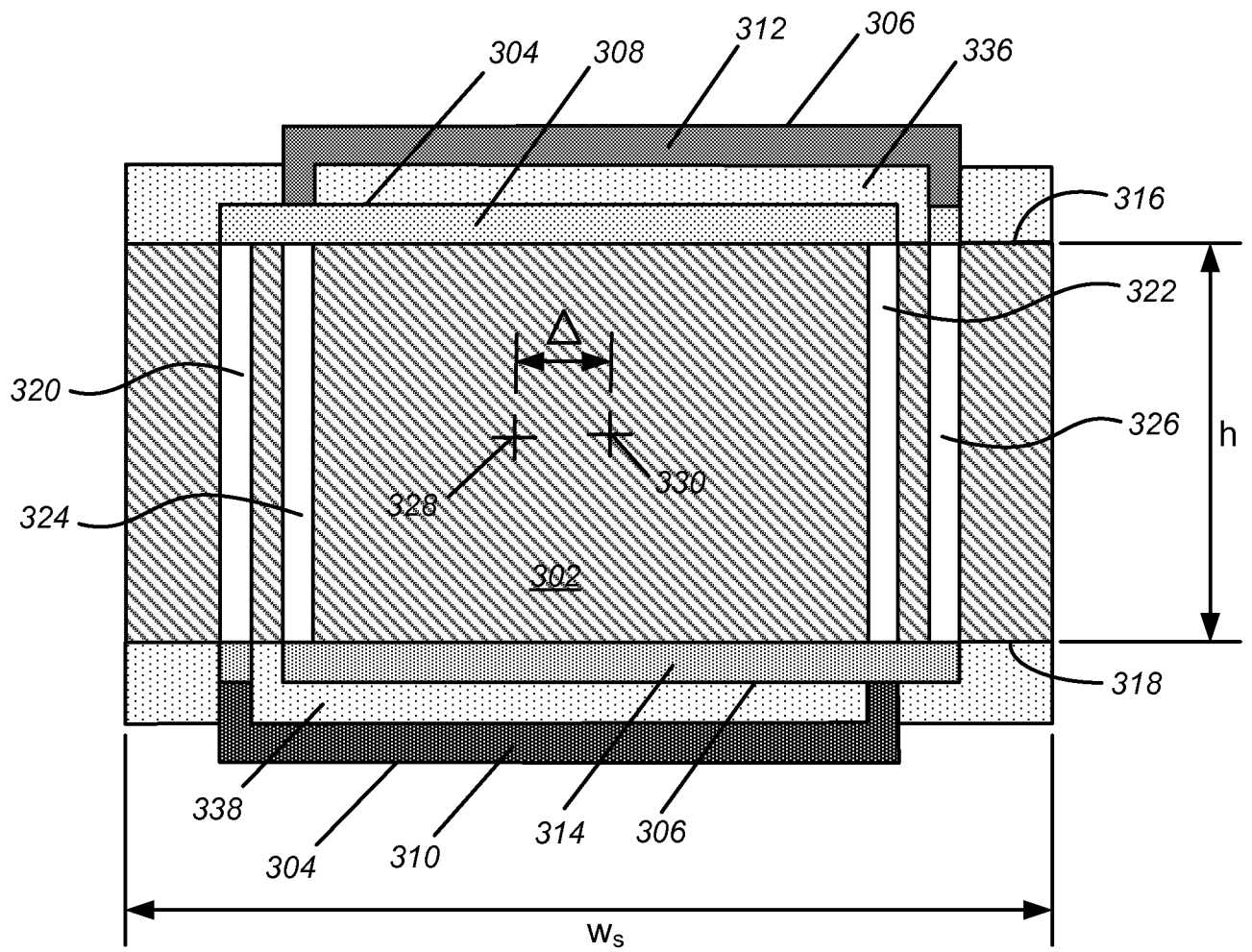




**FIG. 3**

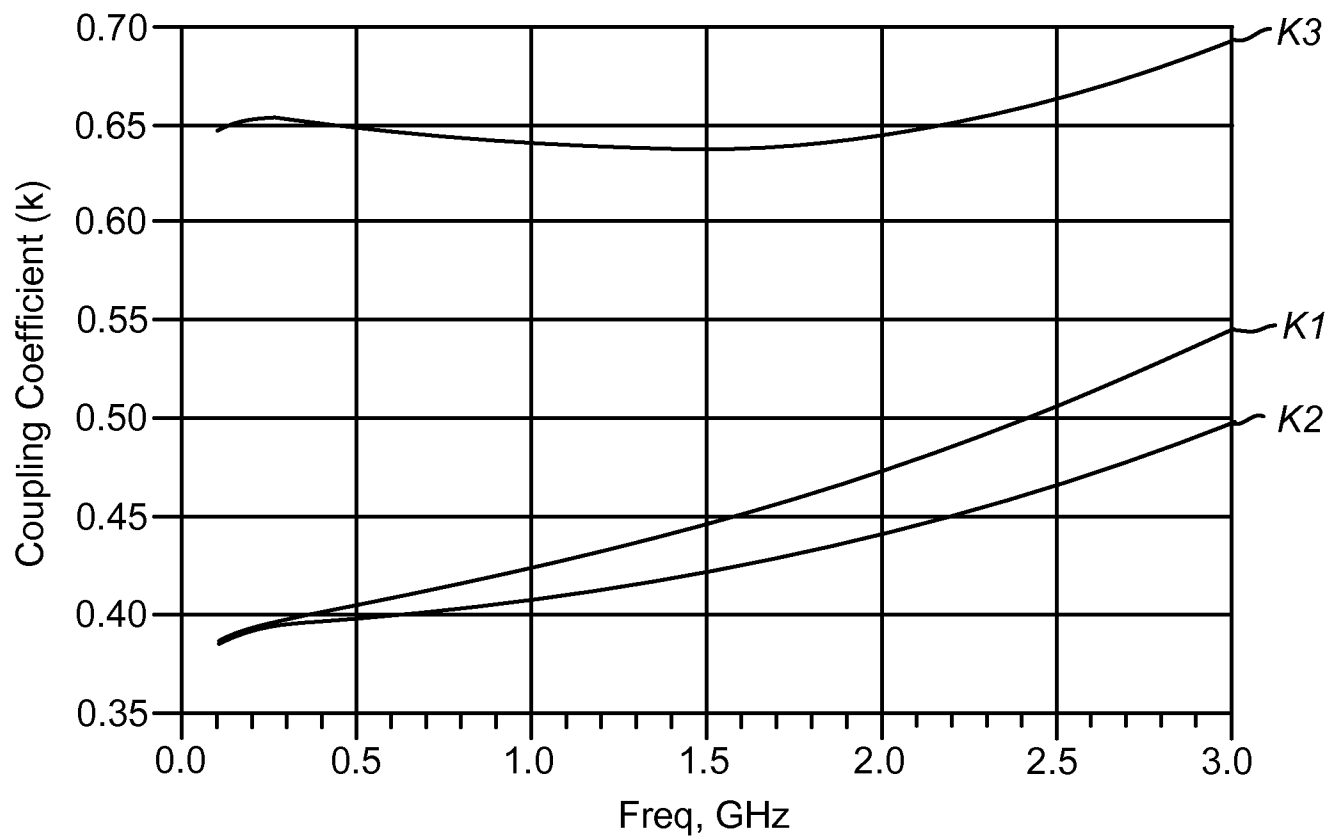
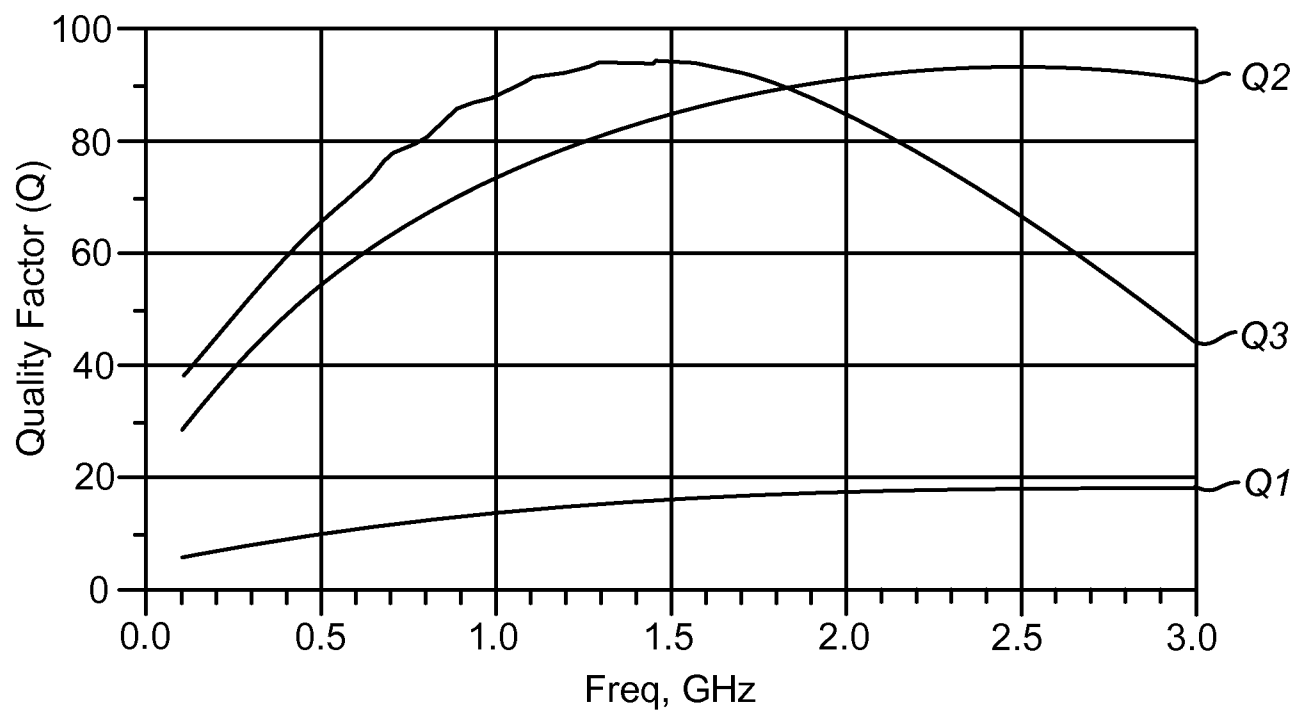
4 / 14

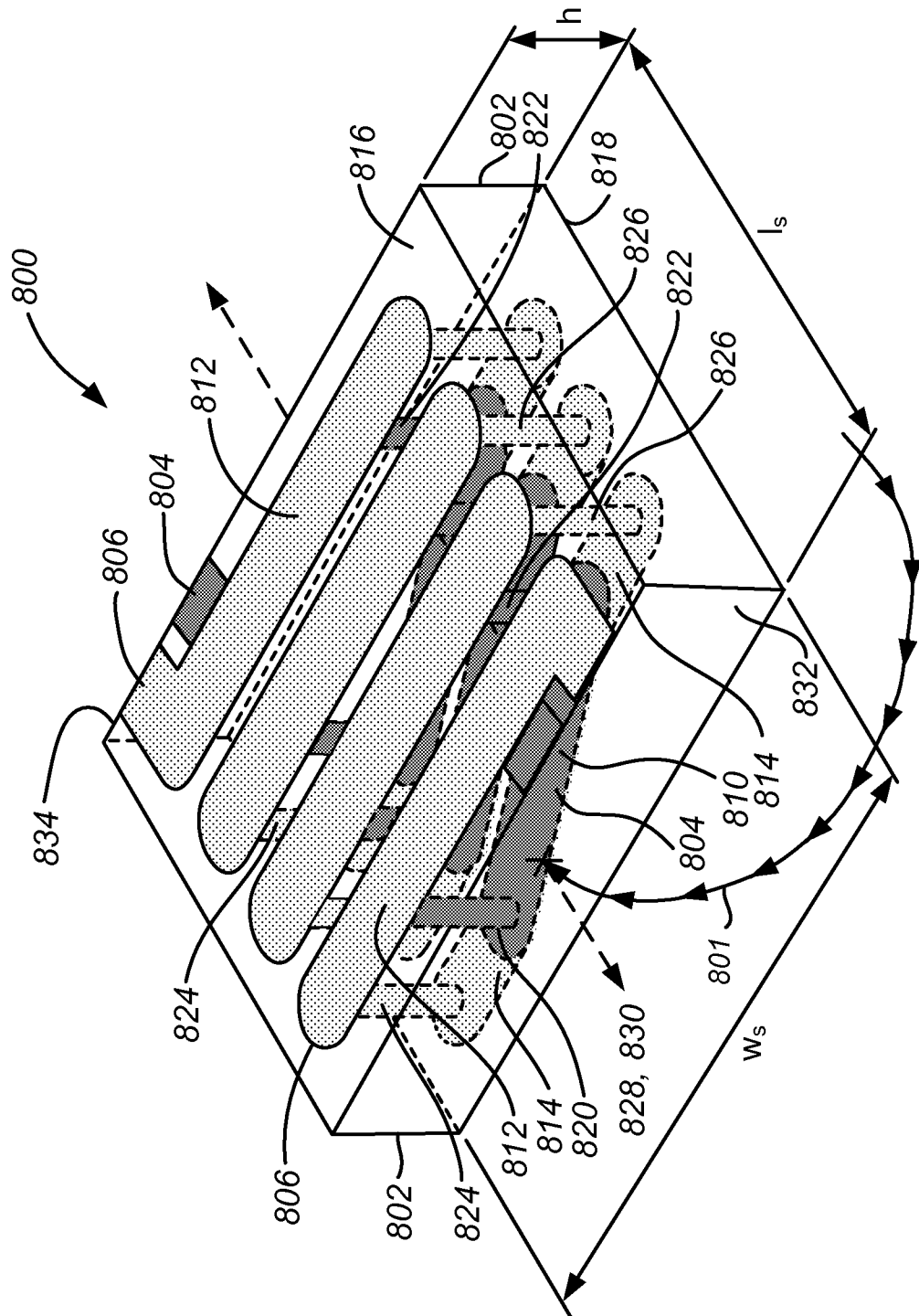
**FIG. 4A****FIG. 4B**



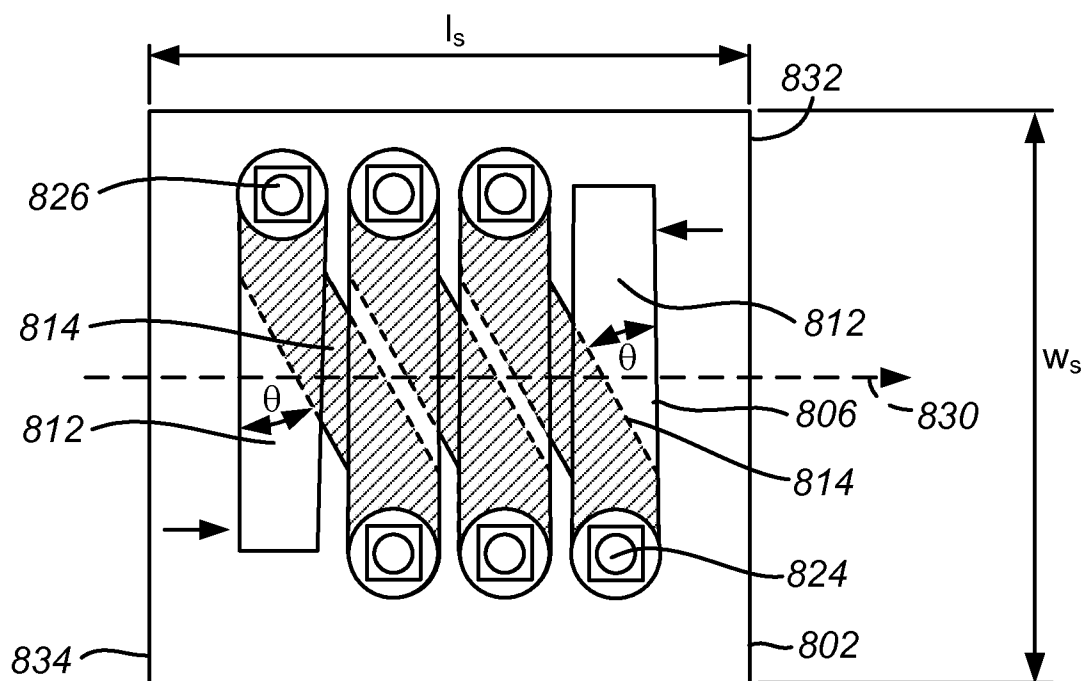
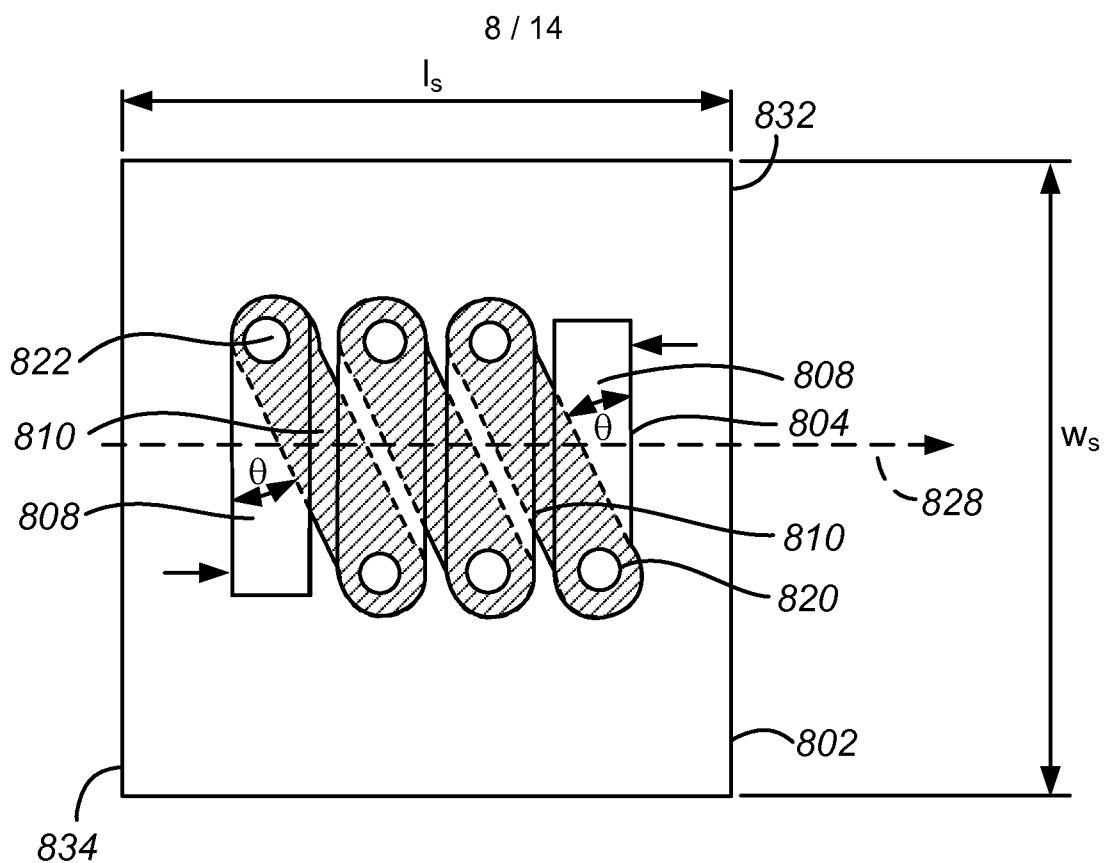
**FIG. 5**

6 / 14

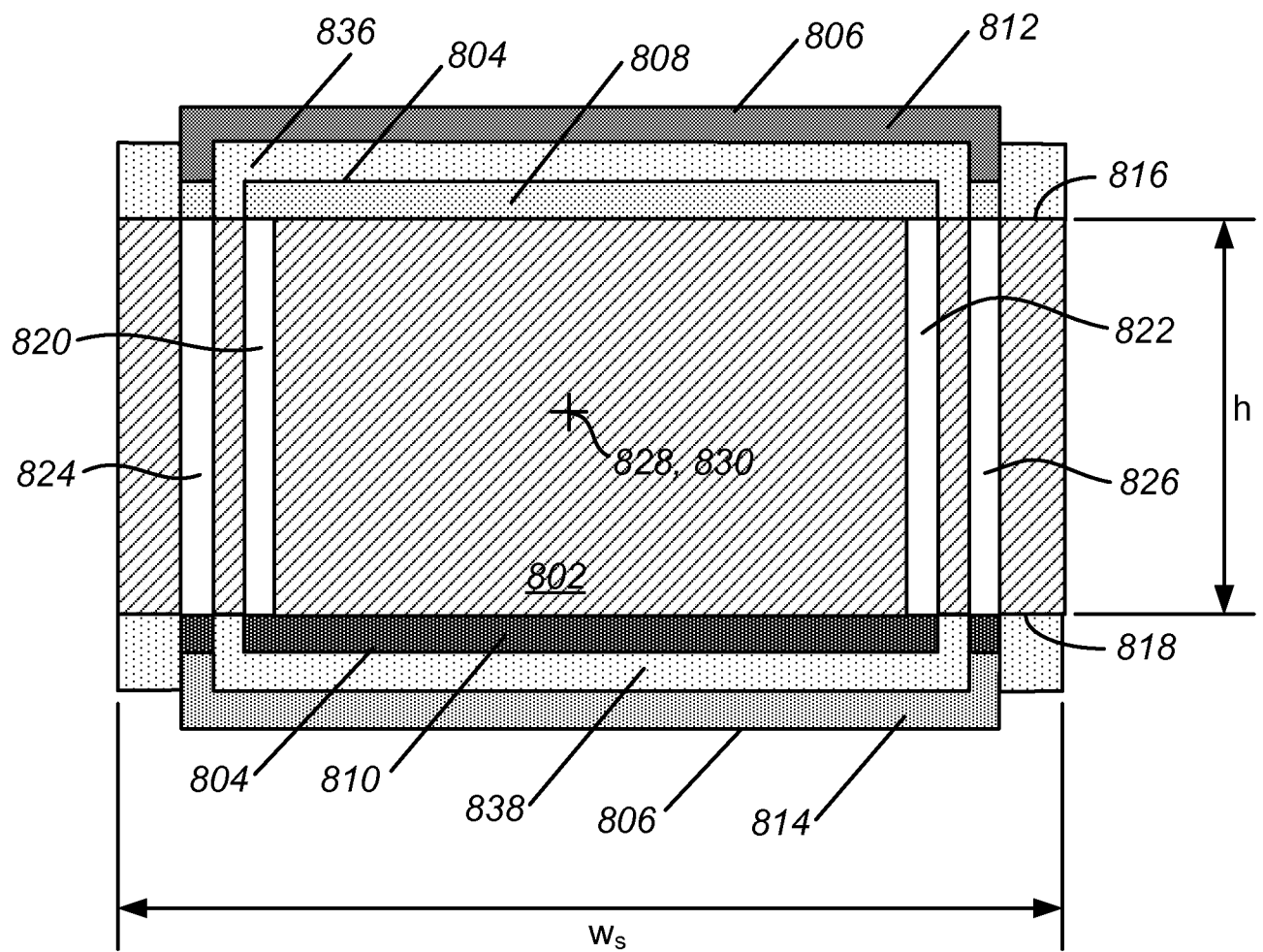
**FIG. 6****FIG. 7**

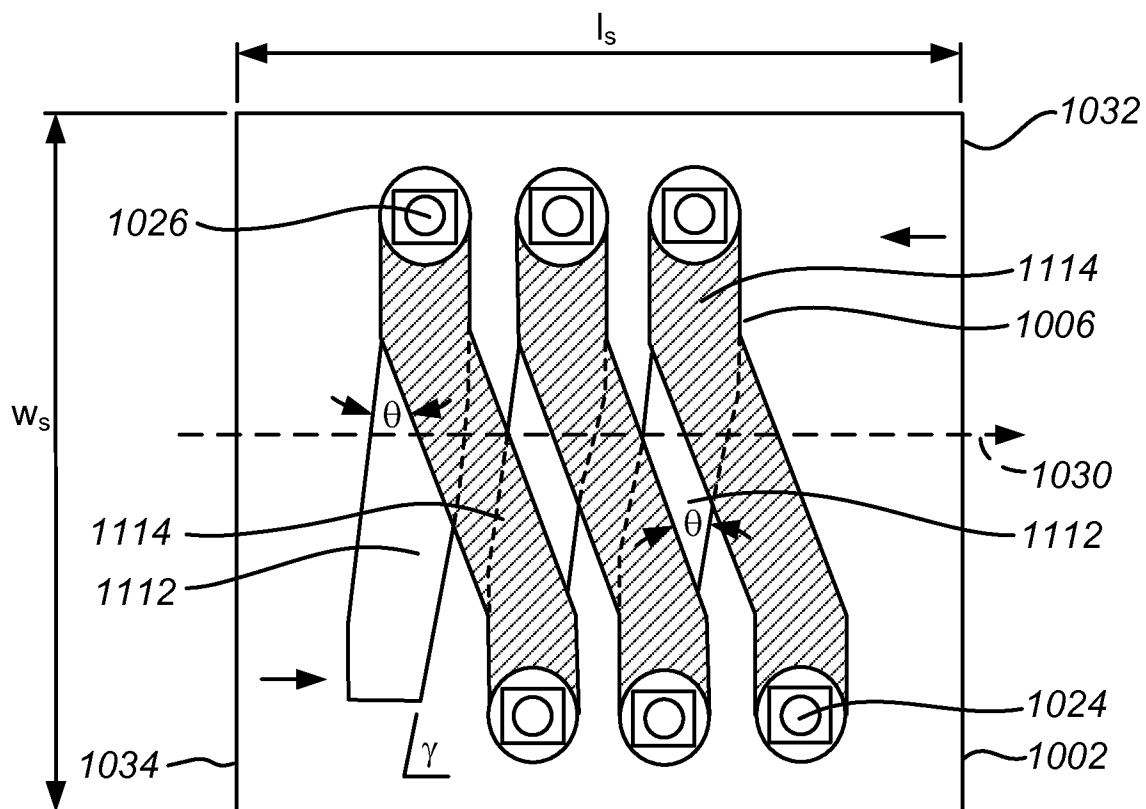
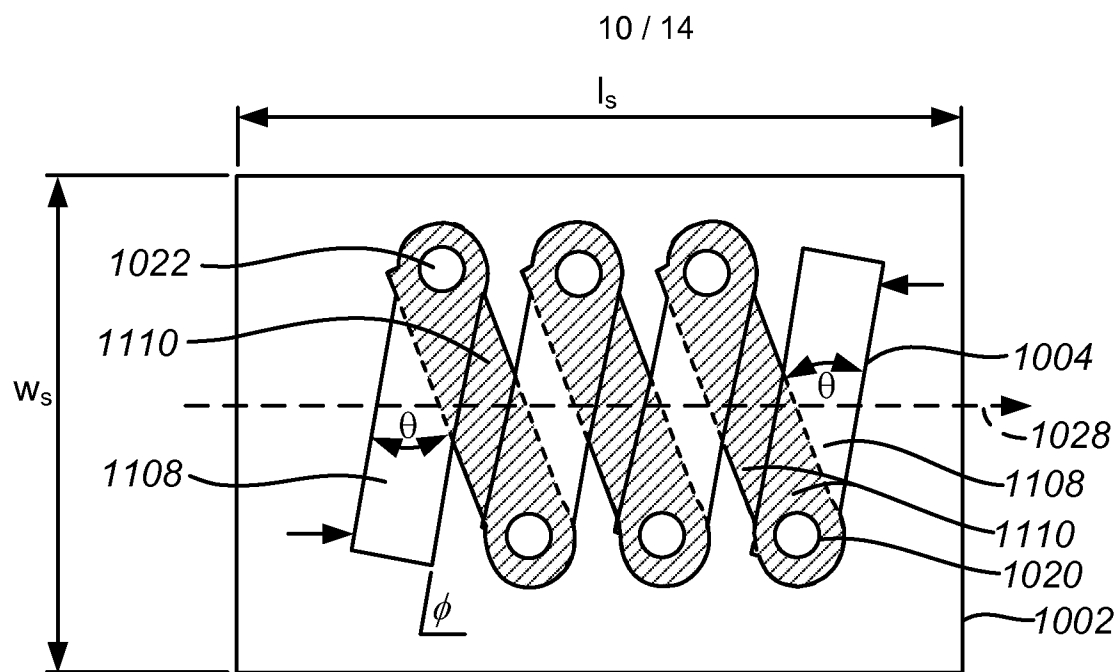


**FIG. 8**



9 / 14

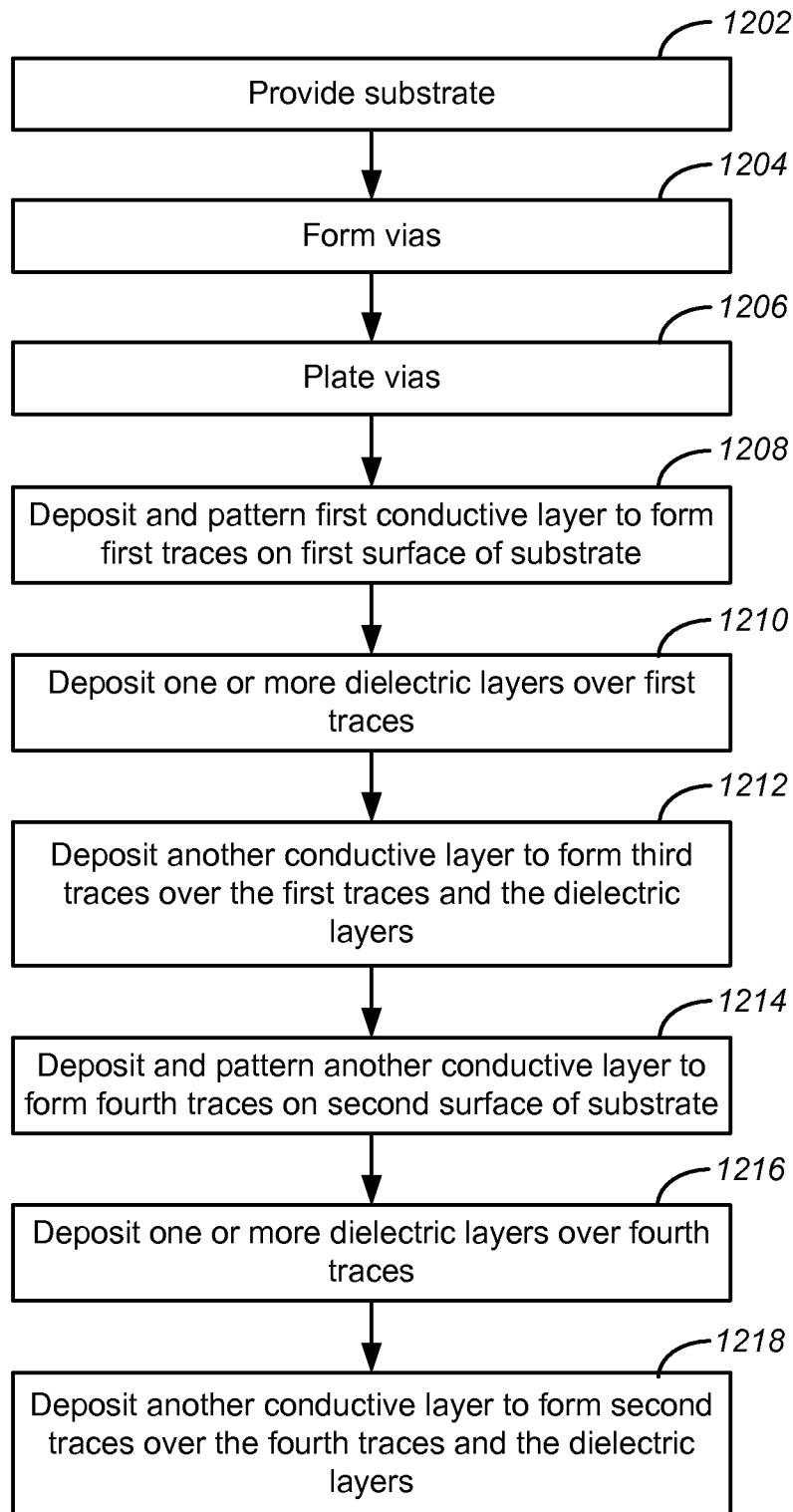
**FIG. 10**



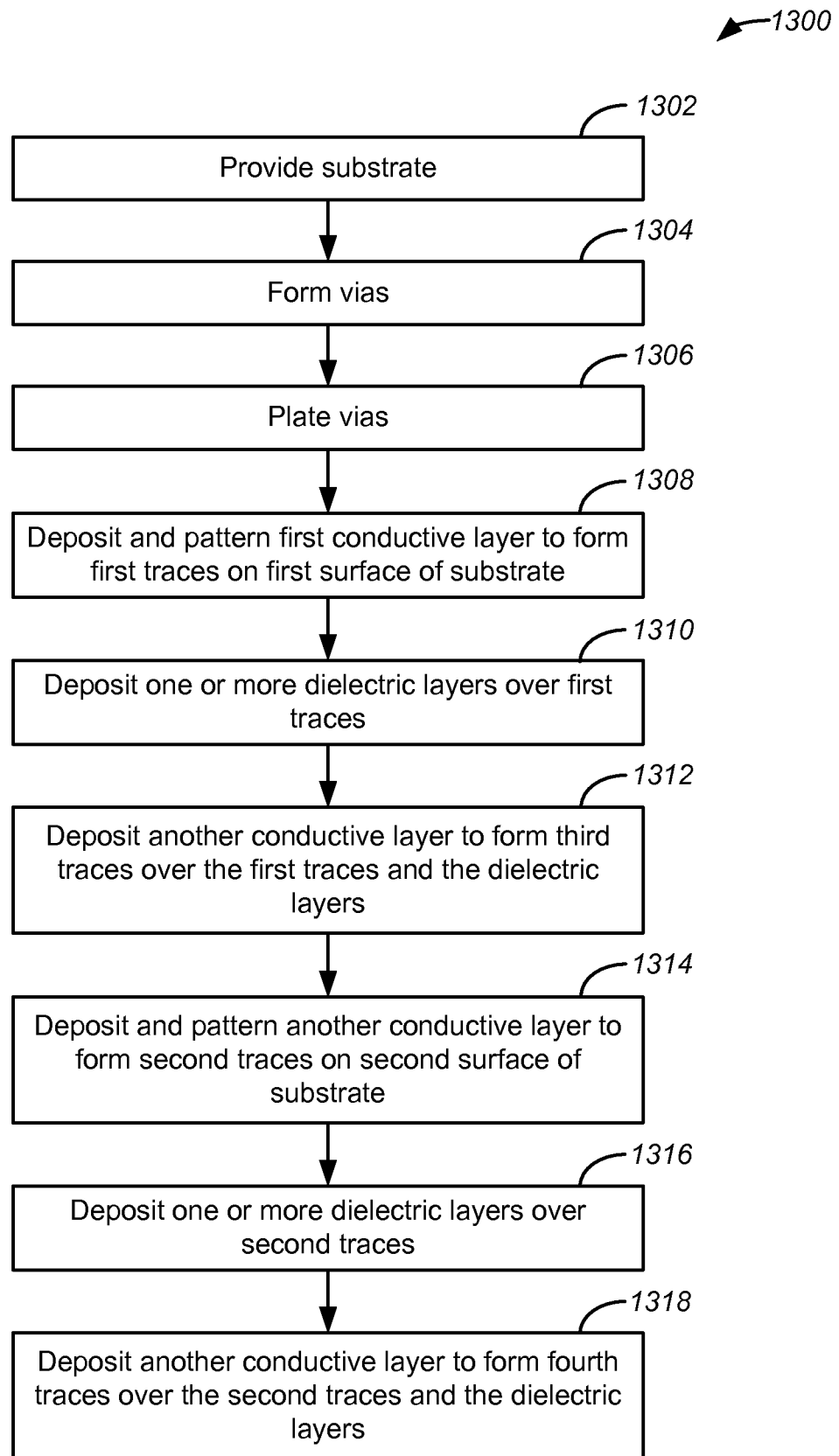


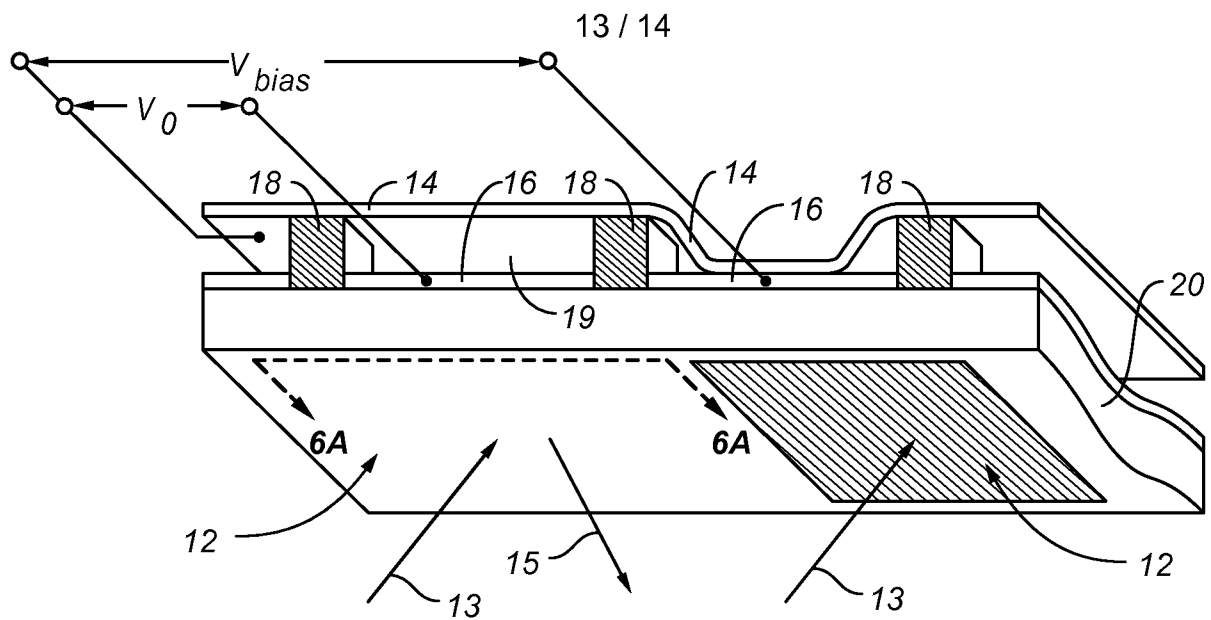
11 / 14

1200

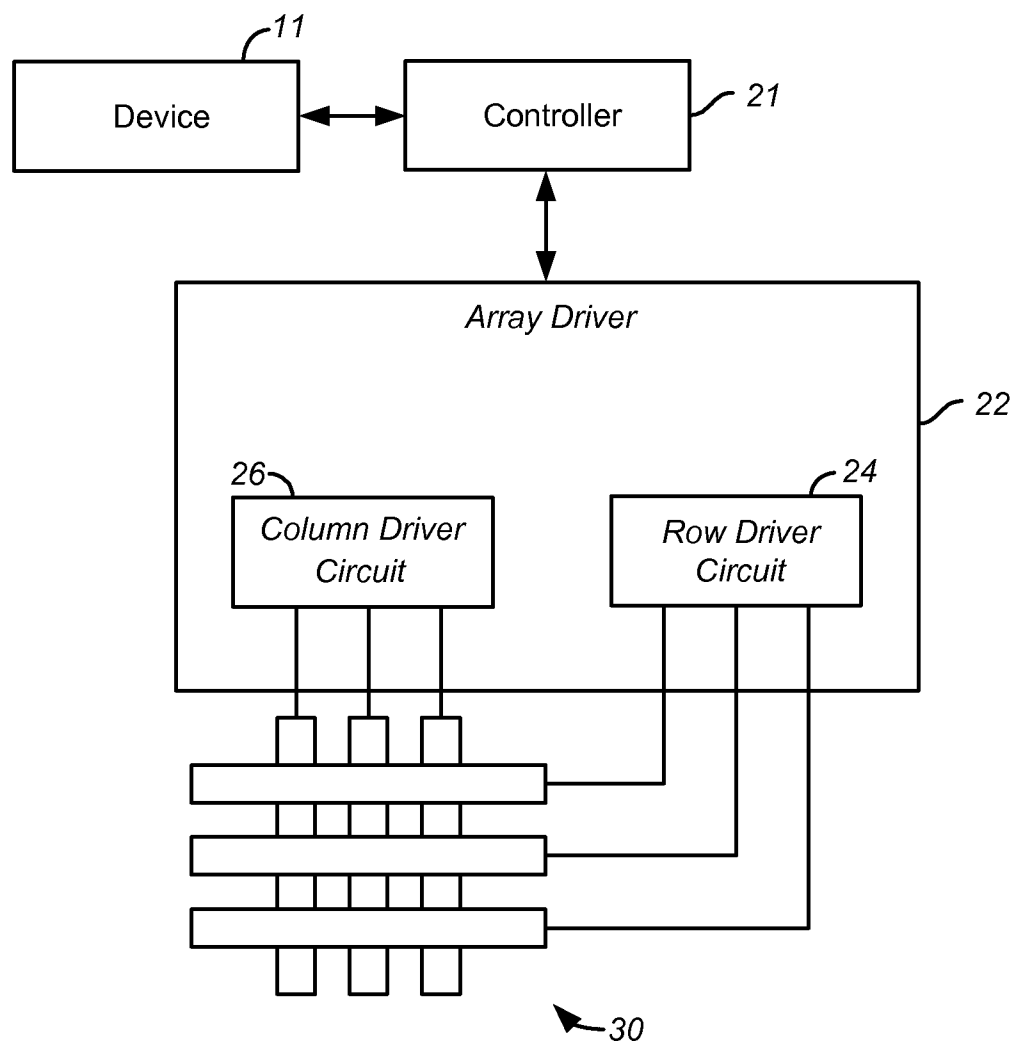
**FIG. 12**

12 / 14

**FIG. 13**

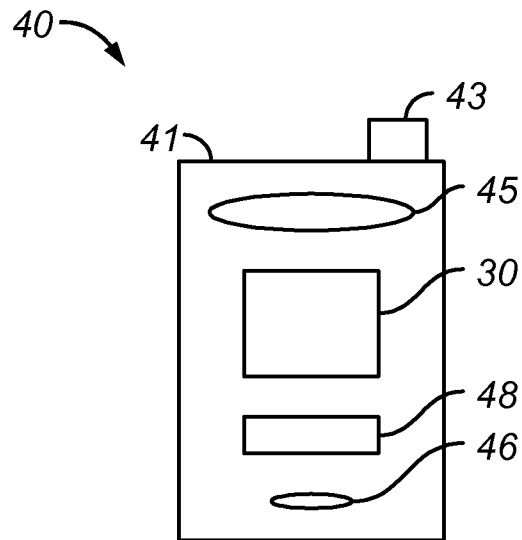
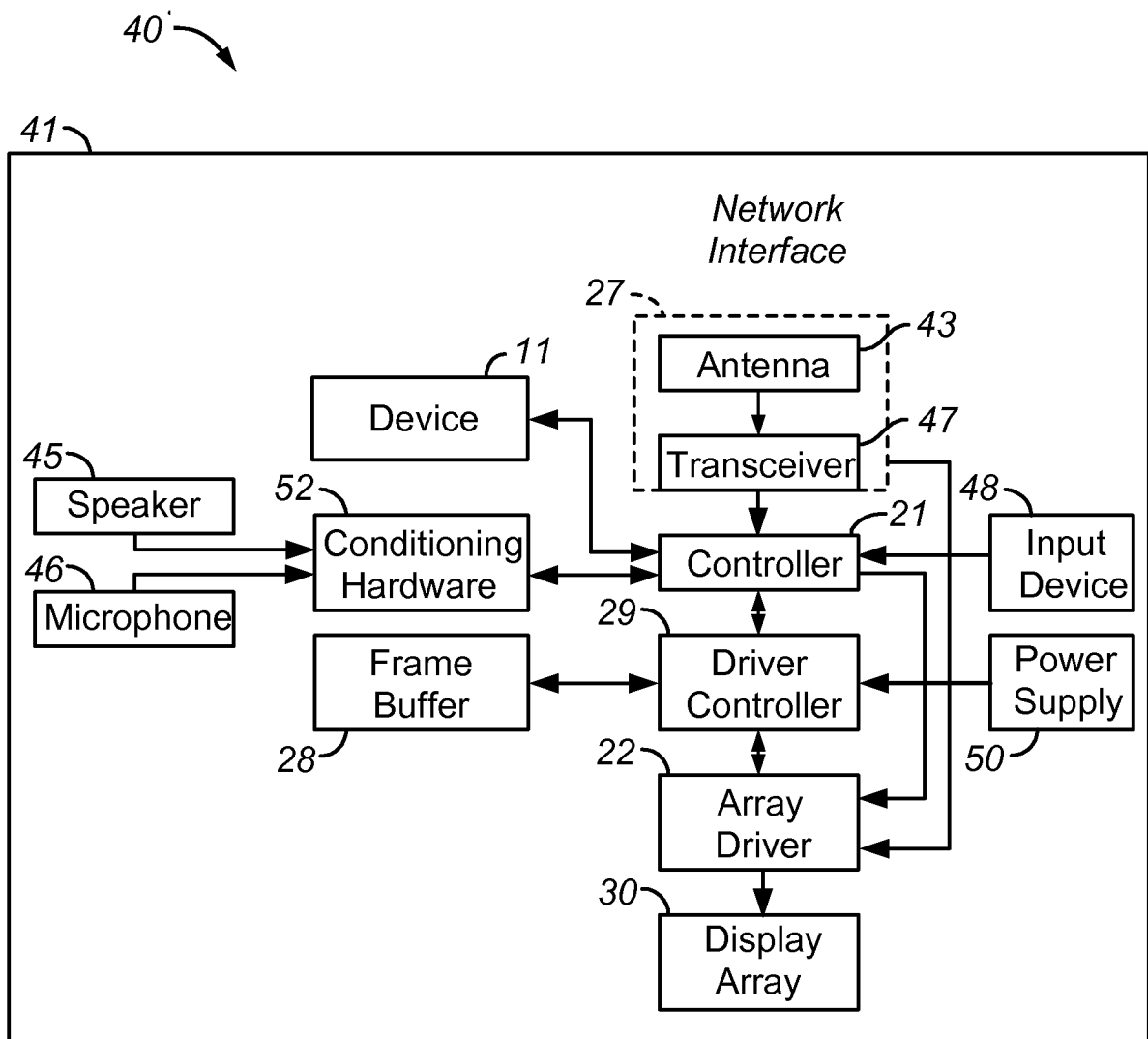


**FIGURE 14A**



**FIGURE 14B**

14 / 14

**FIGURE 15A****FIGURE 15B**

## INTERNATIONAL SEARCH REPORT

International application No

PCT/US2013/037173

## A. CLASSIFICATION OF SUBJECT MATTER

INV. H01F27/28

ADD. H01F17/00

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01F H01L H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 778 593 A1 (CONS RIC MICROELETTRONICA [IT]; SGS THOMSON MICROELECTRONICS [IT] CONS) 11 June 1997 (1997-06-11) column 10, line 7 - column 11, line 34; figures 13,14 column 14, lines 8-13; figure 19 -----	1-6, 12-14, 18,19
X	US 2002/002771 A1 (LIN WEN-YEN [TW] ET AL) 10 January 2002 (2002-01-10)  abstract; figures 4,5,8 paragraphs [0048] - [0055] -----  -/-	1-6, 12-14, 18,19



Further documents are listed in the continuation of Box C.



See patent family annex.

## \* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&amp;" document member of the same patent family

Date of the actual completion of the international search

1 July 2013

Date of mailing of the international search report

11/07/2013

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2  
NL - 2280 HV Rijswijk  
Tel. (+31-70) 340-2040,  
Fax: (+31-70) 340-3016

Authorized officer

Reder, Michael

## INTERNATIONAL SEARCH REPORT

International application No

PCT/US2013/037173

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 856 855 A2 (MITSUBISHI ELECTRIC CORP [JP]) 5 August 1998 (1998-08-05)  column 13, line 52 - column 15, line 29; figure 13 column 16, line 3 - column 17, line 26; figure 14  -----	1-6, 12-14, 18,19
A	US 6 031 445 A (MARTY MICHEL [FR] ET AL) 29 February 2000 (2000-02-29) abstract; figures 3-8 column 3, lines 49-67 column 8, lines 26-35  -----	1-21

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2013/037173

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0778593	A1	11-06-1997	DE 69519476 D1 28-12-2000
			DE 69519476 T2 28-06-2001
			EP 0778593 A1 11-06-1997
			US 5936298 A 10-08-1999
-----			
US 2002002771	A1	10-01-2002	NONE
-----			
EP 0856855	A2	05-08-1998	EP 0856855 A2 05-08-1998
			JP H10223447 A 21-08-1998
-----			
US 6031445	A	29-02-2000	EP 0920036 A1 02-06-1999
			FR 2771843 A1 04-06-1999
			US 6031445 A 29-02-2000
-----			