Title: 2-TRANSISTOR MEMORY CELL WITH MODIFIED ACCESS GATE

Abstract: An array of 2-transistor memory devices is provided, the array comprising a plurality of stacked gate transistors with a floating gate and a control gate and a plurality of access transistors with an access gate. The access gate of the access transistor is formed by a first conductive layer and a second conductive layer electrically connected to each other, whereby at least one of the slits separating adjacent floating gates runs form one floating gate to an adjacent floating gate through a position occupied by the respective access gate. Furthermore, a method for the manufacturing of such an array of 2-transistor memory devices is provided.
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2-Transistor Memory Cell With Modified Access Gate

The present invention relates to an array of 2-transistor flash memory devices and a method for manufacturing such an array. More particularly, the invention relates to an array of 2-transistor flash memory devices comprising a stacked gate transistor and an access transistor, wherein the access gate of the access transistor is formed by two conductive layers being electrically connected with each other.

Non-volatile memories (NVMs) are used in a wide variety of commercial and military electronic devices and equipment, such as e.g. hand-held telephones, radios and digital cameras. The market for these electronic devices continues to demand devices with a lower operating voltage, lower power consumption and a decreased chip size.

Flash memories or flash memory cells comprise a MOSFET with a floating gate (FG) or a plurality of floating gates between a control gate (CG) and a channel region, the floating gate(s) and the control gate being separated by a dielectric layer. With the improvement of fabrication technologies, the FG size has been reduced to dimensions of about 100 nm. These devices are basically miniature EEPROM cells in which electrons or holes are injected in a floating gate by means of tunneling through an oxide barrier. Charges stored in the FG modify the device threshold voltage. In this way, data is stored. The CG controls the potential of the FG. The CG to FG coupling ratio, which is related to the areal overlap between the FG and the CG, affects the read/write speed of the flash memory. Furthermore, the better, i.e. higher, the coupling ratio, the more the required operation voltage of the memory cell can be reduced.

Access gate (AG) transistors are widely used in flash memories to isolate each cell in an array. This isolation transistor can be used to allow the flash cells to have a negative threshold voltage (i.e., no over-erase, which allows the cells to be read at a gate voltage close to ground), to enable the cells to be programmed and erased by Fowler-Nordheim tunneling to and from the channel, and/or to avoid disturbances of the cells during programming and erasing. Flash (or EEPROM) memories with an AG for each individual cell or for a plurality of cells (i.e. NAND flash) are widely used. The presence of the AG
transistor makes the cell larger but has many advantages in the operation of the memory which is particularly beneficial for embedded applications. A relatively compact 2-T cell can be made by treating the AG as a floating gate (FG) cell (i.e. processed on the tunnel oxide and having a stacked gate configuration) with a contacted FG.

Besides these advantages, this approach has some drawbacks as well, for instance the high resistance of the AG (it is not salicidised) and the fact that the FG slits used to separate adjacent FG's on the same word line (the so-called SFG slits) cannot be long lines across the entire array, because they would segment the AG lines. To decrease the AG resistance, which is needed to get a fast access time, low-ohmic metal straps have to be used for shunting the AG, which decreases the area efficiency. The fact that the SFG slits cannot cross the AG’s in the array has a negative influence on the cell size. Due to effects as line-end shortening, misalignment, CD control etc., margins have to be ‘built in’ in the cell design. Without these margins, the SFG slits could cut an AG line, if the slits are too long, or, the other way around, not isolate two adjacent FG’s if the slits are too short.

Fig. 1 shows flash-specific masks used to fabricate a standard 2-T cell. The array configuration in Fig. 1 is a so-called common-ground NOR configuration, but those skilled in the art will appreciate that this is not the only possible connection scheme. One implementation of the common ground lines are so-called local interconnect lines (LIL). Other possibilities are for example a common source line 2 (see Fig. 1 and 2) or source connections by means of contacts to an overlying metal layer, or a combination of these approaches. Figs. 2, 3 and 4 show three cross-sections of the finished devices according to the prior art. Fig. 2 shows a cross-section along the bit line direction according to the dotted line II-II’ as indicated in Fig. 1. From Fig. 2 it can be seen that the device comprises a CG/FG stack 3 comprising a FG 4, a CG 5 and a dielectric layer 6 in between the FG 4 and the CG 5.

The device furthermore comprises an AG 7, which is covered by dielectric layer 6 and by material from the conductive layer from which the CG 5 was formed. Furthermore, bitline contacts 8 and common source lines 1 are provided, in this example made with LIL lines. Fig. 3 and Fig. 4 show cross-sections according to dashed lines III-III’, i.e. through the stacked gate memory transistor 9, respectively according to dashed lines IV-IV’, i.e. through the access transistor 10. Furthermore, floating gate slits SFG 11 are provided in between two FGs 4 which are adjacent in the direction indicated by dashed lines III-III’. These SFGs 11 filled up with material from the conductive layer of which the CG 5 is formed.

Contacts to the active areas in the substrate 14 and the CGs 5 are made in the conventional way by salicidation, whereas contacts 17 to FG poly, which are required to
connect the AGs 7, are made by locally removing the polysilicon of the CG 5 and dielectric layer 6 prior to the formation of HDD spacers 12, i.e. a so-called contact to FG poly or CFP etch, as is shown in Fig. 3. For clarity, the HDD offset spacers 12 have not been drawn in the cross-sections, but are illustrated in Fig. 5.

It is apparent from Figs. 1 to 5 that the material of the AG 7 cannot be salicidised, except for in the CFP holes 15 used for contacting. At the same time, salicide 16 is also deposited onto the CG polysilicon, as illustrated in Fig. 5. This salicide 16 is important for decreasing the contact resistance. The black arrows in Fig. 1 indicate critical points of the SFG definition (SFG etch). The short SFGs 11 should terminate exactly between the AG 7 and CG 5 of stacked gate memory transistor 9, which leads to litho-, overlay- and etching problems, since the width of the SFGs 11 has to be as small as possible in order to reduce the cell size.

It is known from the background section of US 2002/0020872 that a selection transistor associated with a memory cell may consist of either a single layer of polysilicon or of two superposed layers of polysilicon provided above a gate oxide, with an interpoly dielectric layer optionally interposed. Thus, when no interpoly dielectric layer is interposed between the two polysilicon layers forming the AG, it becomes, with respect to the above-described device, easy to salicidize the AG.

Depending on the memory cell architecture, however, the methods for forming such a selection transistor, known up till now, do not allow to combine this access gate transistor and long slits in one device, as the AGs would be disconnected by crossing slits. The formation of longer slits of the same width as the known small slits would, however, give much less technological problems, enabling more aggressive design rules, i.e. leading to smaller cells, and would eliminate the failure mechanism of electrical shorts between two adjacent cells in the CG direction, i.e. horizontal fence leakage.

It is an object of the present invention to provide an array and a method for manufacturing an array of 2-transistor flash memory devices comprising long slits and salicidized AGs.

The above objective is accomplished by a method and device according to the present invention. In particular, the slits between adjacent floating gates are formed such that they form long lines extending from a first side of a substrate surface on which the flash memory devices are positioned to a second side of the substrate surface.
In a first aspect of the invention, a method for the manufacturing of an array of 2-transistor memory devices is provided. The array of 2-transistor memory devices comprises a stacked gate transistor, having a floating gate and a control gate, and an access gate transistor having an access gate adjacent to each other in a first direction. The method comprises:

- depositing a first conductive layer, and
- patterning said first conductive layer to form slits for separating floating gates adjacent to each other in a second direction, the second direction being different from the first direction.

According to the present invention, at least one of said slits runs from one floating gate to an adjacent floating gate through a position occupied by the respective access gate.

The first direction may be substantially perpendicular to the second direction. Depositing the first and second conductive layer may be performed by any conventional deposition technique and may for example be performed by depositing a polysilicon layer.

In one embodiment of the invention, all slits may run from one floating gate to an adjacent floating gate through a position occupied by the respective access gate. The slits may run over substantially the complete width of the array.

An advantage of the method according to the invention is that it gives rise to memory devices comprising an access gate, whereby the access gate is formed in such a way that the it can cross a floating gate slit without causing an electrical open circuit. This allows to use long slits extending over the area of the substrate. Floating gate slits crossing the access gates do not disconnect the access gates, as material of the second conductive layer bridges the gaps.

The method according to the invention may furthermore comprise:

- depositing a dielectric layer on top of the patterned first conductive layer and in the slits, and
- depositing and patterning a second conductive layer to form the control gate.

The dielectric layer may for example be an ONO layer.

Forming the access transistors, may, according to an embodiment of the invention, be performed while forming the stacked gate transistor. The access gate of the access transistor may be formed from the first conductive layer and the second conductive layer. The method may then furthermore comprise, after depositing the dielectric layer on top of the first conductive layer and before depositing the second conductive layer, partially
removing the dielectric layer at that side of a stacked gate transistor where the access gate of the access transistor is to be formed.

The method may furthermore comprise providing a salicide on top of the access gate. This is another advantage of the approach according to this invention. The method allows to salicidize the access gate, thus enabling a longer stitch period for metal straps, yielding an improved efficiency. The access gates are now intrinsically shunted by the salicidation of the control gate, thus significantly reducing the gate resistance. This is an advantage with respect to methods according to the prior art, as in those cases salicidizing of the access gate could not be performed.

The method may also comprise forming isolation zones in the substrate. The isolation zones may, in one embodiment, be performed by forming shallow trench isolations (STI).

In a second aspect of the invention, an array of 2-transistor memory devices is provided. The array comprises:

- a plurality of stacked gate transistors, each stacked gate transistor having a floating gate and a control gate, adjacent floating gates in a second direction being separated by slits, and
- a plurality of access transistors, each access transistor having an access gate, the access gate being formed by a first conductive layer and a second conductive layer electrically connected to each other.

According to the present invention, at least one of the slits runs from one floating gate to an adjacent floating gate through a position occupied by the respective access gate.

In one embodiment, all slits may run from one floating gate to an adjacent floating gate through a position occupied by the respective access gate.

According to the invention, at least one of the slits may run over substantially the complete width of the array in a first direction, being different from the second direction. The first direction may be substantially perpendicular to the second direction.

An advantage of the device according to the invention is that the memory device comprises an access gate formed in such a way that it can cross a floating gate slit without causing an electrical open circuit. This allows to use long slits extending over the area of the substrate. Floating gate slits crossing the access gates do not disconnect the access gates, as material of the second conductive layer bridges the gaps.
The first conductive layer and the second conductive layer may for example be formed out of polysilicon. The floating gate may be formed from the first conductive layer, while the control gate may be formed from the second conductive layer.

The device may furthermore comprise a salicide on top of the access gate and may furthermore comprise a dielectric layer between the floating gate and the control gate of the stacked gate transistor. The dielectric layer may for example be an ONO layer.

According to the invention, the device may furthermore comprise isolation zones which may for example be STI zones.

These and other characteristics, features and advantages of the present invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, which illustrate, by way of example, the principles of the invention. This description is given for the sake of example only, without limiting the scope of the invention. The reference figures quoted below refer to the attached drawings.

Fig. 1 is a top view of a standard 2-T flash memory array according to the prior art.

Fig. 2 to 4 show different cross-sections of the memory array of Fig. 1.

Fig. 5 is a detailed cross-section of the contact to floating gate poly (CFP) construction as used in a standard 2-T flash memory device according to the prior art.

Fig. 6 to 21 illustrate subsequent steps in a possible process flow for the manufacturing of 2-T flash memory devices according to an embodiment of the present invention.

Fig. 22 shows an array of memory devices according to another embodiment of the invention.

In the different figures, the same reference figures refer to the same or analogous elements.

The present invention will be described with respect to particular embodiments and with reference to certain drawings but the invention is not limited thereto but only by the claims. The drawings described are only schematic and are non-limiting. In the drawings, the size of some of the elements may be exaggerated and not drawn on scale for illustrative purposes. Where an indefinite or definite article is used when referring to a
singular noun e.g. "a" or "an", "the", this includes a plural of that noun unless something else is specifically stated.

Furthermore, the terms first, second, third and the like in the description and in the claims, are used for distinguishing between similar elements and not necessarily for describing a sequential or chronological order. It is to be understood that the terms so used are interchangeable under appropriate circumstances and that the embodiments of the invention described herein are capable of operation in other sequences than described or illustrated herein.

Moreover, the terms top, bottom, over, under and the like in the description and the claims are used for descriptive purposes and not necessarily for describing relative positions. It is to be understood that the terms so used are interchangeable under appropriate circumstances and that the embodiments of the invention described herein are capable of operation in other orientations than described or illustrated herein.

It is to be noticed that the term “comprising”, used in the claims, should not be interpreted as being restricted to the means listed thereafter; it does not exclude other elements or steps. Thus, the scope of the expression “a device comprising means A and B” should not be limited to devices consisting only of components A and B. It means that with respect to the present invention, the only relevant components of the device are A and B.

The present invention provides a method for the manufacturing of an array of 2-T flash cells each comprising a stacked gate transistor and an access transistor. The stacked gate transistor comprises a floating gate (FG), formed from a first conductive layer, and a control gate (CG), formed from a second conductive layer, the FG and the CG being separated by a dielectric layer. The access transistor comprises an access gate (AG), formed from the first and second conductive layer which are, at the access gate, electrically connected to each other. The AG is formed such that it can cross a floating gate slit (SFG) without causing an electrical open circuit, allowing for long slits, i.e. slits having a length which is larger than the length of one single 2-T flash cell in the array, the slits forming long lines running all over the array, or at least over a substantial part of the substrate used for making the array of memory devices. Furthermore, the approach according to the present invention allows the AG to be salicidised, thus enabling a longer stitch period for the metal straps, giving an improved area efficiency.

Hereinafter, the subsequent steps in the manufacturing of a 2-transistor (2-T) flash memory device 50 according to an embodiment of the present invention, will be described by means of Fig. 6 to 21. It has to be noted that the process flow discussed
hereinafter is only given as an example and is not intended to be limiting for the present invention.

In a first step, a substrate 20 is provided. In embodiments of the present invention, the term “substrate” may include any underlying material or materials that may be used, or upon which a device, a circuit or an epitaxial layer may be formed. In other alternative embodiments, this “substrate” may include a semiconductor substrate such as e.g. a doped silicon, a gallium arsenide (GaAs), a gallium arsenide phosphide (GaAsP), an indium phosphide (InP), a germanium (Ge), or a silicon germanium (SiGe) substrate. The “substrate” may include for example, an insulating layer such as a SiO₂ or a Si₃N₄ layer in addition to a semiconductor substrate portion. Thus, the term substrate also includes silicon-on-glass, silicon-on sapphire substrates. The term “substrate” is thus used to define generally the elements for layers that underlie a layer or portions of interest. Also, the “substrate” may be any other base on which a layer is formed, for example a glass, plastic or metal layer.

The substrate 20 is provided with isolation zones 21 (see further in Fig. 9).

The isolation zones 21 may for example be shallow trench isolation (STI) zones or thermally grown field oxide (LOCOS – Local Oxidation of Silicon) regions. However, STI zones are preferred over LOCOS regions as they can be formed in a smaller dimension than that of the LOCOS regions, which allows the reduction of the cell dimensions, so that cell density can be increased. Therefore, in the following description, only STI zones are further considered, but it should be understood that the present invention includes the process steps described below carried out with for example LOCOS regions as well.

In the present invention, a substrate 20 is provided with STI zones 21, as illustrated in Fig. 6 to 9, in order to isolate subsequent memory cells from each other. Between two STI zones 21, an active area 22 is formed in the remaining substrate 20. For the formation of the STI zones 21, in a first step, a photoresist mask 23 may be provided on top of the substrate 20, as can be seen from Fig. 6. STI zones 21 may then be formed by initially creating a shallow trench 24 in the semiconductor substrate 20, e.g. by a conventional photolithographic and anisotropic etch process such as dry etch process, e.g. a reactive ion etching (RIE) procedure, using e.g. Cl₂ as etchant. The shallow trench 24 is created to a depth of, for example, between about 200 to 600 nm in the semiconductor substrate 20 (see Fig. 7). After removal of the photoresist mask 23 used for shallow trench definition, e.g. by plasma oxygen ashing and careful wet cleaning, an insulating layer 25 such as for example a silicon oxide layer is deposited, for example by a low pressure chemical vapor deposition (LPCVD) procedure or by a plasma enhanced chemical vapor deposition (PECVD) procedure or other
procedure, to a thickness between about 300 to 1500 nm, such that the shallow trenches 24 are completely filled. This is illustrated in Fig. 8. Removal of the material of the insulating layer 25, which is silicon oxide in the example given, from regions other than inside the shallow trenches 24 is accomplished using any suitable technique, such as either a chemical mechanical polishing (CMP) procedure, or via a RIE procedure using a suitable etchant, resulting in insulator filled STI zones 21 (see Fig. 9).

If instead of STI zones 21, LOCOS isolation zones would be provided in the substrate 20, they may be formed via initially forming an oxidation resistant mask, such as silicon nitride, then exposing regions of the semiconductor substrate 20 not protected by the silicon nitride masking pattern, to a thermal oxidation procedure. LOCOS isolation zones are thus created at a thickness equal to the depth of STI regions 21. After formation of the LOCOS region, the oxidation resistant mask is removed.

Both the processing for STI zones 21 and the processing for LOCOS isolation zones, have the disadvantage that they may introduce topography on the substrate 20. This topography can introduce etch problems in the further processing of the non-volatile memory. In the example given, STI can give rise to ditches next to the active area 22. These ditches are formed during the etching back of the insulating layer formed in order to level the insulating layer in the trench to the same height as the active areas 22. When a memory stack, comprising a FG and a CG (see further), would be deposited onto the formed STI topography, this topography would remain due to conformal deposition of for example polysilicon layers. This problem can be overcome by preliminary removal of the STI topography, for example by using chemical mechanical polishing (CMP) after the deposition of a layer comprising FG material (see further). The STI topography will then not be introduced to the next layer(s).

In a next step, a tunnel oxide 26 is grown onto the active area 22 (Fig. 10). The tunnel oxide 26 may for example comprise silicon dioxide, and may preferably be formed by thermally growing it in an oxygen-steam ambient, at a temperature between about 600 to 1000°C, to a thickness between about 7 to 12 nm, preferably 8 nm. Alternatively, Rapid Thermal Oxidation (RTO) with in-situ steam generation (ISSG) can be used to obtain the tunnel oxide layer 26.

Then, on top of the structure so far obtained, a first conductive layer 27, which in an embodiment of the invention, may for example be polysilicon, and which will later on form the FG, is deposited. The deposition of the first conductive layer 27 may preferably be done by a CVD procedure, to a thickness between about 50 to 400 nm. Doping of the first
conductive layer 27 may either be accomplished in situ, during deposition, e.g. via the
addition of arsine or phosphine to a silane ambient, or via an ion implantation procedure,
using for example arsenic, phosphorous or boron ions applied to an intrinsic polysilicon
layer.

Next, FG slits (SFG) 28 (see Fig. 12) are patterned in the first conductive layer
27 by a common exposure step. A resist layer 29 is therefore applied on top of the first
conductive layer 27, as illustrated in Fig. 11, and some parts thereof (depending on the
desired pattern) are exposed. Subsequently, the non-exposed parts (or the exposed parts,
depending on the kind of resist used) are washed away, leaving behind a certain pattern of
resist, allowing layers not covered by the remaining resist layer to be etched away. In case the
first conductive layer 27 is a polysilicon layer, the etch comprises a polysilicon main etch
through this polysilicon layer, stopping on the STI 21. In that way, FGs 30 separated from
each other by the SFGs 28 are formed (Fig. 12). Before removing the remainder of the resist
layer 29, possible polymers and native oxide (not shown) are removed from the FG sidewalls
31. Next, the remainder of the resist layer 29 is removed, e.g. via plasma oxygen ashing and
careful wet cleaning. The result is illustrated in Fig. 12. According to the invention, SFGs 28
are formed such that they form long lines, i.e. lines longer than the width of a single memory
device, running from a first side of the substrate 20 to a second side of the substrate 20, the
first side being opposite to the second side, in a direction substantially perpendicular to the
direction of the second conductive layer from which the CG 32 (see further) will be formed.
The SFGs 28 are lying in a first plane and the second conductive layer, and hence the CG 32,
is substantially lying in a second plane, both the first and second plane being substantially
parallel to the plane of the substrate 20, as can be seen from Fig. 20.

During further processing, and illustrated in Fig. 13, a dielectric layer 33 is
deposited on top of the complete structure as obtained up to now and which is shown in
Fig. 12. According to an embodiment of the invention, the FG 30 and the CG 32 (see further)
may be polysilicon. In that case, the dielectric layer 33 lying in between the FG 30 and the
CG 32 may be called interpoly-dielectric (IPD). As, according to this invention, the FG 30
and CG 32 are preferably formed out of a polysilicon layer, in the further description the
dielectric layer 33 will be referred to as (IPD) 33. The IPD 33 preferably comprises a
plurality of insulating materials, e.g. an Oxide Nitride Oxide (ONO) layer, and may be
formed or grown by conventional techniques. An ONO layer preferably comprises successive
layers of silicon dioxide, silicon nitride and silicon dioxide. The total dielectric thickness of
the ONO layer may generally be between about 10 to 50 nm. The IPD may, however, also be
formed out of more advanced materials may be used such as e.g. HfO₂ or Al₂O₃. These materials show higher k-values than ONO, i.e. for a same thickness they give rise to a higher capacitance and hence, a higher CG-to-FG coupling, with respect to ONO.

After IPD formation, the IPD 33 is removed selectively at the sites where, later on, the AG 38 will be defined (see further). This is illustrated in Fig. 14 to 17. Fig. 14 shows a top view of the position of the mask 34 used for the IPD removal. Figs. 15-17 show cross-sections according to respectively XV-XV', XVI-XVI' and XVII-XVII' as indicated in Fig. 14. The local IPD removal may be done by for example applying a photo resist mask 34 to protect the IPD regions that will form the future stacked gate memory transistor or stacked gate transistor 35 i.e. that region where later on a FG/IPD/CG-stack 36 will be formed. For reliability reasons, a thin layer of a suitable material (not shown in the drawings), a so-called buffer layer, may be deposited on top of the IPD 33 prior to application of the photo resist mask 34. In this way, it is not necessary to do resist processing on top of the IPD 33, which could cause reliability hazards. Optionally, this buffer layer could even be used as a hard mask for the IPD etch. In the non-masked areas 37, where later the AG 38 will be formed, the IPD 33 is removed. That part of the first conductive layer 27 not covered by the photoresist mask 34, will form a first conductive part 38a of the AG 38. The removal of the IPD 33 may be done by any suitable means, e.g. by wet or dry etching, or by means of anisotropic etching. In that latter case, a problem may arise in that the IPD 33 is not completely removed from the FG sidewalls 31. This is, however, harmless, as the top surface of the first conductive layer 27 in the non-masked area 37 provides sufficient contact area with the conductive material of the CG 32 subsequently to be applied.

After the IPD etch and subsequent removal of the photo resist mask 34, a second conductive layer is deposited, from which the CG 32 will be formed during a subsequent FG/IPD/CG stack etch through which the FG/IPD/CG stack 36 and a second part 38b of the AG 38 are defined, as is illustrated in Figs. 18 to 21. The second conductive layer may preferably be polysilicon. In that case, and if the buffer layer used between the photoresist mask 34 and the IPD 33 is e.g. a thin polysilicon layer, this thin polysilicon layer does not have to be removed prior to deposition of the second conductive layer because it will just be part of the polysilicon layer forming the CG 32 in the FG/IPD/CG stack 36. Because of the FG/IPD/CG stack etch, a vertical misalignment in Fig. 14, i.e. a misalignment in the longitudinal direction of the SFGs 28, of the photoresist mask 34, used for the local removal of the IPD, is not critical as long as the edges of the mask 34 are between the future CG and AG lines, since the final gates are defined by the subsequent stack etch.
Fig. 18 shows a top view of a 2-T flash memory device array according to the present invention, while Fig. 19, 20 and 21 show cross-sections of the 2-T flash memory device array according to respectively cross-sections XIX-XIX’, XX-XX’ and XXI-XXI’ as indicated in Fig. 18. The dotted lines in Figs. 3, 19 and 21 indicate the conductive interface 40 between the first part 38a and the second part 38b of the AG 38 of the access gate transistor 39.

The flash memory device 50 may then be finished by methods known by a person skilled in the art such as side wall oxidation, formation of source 41 and drain 42, salicidation of the second conductive layer, which results in the formation of a salicide 43 on top of the FG/IPD/CG stack 36 of the stacked gate transistor 35 and on the AG 38 of the AG transistor 39. Furthermore, bit line contacts 44 and a common source line contact 45 may be provided (see Fig. 18 and 19). For the operation of the flash memory devices, the CFP mask to make contacts to the FG 30 is not necessary anymore, since the FG 30 is contacted by means of a ‘normal’ contact to the CG conductive material.

The above described process flow is only indicative and not limiting and in case of other applications, such as embedded applications, some additional steps or a different order of steps may be applied.

By removing the IPD 33 between the first 27 and second conductive layer in those areas where the AG 38 will be formed, the method according to the present invention thus provides a way to form a flash memory device 50 comprising an AG 38, whereby the AG 38 is formed in such a way that the it can cross an SFG 28 without causing an electrical open circuit. This allows to use long slits extending over the area of the substrate 20. The gate of the access transistors hence comprises a first part 38a and a second part 38b, respectively formed out of the first conductive layer 27 applied for forming the FG 30 and the second conductive layer applied for forming the CG 32. As can be seen from Fig. 21, SFG slits 28 crossing the AG 38 do not disconnect the AGs 38, as the material of the second conductive layer bridges the gaps.

Moreover, the approach according to this invention allows to salicidize the AG 38, thus enabling a longer stitch period for metal straps, yielding an improved efficiency. The AGs 38 are now intrinsically shunted by the salicidation of the CG 32, thus reducing the gate resistance significantly. This is an advantage with respect to methods according to the prior art, as in those cases salicidizing of the AG 32 could not be performed.

Although, according to the present invention, an additional mask is needed for the local removal of the IPD 33, the total mask count does not necessarily increase because,
contrary to prior art methods, a CFP mask can be skipped. Nevertheless, one could still need the CFP mask for making FG-to-CG capacitors in the periphery. However, alternatively back-end capacitors may be used instead.

It is to be understood that although preferred embodiments, specific constructions and configurations, as well as materials, have been discussed herein for devices according to the present invention, various changes or modifications in form and detail may be made without departing from the scope and spirit of this invention.

For example, the method of the invention may also be applied to arrays of memory devices with a NAND configuration which is different from the one described in the embodiments of this invention. In Fig. 22, an array of memory devices comprises alternately 8 stacked gate transistors, comprising a floating gate 30 and a control gate 32, and 2 access transistors comprising an access gate 38. The memory devices according to Fig. 22 are read out in block. It is to be understood that also in such a configuration the method of the invention may be applied in order to achieve the advantages of the invention, i.e. the use of long slits without causing an electrical open circuit.
CLAMS:

1. A method for the manufacturing of an array of 2-transistor memory devices (50), each memory device (50) comprising a stacked gate transistor (35) having a floating gate (30) and a control gate (32), and an access transistor (39) having an access gate (38), adjacent to each other in a first direction, the method comprising:
   - depositing a first conductive layer (27), and
   - patterning said first conductive layer (27) to form slits (28) for separating floating gates (30) adjacent to each other in a second direction, the second direction being different from the first direction,
   and wherein at least one of said slits (28) runs from one floating gate (30) to an adjacent floating gate (30) through a position occupied by the respective access gate (38).

2. A method according to claim 1, wherein all slits (28) run from one floating gate (30) to an adjacent floating gate (30) through a position occupied by the respective access gate (38).

3. A method according to claim 1, wherein the at least one slit (28) runs over substantially the complete width of the array.

4. A method according to claim 1, furthermore comprising:
   - depositing a dielectric layer (33) on top of the patterned first conductive layer (27) and in the slits (28),
   - depositing and patterning a second conductive layer to form the control gate (32).

5. A method according to claim 4, wherein forming the access transistors (39) is performed while forming the stacked gate transistors (35).

6. A method according to claim 5, wherein the access gate (38) is formed from the first conductive layer (27) and the second conductive layer.
7. A method according to claim 6, furthermore comprising, after depositing the dielectric layer (33) on top of the first conductive layer (27) and before depositing the second conductive layer, partially removing said dielectric layer (33) at that side of a stacked gate transistor (35) where the access gate (38) is to be formed.

8. An array of 2-transistor memory devices comprising:
- a plurality of stacked gate transistors (35), each stacked gate transistor (35) having a floating gate (30) and a control gate (32), adjacent floating gates (30) in a second direction being separated by slits (28),
- a plurality of access transistors (39), each access transistor (39) having an access gate (38), said access gate (38) being formed by a first conductive layer (27) and a second conductive layer electrically connected to each other, wherein at least one of said slits (28) runs form one floating gate (30) to an adjacent floating gate (30) in a first direction different from the second direction through a position occupied by the respective access gate (38).

9. An array according to claim 8, wherein all slits (28) run from one floating gate (30) to an adjacent floating gate (30) through a position occupied by the respective access gates (38).

10. An array according to claim 8, wherein the at least one slit runs over substantially the complete width of the array.
FIG. 1 - PRIOR ART

FIG. 2 - PRIOR ART

FIG. 3 - PRIOR ART

FIG. 4 - PRIOR ART
FIG. 16

FIG. 17
### INTERNATIONAL SEARCH REPORT

**A. CLASSIFICATION OF SUBJECT MATTER**

IPC 7  H01L27/115  H01L21/8247

According to International Patent Classification (IPC) or to both national classification and IPC.

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

IPC 7  H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched.

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

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Date of the actual completion of the international search: 6 September 2005

Date of mailing of the international search report: 14/09/2005

Name and mailing address of the ISA:

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