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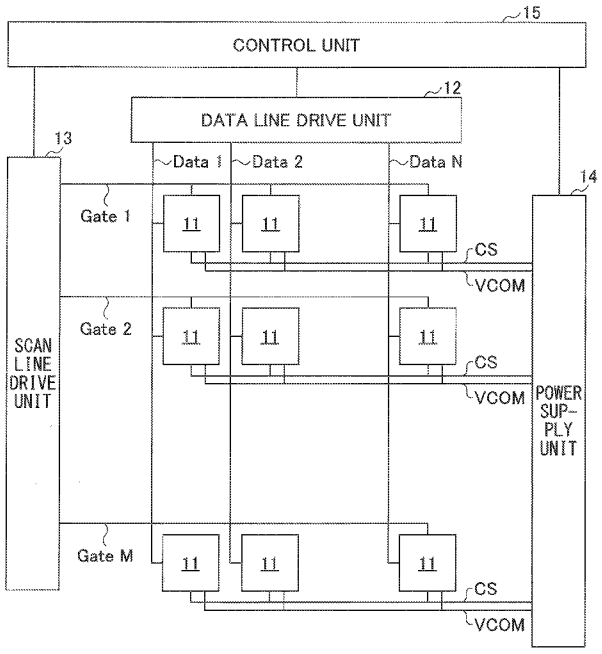

[Fig. 1]

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(57) Abstract: An electronic paper display (EPD) (10) and display method performed by an electronic paper display (10). An electronic paper display (10) comprises a plurality of pixels (11), a data line drive unit (12), a scan line drive unit (13), and a power supply unit (14). A pixel (11) includes a data hold unit (22) and a micro element (23), wherein when a scan line is activated. The micro element (23) includes a pixel electrode (24), a common electrode (25), and an electrophoresis element (26) intervening between the pixel electrode (24) and the common electrode (25). According to a voltage supplied to the micro element (23), charged particles included in the electrophoresis element (26) move toward the pixel electrode (24) or the common electrode (25), to thereby change an appearance of a pixel (11). The power supply unit (14) supplies a first constant voltage to the common electrode (25) in a predetermined number of sub-frames of the frame period, while it supplies a second constant voltage to the common electrode (25) in remaining sub-frames, the

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second constant voltage is different from the first constant voltage.

ELECTRONIC PAPER DISPLAY AND DISPLAY METHOD

TECHNICAL FIELD

[0001] Embodiments described herein relate to an electronic paper display and a display method.

BACKGROUND

[0002] Recently, electronic paper displays (EPDs) have become popular as devices to display information. Reasons why the electronic paper display (EPD) are preferred includes:

(1) Low power consumption: e.g., theoretically, it does not require electrical power to hold a display of some information such as letters, graphics or the like.

(2) Visibility: e.g., the view angle is wide. Because it does not need a backlight, it is easy to see even in a bright environment. As the display does not generate blue-light, it is safe for eyes.

(3) Portability: e.g., it is thin and light.

[0003] Electronic paper displays (EPDs) may be applied to a variety of applications in addition to E-books, such as tablets, digital signage, price tags, electronic shelf labels (ESL) or the like. In addition, electronic paper displays (EPDs) may be applied even to a field of education.

SUMMARY

[0004] Patent Document: Japanese Patent Publication No. 2008-262105

Patent Document: Japanese Patent Publication No. 2009-229853

[0005] Generally, the optical response rate in electronic paper displays (EPD) is slower than that of other display devices, such as liquid crystal displays (LCDs), organic light emitting diodes (OLED), ultra-light emitting diodes (uLED), or the like. Thus, conventional electronic paper displays (EPDs) might not be suitable for applications such as playing back movies which requires a high frame rate.

[0006] The embodiments of the invention as described in the present application provide EPDs that have increased display rates.

[0007] An embodiment in one aspect described herein provides an electronic paper display (EPD). The electronic paper display comprising:

a plurality of pixels;

a data line driver configured to supply data signals to a plurality of data lines which are coupled with the plurality of pixels;

a scan line driver configured to drive a plurality of scan lines which are coupled with the plurality of pixels; and

a power supplier configured to supply a predetermined voltage to the plurality of pixels;

wherein each pixel of the plurality of pixels includes a data hold unit and a micro element, wherein when a scan line coupled to the pixel is activated, the data hold unit receives the data signal from a data line coupled to the pixel and holds electrical charge;

wherein the micro element includes a pixel electrode, a common electrode, and an electrophoresis element intervening between the pixel electrode and the common electrode;

wherein according to a voltage supplied to the micro element by the data holder, charged particles included in the electrophoresis element move toward the pixel electrode or the common electrode, to thereby change an appearance of a pixel;

wherein during each sub-frame of a plurality of sub-frames which compose a frame period, the scan line driver drives the plurality of scan lines, and the appearance of the one or more pixels is changed in accordance with the frame period;

wherein the power supply unit supplies a first constant voltage to the common electrode in a predetermined number of sub-frames of the frame period, while it supplies a second constant voltage to the common electrode in remaining sub-frames, the second constant voltage being different from the first constant voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figure 1 illustrates an electronic paper display (EPD) according to an embodiment.

Figure 2 illustrates pixels in detail.

Figure 3 illustrates a timing chart for various signals that may be used in an electronic paper display (EPD).

Figure 4 illustrates exemplary optical response property for Ink voltage.

Figure 5 illustrates a relation between Ink voltage and response time.

Figure 6 illustrates a drawing for explaining a principle of overdrive technology.

Figure 7 illustrates a drawing for explaining a principle of overdrive technology.

Figure 8 illustrates a flowchart of operations according to an embodiment.

Figure 9 illustrates a timing chart for various signals that may be used in an electronic paper display (EPD) according to an embodiment.

Figure 10 illustrates a timing chart for various signals that may be used in an electronic paper display (EPD) according to an embodiment.

Figure 11 illustrates a relation between Ink voltage and response time.

Figure 12 illustrates effects according to an embodiment.

Figure 13 illustrates effects according to an embodiment.

Figure 14 illustrates effects according to another embodiment.

Figure 15 illustrates a variation when implementing an electronic paper display (EPD).

Figure 16 illustrates a variation when implementing an electronic paper display (EPD).

Figure 17 illustrates a variation when implementing an electronic paper display (EPD).

Figure 18 illustrates an electronic device in which an electronic paper display (EPD) according to an embodiment may be used.

DETAILED DESCRIPTION

[0009] Hereinafter, embodiments will be described with reference to the drawings. In the drawings, the same reference number or reference symbol is assigned to the same element.

[0010] Partitions in the following description are not essential for embodiments. Descriptions in two or more partitions may be combined, and descriptions in one of partitions may be applied to descriptions in another partition (unless contraindicated), if necessary.

[0011] <System Overview>

Figure 1 illustrates an electronic paper display (EPD) 10 according to an embodiment. The electronic paper display (EPD) includes a plurality of pixels 11, a data line drive unit 12, a scan line drive unit 13, a power supply unit, and a control unit 15.

[0012] When a scan line Gate i coupled to the pixel is activated, each pixel of the plurality of pixels 11 illustrates a display according to a data signal which is supplied from a data line Data j coupled to the pixel. Where, i is an index to indicate a scan line, and j is an index to indicate a data line (the same shall apply hereinafter).

[0013] The control unit 15 controls the data line drive unit 12 to supply data signals to a plurality of data lines Data 1 to Data N which are coupled with the plurality of pixels 11.

[0014] The control unit 15 controls the scan line drive unit 13 drives a plurality of scan lines Gate 1 to Gate M which are coupled with the plurality of pixels 11.

[0015] The control unit 15 controls the power supply unit 14 to supply a predetermined voltage to the plurality of pixels 11.

[0016] N and M may be any suitable positive integer. For examples, N and M may be hundreds, thousands or the like.

[0017] Figure 2 illustrates pixels in detail, more specifically, a partial equivalent circuit for the electronic paper display (EPD) 10 as depicted in Fig. 1. For the purpose of illustration, N=M=3 is used. However, other numerical values may be used in other embodiments.

[0018] Each pixel of the plurality of pixels 11 includes a transmission switch unit 21, a data hold unit 22, and a micro element 23.

[0019] The transmission switch unit 21 connects or disconnects between a data line Data j and a pixel node Pix i-j depending on whether the scan line Gate i coupled to the pixel is activated or deactivated. The transmission switch unit 21 may be composed using a thin film transistor (TFT), e.g., a N-type field effect transistor (FET) which a gate is coupled to the gate line Gate i, a source is coupled to the data line Data j, and a drain is connected to one end of the data hold unit 22. A P-type FET may be used in the other embodiments.

[0020] When a scan line Gate i coupled to the pixel is activated, the data hold unit 22 may receive a data signal from a data line Data j coupled to the pixel and hold electrical charge. Although theoretically the data hold unit 22 may be composed by one capacitor, an embodiment is not limited to such an example, and it may be composed by means of any suitable element which can hold electrical charge. One end of the data hold unit 22 is coupled to a pixel node Pix i-j, while other end of the data hold unit 22 is coupled to a voltage CS of a backplane (not shown) of the electronic paper display (EPD) 10. The backplane voltage CS is a common voltage for the plurality of pixels 11, and is supplied from the power supply unit 14.

[0021] The micro element 23 includes a pixel electrode 24, a common electrode 25, and an electrophoresis element 26 intervening between the pixel electrode 24 and the common electrode 25.

[0022] The electrophoresis element 26 includes at least first color particles which are electrically charged, and second color particles which are electrically charged. The second color is different from the first color. The first color particles may be composed of pigment which is negatively

charged. The second color particles may be composed of black pigment which is positively charged. The micro element 23 may be arranged in order to implement two-color electronic ink in a microcapsules scheme. The micro element 23 may be arranged in order to implement three-color electronic ink in a microcup scheme. The micro element 23 may be arranged by means of any suitable material such that an electronic ink using electrophoresis is implemented.

[0023] The pixel electrode 24 is coupled to the pixel node Pix i-j. The common electrode 25 is coupled to a common voltage VCOM which is common for the plurality of pixels 11. The common voltage VCOM is supplied from the power supply unit 14. In an embodiment, an electrode (not shown) providing the common voltage VCOM is located opposing to a backplane which provides the voltage CS, which may be referred to as an opposing electrode. Because the opposing electrode is electrically coupled to the backplane, the common voltage VCOM and the voltage CS are same.

[0024] In an embodiment, a side in which there is the opposing electrode supplying the common voltage VCOM is a side from which a user views the electronic paper display (EPD) 10. Thus, for example, if the common electrical voltage VCOM is set to 0 [V] and the voltage of the pixel node Pix i-j is positive, a side of the common electrical voltage VCOM is in a relatively low voltage, and positively charged particles (e.g., black pigment) are gathered, and so the pixel will appear to be black. Conversely, if the common electrical voltage VCOM is set to 0 [V] and the voltage of the pixel node Pix i-j is negative, a side of the common electrical voltage VCOM is in a relatively high voltage, and negatively charged particles (e.g., white pigment) are gathered, and so the pixel will appear to be white. However, an embodiment is not limited to such an example.

[0025] <Basic Operation>

When the data hold unit 22 holds an electrical charge, an electrical voltage due to the electrical charge is generated. According to the voltage, charged particles included in the electrophoresis element 26 move toward the pixel electrode or the common electrode due to electrophoresis. The resultant situation is reflected on a display of the pixel 11. The voltage causing the electrophoresis is an Ink voltage which is applied to the micro element 23, the Ink voltage is defined as a difference between a voltage of the pixel node Pix i-j and the common voltage VCOM. In addition, in a conventional technology, VCOM is always set to be 0 [V]. Thus, Ink voltage is expressed as follows:

$$\text{Ink voltage} = (\text{Pix i-j}) \quad \cdots (1)$$

Thus, the Ink voltage is equal to a voltage of a data signal Data* which is supplied from a data line. As long as there is no risk of confusion, Pix i-j may represent a pixel node or a voltage at the pixel node.

[0026] Figure 3 illustrates an exemplary timing chart for various signals that may be used in an electronic paper display (EPD) in Figure 1 and Figure 2. During each sub-frame of a plurality of sub-frames which compose a frame period, the scan line drive unit 13 drives the plurality of scan lines.

[0027] In an example as depicted in Fig. 3, the frame period includes 10 sub-frames. As one of examples, one sub-frame is 50 ms, and one frame period is 500 ms. The total number N of the scan lines Gate i is 3, and the total number M of the data lines Data j is 3. These specific numerical values are merely set for the purpose of illustration, and other numerical values may be used in the other embodiments.

[0028] At a timing t=t0, H-level voltage (15 [V] in an example as depicted in the figure) is applied to a data line Data*. In this example, the data signal Data* is supplied such that a black color is displayed. "*" is an index to distinguish a data line, corresponds to j in the above explanation, and equals to 1, 2 or 3 in the present situation. At the timing t=t0, any of scan line Gate i is not activated. 0 [V] is supplied in the common voltage VCOM (and CS).

[0029] As depicted in three rows on the lower side in Figure 3, scan lines Gate 1, Gate 2, and Gate 3 are sequentially activated for every sub-frame. The scan line's drive is performed instantaneously by means of a pulse. In this example, because one frame period includes 10 sub-frames, Gate 1 is driven 10 times during one frame period. Gate 2 and Gate 3 are also driven 10 times during one frame period. As one of examples for the purpose of operation illustration, we will focus on pixels in the second row. The pixel node voltage Pix 2-* at this timing is 0 [V].

[0030] In the first sub-frame t0 to t1 which is the first sub-frame of the first frame period t0 to t10, the voltages of pixel nodes of three pixels belonging to the second row are maintained at the same state (0 [V]) until the scan line Gate 2 is activated. When the scan line Gate 2 is activated, three pixels belonging to the second row receive data signals from their data line Data*, and the pixel node voltage Pix 2-* becomes the voltage of Data* (the H-level voltage of 15 [V] in the example as depicted in the figure 3). Thus, at the timing when the scan line Gate 2 is activated, the pixel node voltage Pix 2-* transitions from 0 [V] to 15 [V]. After that, the scan line Gate 2 is deactivated, and it stops receiving the data signal. Because the data hold unit 22 continues to hold the accumulated electrical charge, the pixel node voltage Pix 2-* is also maintained.

[0031] The situation in the second sub-frame t1 to t2 is also similar. The voltages of pixel nodes of three pixels belonging to the second row are maintained at the same state (15 [V]) until the scan line Gate 2 is activated. When the scan line Gate 2 is activated, three pixels belonging to the second row receive data signals from their data line Data*, and the pixel node voltage Pix 2-* becomes the voltage of Data* (the H-level voltage of 15 [V] in the example as depicted in the figure 3). After that, the scan line Gate 2 is deactivated, and it stops receiving the data signal. Because the data hold unit 22 continues to hold the accumulated electrical charge, the pixel node voltage Pix 2-* is also maintained.

[0032] After that, similar operations are performed. In the example as depicted in the figure 3, in the last sub-frame t9 to t10 of the first frame period, the voltages of pixel nodes of three pixels belonging to the second row are maintained at the same state (15 [V]) until the scan line Gate 2 is activated. In this sub-frame, Data* is maintained at 0 [V]. When the scan line Gate 2 is activated, three pixels belonging to the second row receive data signals from their data line Data*, and the pixel node voltage Pix 2-* becomes the voltage of Data* (0 [V] in the example as depicted in the figure 3). Thus, at the timing when the scan line Gate 2 is activated, the pixel node voltage Pix 2-* transitions from 15 [V] to 0 [V].

[0033] In this way, drive and display for one pixel is performed once for every one sub-frame and performed two or more times for every one frame period. As depicted in Figure 3, a switching of the appearance of the pixel (e.g., black to white, or vice versa) is performed according to the frame period. It should be noted that such a color switching is not performed for every sub-frame. Thus, drive and display for the pixel is performed two or more times for every one frame period.

[0034] In the example as depicted in the figure 3, at t=t10 which is a start timing of a second frame period, the voltage of the Data* is a L-level voltage of -15 [V]. In the second frame period t=t10 to t20, operations similar to the first frame period t=t0 to t10 are performed. However, in the second frame period, the data signal Data* is supplied such that a white color is displayed, which is different from that of the first frame period.

[0035] An appearance of the pixel is based on a voltage applied to the pixel, more specifically, Ink voltage (mathematical formula (1)) as described before.

$$\text{Ink voltage} = (\text{Pix i-j})$$

If the Ink voltage changes, the charged particle moves due to electrophoresis, and the appearance of the pixel will change.

[0036] Figure 4 illustrates exemplary optical response property (Response Time) for Ink voltage (Waveform). In the optical response property as depicted in Figure 4, 100 % corresponds to a state in which all pixels display white color while 0 % corresponds to a state in which all pixels display black color. In an example as depicted in Figure 4, a waveform of the Ink voltage is represented using rectangular wave. Specifically, white color is displayed in 0-2 seconds, then black color and white color alternate for every 4 seconds. Thus, one frame period is 4 seconds.

[0037] The optical response property as depicted in Figure 4 may be evaluated using "Rise time" and "Fall time". As one of examples, the Rise time may be defined as a time interval from 10 % to 90 % in the response outputs when a waveform which increases like a step function is applied. However, other definitions may be used in the other embodiments. As one of examples, the Fall time may be defined as a time interval from 90 % to 10 % in the response outputs when a waveform which decreases like a step function is applied. However, other definition may be used in the other embodiments.

[0038] Figure 5 illustrates Response time when the Ink voltage amplitude as depicted in Figure 4 changes from 5 [V] to 20 [V]. "Rise" indicates Rise time. "Fall" indicates Fall time. Rise time and Fall time tend to decrease as the Ink voltage increases. For example, when the Ink voltage amplitude is 5 [V], Rise time and Fall time are about 900 ms (about 1 second). When the Ink voltage amplitude is 20 [V], Rise time and Fall time are about 100 ms (= one ninth of time when 5 [V]). Thus, it is desirable to increase the Ink voltage amplitude in order to decrease response time.

[0039] In the example illustrated in Figure 3, the Ink voltage (Pix i-j) is equal to the voltage of the data signal Data*. Thus, "to increase the Ink voltage" means "to increase the voltage of the data signal Data*". The data signal Data* is supplied from the data line drive unit 12 (Figure 1), which is typically determined by means of a power supply voltage which is supplied to a Display Drive Integrated Circuit (DDIC). In an implementation, we have to pay attention to a withstand voltage for the Display Drive Integrated Circuit (DDIC). In an embodiment, the data signal amplitude is set to be 15 [V] (DDIC setting) from a point of view that the Ink voltage is as large as possible while taking the withstand voltage of the DDIC into account. An embodiment is not limited to this numerical example. Other numerical values may be used in the other embodiments.

[0040] <Overdrive technology >

In an embodiment, overdrive technology is used to further increase a display rate.

[0041] Figure 6 illustrates a drawing for explaining a principle of overdrive technology. For example, the dotted line shows a system that has a response property which changes like dot-line ("Normal Driving" in <Apply voltage> in Figure 6) when a rectangular waveform which changes like a step function ("Normal Driving" in <Repose time> in Figure 6) is applied to the system.

[0042] However, if a higher voltage is applied to the system ("Overdrive" in <Apply voltage> in Figure 6), the system responds in the manner shown by the solid line ("Overdrive" in <Repose time> in Figure 6). In other words, the response time may be shorted by transiently applying a higher voltage than its original one.

[0043] Figure 7 illustrates an example in which a principle of overdrive technology is applied to an Ink voltage. In the drawing, a waveform indicated as "Normal" is a waveform to which the overdrive technology has not been applied, which relates to Pix 2-* in the Figure 3. A waveform indicated as "Overdrive" is a waveform to which the overdrive technology has been applied. The waveform to display black color is modified as depicted in Figure 6. The waveform to display white color is modified in a different manner, and will be described in detail later.

[0044] <Operations when applying Overdrive technology>

Operations according to an embodiment will be described with reference to Figure 8 and Figure 9. Figure 8 illustrates a flowchart showing operations according to an embodiment. Figure 9 illustrates a timing chart for various signals that may be used in an electronic paper display as depicted in Figure 1 and Figure 2.

[0045] In the following descriptions about operations, it is assumed that a frame period includes 10 sub-frames. The total number N of the scan lines Gate i is 3, and the total number M of the data lines Data j is 3. These specific numerical values are merely set for the purpose of illustration, and other numerical values may be used in the other embodiments.

[0046] The flowchart in Figure 8 starts with step 801, and proceeds to step 802. At step 802, the common voltage VCOM is set to a predetermined overdrive voltage. As one of example, the overdrive voltage is -5 [V]. However, other numerical values may be used in the other embodiments. As depicted in Figure 9, in a predetermined number of sub-frames of the frame period, the common voltage VCOM is set to -5 [V]. This is done by supplying a first constant voltage (-5 [V] in this example) to the common electrode 25 (Figure 2) by means of the power supply unit 14 (Figure 1). As mentioned before, the voltage CS is equal to the common voltage VCOM.

[0047] The predetermined number of sub-frames of the frame period may be referred as "overdrive period", which is one sub-frame in this embodiment. The other numerical values may be used in the other embodiments. For example, the predetermined number may be 2. When taking a restriction such as the withstand voltage of the Display Drive IC (DDIC) into account, it may not be desirable for the predetermined number to be equal to or more than a majority of the total number of sub-frames included in the frame period.

[0048] At step 803 in Figure 8, drive and display for all pixels are performed.

[0049] At a timing t=t0 (Figure 9), H-level voltage (15 [V] in an example as depicted in the figure) is applied to data line Data*. In this example, the data signal Data* is supplied such that a black color is displayed. "*" is an index to distinguish a data line, and is equal to 1, 2 or 3 in the present situation. At the timing t=t0, any of scan line Gate i is not activated. -5 [V] is supplied in the common voltage VCOM (and CS). As one of examples for the purpose of operation illustration, we will focus on pixels in the second row. The common voltage VCOM (and CS) affects the pixel node voltage Pix 2-* due to coupling. Thus, the pixel node voltage Pix 2-* becomes -5 [V].

[0050] As depicted in three rows on the lower side in Figure 9, scan lines Gate 1, Gate 2, and Gate 3 are sequentially activated for every sub-frame. The scan line drive is performed instantaneously by means of a pulse. In this example, because one frame period includes 10 sub-frames, Gate 1 is driven 10 times during one frame period. Gate 2 and Gate 3 are also driven 10 times during one frame period.

[0051] In the first sub-frame t0 to t1, which is the first sub-frame of the first frame period t0 to t10, the pixel node voltages of three pixels belonging to the second row are maintained at the same state (-5 [V]) until the scan line Gate 2 is activated. When the scan line Gate 2 is activated, three pixels belonging to the second row receive data signals from their data line Data*, and the pixel node voltage Pix 2-* becomes the voltage of Data* (the H-level voltage of 15 [V] in the example as depicted in the figure 9). Thus, at the timing when the scan line Gate 2 is activated, the pixel node voltage Pix 2-* transitions from -5 [V] to 15 [V]. After that, the scan line Gate 2 is deactivated, and it stops receiving the data signal. Because the data hold unit 22 continues to be held the accumulated electrical charge, the pixel node voltage Pix 2-* is also maintained.

[0052] At step 804 in Figure 8, it is determined if the overdrive period is finished. Since the overdrive period is equal to an interval of one sub-frame, the operation flow proceeds to step 806 at the timing t=t1. If the overdrive period is equal to an interval of two sub-frames, the operation flow

proceeds to step 805 at the timing t=t1, operations already described are performed, then the operation flow proceeds to step 806 at the timing t=t2.

[0053] At step 806, the common voltage VCOM is set to a predetermined voltage. In a start timing t1 of the second sub-frame t=t1 to t2 as depicted in Figure 9, the common voltage VCOM (and CS) is set to 0 [V] before the scan line Gate 2 is activated yet. This is done by supplying a first constant voltage (0 [V] in this example) to the common electrode 25 (Figure 2) by means of the power supply unit 14 (Figure 1). The data hold unit 22 continues to hold the accumulated electrical charge. Thus, the pixel node voltage Pix 2-* increases from 15 [V] to 20 [V]. The three pixels belonging to the second row are maintained at the same state (20 [V]) until the scan line Gate 2 is activated.

[0054] At step 807 in Figure 8, drive and display for all pixels are performed. In the second sub-frame t1 to t2, when the scan line Gate 2 is activated, three pixels belonging to the second row receive data signals from their data line Data*, and the pixel node voltage Pix 2-* becomes the voltage of Data* (the H-level voltage of 15 [V] in the example as depicted in the figure 9). Thus, at the timing when the scan line Gate 2 is activated, the pixel node voltage Pix 2-* transitions from 20 [V] to 15 [V]. After that, the scan line Gate 2 is deactivated, and it stops receiving the data signal. Because the data hold unit 22 continues to hold the accumulated electrical charge, the pixel node voltage Pix 2-* is also maintained.

[0055] At step 808 in Figure 8, it is determined if all sub-frames belonging to one frame period is finished. Since it has not been finished yet at the timing t=t2, the operation flow proceeds to step 809.

[0056] In the third sub-frame t2 to t3, the three pixels belonging to the second row are maintained at the same state (15 [V]) until the scan line Gate 2 is activated. When the scan line Gate 2 is activated, three pixels belonging to the second row receive data signals from data their line Data*, and the pixel node voltage Pix 2-* becomes the voltage of Data* (the H-level voltage of 15 [V] in the example as depicted in the figure 9). After that, the scan line Gate 2 is deactivated, and it stops receiving the data signal. Because the data hold unit 22 continues to hold the accumulated electrical charge, the pixel node voltage Pix 2-* is also maintained.

[0057] With regard to from the third sub-frame t2 to t3 to the ninth sub-frame t8 to t9, steps 807, 808, and 809 of Figure 8 are repeated.

[0058] In the tenth sub-frame t9 to t10 which is the last sub-frame in the first frame period, the three pixels belonging to the second row are maintained at the same state (15 [V]) until the scan line Gate 2 is activated. In this sub-frame, Data* is maintained at 0 [V]. When the scan line Gate 2 is activated, three pixels belonging to the second row receive data signals from their data line Data*, and the pixel node voltage Pix 2-* becomes the voltage of Data* (0 [V] in the example as depicted in the figure 9). Thus, at the timing when the scan line Gate 2 is activated, the pixel node voltage Pix 2-* transitions from 15 [V] to 0 [V].

[0059] After step 807 for the tenth sub-frame, at step 808, it is determined if all sub-frames belonging to one frame period is finished. Since it has been finished at the timing t=t10, the operation flow proceeds to step 810.

[0060] At step 810, it is determined if all frame periods are finished. Since it has not been finished yet at the timing t=t10, the operation flow proceeds to step 802 through step 811. After that, with regard to the second frame period t=t10 to t20, operations of the steps 802 to 810 which have already described are performed. If all frame periods are finished, the flow proceeds to step 812, then the flow ends.

[0061] In the example as depicted in Figure 9, black color is displayed in the first frame period while white color is displayed in the second frame period. Thus, the voltage of the data signal Data* in the

first frame period has an opposite polarity to the voltage of the data signal Data* in the second frame period.

[0062] At the timing t=t10, which is the start timing of the second frame period, the common voltage VCOM (and CS) is set to the predetermined overdrive voltage (-5 [V]). In this example, the data signal Data* is supplied such that while color is displayed. L-level voltage (-15 [V] in an example as depicted in the figure) is applied to data line Data*. At the timing t=t10, any of scan line Gate i is not activated. The common voltage VCOM (and CS) affects the pixel node voltage Pix 2-* due to coupling. Thus, the pixel node voltage Pix 2-* becomes -5 [V].

[0063] In the first sub-frame t10 to t11 of the second frame period, the pixel node voltages of three pixels belonging to the second row are maintained at the same state (-5 [V]) until the scan line Gate 2 is activated. When the scan line Gate 2 is activated, three pixels belonging to the second row receive data signals from their data line Data*, and the pixel node voltage Pix 2-* becomes the voltage of Data* (the L-level voltage of -15 [V] in the example as depicted in the figure 9). Thus, at the timing when the scan line Gate 2 is activated, the pixel node voltage Pix 2-* transitions from -5 [V] to -15 [V]. After that, it stops receiving the data signal. Because the data hold unit 22 continues to hold the accumulated electrical charge, the pixel node voltage Pix 2-* is also maintained.

[0064] In a start timing t11 of the second sub-frame t=t11 to t12 of the second frame period, the common voltage VCOM (and CS) is set to 0 [V] before the scan line Gate 2 is activated yet. The data hold unit 22 continues to hold the accumulated electrical charge. Thus, the pixel node voltage Pix 2-* increases from -15 [V] to -10 [V]. The three pixels belonging to the second row are maintained at the same state (-10 [V]) until the scan line Gate 2 is activated.

[0065] In the second sub-frame t11 to t12, when the scan line Gate 2 is activated, three pixels belonging to the second row receive data signals from their data line Data*, and the pixel node voltage Pix 2-* becomes the voltage of Data* (the L-level voltage of -15 [V] in the example as depicted in the figure 9). Thus, at the timing when the scan line Gate 2 is activated, the pixel node voltage Pix 2-* transitions from -10 [V] to -15 [V]. After that, the scan line Gate 2 is deactivated, and it stops receiving the data signal. Because the data hold unit 22 continues to hold the accumulated electrical charge, the pixel node voltage Pix 2-* is also maintained.

[0066] With regard to from the third sub-frame t12 to t13 to the ninth sub-frame t18 to t19 in the second frame period, the steps 807, 808, and 809 in Figure 8 are repeated.

[0067] In the tenth sub-frame t19 to t20 which is the last sub-frame in the second frame period, the three pixels belonging to the second row are maintained at the same state (15 [V]) until the scan line Gate 2 is activated. In this sub-frame, Data* is maintained at 0 [V]. When the scan line Gate 2 is activated, three pixels belonging to the second row receive data signals from their data line Data*, and the pixel node voltage Pix 2-* becomes the voltage of Data* (0 [V] in the example as depicted in the figure 9). Thus, at the timing when the scan line Gate 2 is activated, the pixel node voltage Pix 2-* transitions from -15 [V] to 0 [V].

[0068] As described before, an appearance of the pixel is based on the Ink voltage which is applied to the micro element 23 of the pixel:

$$\text{Ink voltage} = (\text{Pix i-j}) - \text{VCOM} \quad \cdots (2)$$

[0069] In the conventional technology, the VCOM was always set to be 0. However, in the example as depicted in Figure 9, the common voltage VCOM (and CS) is -5 [V] in the overdrive period, and is 0 [V] in the other periods. As depicted in Figure 9, in the first sub-frame and the second sub-frame, the waveform of the Ink voltage indicates 20 [V] which is greater than the voltage of the data signal Data*. Such a voltage waveform strongly affects the electrophoresis of the charged particles, thereby the response time (Fall time) for the display of black color can be shorted.

[0070] In this example, when the scan line Gate 2 is activated, three pixels belonging to the second row receive data signals from their data line Data*. The data signals from the data lines Data 1, Data 2, and Data 3 are not necessarily same. For example, Data 1 may be a data signal for black color while Data 2 may be a data signal for white color (Figure 10).

[0071] However, the common voltage VCOM (and CS) is common for all pixels. Thus, it is impossible to simultaneously apply the overdrive technology to both a pixel displaying black color and a pixel displaying white color (pixels Pix 2-1 and Pix 2-2 in Figure 10).

[0072] As described with reference to Figure 4, a transition time from white color to black color is evaluated by means of the Fall time in an optical response property represented with reflectivity. A transition time from black color to white color is evaluated by means of the Rise time in an optical response property represented with reflectivity. In order to increase a display rate in a pixel, it is required to decrease the Rise time and/or the Fall time which define(s) the response property.

[0073] More specifically, by applying the overdrive technology to the transition from white color to black color, Fall time in the optical response property may be shorted. In this case, the overdrive technology is not applied to the transition from black color to white color (No-overdrive). Technologically, the overdrive technology can be reversely applied. That is, by applying the overdrive technology to the transition from black color to white color, the Rise time in the optical response property may be shorted. In this case, the overdrive technology is not applied to the transition from white color to black color (No-overdrive).

[0074] "Whether it is better to improve the Rise time or the Fall time" may be appropriately determined depending on the system to be used, particularly materials to be used for charged particles. In case of the system to be used in the example as depicted in Figure 9, there is a certain relation between the Ink voltage amplitude and the optical response time as depicted in Figure 11 (the graph itself in Figure 11 is same as that of Figure 5). The Rise time and the Fall time tend to decrease as the Ink voltage increases. In an embodiment, the data signal amplitude is set to be 15 [V] (DDIC setting) from a point of view that the Ink voltage is as large as possible while taking the withstand voltage of the Display Drive IC (DDIC) into account.

[0075] As depicted in Figure 11, the Rise time (Rise) and the Fall time (Fall) are not necessarily same. When the data signal amplitude is 15 [V], the Rise time is about 100 ms while Fall time is about 200ms, the latter is longer than the former. Thus, in such a system, it is more desirable to improve the Fall time (Fall) than the Rise time (Rise). Thus, in the embodiment as depicted in Figure 9, it is intended to decrease the Fall time in the optical response property by applying the overdrive technology to the transition from white color to black color.

[0076] <Effects of Embodiments>

Figure 12 illustrates effects according to such an embodiment. With regard to Rise time (right side) and Fall time (left side), case 1 in which the overdrive technology is not applied (No Overdrive) and case 2 in which the overdrive technology is applied (5V Overdrive) are shown. As depicted with two arrows in right side in the figure, they tend to be similar for Rise time. However, as depicted with two arrows in left side in the figure, case 2 is shorter than case 1 with regard to Fall time.

[0077] Figure 13 illustrates effects according to an embodiment in terms of contrast comparison. Contrast may be represented as (brightness of white color)/(brightness of white color). As depicted in the figure, contrast is improved from 10.7 to 13.29 by applying the overdrive technology. In terms of Ghost elimination or the like, it is preferred to use a higher contrast.

[0078] Figure 14 illustrates effects according to another embodiment. In this example, Rise time is improved. Rise time is improved from 130 ms to 110 ms by applying the overdrive technology to the transition from black color to white color.

[0079] <Variations>

Figures 15-17 illustrate variations when implementing an electronic paper display (EPD).

[0080] "Panel" represents a display panel which mainly corresponds to an array of pixels 11 in Figure 1.

"DDIC" represents a Display Drive Integrated Circuit which mainly corresponds to the data line drive unit 12 in Figure 1.

"TCON" represents a timing controller which mainly corresponds to the control unit 15 in Figure 1.

"VCOM Control Switch" (VCS) represents a component to supply the common voltage VCOM to the pixels, which functions as a switch to selectively supply 0 or -5 [V] depending on a sub-frame.

"Power" is a power supply to supply a voltage of 0 or -5 [V]. The VCOM Control Switch (VCS) and the power supply (Power) mainly correspond to the power supply unit 14 in Figure 1.

[0081] In the example as depicted in Figure 15, the timing controller (TCON), the VCOM Control Switch (VCS) and the power supply (Power) are implemented on a print circuit board (PCB). The Display Drive IC (DDIC) is implemented on a Flexible Printed Circuits (FPC) which is located between the Panel and the PCB.

[0082] In the example as depicted in Figure 16, the VCOM Control Switch (VCS) is incorporated into the Display Drive IC (DDIC). Thus, it is possible to decrease the number of components implemented on the print circuit board (PCB).

[0083] In the example as depicted in Figure 17, a component which supplies the voltage of -5 [V] is also incorporated into the Display Drive IC (DDIC). That is, with regard to components which allow to perform functions according to the embodiments, they are incorporated into the Display Drive IC (DDIC). Thus, the number of components implemented on the print circuit board (PCB) may be comparable to the conventional structure.

[0084] In the example as depicted in Figure 15, the Display Drive IC (DDIC) may be implemented by means of a general product. This is preferred in terms of a short development interval of EPD products.

In the example as depicted in Figure 17, since a dedicated and optimized Display Drive IC (DDIC) can be used, it is preferred in terms of easy implementation.

[0085] <System architecture>

Figure 18 illustrates an electronic device 100 in which an electronic paper display (EPD) according to an embodiment may be used. The electronic device 101 may include a bus 110, a processor 120, a memory 130, an input/output interface 150, a display 160, and a communications interface 170. In some implementations, the electronic device 101 may omit at least one of the foregoing elements or may further include another element.

[0086] The bus 110 may include circuitry, such as, that interconnects the components 110-170 and delivers communications (such as control messages and/or data).

[0087] The processor 120 may include one or more central processing units (CPU), an application processor (AP), and/or a communication processor (CP). For example, the processor 120 may perform an operation or data processing related to control and/or communication of at least another component of the electronic device 101.

[0088] Memory 130 may include volatile memory and/or non-volatile memory. The memory 130 may store, for example, an instruction or data related to at least another component of the electronic device 101. Based on one implementation, the memory 130 may store software and/or programs. The program may include a kernel (Core) 141, a middleware 143, an application programming interface API 145, and/or an application program (or "application") 147. At least some of the kernel 141, the middleware 143, and the API 145 may be referred to as an operating system (OS).

[0089] The kernel 141 may control or manage, for example, system resources (such as the bus 110, the processor 120, and the memory 130) for performing operations or functions implemented in other programs (such as the middleware 143, the API 145, and the application program 147). In addition, the kernel 141 may provide an interface, and the middleware 143, API 145 or the application program 147 may access separate elements of the electronic device 101 by using the interface to control or manage system resources.

[0090] For example, middleware 143 may be used as an intermediary to allow API 145 or application 147 to communicate with kernel 141 to exchange data.

[0091] The middleware 143 may process, based on priorities of the task requests, the one or more tasks requests received from the application program 147. For example, the middleware 143 may allocate, to at least one of the application programs 147, a priority of a system resource (such as the bus 110, the processor 120, and the memory 130) used for using the electronic device 101. For example, the middleware 143 may perform scheduling or load balancing for one or more tasks requests by processing the one or more tasks requests based on the priorities assigned to the task requests.

[0092] The API 145 is an interface used by the application 147 to control functions provided by the kernel 141 or the middleware 143, and may include, for example, at least one interface or function (such as instructions) for file control, window control, image processing, or text control.

[0093] The input/output interface 150 may serve as, for example, an interface to transfer an instruction or data input from a user or another external device to another (other) element of the electronic device 101. In addition, the input/output interface 150 may output an instruction or data received from another (other) element of the electronic device 101 to a user or another external device.

[0094] The display 160 may include, for example, a liquid crystal display (LCD or IXD), a light emitting diode (LED) display, an organic light emitting diode (OLED) display, a micro-electro-mechanical system (MEMS) display, and an electronic paper display (EPD). As the electronic paper display (EPD), the electronic paper display (EPD) 10 according to the embodiments may be used. Display 160 may display various types of content (such as a text, an image, a video, an icon, or a symbol) to a user. The display 160 may include a touchscreen and receive touch input, posture input, proximity input or hover input, such as using an electronic pen or a part of the body of a user.

[0095] For example, the communications interface 170 may establish communication between the electronic device 101 and an external device (such as a first external electronic device 102, a second external electronic device 104, or a server 106). For example, the communications interface 170 may be connected to the network 162 through wireless or wired communication, to communicate with the external device (such as the second external electronic device 104 or the server 106).

[0096] The wireless communication may use, for example, at least one of the following as a cellular communication protocol: such as long term evolution (LTE), high level LTE (LTE-A), code division multiple access (CDMA), wideband CDMA (WCDMA), universal mobile telecommunications system (UMTS), wireless broadband (WiBro), and global mobile telecommunications system (GSM). In addition, wireless communications may include, for example, short-range communications 164. The short-range communication 164 may include at least one of the following: for example, Wi-Fi, Bluetooth®, near field communication (NFC), and global navigation satellite system (GPS). The wired communication may include at least one of the following: for example, a universal serial bus (USB), a high-definition multimedia interface (HDMI), a recommendation standard 232 (RS-232), and a plain old telephone service (POTS). The network 162 may include at least one of the following: a communications network (such as a computer network (such as a LAN or a WAN)), the Internet, and a telephony network.

[0097] The first external electronic device 102 and the second external electronic device 104 may be devices of a same type or different types as the electronic device 101. Based on one implementation, the servers 106 may include a group having one or more servers. In various implementations, all or some of the operations performed in the electronic device 101 may be performed in another electronic device or a plurality of electronic devices (such as the electronic device 102 or 104 or server 106).

[0098] The electronic device 101 may include a motion sensor 190. The motion sensor is electrically connected to the processor 120, and obtains motion information of the electronic device 120. The motion sensor 190 may include at least one of the following: a linear acceleration sensor, a gyro sensor, and a geomagnetic sensor, which may sense linear acceleration, rotational angular acceleration or orientation information of the electronic device. The electronic device 101 may obtain motion information of the electronic device 101 based on an output value from a sensor. For example, the electronic device 101 may obtain the linear acceleration of the electronic device 101 based on an output value from the linear acceleration sensor. The electronic device 101 may obtain the rotational angular acceleration of the electronic device 101 based on an output value from a gyro sensor. The electronic device 101 may obtain the motion orientation information of the electronic device 101 based on an output value from each of the gyro sensor and the geomagnetic sensor.

[0099] In various implementations of this application, the processor 120 may be electrically connected to a display 160. In addition, the processor 120 may be electrically connected to a memory 130. The memory 130 may store instructions to instruct the processor 120 to perform inertial force correction to remove an inertial force component from the obtained motion information, and display a screen corresponding to the inertial force corrected motion information.

[0100] In various implementations of this application, the memory 130 may further store an instruction used to instruct, when the instruction is executed, the processor 120 to perform the following operations: obtaining an inertial component.

[0101] In various implementations of this application, the communications module 170 may receive an inertial component from another electronic device physically separate from the electronic device, and sense the inertial component.

[0102] In various implementations of this application, the memory 130 may further store an instruction used to instruct, when the instruction is executed, the processor 120 to perform the following operations: generating a correction vector by adding an inverse vector of the inertial acceleration corresponding to the inertial force and the acceleration corresponding to the motion information; and control display 160 to display the screen corresponding to the generated correction vector.

[0103] In various implementations of this application, the memory 130 may further store an instruction that is used to instruct, when the instruction is executed, the processor 120 to perform the following operations: obtaining a biometric measurement signal from at least one body part of the user when the user moves the electronic device; and removing an inertial component corresponding to the motion information obtained when the biometric measurement signal is not obtained. The electronic device 101 may further include a sensor. The sensor may obtain a biological measurement signal, and the processor 120 may obtain a biological measurement signal from the biological measurement signal sensor.

[0104] The method described in the embodiments of this application may be applied to a processor or may be implemented by a processor. The processor 930 may be an integrated circuit chip and has a signal processing capability. In an embodiment process, steps in the foregoing methods can be implemented by using a hardware integrated logical circuit in the processor, or by using instructions in a form of software. The foregoing processor may be a general purpose processor, a digital signal processor (Digital Signal Processing, DSP), an application-specific integrated circuit (Application Specific Integrated Circuit, ASIC), a field-programmable gate array (Field-Programmable Gate Array, FPGA) or another programmable logic device, a discrete gate or a transistor logic device, or a discrete hardware component. The processor may implement or perform the methods, the steps, and logical block diagrams that are described in the embodiments of this application. The general purpose processor may be a microprocessor, or the processor may be any conventional processor or the like.

Steps of the methods described with reference to the embodiments of this application may be directly executed and accomplished by using a hardware decoding processor, or may be executed and accomplished by using a combination of hardware and software modules in the decoding processor. A software module may be located in a mature storage medium in the art, such as random access memory, flash memory, read-only memory, programmable read-only memory, electrically erasable programmable memory, or a register. The storage medium is located in the memory, and a processor reads information in the memory and completes the steps of the foregoing methods in combination with hardware of the processor. All or some of the foregoing embodiments may be implemented by using software, hardware, firmware, or any combination thereof. When software is used to implement the embodiments, the embodiments may be implemented completely or partially in the form of a computer program product.

[0105] The computer program product includes one or more computer instructions. When the computer program instructions are loaded and executed on the computer, the procedure or functions according to the embodiments of this application are all or partially generated. The computer may be a general-purpose computer, a dedicated computer, a computer network, or other programmable apparatuses. The computer instructions may be stored in a computer readable storage medium or may be transmitted from a computer readable storage medium to another computer readable storage medium. For example, the computer instructions may be transmitted from a website, computer, server, or data center to another website, computer, server, or data center in a wired (for example, a coaxial cable, an optical fiber, or a digital subscriber line (DSL)) or wireless (for example, infrared, radio, or microwave) manner. The computer readable storage medium may be any usable medium accessible by a computer, or a data storage device, such as a server or a data center, integrating one or more usable media. The usable medium may be a magnetic medium (for example, a floppy disk, a hard disk, or a magnetic tape), an optical medium (for example, a DVD), a semiconductor medium (for example, a solid state disk (Solid State Disk, SSD)), or the like.

[0106] In the several embodiments provided in this application, it should be understood that the disclosed system, apparatus, and method may be implemented in other manners. For example, the described apparatus embodiment is merely an example. For example, the unit division is merely

logical function division and may be other division in actual embodiment. The indirect couplings or communication connections between the apparatuses or units may be implemented in electronic, mechanical, or another form.

[0107] The units described as separate parts may or may not be physically separate, and parts displayed as units may or may not be physical units, and may be located in one position, or may be distributed on a plurality of network units. Some or all of the units may be selected based on actual requirements to achieve the objectives of the solutions of the embodiments.

[0108] In addition, function units in the embodiments of this application may be integrated into one processing unit, or each of the units may exist alone physically, or two or more units may be integrated into one unit. The integrated unit may be implemented in a form of hardware, or may be implemented in a form of a software function unit.

[0109] When the integrated unit is implemented in the form of a software function unit and sold or used as an independent product, the integrated unit may be stored in a computer readable storage medium. Based on such an understanding, the technical solutions of this application essentially, or the part contributing to the prior art, or all or some of the technical solutions may be implemented in the form of a software product. The computer software product is stored in a storage medium and includes several instructions for instructing a computer device (which may be a personal computer, a server, or a network device) to perform all or some of the steps of the methods described in the embodiments of this application. The foregoing storage medium includes any medium that can store program code, such as a USB flash drive, a removable hard disk, a read-only memory (Read-Only Memory, ROM), a random access memory (Random Access Memory, RAM), a magnetic disk, or a compact disc.

[0110] The foregoing embodiments are merely intended for describing the technical solutions of this application, but not for limiting this application. Although this application is described in detail with reference to the foregoing embodiments, persons skilled in the art should understand that they may still make modifications to the technical solutions described in the foregoing embodiments or make equivalent replacements to some technical features thereof, without departing from the spirit and scope of the technical solutions of the embodiments of this application.

LIST OF REFERENCE SYMBOLS

[0111] 10 Electronic paper display

11 Pixel

12 Data line drive unit

13 Scan line drive unit

14 Power supply unit

15 Control unit

CLAIMS

1. An electronic paper display comprising:

a plurality of pixels;

a data line driver configured to supply data signals to a plurality of data lines which are coupled with the plurality of pixels;

a scan line driver configured to drive a plurality of scan lines which are coupled with the plurality of pixels; and

a power supplier configured to supply a predetermined voltage to the plurality of pixels;

wherein each pixel of the plurality of pixels includes a data holder and a micro element, wherein when a scan line coupled to the pixel is activated, the data holder receives the data signal from the data line coupled to the pixel and holds electrical charge;

wherein the micro element includes a pixel electrode, a common electrode, and an electrophoresis element intervening between the pixel electrode and the common electrode;

wherein according to a voltage supplied to the micro element by the data holder, charged particles included in the electrophoresis element move toward the pixel electrode or the common electrode, to thereby change an appearance of a pixel;

wherein during each sub-frame of a plurality of sub-frames which compose a frame period, the scan line driver drives the plurality of scan lines, and the appearance of the one or more pixels is changed in accordance with the frame period;

wherein the power supplier supplies a first constant voltage to the common electrode in a predetermined number of sub-frames of the frame period, while it supplies a second constant voltage to the common electrode in remaining sub-frames, the second constant voltage being different from the first constant voltage.

2. The electronic paper display according to claim 1, wherein the charged particles include positively charged black pigment and negatively charged white pigment which are used for two-color ink in a microcapsules scheme.

3. The electronic paper display according to claim 1, wherein the first constant voltage is determined such that the common electrode attracts positively charged particles.

4. The electronic paper display according to claim 1, wherein the data line driver and the scan line driver are included in a display drive integrated circuit (DDIC).

5. The electronic paper display according to claim 1, wherein the data line driver, the scan line driver and the power supplier are included in a display drive integrated circuit (DDIC).

6. Display method performed by an electronic paper display, the elector paper display comprising:

a plurality of pixels;

a data line driver configured to supply data signals to a plurality of data lines which are coupled with the plurality of pixels;

a scan line driver configured to drive a plurality of scan lines which are coupled with the plurality of pixels; and

a power supplier configured to supply a predetermined voltage to the plurality of pixels;

the method comprising:

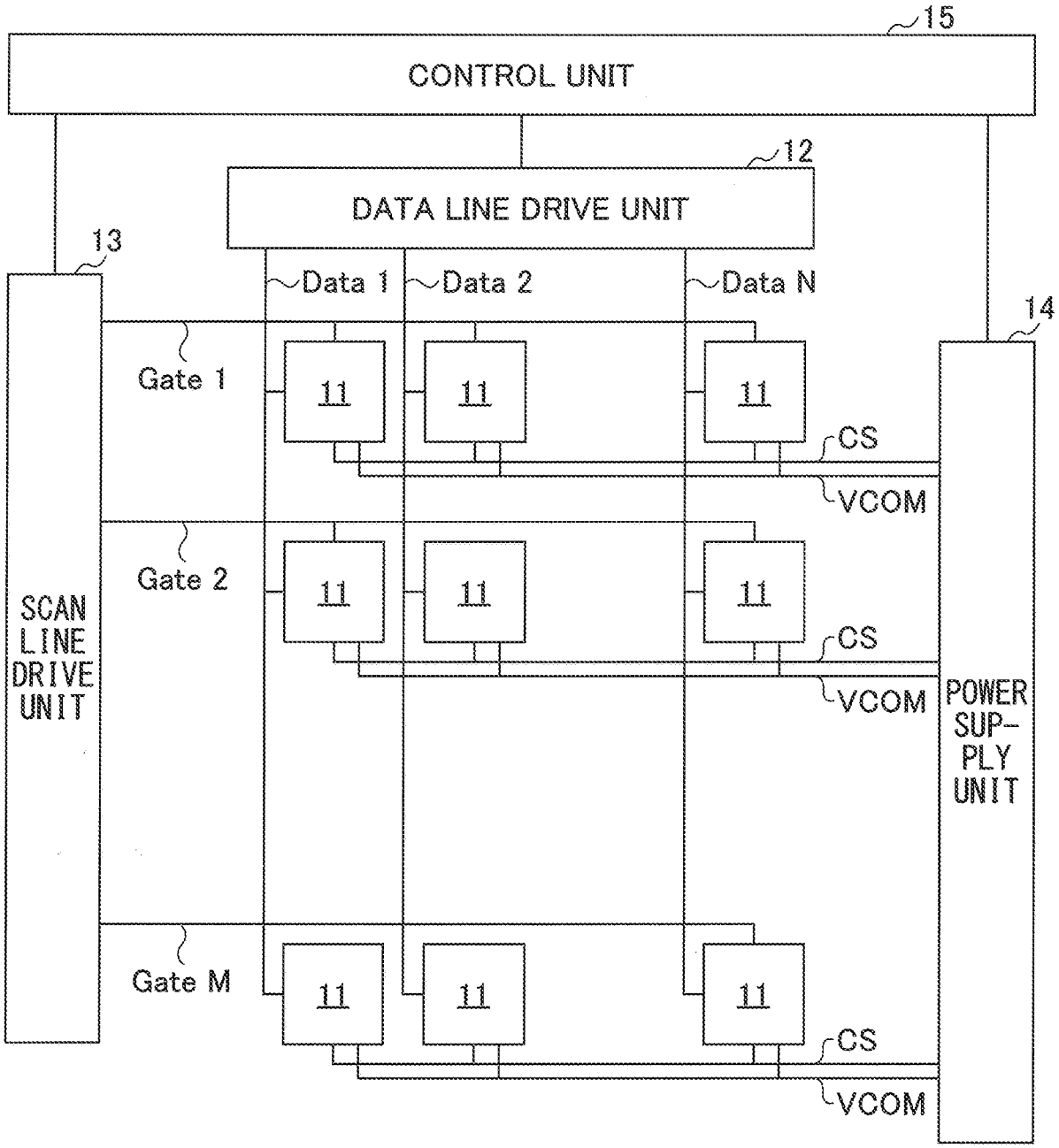
during each sub-frame of a plurality of sub-frames which compose a frame period, by the scan line driver, driving the plurality of scan lines;

wherein each pixel of the plurality of pixels includes a data holder, wherein when a scan line coupled to the pixel is activated, the data holder receives the data signal from a data line coupled to the pixel and holds electrical charge;

wherein according to a voltage which is held in the data holder, charged particles which are included in an electrophoresis element move toward the pixel electrode or the common electrode, to thereby change an appearance of a pixel, wherein the electrophoresis element intervenes between the pixel electrode and the common electrode;

wherein the appearance of the one or more pixels is changed in accordance with the frame period; and

wherein the power supplier supplies a first constant voltage to the common electrode in a predetermined number of sub-frames of the frame period, while it supplies a second constant voltage to the common electrode in remaining sub-frames, the second constant voltage being different from the first constant voltage.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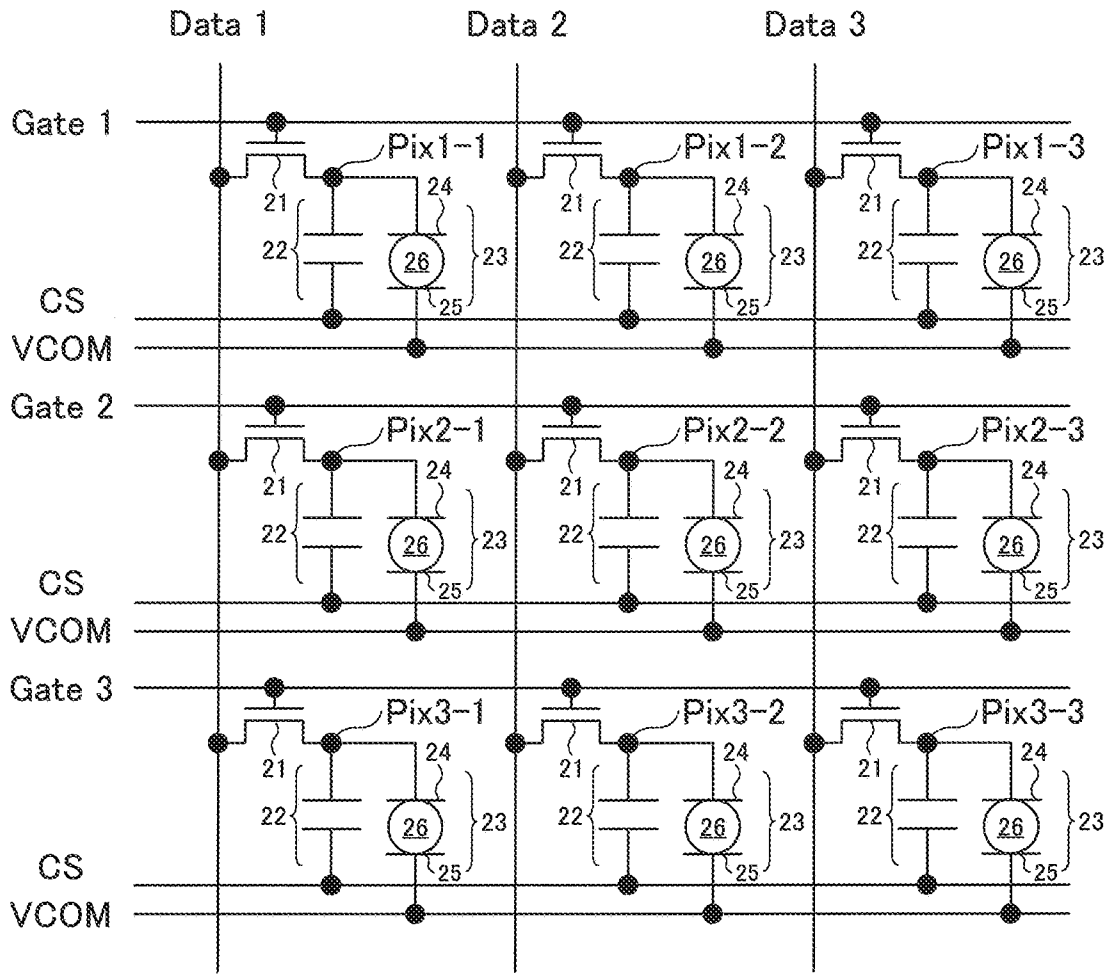
12
DATA LINE DRIVE UNIT
13
Data 1
Data 2
Data N
14
Gate 1
Gate 2
Gate M
11
CS
VCOM
SCAN LINE DRIVE UNIT
POWER SUP-PLY UNIT

10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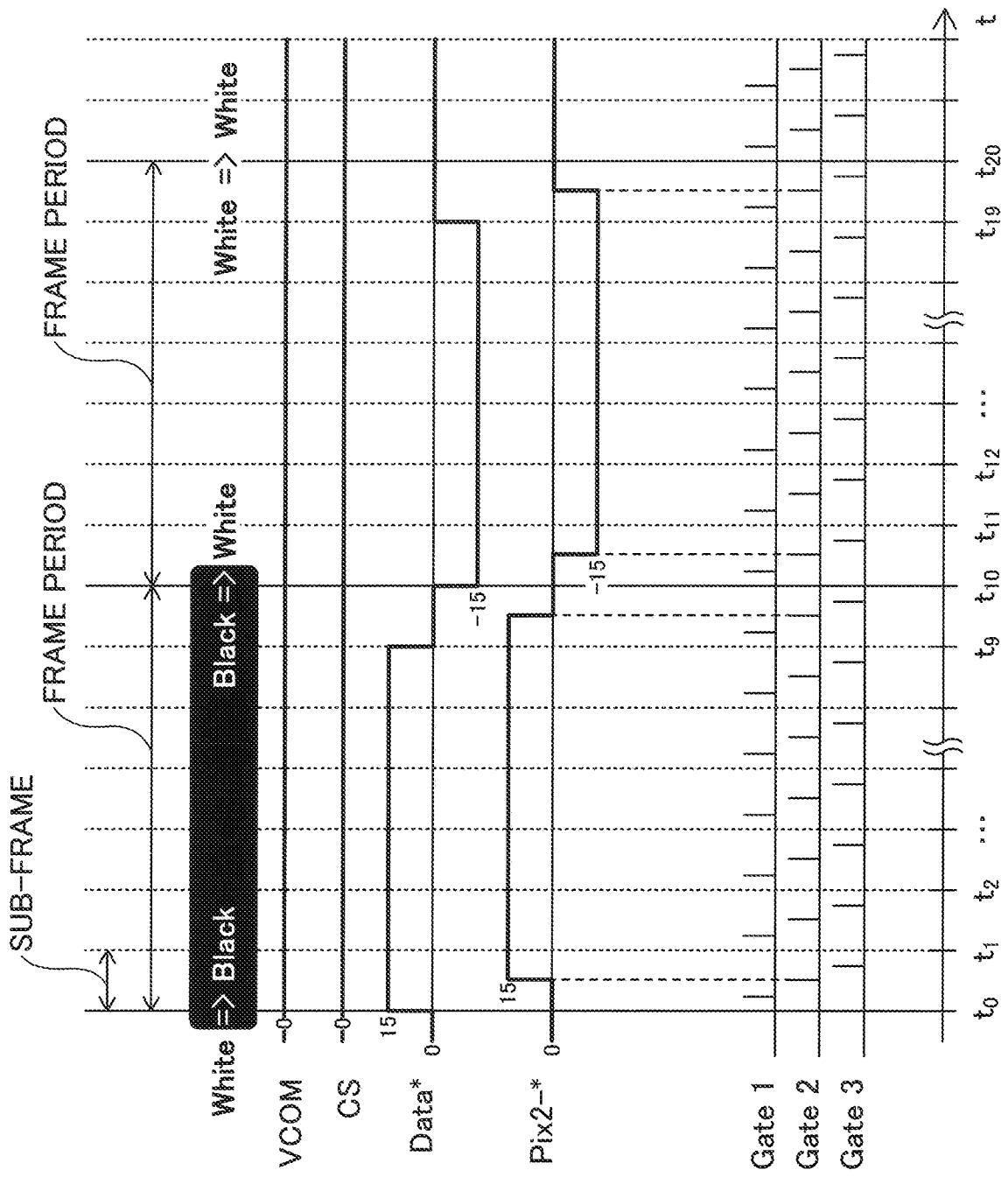
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FRAME PERIOD
FRAME PERIOD
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Black => White
White => White
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Gate 2
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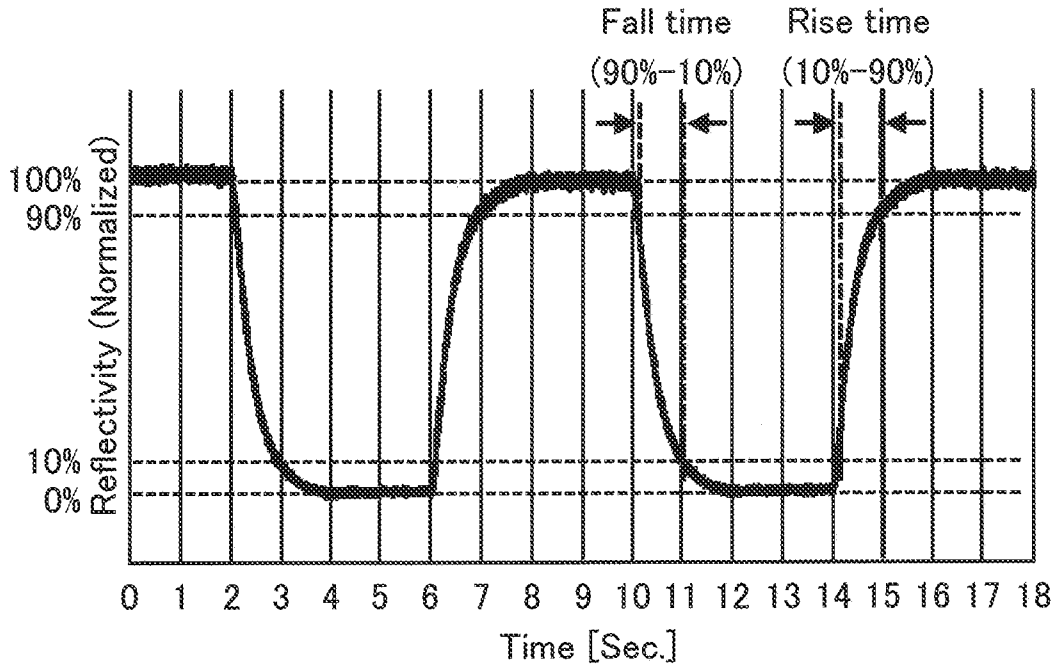

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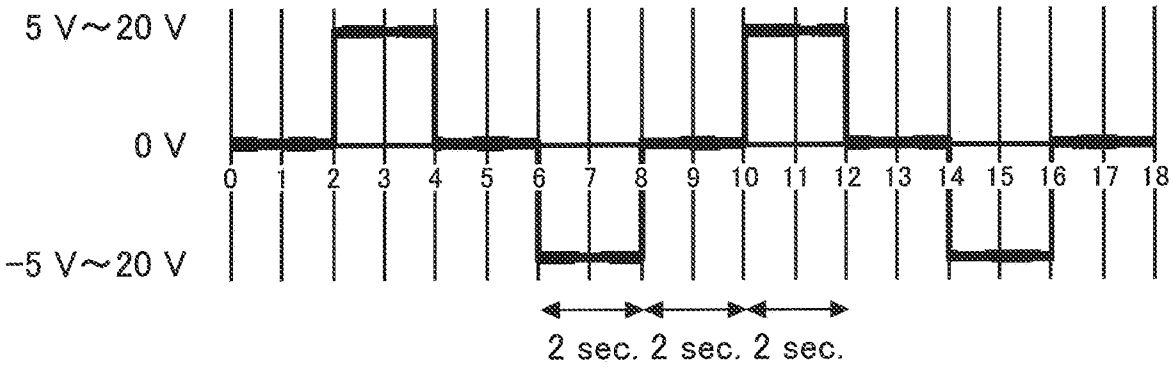

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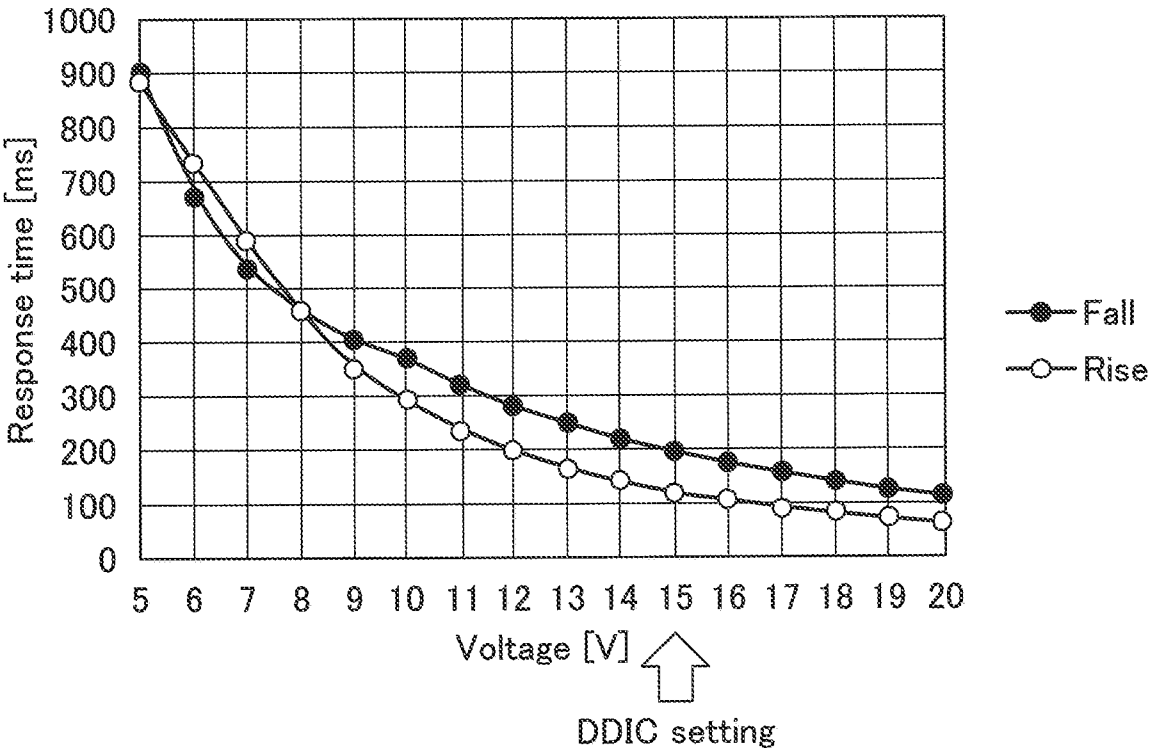
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900
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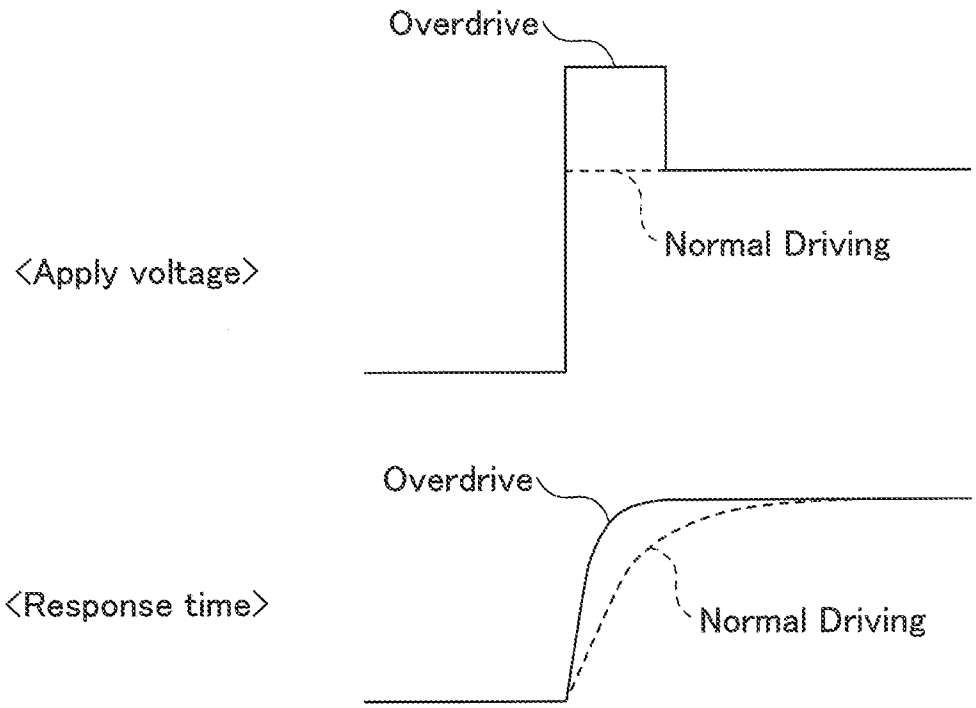
Voltage [V]
DDIC setting
Fall
Rise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Normal Driving
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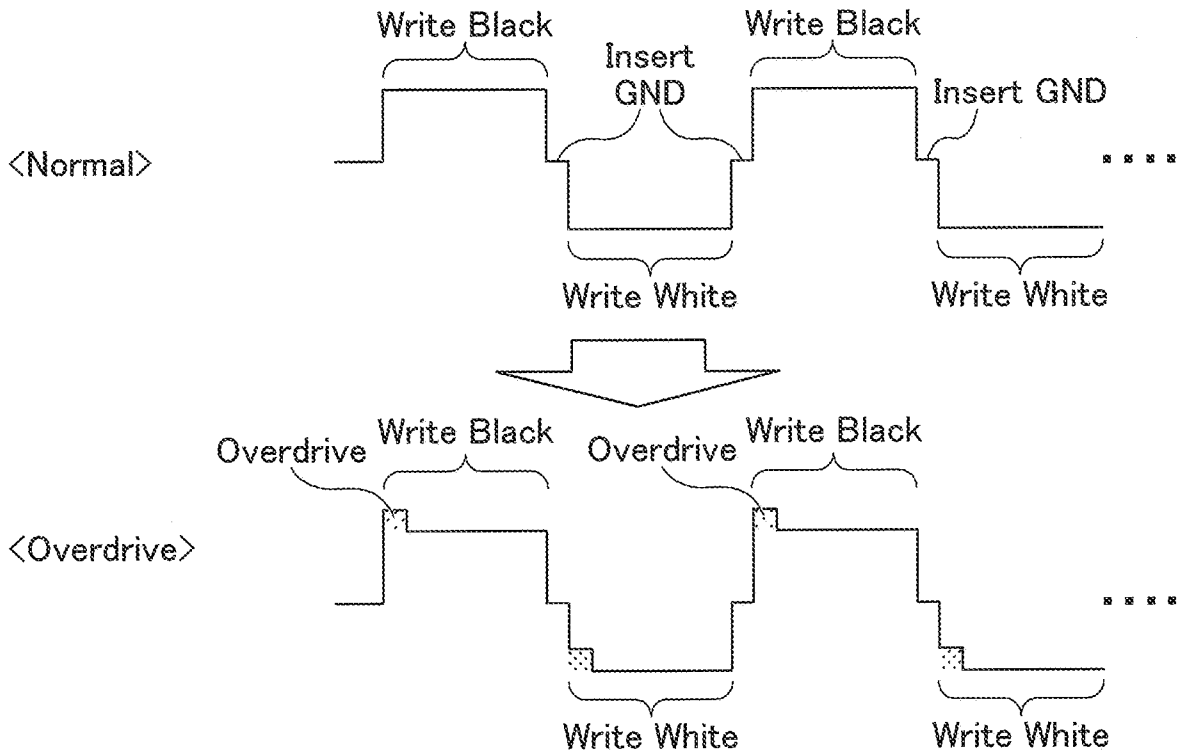
【Fig. 7】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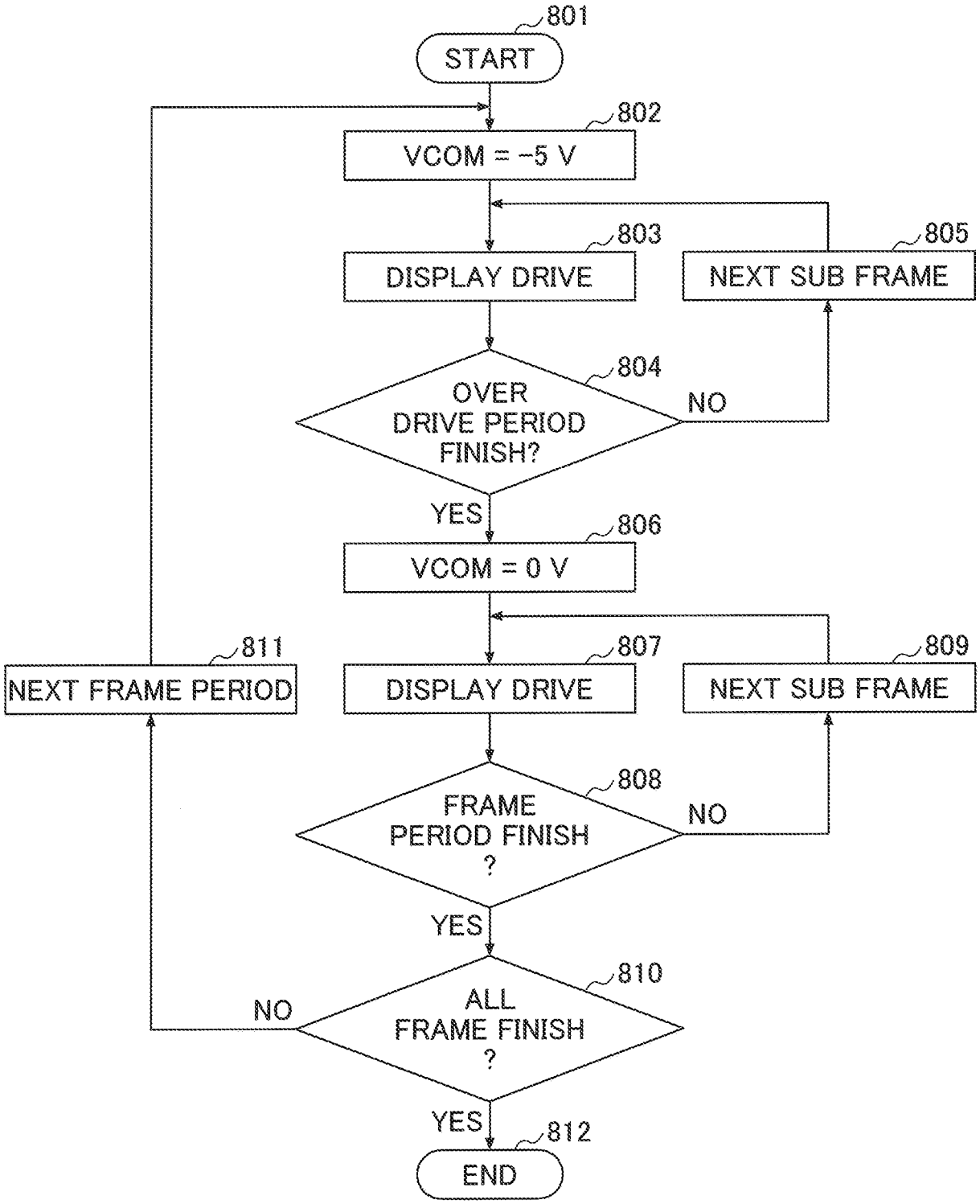
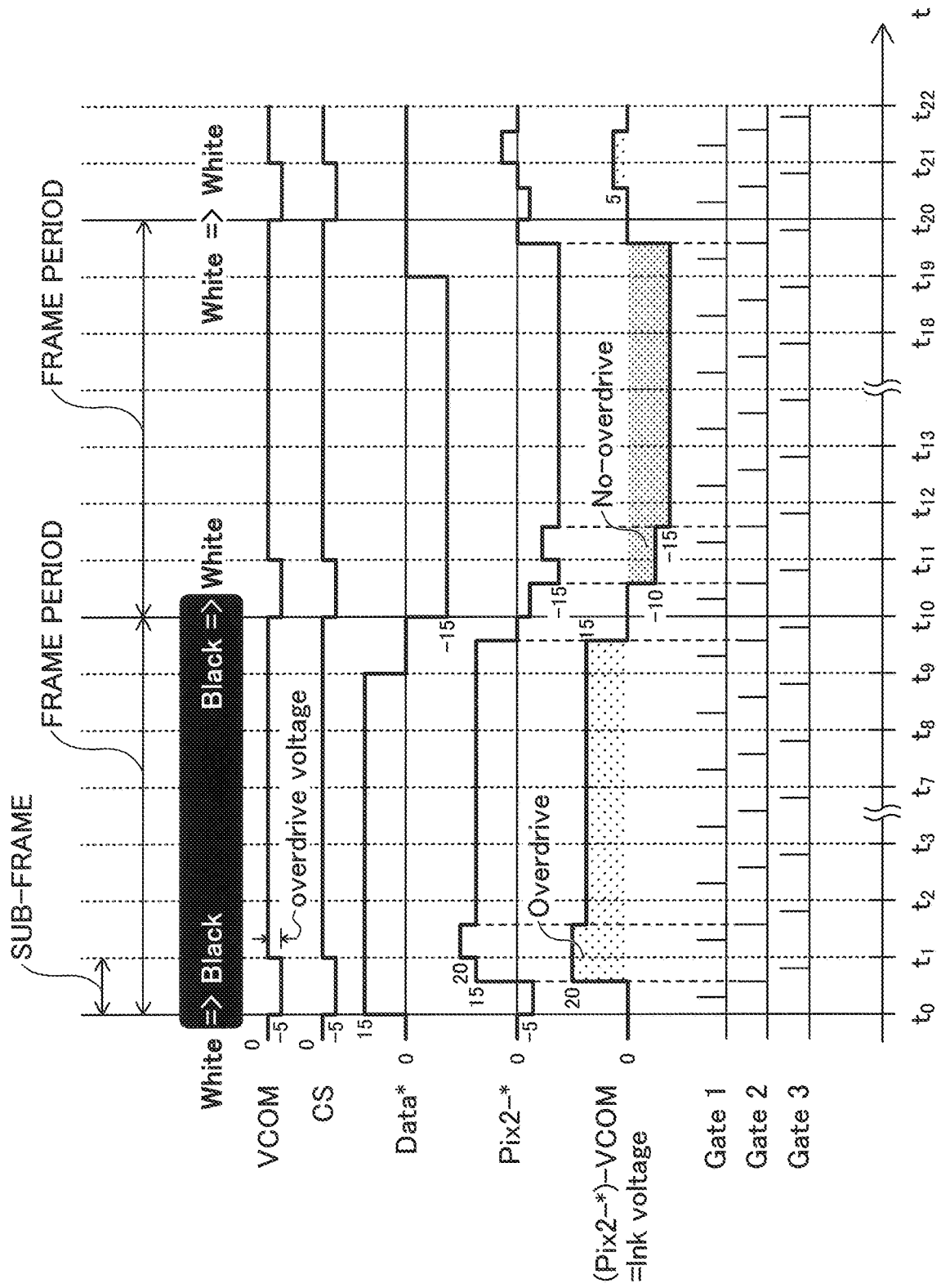
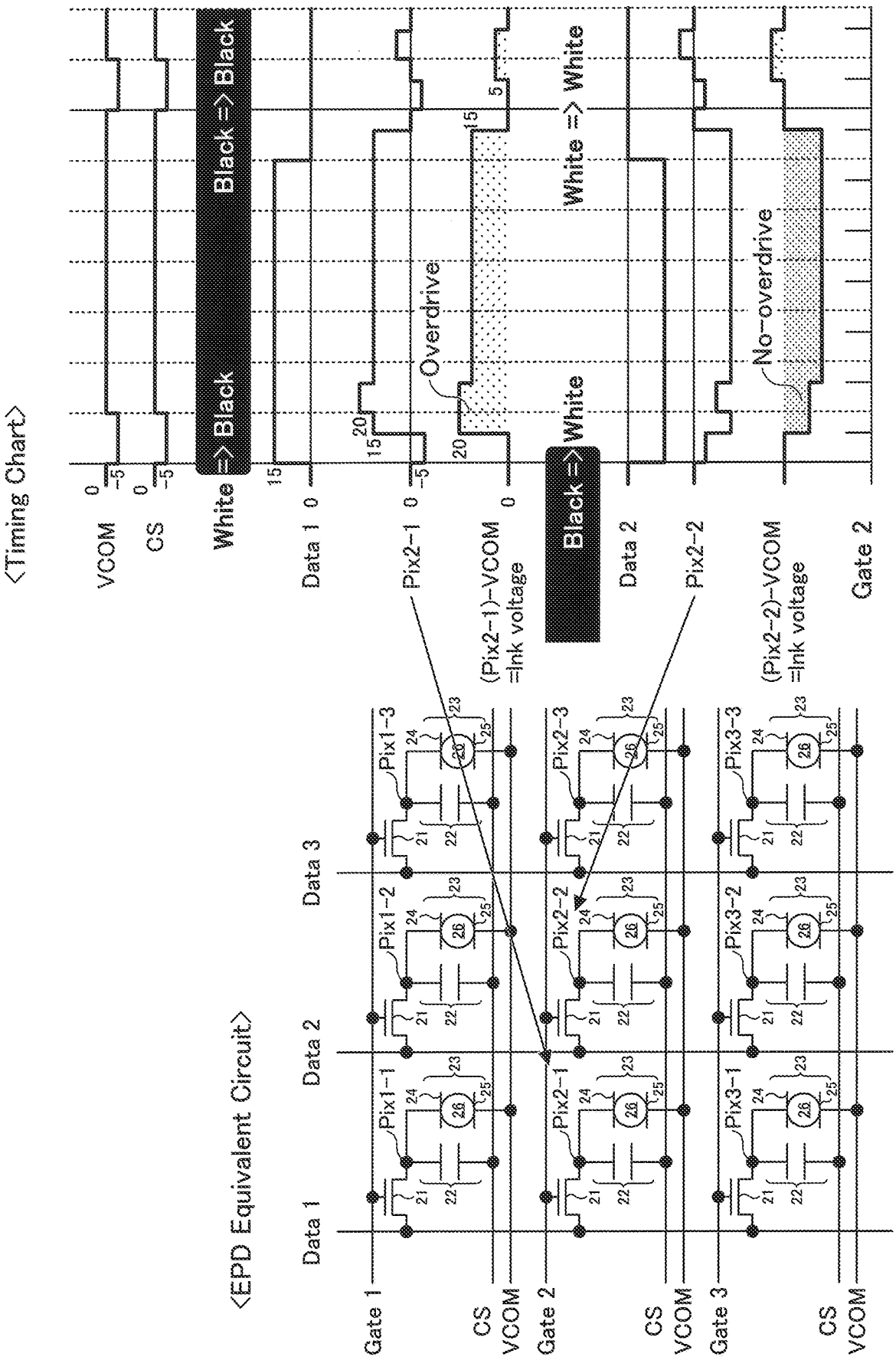
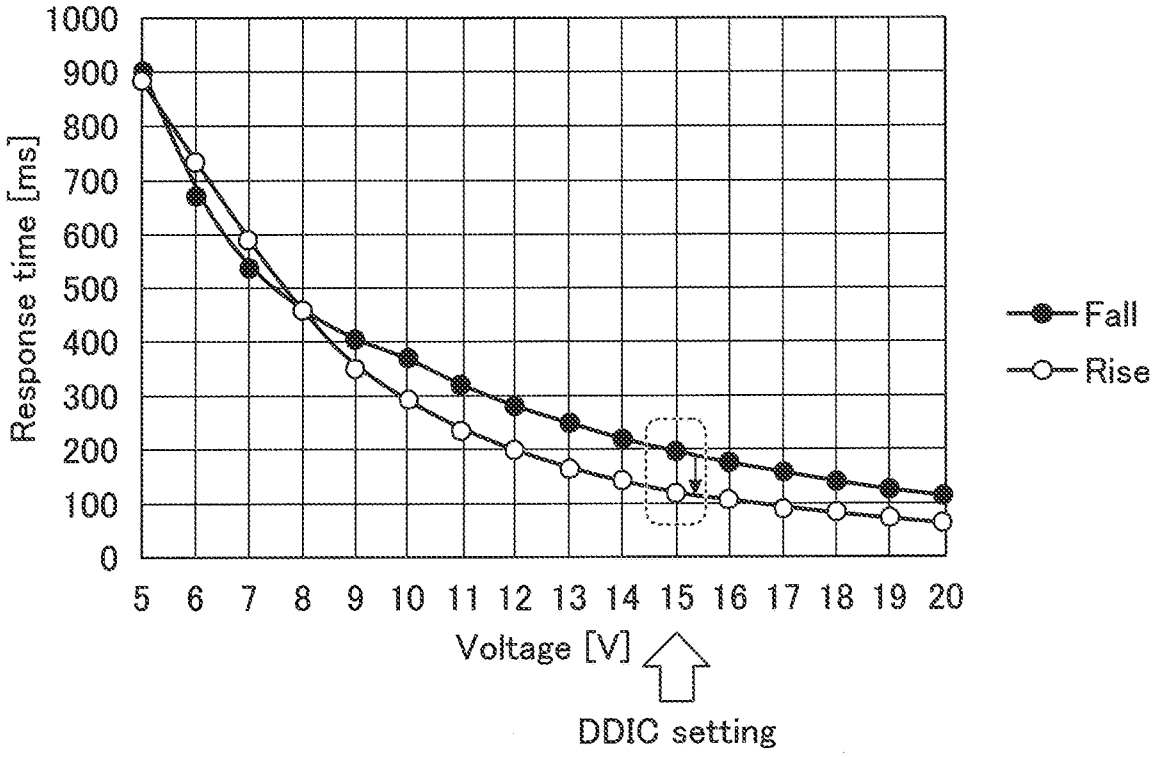
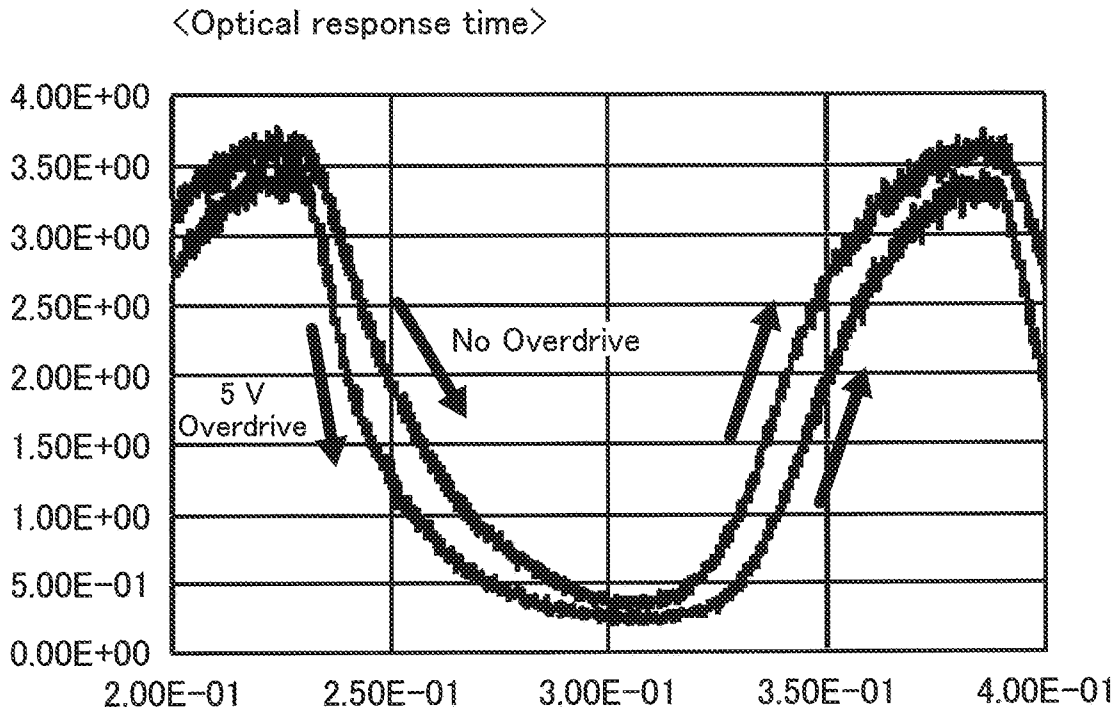

801
START
802
VCOM = −5 V
803
DISPLAY DRIVE
805
NEXT SUB FRAME
804
OVER DRIVE PERIOD FINISH?
NO
YES
806
VCOM = 0 V
811
NEXT FRAME PERIOD
807
DISPLAY DRIVE
809
NEXT SUB FRAME
808
FRAME PERIOD FINISH ?
NO
YES
810
ALL FRAME FINISH ?
NO
YES
812
END

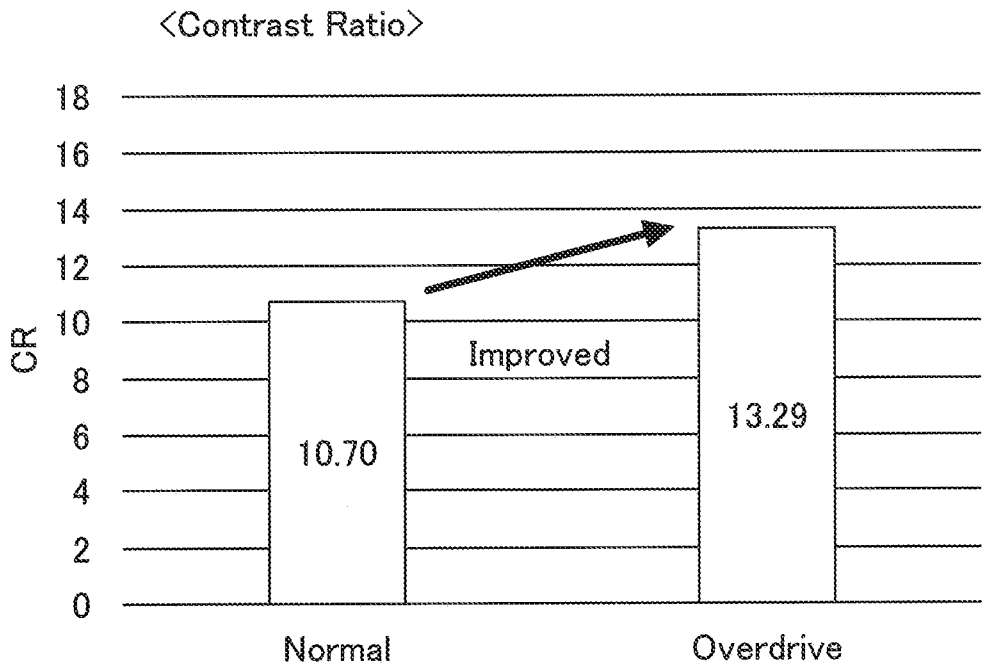

SUB-FRAME
FRAME PERIOD
FRAME PERIOD
White => Black
Black => White
White => White
overdrive voltage
Overdrive
No-overdrive
VCOM
CS
Data*
Pix2-*
(Pix2-*)-VCOM
=lnk voltage
Gate 1
Gate 2
Gate 3
t
t0 t1 t2 t3 t7 t8 t9 t10 t11 t12 t13 t18 t19 t20 t21 t22

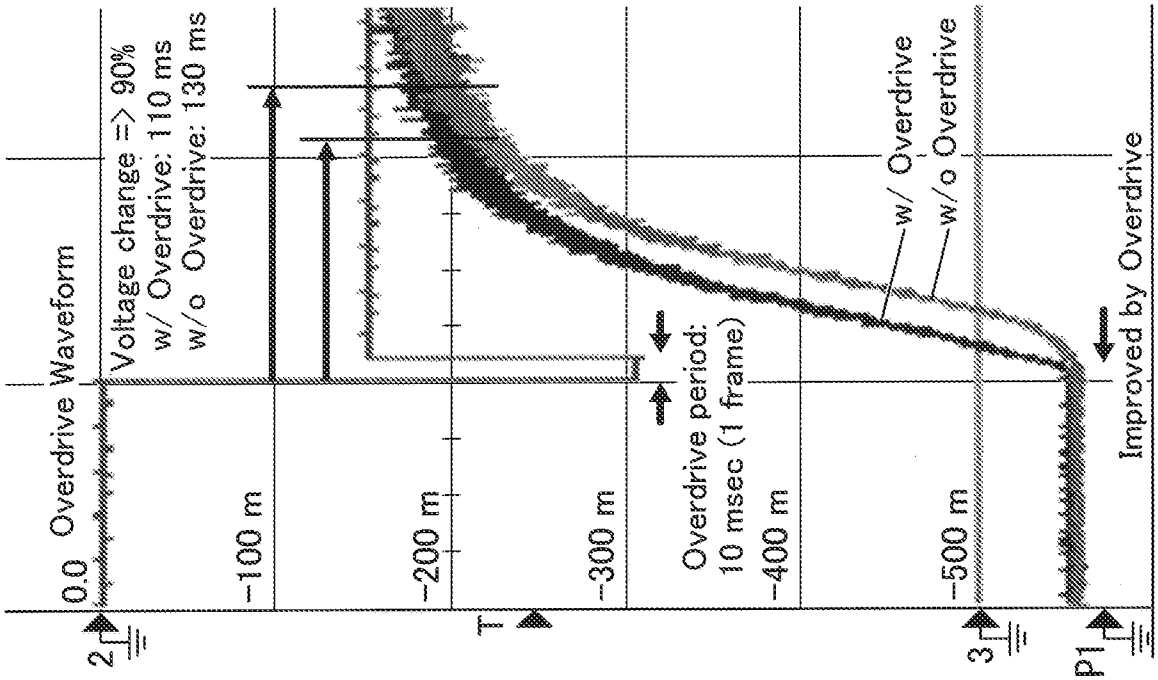

〈Timing Chart〉
VCOM
CS
White => Black
Black => Black
Data 1
Pix2-1
Overdrive
White => White
No-overdrive
(Pix2-1)-VCOM =Ink voltage
Black => White
Data 2
Pix2-2
(Pix2-2)-VCOM =Ink voltage
Gate 2
〈EPD Equivalent Circuit〉
Data 1
Data 2
Data 3
Gate 1
Gate 2
Gate 3
CS
VCOM
Pix1-1
Pix1-2
Pix1-3
Pix2-1
Pix2-2
Pix2-3
Pix3-1
Pix3-2
Pix3-3

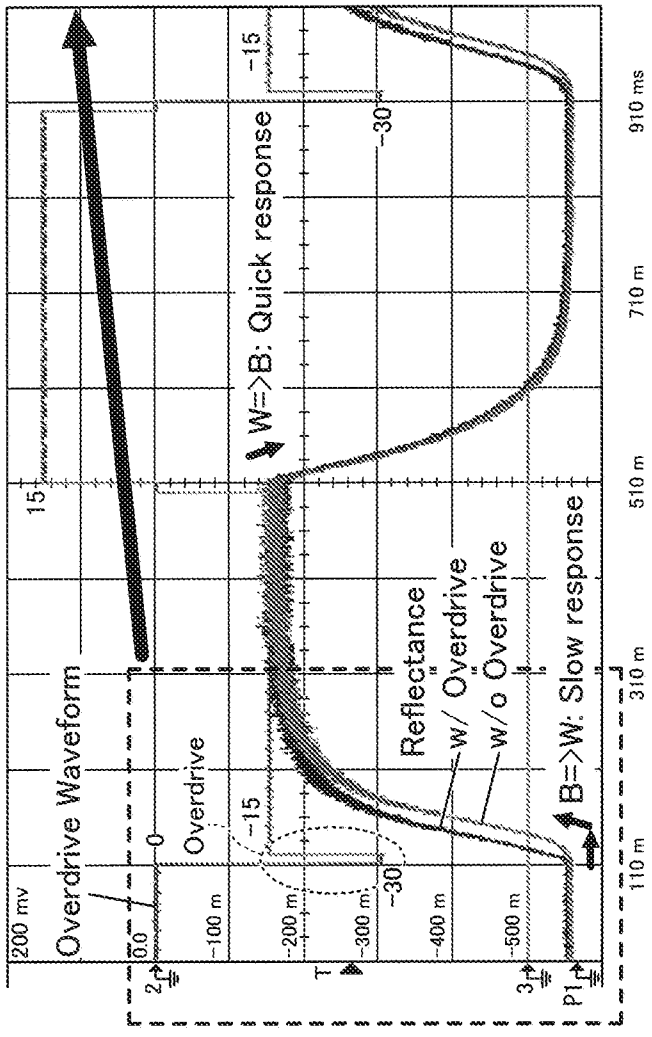

1000
900
800
700
600
500
400
300
200
100
0
Response time [ms]
5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
Voltage [V]
DDIC setting
Fall
Rise

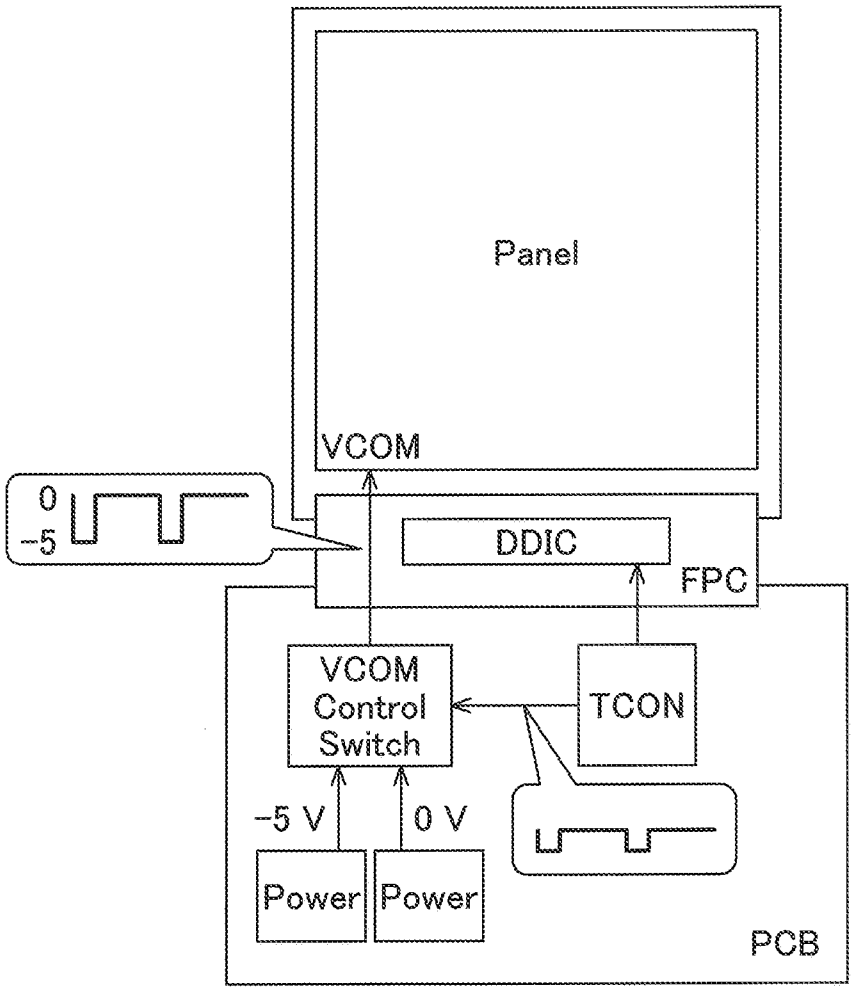

<Optical response time>
4.00E+00
3.50E+00
3.00E+00
2.50E+00
2.00E+00
1.50E+00
1.00E+00
5.00E-01
0.00E+00
2.00E-01
2.50E-01
3.00E-01
3.50E-01
4.00E-01
No Overdrive
5 V
Overdrive

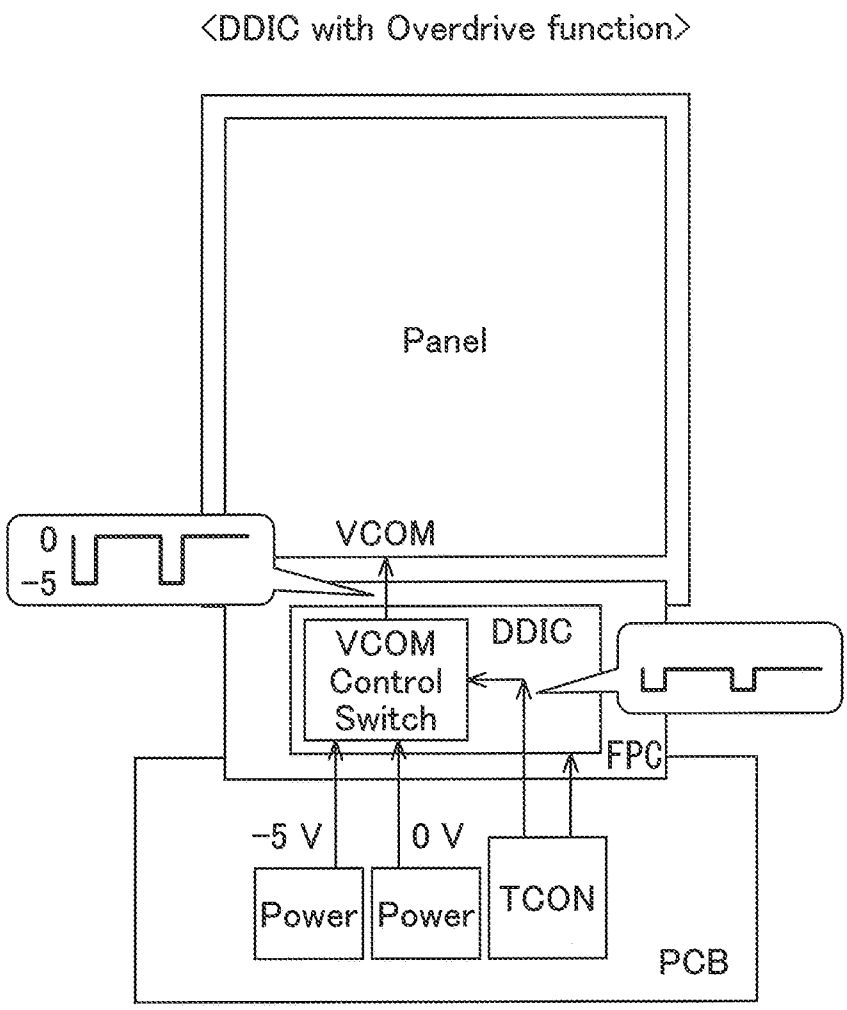
【Fig. 13】

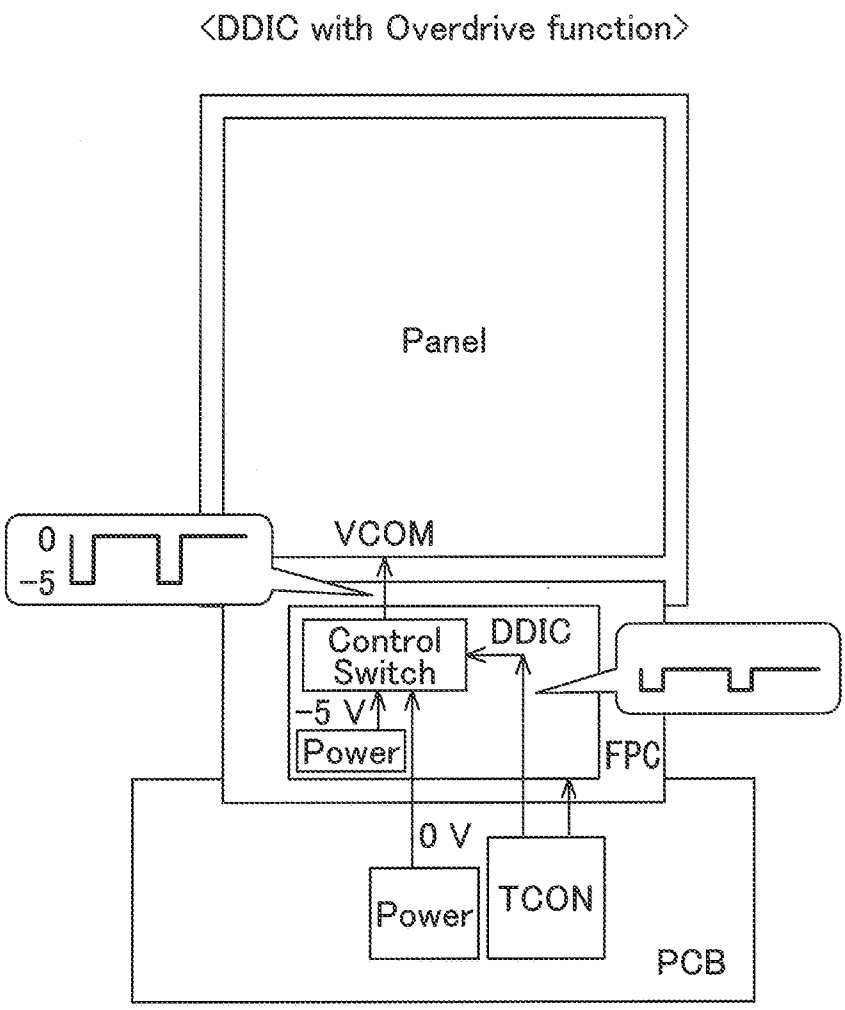

<Contrast Ratio>
CR
18
16
14
12
10
8
6
4
2
0
10.70
13.29
Improved
Normal
Overdrive

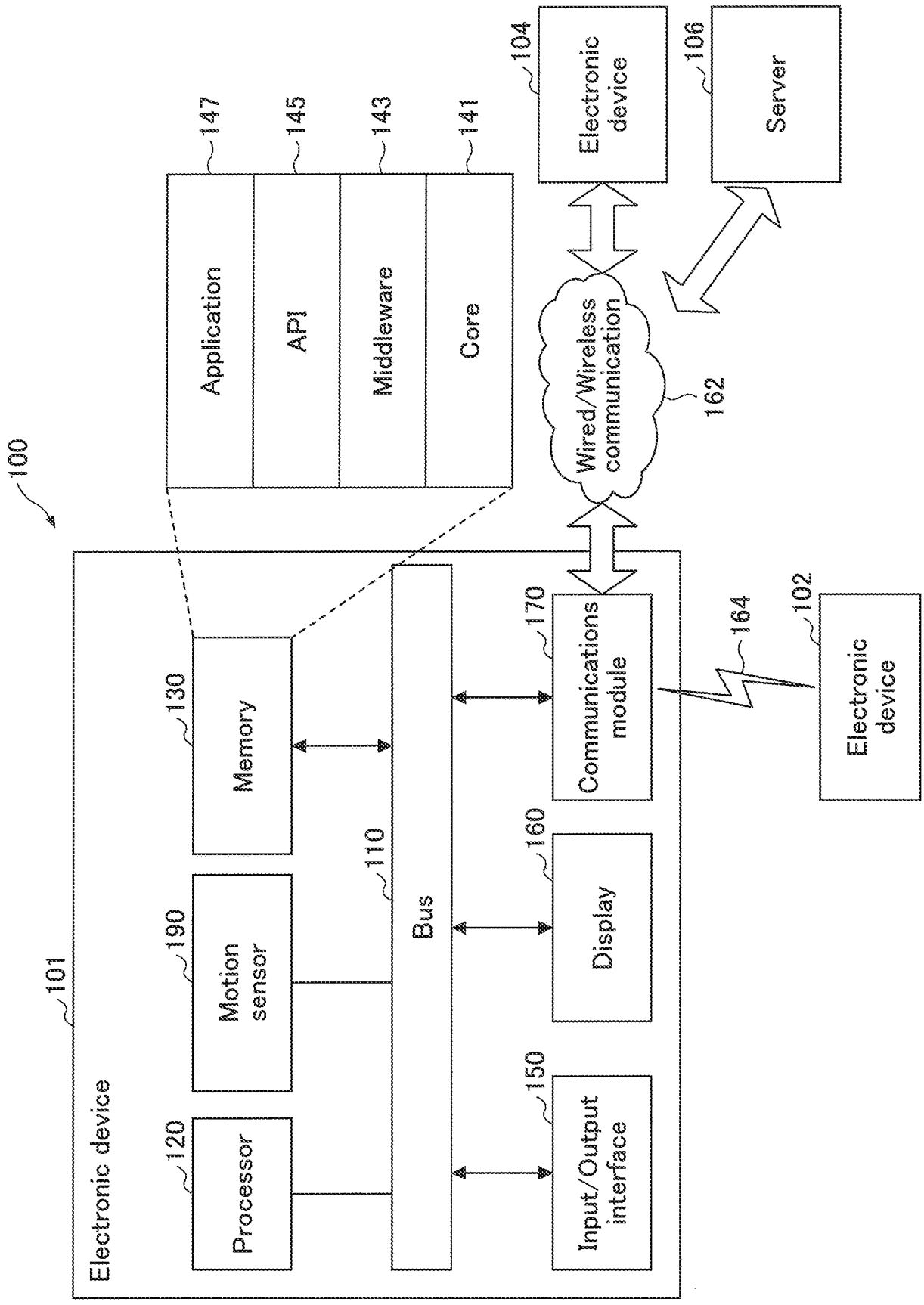

0.0 Overdrive Waveform
Voltage change => 90%
w/ Overdrive: 110 ms
w/o Overdrive: 130 ms
-100 m
-200 m
-300 m
-400 m
-500 m
Overdrive period:
10 msec (1 frame)
w/ Overdrive
w/o Overdrive
Improved by Overdrive
2
T
3
P1


200 mv
Overdrive Waveform
15
0
-15
-30
W=>B: Quick response
B=>W: Slow response
Reflectance
w/ Overdrive
w/o Overdrive
0.0
-100 m
-200 m
-300 m
-400 m
-500 m
110 m
310 m
510 m
710 m
910 ms
2
T
3
P1


Panel
VCOM
0
−5
DDIC
FPC
VCOM
Control
Switch
TCON
−5 V
0 V
Power
Power
PCB


<DDIC with Overdrive function>
Panel
0
-5
VCOM
VCOM
Control
Switch
DDIC
FPC
-5 V
0 V
Power
Power
TCON
PCB


<DDIC with Overdrive function>
Panel
0
-5
VCOM
Control Switch
DDIC
-5 V
Power
FPC
0 V
Power
TCON
PCB


100
Application
API
Middleware
Core
147
145
143
141
104
Electronic device
106
Server
Wired/Wireless communication
162
101
Electronic device
130
Memory
110
Bus
170
Communications module
164
102
Electronic device
190
Motion sensor
160
Display
120
Processor
150
Input/Output interface

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2022/085292

A. CLASSIFICATION OF SUBJECT MATTER

G02F 1/167(2019.01)i; G09G 3/34(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G02F; G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI;EPODOC;CNKI;CNPAT: electronic w paper, display, electrophoresis, pixel?, scan+, data, signal, capacitance, common w electrode, frame?, voltage

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 103676395 A (NLT TECHNOLOGIES LTD.) 26 March 2014 (2014-03-26) description, paragraphs [0004]-[0395], figures 1-63	1-6
Y	CN 101859545 A (SEIKO EPSON CORP.) 13 October 2010 (2010-10-13) description, paragraphs [0050]-[0122], figures 1-14	1-6
Y	CN 101083067 A (SEMICONDUCTOR ENERGY LAB) 05 December 2007 (2007-12-05) description, page 70	1-6
A	CN 101493627 A (SEIKO EPSON CORP.) 29 July 2009 (2009-07-29) the whole document	1-6
A	CN 1864194 A (E-INK CORP. et al.) 15 November 2006 (2006-11-15) the whole document	1-6
A	JP 2013050565 A (MEIDEN SOFTWARE CORP.) 14 March 2013 (2013-03-14) the whole document	1-6

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
05 December 2022	**19 December 2022**
Name and mailing address of the ISA/CN **National Intellectual Property Administration, PRC** **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing** **100088, China** Facsimile No. **(86-10)62019451**	Authorized officer **ZOU,Lina** Telephone No. **86-(10)-53962622**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2022/085292

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				JP	2007507737	A	29 March 2007
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				EP	1671310	A1	21 June 2006
				KR	20060090681	A	14 August 2006
				US	8300006	B2	30 October 2012
JP	2013050565	A	14 March 2013	None			