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(54) INTERNAL COMBUSTION ENGINE FUEL INJECTOR CONTROL SYSTEM

KRAFTSTOFFEINSPRITZSTEUERVORRICHTUNG FÜR EINE BRENNKRAFTMASCHINE

**SYSTEME DE COMMANDE DES INJECTEURS DE CARBURANT D'UN MOTEUR A COMBUSTION
INTERNE**

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(56) References cited:

EP-A- 0 212 777 **EP-A- 0 305 344**
EP-A- 0 548 915 **EP-A- 0 563 760**
US-A- 5 161 510

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Description

Technical Field

The present invention relates to a system for controlling the inductive loads of internal combustion engine fuel supply injectors.

Background Art

As is known, for controlling internal combustion engine injectors, these must be supplied with current the pattern of which generally comprises a rapidly increasing portion, a more slowly increasing portion, a portion oscillating about a mid value, and a rapidly decreasing portion.

The EP-A-548 915 describes an internal combustion engine fuel injector control system. This circuits comprise a low-voltage supply source, and a capacitor for storing the energy required for producing a rapid current pulse in the inductive load of the injector.

The capacitor is charged by the supply source to a given voltage value, and is then connected by a first electronic switch to the injector to form a resonant circuit and transfer energy from the capacitor to the injector which thus receives the initial current pulse required for opening it.

This circuit also comprises a second electronic switch.

This circuit is connected to an electronic control unit for activating the first and second switch for predetermined time intervals and so supplying the injector with current presenting the aforementioned pattern.

DISCLOSURE OF INVENTION

It is an object of the present invention to provide a system for flexibly calculating the closing/opening times of the first and second switch so that said times are correlated with the pattern of a number of circuit quantities and with a number of injector parameters.

According to the present invention, there is provided a system as claimed in Claim 1.

BRIEF DESCRIPTION OF DRAWINGS

The present invention will be described with reference to the accompanying drawings, in which:

Figure 1 shows a system for controlling the inductive loads of internal combustion engine fuel supply injectors;

Figure 2 shows a simplified electric diagram of a circuit forming part of the electronic system according to the present invention;

Figure 3 shows time graphs of a number of quantities in the Figure 2 system;

Figure 4 shows a detail of the Figure 1 circuit.

BEST MODE FOR CARRYING OUT THE INVENTION

Number 1 in Figure 1 indicates an electronic system for controlling the inductive loads of injectors 7 of a known fuel injection system 8 of an internal combustion engine 9, in particular a supercharged diesel engine.

System 1 comprises a control circuit 100 for controlling injectors 7 and to which the injectors are connected over respective control lines 10.

System 1 also comprises an electronic control unit 12 supplied with a number of information signals (e.g. engine speed, accelerator position, etc.) from engine 9, and cooperating with control circuit 100.

With reference to Figure 2, circuit 100 comprises two input terminals 102 and 103 for connection to a supply source B consisting of a battery with a low voltage V_{batt}.

More specifically, terminal 102 is connected to the anode of a diode D2, the cathode of which is connected to a first common line (actuator line) 104, while terminal 103 is connected directly to a second common line (ground) 105.

Circuit 100 also comprises a number of actuator circuits 106 connected to one another in parallel between lines 104 and 105, and each comprising an actuator L_i, a coupling diode D_i, a controlled electronic switch SW_i (conveniently formed by a power MOSFET transistor), and a common capacitor C_i.

More specifically, each actuator L_i consists of the coil of a respective injector 7, and presents one terminal connected to line 104, and the other terminal, defining node 107, connected to the anode of diode D_i which connects actuator L_i to a third common line (capacitance line) 112.

The cathode of each diode D_i is connected to a second node 113 in turn connected to capacitance line 112 and to a first terminal of common capacitor C_i which provides for storing energy at a higher voltage than V_{batt}. The other terminal of capacitor C_i is connected to ground line 105.

Each switch SW_i provides for connecting actuator L_i to battery B and for transferring energy from actuator L_i to capacitor C_i; is interposed between node 107 and ground 105; and presents a control input 108 connected to control unit 12 by a respective control line 56 over which control unit 12 supplies an actuator selecting signal s_i.

Circuit 100 also comprises the series connection of an electronic switch SWR (conveniently formed by a power MOSFET transistor) which provides for connecting capacitance line 112 to actuator line 104, and for recirculating the current of load L_i.

More specifically, switch SWR presents a first terminal connected to capacitance line 112; a second terminal connected to actuator line 104; and a control terminal connected to a control circuit 114 (described in more detail later on) in turn connected to control unit 12 by a control line 58 over which unit 12 supplies a signal

s_1 for controlling switch SWR.

Finally, capacitance line 112 is connected to control unit 12 over line 59 for permitting control unit 12 to monitor the voltage on line 112.

Control unit 12 is also supplied by a line 113a with a signal proportional to voltage V_{batt} , and provides for measuring (by means of a measuring circuit not shown) the value of inductance L of actuators Li .

Circuit 100 charges capacitor C_i to an appropriate voltage value, and supplies one of actuators Li with a current I_i the pattern of which presents a high-amplitude portion with a rapid leading edge, followed by a lower-amplitude portion terminating with a rapid trailing edge.

The above pattern is achieved by controlling switches SWR and SWi as described below.

With reference to Figure 3, it is assumed to begin with that switches SWR and SWi are open (low logic level of signals s_1 and s_i), and that capacitor C_i is charged to a predetermined high value V_C (voltage V_C higher than V_{batt}) so that the voltage drop between capacitance line 112 and actuator line 104 is such as to maintain a reverse bias of diode D2, and no current I_i flows in the actuators.

At instant t_0 , switch SWR is closed so that actuator line 104 is brought to the voltage level of capacitance line 112.

At instant t_1 , control unit 12 selects the desired actuator Li by switching respective signal s_i to high and closing the relative switch SWi.

The selected actuator Li is thus connected between capacitance line 112 and ground 105, in parallel with capacitor C_i with which it forms a resonant circuit.

The selected actuator is therefore supplied with a current pulse formed by a high-frequency sinusoid portion (the value of which is determined by the inductance of actuator Li and the capacitance of capacitor C_i) and produced by rapid discharging of the energy stored in capacitor C_i whose voltage V_C falls rapidly.

The capacitor continues discharging up to instant t_2 at which voltage V_C on line 112 approximately equals voltage V_{batt} , so that diode D2 is biased directly and connects battery B to actuator line 104.

After instant t_2 , the selected actuator Li is supplied by low-voltage battery B and, from this point on, injector Li is supplied with a current proportional to V_{batt}/L , where L is the value of the inductance of actuator Li selected by control unit 12.

At this step, diode Di of the selected actuator continues to be reverse biased.

The current in the injector therefore increases slowly until, after a time T_{bypass} from instant t_1 (instant t_3), it reaches a value I_{peak} .

According to the present invention, the closing time T_{bypass} of switch SWi is calculated by unit 12 using an electronic map M1 which supplies T_{bypass} as a function of V_{batt}/L input values.

More specifically, map M1 supplies T_{bypass} values increasing alongside an increase in inductance L and

alongside a fall in V_{batt} .

At instant t_3 , therefore, switch SWi is opened (high-to-low switching of signal s_i).

Consequently, diode Di of the selected actuator is biased directly and acts as a freewheeling diode for discharging the formerly charged actuator Li and recirculating current I_i via capacitance line 112 and switch SWR. At this step, current I_i tends to fall in proportion to $-(V_{d2})/L$ - where V_{d2} is the voltage drop across diode D2, and L the inductance of selected actuator Li - until it reaches a value $I_{offchop}$ at instant t_4 .

Opening time $T_{delay}=t_4-t_3$ of switch SWi is calculated by unit 12 which presents an interpolation unit C1 for supplying T_{delay} according to the equation:

$$T_{delay}=K1+A*(L-K2)$$

where L is the inductance of selected actuator Li expressed in μH ; $K1$ and $K2$ are two experimental numeric constants; and A is an experimental gain coefficient.

At instant t_4 , switch SWi is again closed, so that selected actuator Li is again charged by battery B and disconnected from capacitance line 112 by relative diode Di.

In the instants following instant t_4 , the current I_i in actuator Li again increases in proportion to V_{batt}/L . As of instant t_4 , the current increases for a time T_{onchop} until it reaches value I_{onchop} at instant t_5 at which switch SWi is again opened.

According to the present invention, time T_{onchop} is calculated by unit 12 using an electronic map M2 which supplies T_{onchop} as a function of V_{batt}/L input values.

More specifically, map M2 supplies T_{onchop} values increasing alongside an increase in inductance L of selected actuator Li and alongside a fall in voltage V_{batt} .

Opening of switch SWi (instant t_5) again discharges actuator Li for time $T_{offchop}$.

Time $T_{offchop}$ is calculated by unit 12 which presents an interpolation unit C2 for supplying $T_{offchop}$ according to the equation:

$$T_{offchop}=K3+B*(L-K4)$$

where L is the inductance of selected actuator Li expressed in μH ; $K3$ and $K4$ are two experimental numeric constants; and B is an experimental gain coefficient.

As such, switch SWi is appropriately opened and closed successively to maintain a current in selected actuator Li oscillating about a predetermined medium-low value.

Switches SWR and SWi are opened successively for rapidly discharging actuator Li .

More specifically, at instant t_6 , switch SWi is opened with switch SWR open. At this step, diode Di is biased directly to connect actuator Li to capacitance line 112 and again form a resonant circuit, so that actuator Li dis-

charges rapidly into capacitor C_i , current I_i decreases in the form of a high-frequency sinusoid portion, and the energy formerly accumulated by actuator L_i is transferred to capacitor C_i -whose voltage increases rapidly.

This step continues until all the current in actuator L_i is discharged, and which corresponds to a first charge of capacitor C_i to voltage V_2 , at which point diode D_i is disabled to prevent a sign inversion of the current in the actuator (instant t_7).

Subsequently, being isolated from the rest of the circuit, capacitor C_i remains charged to voltage value V_2 .

As shown in Figure 3, at instant t_8 , control unit 12 again closes one or more switches SW_i for time T_{onric} , so as to again close the circuit including battery B and each actuator L_i with a closed switch SW_i .

As such, each actuator L_i is supplied with increasing current and, in this step, capacitor C_i remains isolated.

At instant t_8 , switch SW_i (or all the switches closed previously) is again opened so that, for time T_{offric} , as in interval t_6 - t_7 , energy is transferred from the actuator to capacitor C_1 , current I_i in actuator L_i falls to zero (instant t_{10}), and the voltage of capacitance line 112 increases.

By repeating the above two steps n times, it is therefore possible to gradually charge the capacitor to the desired V_C level by first charging actuators L_i simultaneously to such a value as not to activate them (and so open the injectors), and then discharging the actuator current into the capacitor.

According to the present invention, recharge time T_{onric} (t_9 - t_8) is calculated by unit 12 using an electronic map $M3$ for supplying T_{onric} as a function of V_{batt}/L input values.

More specifically map $M3$ supplies T_{onric} values increasing alongside an increase in inductance L and alongside a fall in V_{batt} .

Control unit 12 also presents an electronic map $C3$ for supplying time T_{offric} .

Unit 12 also supplies the n number of recharge steps as a function of voltage V_2 of capacitor C_i at the end of the injection cycle.

The n number is calculated by unit 12 using an electronic map $M4$ for supplying n as a function of an input V_2 value.

Figure 4 shows a detail of control circuit 114 supervising switches of MOSFET SWR.

In particular, Figure 4 shows details of the MOSFET source and drain terminals connected respectively to line 112 and node 113.

Circuit 114 comprises a first capacitor C_1 with a first terminal connected to line 112, and a second terminal connected to the cathode of a diode D_r , the anode of which is connected to node 113.

Circuit 114 comprises a second capacitor C_2 connected parallel to a Zener diode D_z and presenting a first terminal connected to line 112, and a second terminal connected to the cathode of diode D_r via a resistor R .

Circuit 114 also comprises a first electronic switch

SWB (conveniently formed by an optoisolator) located between line 112 and a control terminal (GATE) 115 of MOSFET SWR; and a second electronic switch SWA (conveniently formed by an optoisolator) interposed between control terminal 115 and the node 116 common to diode D_z , capacitor C_2 and resistor R .

Switches SWA and SWB are controlled in complementary manner by the logic signal from control unit 12, i.e. one is always on while the other is off.

In actual use, when charging capacitor C_i as described previously, the magnetic energy accumulated by the injectors is transferred to capacitors C_i and C_1 which are charged as a function of the respective capacitance values. More specifically, as the ratio of the capacitance values of capacitors C_1 and C_i is less than 1, capacitor C_1 is charged to a voltage V_1 lower than that at the terminals of capacitor C_i , so that diode D_r is disabled, and capacitor C_1 is isolated from capacitor C_i and acts as a constant voltage source with one terminal connected to the source terminal of MOSFET SWR.

Moreover, capacitor C_2 is charged to a voltage V_z which is determined by Zener diode D_z , is lower than the charge voltage V_1 of capacitor C_1 , and is higher than the threshold voltage V_{gsth} required for closing MOSFET SWR.

For disabling MOSFET SWR, switch SWA is opened and switch SWB closed, so that voltage V_{gs} between control terminal 115 and the source terminal of MOSFET SWR equals zero, thus disabling the MOSFET.

For closing MOSFET SWR, switch SWB is opened and switch SWA closed, so that voltage V_z at the terminals of capacitor C_2 is applied between control terminal (GATE) 115 and the source terminal of the MOSFET which thus closes. During this step, the current supplied to MOSFET SWR is limited by resistance R , while Zener diode D_z protects GATE 115 of the MOSFET against overvoltage.

As the switching times of MOSFET SWR are not negligible, switches SWA and SWB are activated in advance with respect to the start and end of injection.

Circuit 114 therefore provides for obvious advantages by supplying MOSFET SWR at all times with sufficient voltage for rapidly closing it, and by drawing no energy from capacitor C_i for biasing optoisolators SWA and SWB.

Moreover, circuit 114 is extremely straightforward and reliable.

The system according to the present invention therefore provides for flexibly calculating, for each selected actuator L_i , the control times of first and second switches SW_i , SWR, by virtue of said times being correlated to the inductance L of the selected actuator L_i and to the voltage V_{batt} of battery B .

As such, the current supplied to each injector 7 is regulated as a function of the inductance L of the injector coil. Since the coils of injectors 7 of system 8 invariably present differing inductance values L (due to manufac-

turing tolerances), each injector 7 is therefore automatically supplied with the most appropriate current value.

More specifically, an increase in inductance L makes it increasingly difficult (for known physical reasons) to inject current into actuator Li , so that time T_{bypass} is automatically increased to permit the current supplied to the injector to reach the predetermined I_{peak} value.

Similarly, a fall in battery voltage V_{batt} reduces the current gradient in interval t_3-t_2 , so that time T_{bypass} is again increased to permit the current supplied to the injector to reach the predetermined I_{peak} value.

Clearly, changes may be made to the system as described and illustrated herein without, however, departing from the scope of the present invention.

For example, the number of circuits 106 depends on the number of actuators Li and may vary as required.

Claims

1. A system for controlling the inductive loads of injectors, comprising:

a control circuit (100) with a first and second input terminal (102, 103) connectable to a low-voltage supply source (V_{batt});

an energy storing circuit (106) connected between said input terminals and including a capacitive element (C_i) and at least one inductive load (Li) of an injector;

a first controlled switching element (SW_i) interposed between said inductive load (Li) and a reference line (105), for selectively supplying said inductive load (Li); a second controlled switching element (SWR) for rapidly discharging said capacitive element into said inductive load; and

a control unit (12) generating control signals (s_i, s_1) for said first and second switching elements (SW_i, SWR);

characterized in that said control unit comprises computing means ($M1, C1, M2, C2$) for processing, on the basis of input information signals (V_{batt}/L), including the inductance (L) of said inductive load (Li), the duration of control time intervals ($T_{bypass}, T_{delay}, T_{onchop}, T_{offchop}$) of at least one of said switching elements (SW_i, SWR) for supplying said load with a current (I_i) presenting a high-amplitude portion with a rapid leading edge, a slowly increasing portion, and an oscillating-amplitude portion wherein said current is maintained about a sensibly constant mid value.

2. A system as claimed in Claim 1, characterized in that said control unit comprises:

first computing means ($M1$) for processing a first time (T_{bypass}) wherein said first switching element (SW_i) is maintained closed while said second switching element (SWR) is closed and said capacitive element (C_i) is charged, for rapidly discharging said capacitive element into said load (Li);

second computing means ($C1$) for processing a second time (T_{delay}) wherein said first switching element (SW_i) is maintained open while said second switching element (SWR) is closed, for discharging said load (Li); and

third and fourth computing means ($M2, C2$) for processing respective third and fourth times ($T_{onchop}, T_{offchop}$) wherein said first switching element (SW_i) is alternately closed/opened with said second switching element (SWR) closed, for generating small current pulses in said load with no energy transfer between said load and said capacitive element.

3. A system as claimed in Claim 1 or 2, characterized in that said control unit comprises fifth and sixth computing means ($M3, C3$) for processing respective fifth and sixth times (T_{onric}, T_{offric}) wherein said first switching element (SW_i) is alternately closed/opened with said second switching element (SWR) open, for generating small current pulses in said load and subsequently transferring energy from said load to said capacitive element.

4. A system as claimed in Claim 2 and 3, characterized in that said first ($M1$), third ($M2$) and fifth ($M3$) computing means comprise electronic maps ($M1, M2, M3$) supplied with said information signals (V_{batt}/L) and in turn supplying said respective first, third and fifth times ($T_{bypass}, T_{onchop}, T_{onric}$).

5. A system as claimed in Claim 4, characterized in that said information signals comprise- the value of the inductance (L) of the coil of said injector, and the value of the voltage (V_{batt}) of said supply source (B);

said electronic maps supplying times ($T_{bypass}, T_{onchop}, T_{onric}$) increasing alongside an increase in the value of said inductance (L) and alongside a fall in said voltage (V_{batt}) of said supply source.

6. A system as claimed in one of the foregoing Claims from 2 to 5, characterized in that said second ($C1$) and fourth ($C2$) computing means determine said second and fourth times ($T_{delay}, T_{offchop}$) by means of linear combinations of said information signals (V_{batt}/L).

7. A system as claimed in Claim 6, characterized in that said second (C1) and fourth (C2) computing means determine said second and fourth times (Tdelay, Toffchop) by means of linear combinations of the type:

$$\text{Time} = \text{coeff.1} + A \cdot (L \cdot \text{coeff.2})$$

where L is the value of the inductance of the injector expressed in μH ; coeff.1 and coeff.2 are two experimental numeric constants; and A is a gain coefficient.

8. A system as claimed in any one of the foregoing Claims, characterized in that said load (Li) is connected by a first terminal (104) to said first input terminal (102); said reference line (105) is connected to said second input terminal (103); said load (Li) is connected to said first switching element (SWi) by a second terminal defining a first node (107) connected to a second node (113) consisting of a first terminal of said capacitive element (Ci); and said second switching element (SWR) is interposed between said second node (113) and said first terminal (104) of said load.

9. A system as claimed in Claim 8, characterized in that said capacitive element (Ci) presents a second terminal connected to said reference line (105).

10. A system as claimed in Claim 8 or 9, characterized in that said first and second nodes (107, 113) are connected to each other by a first unipolar switch (Di) permitting current flow from said load (Li) to said capacitive element (Ci); and, between said first input terminal (102) and said first terminal (104) of said load (Li), there is provided a second unipolar switch (D2) permitting current flow from said first input terminal to said load.

11. A system as claimed in Claim 10, characterized in that said first and second unipolar switches (Di, D2) consist of a junction diode.

12. A system as claimed in one of the foregoing Claims, characterized in that said first and second switching elements (SWi, SWR) each present a control terminal (108) connected to said control unit (12).

13. A system as claimed in one of the foregoing Claims, wherein said second switching element comprises

an electronic semiconductor switch (SWR), in particular a MOSFET transistor; characterized in that it comprises control means (114) for controlling said electronic switch (SWR) and interposed between a control terminal (115) of the

electronic switch and said control unit (12); said control means (114) comprising energy storing means (C1, C2); and unipolar switching means (Dr) interposed between said energy storing means (C1, C2) and said capacitive element (Ci), for permitting energy flow to said energy storing means (C1, C2) when charging said capacitive element (Ci); said control means also comprising first switching means (SWA) controlled by said control unit (12) and interposed between said energy storing means (C1, C2) and said control terminal (115) of said electronic switch (SWR); said first switching means (SWA) being movable between a first open position, and a closed position wherein they supply said electronic semiconductor switch with the energy required for switching it.

14. A system as claimed in Claim 13, characterized in that it comprises second switching means (SWB) interposed between said control terminal (115) and a terminal (source) of said electronic switch;

said second switching means (SWB) being activated by said control unit (12) in a complementary manner with respect to said first switching means (SWA).

15. A system as claimed in Claim 14, characterized in that said energy storing means comprise at least one capacitor (C2), and means for limiting the charge voltage of said capacitor (C2).

Patentansprüche

1. System zur Steuerung einer induktiven Last eines Injektors umfassend

eine Steuerschaltung (100) mit einem ersten und einem zweiten Eingangsanschluß (102, 103), die mit einer Niederspannungsquelle (Vbatt) verbindbar sind,

einer Energiespeicherschaltung (106) geschaltet zwischen den Eingangsanschlüssen, die ein kapazitives Element und wenigstens eine induktive Last eines Injektors umfaßt,

ein erstens gesteuertes Schaltelement (Swi), das zwischen der induktiven Last und einer Referenzleitung (105) geschaltet ist, zur selektiven Versorgung der induktiven Last (Li),

ein zweites gesteuertes Schaltelement (SWR) zum schnellen Entladen des kapazitiven Elements in die induktive Last, und

eine Steuereinheit (12), die Steuersignale (si, sl) für das erste und zweite Schaltelement (SWi, SWR) bildet;

dadurch gekennzeichnet, daß die Steuereinheit Rechenmittel (M1, C1, M2, C2) umfaßt, die auf Grundlage von Informationssignalen (Vbatt/L), die die Induktivität (L) der induktiven Last (Li) umfaßt, die Dauer von Steuerzeitintervallen (Tbypass, Tdelay, Tonchop, Toffchop) für wenigstens eines der Schaltelemente (SWi, SWR) berechnet, um die Last mit einem Strom (Ii) zu versorgen, dessen Verlauf einen Hochstromanteil mit einem schnellen Anstieg, einem Anteil mit einem langsamen Anstieg und einem Anteil mit einer Schwingung um einen Mittelwert umfaßt.

2. System nach Anspruch 1, dadurch gekennzeichnet, daß die Steuereinheit umfaßt

erste Rechenmittel (M1) zur Berechnung einer ersten Zeit (Tbypass), während der das erste Schaltelement (SWi) geschlossen bleibt, während das zweite Schaltelement (SWR) geschlossen ist und das kapazitive Element (Ci) geladen wird um das kapazitive Element schnell in die Last (Li) zu entladen,

zweite Rechenmittel (C1) zur Berechnung einer zweiten Zeit (Tdelay) innerhalb der das erste Schaltelement (SWi) geöffnet bleibt, während das zweite Schaltelement (SWR) geschlossen wird, um die Last (Li) zu entladen,

dritte und vierte Rechenmittel (M2, C2) zur Berechnung entsprechender dritter und vierter Zeiten (Tonchop, Toffchop) während derer das erste Schaltelement (SWi) abwechselnd geschlossen und geöffnet ist, wobei das zweite Schaltelement (SWR) geschlossen ist, zur Bildung kleiner Stromimpulse in der Last wobei kein Energietransfer zwischen der Last und dem kapazitiven Element erfolgt.

3. System nach einem der Ansprüche 1 oder 2, dadurch gekennzeichnet, daß die Steuereinheit fünfte und sechste Rechenmittel (M3, C3) zur Berechnung fünfter und sechster Zeiten (Tonric, Toffric) umfaßt, während derer das erste Schaltelement (SWi) abwechselnd mit dem zweiten Schaltelement (SWR) geschlossen und geöffnet wird, zur Bildung kleiner Stromimpulse in der Last wobei anschließend die Energie von der Last dem kapazitiven Element verschoben wird.

4. System nach Anspruch 2 oder 3, dadurch gekennzeichnet, daß das erste Rechenmittel (M1), das dritte Rechenmittel (M2) und das fünfte Rechenmittel

(M3) elektronische Kennfelder (M1, M2, M3) umfaßt, die mit den Informationssignalen (Vbatt) versorgt werden und ausgehend von diesem die ersten, dritten und fünften Zeiten (Tbypass, Tonchop, Tonric) liefern.

5. System nach Anspruch 4, dadurch gekennzeichnet, daß die Informationssignale den Wert der Induktivität (L) der Spule des Injektors und den Wert der Spannung (Vbatt) der Spannungsquelle (B) beinhaltet, daß die elektronischen Kennfelder Zeiten liefern, die zunehmen bei zunehmenden Werten der Induktivität (L) und bei fallender Batteriespannung (Vbatt) der Spannungsquelle.

6. System nach einem der vorgehenden Ansprüche 2 bis 5, dadurch gekennzeichnet, daß das zweite Rechenmittel (C1) und das vierte (C2) Rechenmittel die zweite und vierte Zeit (Tdelay, Toffchop) mit Mitteln zur linearen Kombination des Informationssignals (Vbatt/L) liefern.

7. System nach Anspruch 6, dadurch gekennzeichnet, daß das zweite (C1) und vierte (C2) Rechenmittel die zweite und vierte Zeit (Tdelay, Toffchop) mit Mitteln zur Linearkombination derart bestimmen, daß die Beziehung

$$\text{Time} = \text{coeff.1} + A * (L - \text{coeff})$$

gilt, wobei L der Wert der Induktivität des Injektors in μH angegeben ist und coeff.1 und coeff.2 experimentell ermittelte numerische Konstanten und A ein Koeffizient ist.

8. System nach einem der vorgehenden Ansprüche, dadurch gekennzeichnet, daß die Last (Li) mit einem ersten Anschluß (104) mit dem ersten Eingangsanschluß (102) verbunden ist, daß die Referenzleitung (105) mit dem zweiten Eingangsanschluß (103) verbunden ist, die Last (Li) mit dem ersten Schaltelement (SWi) über einen zweiten Anschluß verbunden ist, der einen ersten Verbindungspunkt (107) definiert, der mit einem zweiten Verbindungspunkt (103) verbunden ist, der einem ersten Anschluß des kapazitiven Elements (Ci) umfaßt, und daß das zweite Schaltelement (SWR) zwischen dem zweiten Verbindungspunkt (113) und dem ersten Anschluß (104) der Last geschaltet ist.

9. System nach Anspruch 8, dadurch gekennzeichnet, daß das kapazitive Element (Ci) einen zweiten Anschluß umfaßt, der mit der Referenzleitung (105) verbunden ist.

10. System nach Anspruch 8 oder 9, dadurch gekennzeichnet, daß der erste und zweite Verbindungs-

punkt (107, 113) miteinander über einen ersten unipolaren Schalter (Di) verbunden sind, der einen Stromfluß von der Last (Li) zu dem kapazitiven Element (Ci) erlaubt, und daß zwischen dem ersten Eingangsanschluß (102) und dem ersten Anschluß (104) der Last (Li) ein zweites unipolares Schaltelement (D2) angeordnet ist, das einen Stromfluß von dem ersten Eingangsanschluß zu Last erlaubt.

11. System nach Anspruch 10, dadurch gekennzeichnet, daß das erste und zweite unipolare Schaltelement (Di, D2) aus einer Halbleiterdiode besteht. 10
12. System nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß das erste und zweite Schaltelement (SWi, SWR) jeweils einen Steueranschluß (108) beinhaltet, der mit der Steuereinheit (12) verbunden ist. 15
13. System nach einem der vorgehenden Ansprüche, wobei das zweite Schaltelement einen elektronischen Halbleiterschalter (SWR) umfaßt, insbesondere einen MOSFET Transistor, dadurch gekennzeichnet, daß das Steuermittel (114) zur Steuerung des elektronischen Schalters (SWR) umfaßt und zwischen dem Steueranschluß (115) des elektronischen Schalters und der Steuereinheit (12) angeordnet ist, daß das Steuermittel (114) ein energiespeicherndes Mittel (C1, C2) und unipolare Schaltmittel (Dr) umfaßt, die zwischen dem energiespeichernden Mittel (C1, C2) und dem kapazitiven Element (Ci) angeordnet sind, und einen Energiefluß zu dem energiespeichernden Mittel (C1, C2) erlauben wenn das kapazitive Element (Ci) geladen wird, das Steuermittel umfaßt ferner erste Schaltmittel (SWA), die durch die Steuereinheit (12) gesteuert werden und zwischen dem energiespeichernden Mittel (C1, C2) und dem Steueranschluß (115) des elektronischen Schalters (SWR) angeordnet sind, daß das erste Schaltmittel (SWA) zwischen einer ersten offenen Position und einer zweiten geschlossenen Position bewegbar ist, wobei sie der elektronische Halbleiterschalter mit Energie zum Schalten versorgt. 20 25 30 35 40
14. System nach Anspruch 13, dadurch gekennzeichnet, daß es ein zweites Schaltmittel (SWB) umfaßt, das zwischen dem Steueranschluß (115) und einem Anschluß (Source) des elektronischen Schalters angeordnet ist, daß das zweite Schaltmittel (SWB) durch die Steuereinheit (12) in einer komplementären Art in Bezug auf das erste Schaltmittel (SWA) angesteuert wird. 45 50
15. System nach Anspruch 14, dadurch gekennzeichnet, daß das energiespeichernde Element wenigstens einen Kondensator (C2) und Mittel zur Begrenzung der Spannung an dem Kondensator (C2) 55

umfaßt.

Revendications

1. Système de commande des charges inductives d'injecteurs comprenant :

- un circuit de commande (100) avec une première et une seconde borne d'entrée (102, 103) qui se relie à une source d'alimentation basse tension (Vbatt),
- un circuit de stockage d'énergie (106) branché entre les bornes d'entrée et comprenant un élément capacitif (Ci) et au moins une charge inductive (Li) d'un injecteur,
- un premier élément interrupteur commandé (SWi) entre la charge inductive (Li) et une ligne de référence (105) pour alimenter sélectivement la charge inductrice (Li) ;
- un second élément interrupteur commandé (SWR) pour décharger rapidement l'élément capacitif dans la charge inductive,
- une unité de commande (12) régénérant des signaux de commande (s_i , s_r) pour le premier et second élément interrupteur (SWi, SWR),

caractérisé en ce que

l'unité de commande (12) comprend des moyens de calcul (M1, C1, M2, C2) de traitement sur la base de signaux d'information d'entrée (Vbatt/L) comprenant l'inductance (L) de la charge inductive (Li), la durée des intervalles de temps de commande (Tdérivation, Tretard, Tonchop, Toffchop) d'au moins l'un des éléments interrupteurs (SWi, SWR) pour fournir à la charge un courant (Ii) représentant une partie d'amplitude élevée avec un front avant rapide, une partie augmentant lentement et une partie d'amplitude oscillante, ce courant étant maintenu autour d'une valeur moyenne sensiblement constante.

2. Système selon la revendication 1, caractérisé en ce que l'unité de commande comprend :

- un premier moyen de calcul (M1) pour traiter un premier temps (Tdérivation), le premier élément interrupteur (SWi) étant maintenu fermé pendant que le second élément interrupteur (SWR) est fermé et l'élément capacitif (Ci) est chargé, pour décharger rapidement cet élément capacitif dans la charge (Li),
- un second moyen de calcul (C1) pour traiter un second temps (Tretard) en maintenant le premier élément interrupteur (SWi) ouvert pendant que le second élément de commutation (SWR) est fermé pour décharger la charge (Li) et
- un troisième et un quatrième élément de calcul

(M2, C2) pour traiter respectivement le troisième et quatrième instant (Tonchop, Toffchop) le premier élément interrupteur (SWi) étant alternativement fermé/ouvert, le second élément interrupteur (SWR) étant fermé pour créer de petites impulsions de courant dans la charge sans transfert d'énergie entre la charge et l'élément capacitif.

3. Système selon la revendication 1 ou 2, caractérisé en ce que l'unité de commande comprend un cinquième et un sixième moyen de calcul (M3, C3) pour traiter respectivement le cinquième et sixième temps (Tonrif, Toffric), le premier élément de commutation (SWi) étant alternativement fermé/ouvert pendant que le second élément interrupteur (SWR) est ouvert, pour générer de petites impulsions de courant dans la charge, puis transférer l'énergie de la charge dans l'élément capacitif.
4. Système selon la revendication 2 ou 3, caractérisé en ce que le premier (M1), le troisième (M2) et le cinquième (M3) moyen de calcul comprennent des cartes électroniques (M1, M2, M3) recevant les signaux d'information (Vbatt/L) et fournissant à leur tour respectivement un premier et un troisième et un cinquième temps (Tdérivation, Tonchop, Tonric).
5. Système selon la revendication 4, caractérisé en ce que les signaux d'information comprennent la valeur de l'inductance (L) de la bobine de l'injecteur et la valeur de la tension (Vbatt) de la source d'alimentation (B) ; les cartes électroniques fournissent des temps (Tdérivation, Tonchop, Tonric) augmentant en fonction de l'augmentation de l'inductance (L) et en fonction de la diminution de la tension (Vbatt) de la source d'alimentation.
6. Système selon l'une des revendications précédentes 2 à 5, caractérisé en ce que le second (C1) et quatrième (C2) moyen de calcul définissent le second et le quatrième temps (Tretard, Toffchop) par des combinaisons linéaires des signaux d'information (Vbatt/L).
7. Système selon la revendication 6, caractérisé en ce que le second (C1) et quatrième (C2) moyen de calcul définissent le second et quatrième temps (Tretard, Toffchop) par des combinaisons linéaires du type :

$$\text{Temps} = (\text{coeff.1} + A * (L - \text{coeff.2}))$$

relation dans laquelle L est la valeur de l'inductance de l'injecteur exprimée en unité μH , le coefficient 1 et le coefficient 2 sont des constantes numériques expérimentales et A est un gain.

8. Système selon l'une quelconque des revendications précédentes, caractérisé en ce que la charge (Li) est reliée par une première borne (104) à la première borne d'entrée (102), la ligne de référence (105) est reliée à la seconde borne d'entrée (103, la charge (Li) est reliée au premier élément interrupteur (SWi) par une seconde borne définissant un premier noeud (107) relié à un second noeud (113) formé de la première borne de l'élément capacitif (Ci) et le second élément de commutation (SWR) est monté entre le second noeud (113) et la première borne (104) de la charge.
9. Système selon la revendication 8, caractérisé en ce que l'élément capacitif (C1) correspond à une seconde borne reliée à la ligne de référence (105).
10. Système selon la revendication 8 ou 9, caractérisé en ce que le premier et le second noeud (107, 113) sont reliés l'un à l'autre par l'intermédiaire d'un premier interrupteur unipolaire (Di) permettant le passage du courant de la charge (Li) à l'élément capacitif (Ci) et entre la première borne d'entrée (102) et la première borne (104) de la charge (Li), il y a un second interrupteur unipolaire (D2) permettant le passage du courant de la première borne d'entrée vers la charge.
11. Système selon la revendication 10, caractérisé en ce que le premier et le second interrupteur unipolaire (Di, D2) sont constitués par une diode jonction.
12. Système selon l'une des revendications précédentes, caractérisé en ce que le premier et second élément interrupteur (SWi, SWR) ont chacun une borne de commande (108) reliée à l'unité de commande (12).
13. Système selon l'une des revendications précédentes, caractérisé en ce que
 - le second élément de commutation et un interrupteur électronique semi-conducteur (SWR) en particulier un transistor MOSFET,
 - par un moyen de commande (114) qui commande l'interrupteur électronique (SWR) et est monté entre une borne de commande (115) de

l'interrupteur électronique et l'unité de commande (12),

- le moyen de commande (114) comprend un moyen pour stocker de l'énergie (C1, C2) et l'interrupteur unipolaire (Dr) placé entre le moyen de stockage d'énergie (C1, C2) et l'élément capacitif (Ci) permet le passage de l'énergie vers le moyen de stockage d'énergie (C1, C2) lors de la charge de l'élément capacitif (Ci), 5
- le moyen de commande comporte également un premier moyen de commutation (SWA) commandé par l'unité de commande (12) et interposé entre le moyen de stockage d'énergie (C1, C2) et la borne de commande (115) de l'interrupteur électronique (SWR), 10 15
- le premier moyen interrupteur (SWA) étant mobile entre une première position ouverte et une seconde position fermée, pour fournir à l'interrupteur semi-conducteur électrique l'énergie nécessaire à sa commutation. 20

14. Système selon la revendication 13, caractérisé par

- un second moyen interrupteur (SWB) entre la borne de commande (115) et la borne (source) de l'interrupteur électronique, 25
- le second moyen interrupteur (SWB) étant activé par l'unité de commande (12) de façon complémentaire à celle du premier moyen interrupteur (SWA). 30

15. Système selon la revendication 14, caractérisé en ce que

le moyen stockant l'énergie est formé d'au moins un condensateur (C2) et un moyen limitant la tension de charge du condensateur (C2). 35

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FIG. 1

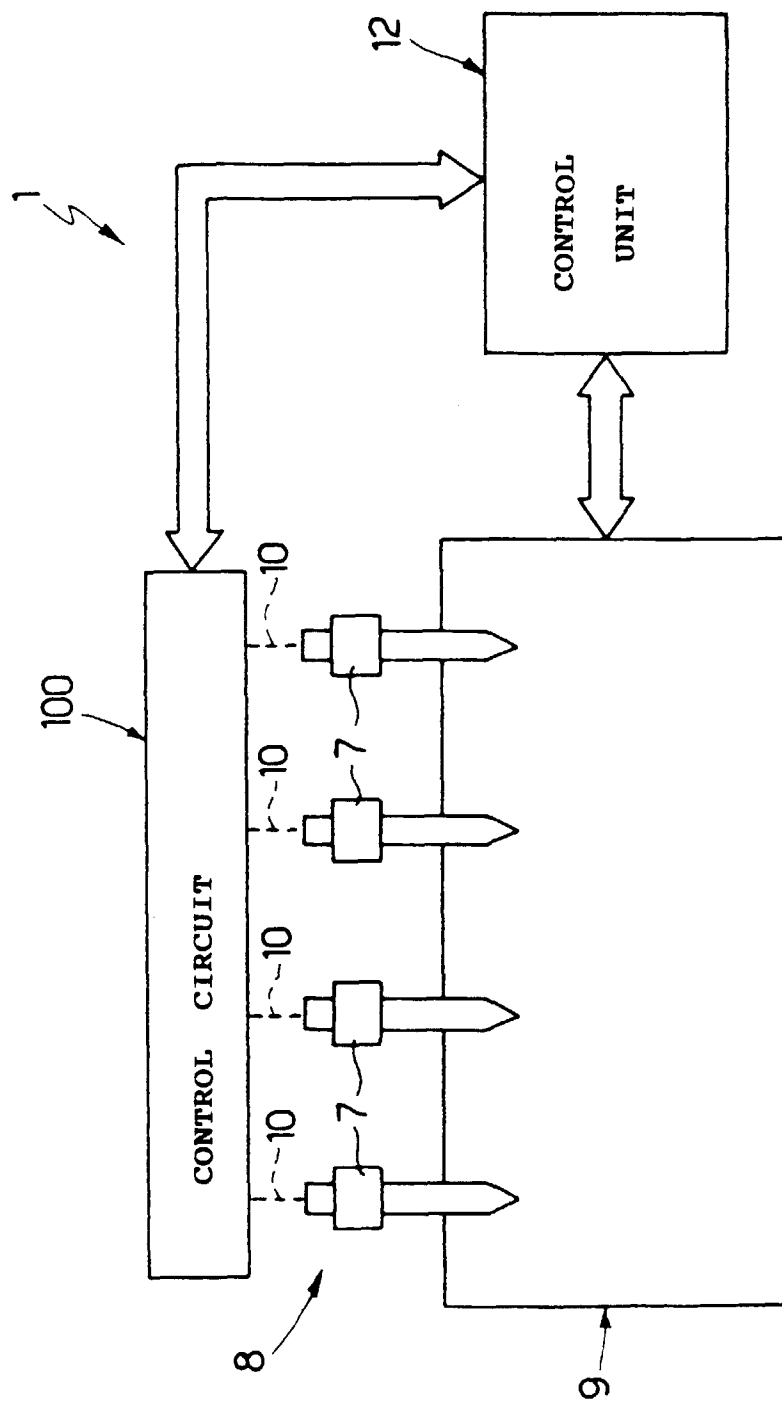
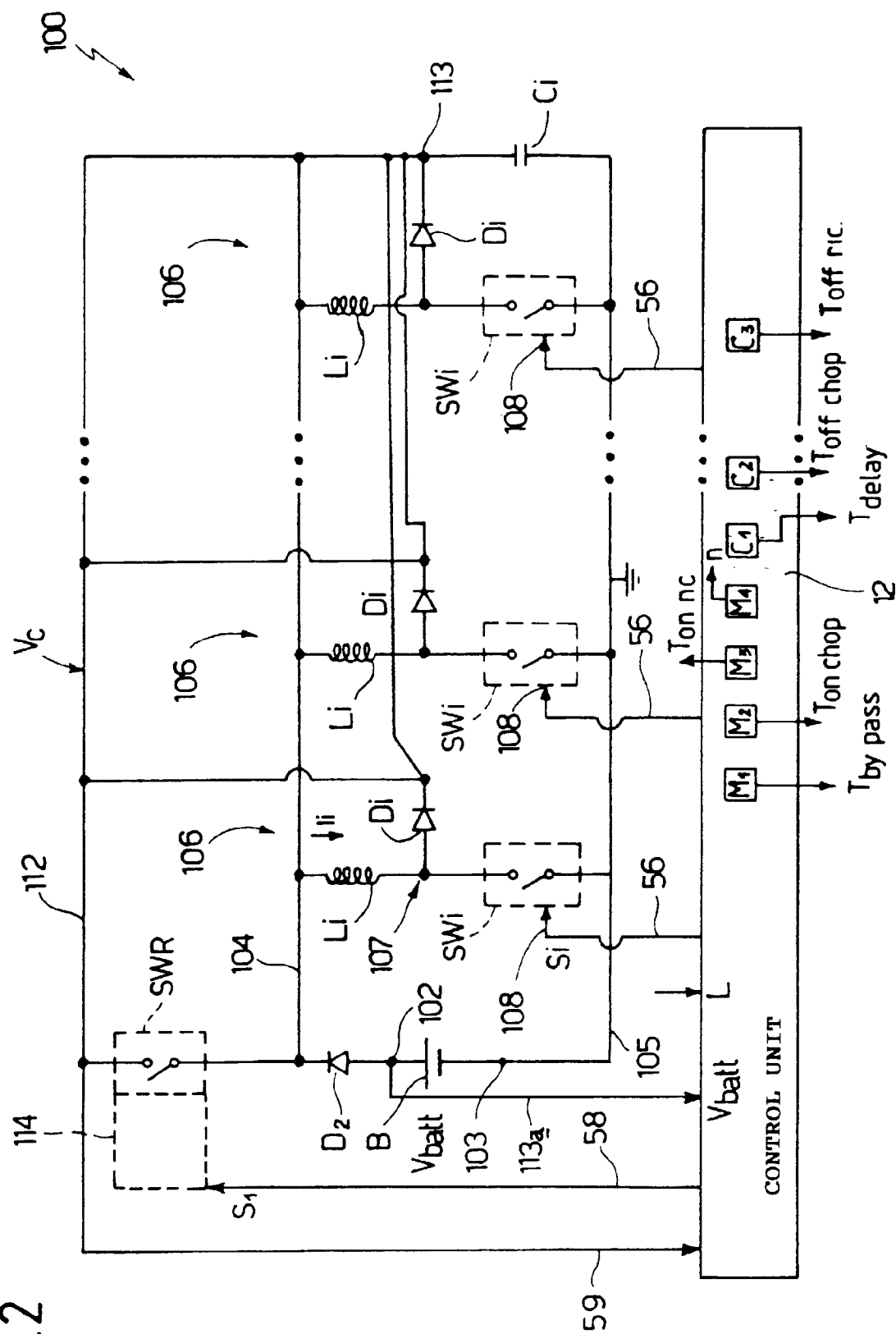
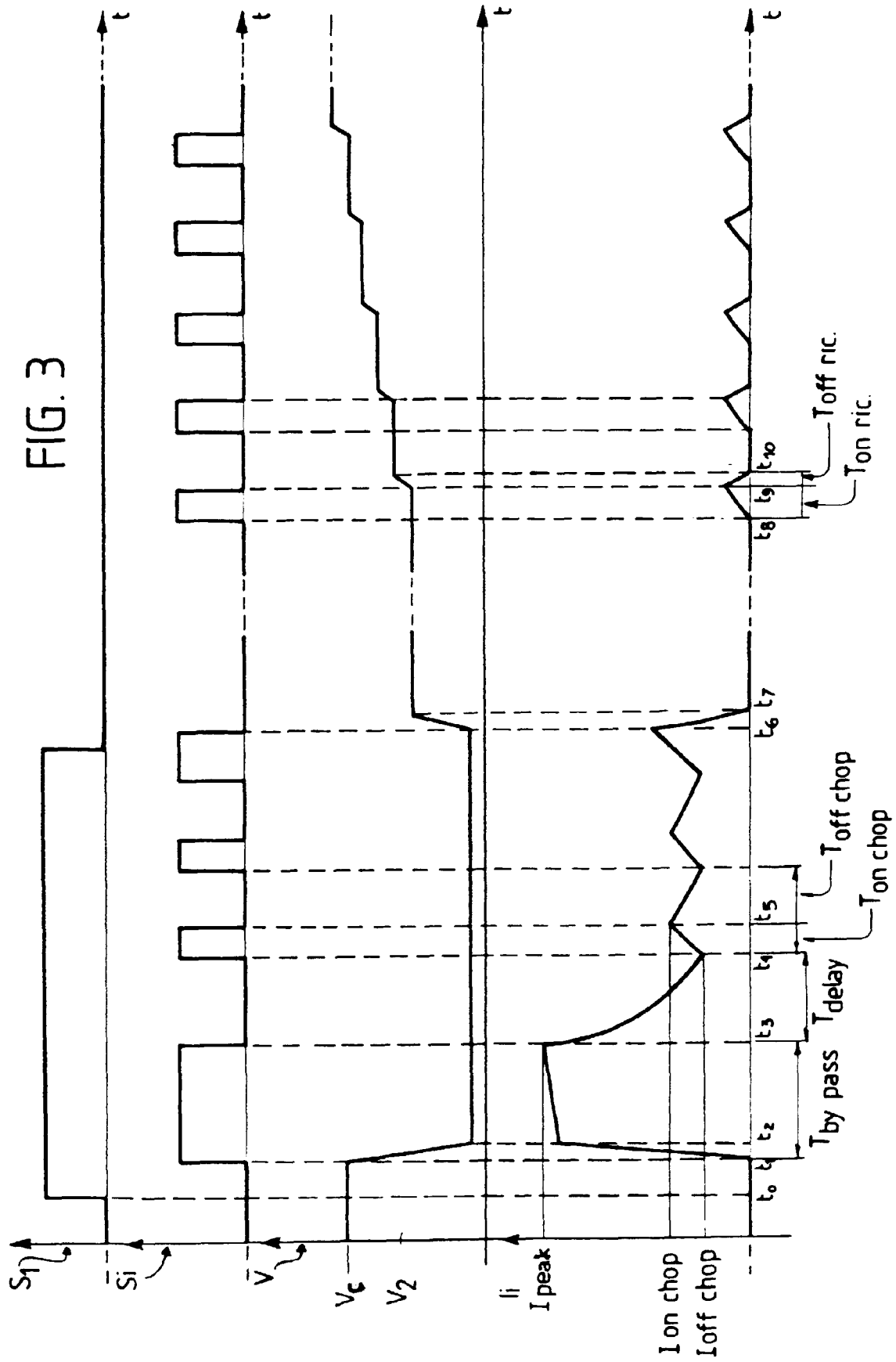


FIG. 2





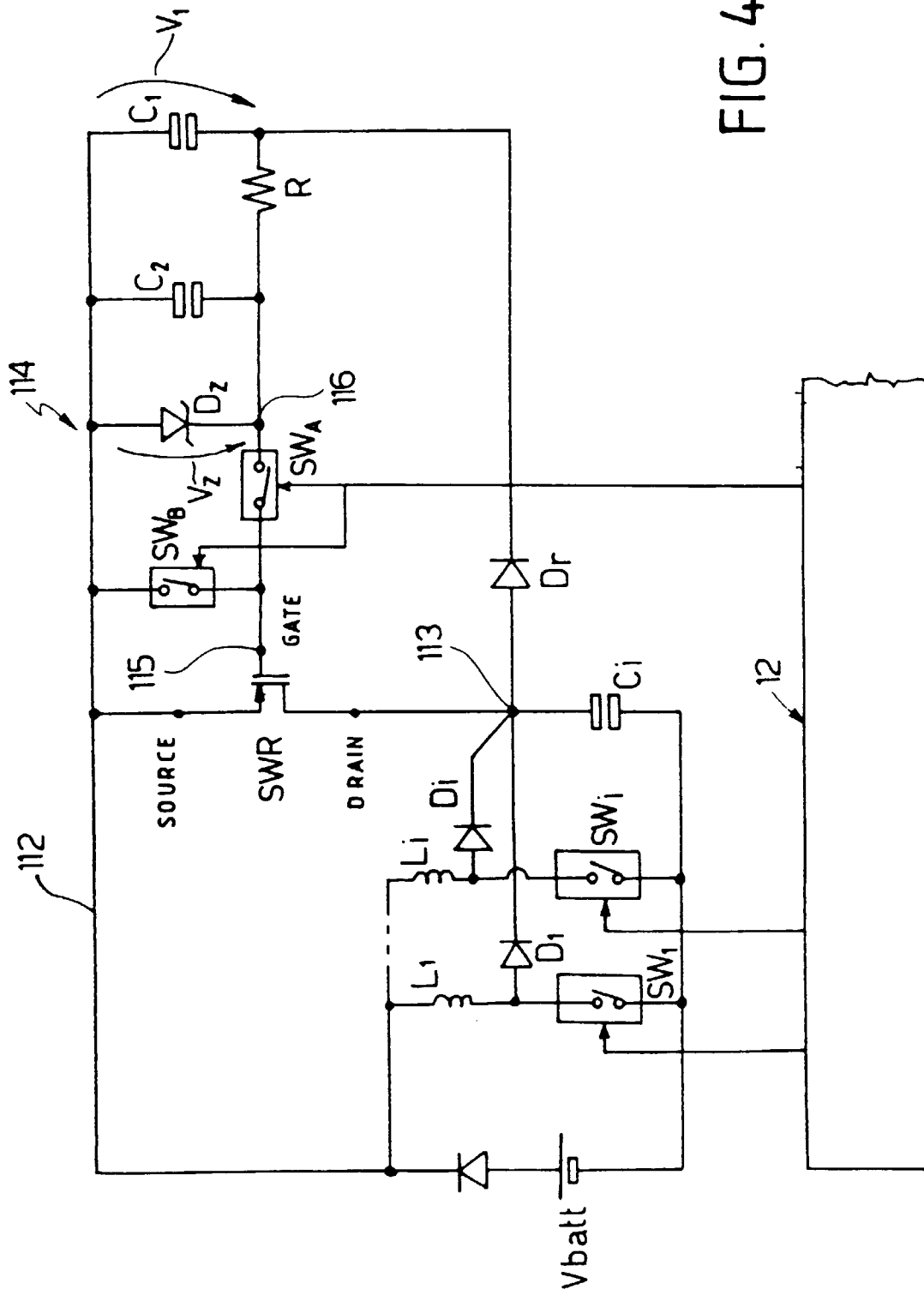


FIG. 4