United States Patent [19]

DuMont et al.

[11] **3,846,801**

[45] **Nov. 5, 1974**

[54] **METHOD AND APPARATUS FOR ELECTROGRAPHIC DRAWING**

[75] Inventors: **Hans-Christoph DuMont,** Malmsheim; **Rainer Strohwald; Helmut Reüm,** both of Stuttgart, all of Germany

[73] Assignee: **Robert Bosch GmbH,** Stuttgart, Germany

[22] Filed: **Mar. 21, 1973**

[21] Appl. No.: **343,397**

[30] **Foreign Application Priority Data**

Mar. 30, 1972 Germany 2215519

[52] **U.S. Cl.** ..... **346/74 E,** 178/6.6 R

[51] **Int. Cl.** **G01d 15/06**

[58] **Field of Search** ..... 346/74 ES, 74 E, 74 SB, 346/74 SC; 178/6.6 R, 6.6 A

[56] **References Cited**

UNITED STATES PATENTS

3,441,946	4/1969	Rudy	346/74 E
3,553,718	1/1971	Schierhorst et al.	346/74 E
3,611,411	10/1971	Mashier et al.	346/74 E
3,613,103	10/1971	Harris	178/6.6 R
3,644,931	2/1972	Stringer et al.	346/74 E

Primary Examiner—Vincent P. Canney

Attorney, Agent, or Firm—Flynn & Frishauf

[57] **ABSTRACT**

Electrographic drawings and facsimiles are made by applying signals sequentially to a multiplicity of writing electrodes in an array in contact with an electrosensitive paper medium. The signals are distributed to the respective electrodes by time-division demultiplexers, and the pulse length of the pulses applied to the electrodes is adjustable to a value less than the burnout time by adjusting the duration of the pulse provided by a monostable flipflop inserted in the signal chain ahead of the demultiplexer input.

11 Claims, 3 Drawing Figures

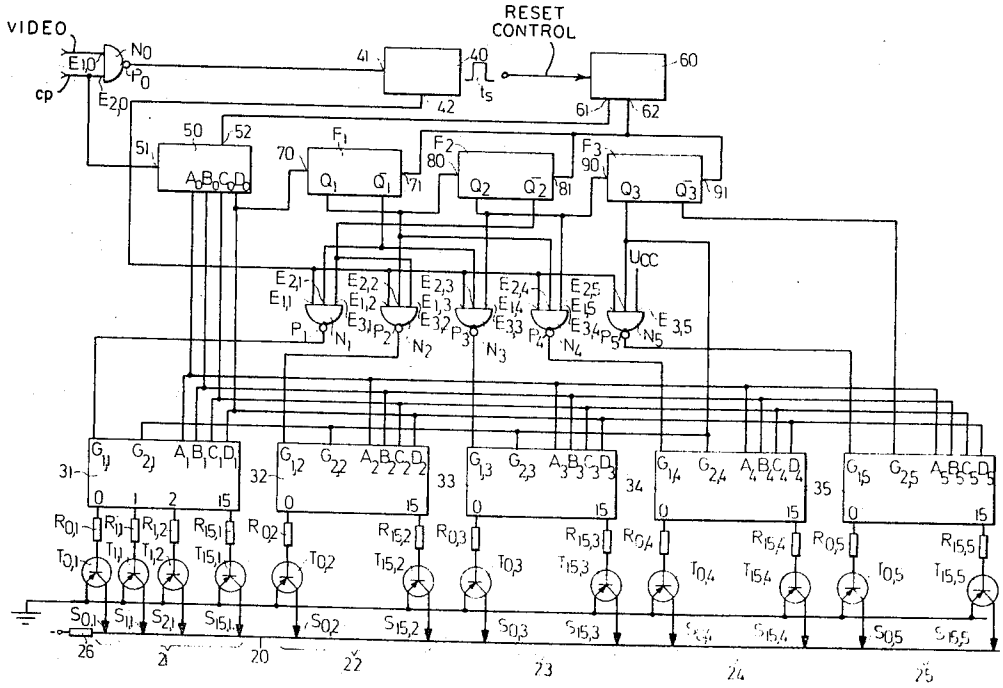


Fig. 1

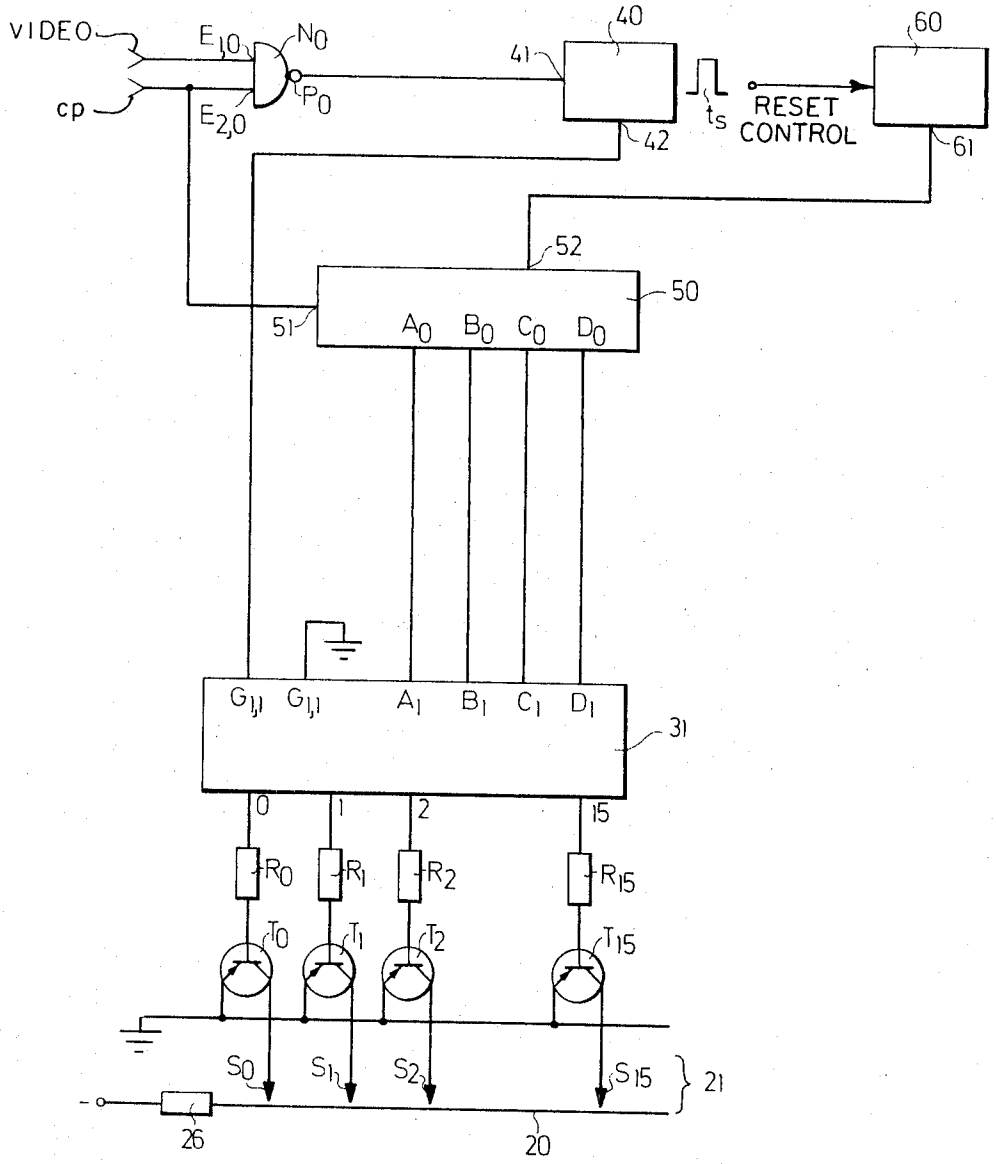

VIDEO
cp
E1,0
E2,0
N0
P0
40
41
42
ts
RESET CONTROL
60
61
52
50
51
A0 B0 C0 D0
G1,1 G1,1 A1 B1 C1 D1
31
0 1 2 15
R0 R1 R2 R15
T0 T1 T2 T15
S0 S1 S2 S15
21
26
20

Fig. 2

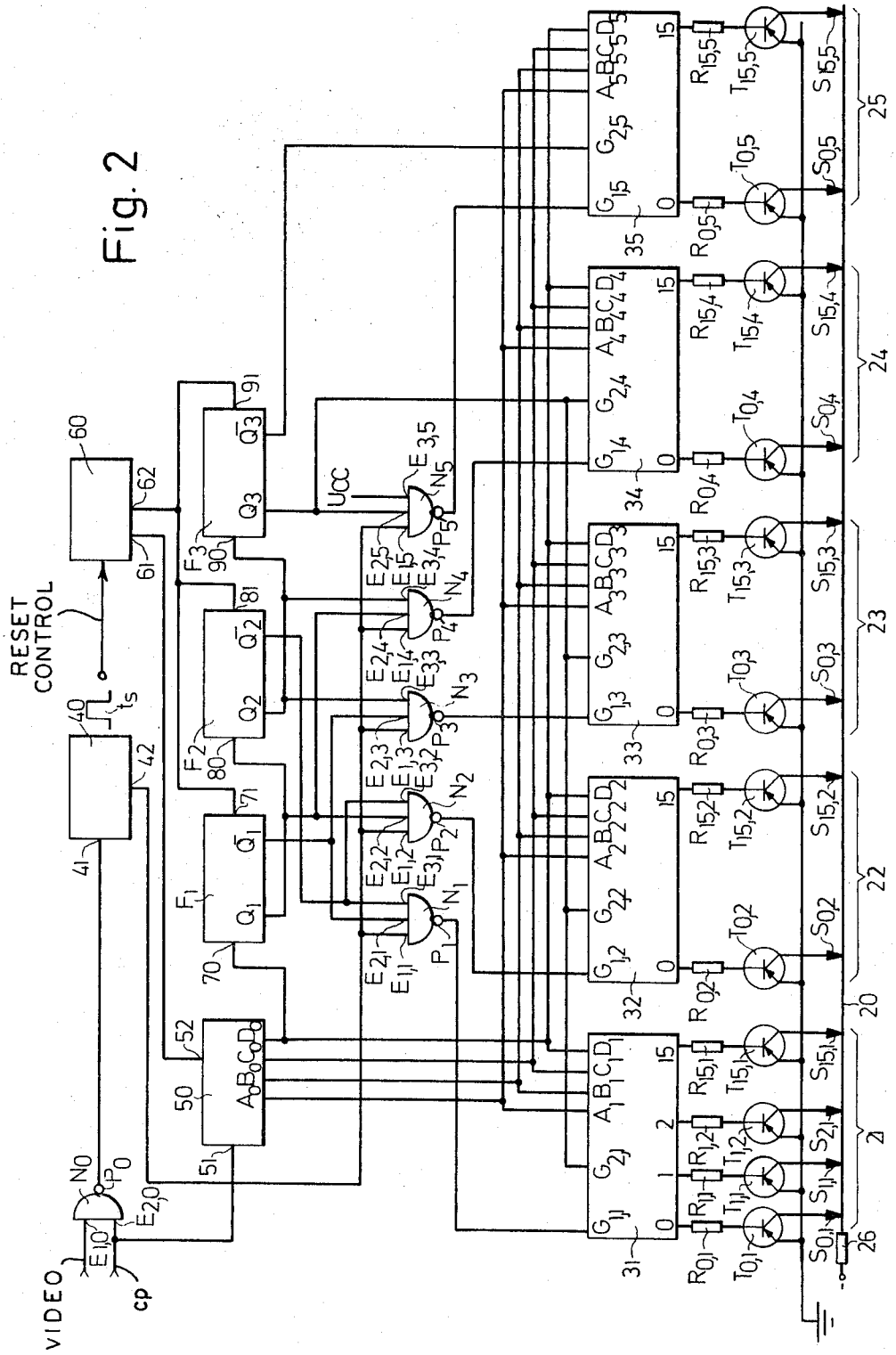
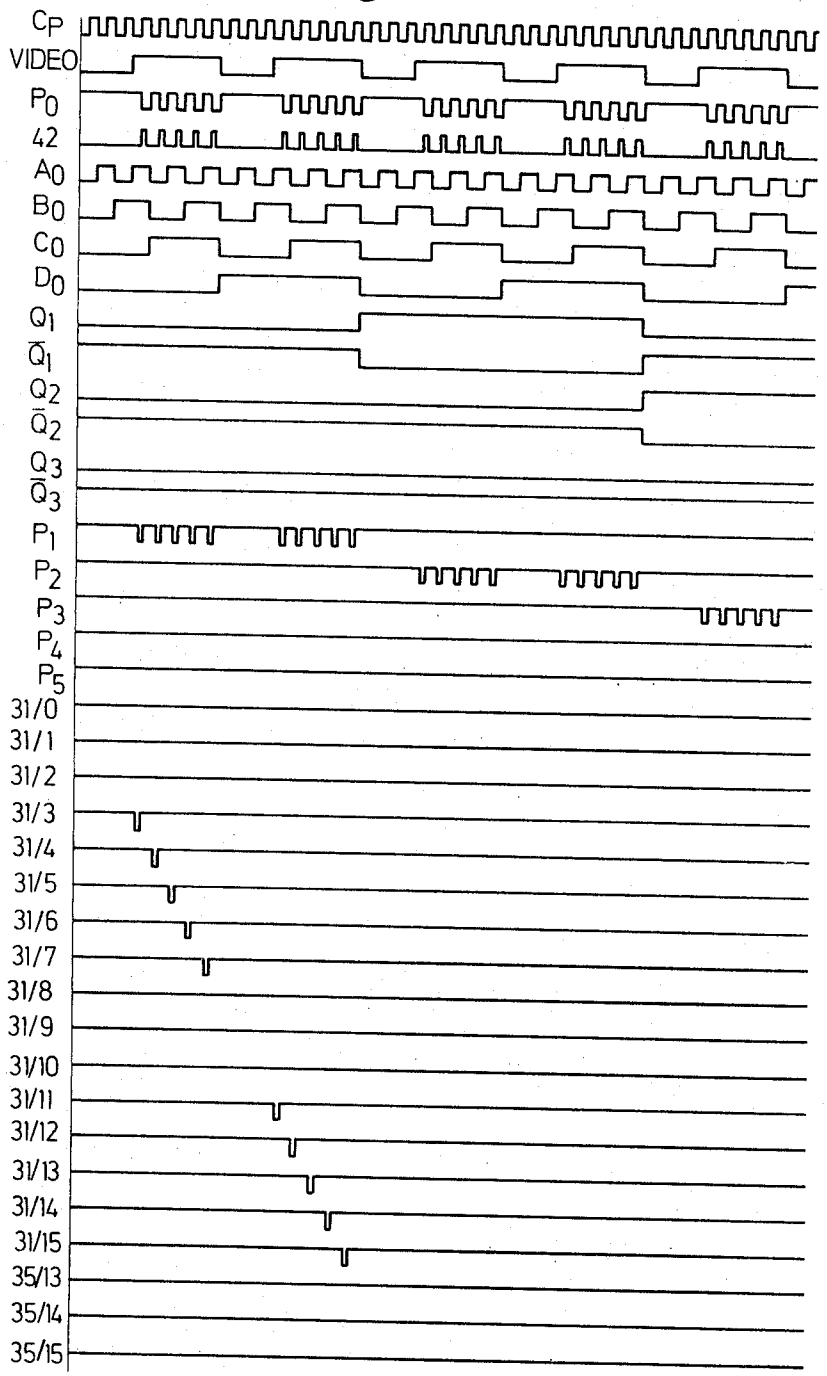


Fig.3


CP
VIDEO
P0
42
A0
B0
C0
D0
Q1
Q̄1
Q2
Q̄2
Q3
Q̄3
P1
P2
P3
P4
P5
31/0
31/1
31/2
31/3
31/4
31/5
31/6
31/7
31/8
31/9
31/10
31/11
31/12
31/13
31/14
31/15
35/13
35/14
35/15

METHOD AND APPARATUS FOR ELECTROGRAPHIC DRAWING

The invention relates to a method and apparatus for recording or reproducing visual information on electrosensitive sheet material, particularly on metallized paper. In particular, the invention concerns the use of writing electrodes arranged next to each other in an array in which each of the electrodes is insulated from the other and is controlled by an individual controllable semiconductor device.

Methods and apparatus of this type are known in which one or more groups of writing electrodes are constructed in the form of a so called electrode comb. In these arrangements, a separate signal source is used for each writing electrode and all of the signal sources simultaneously control the individual writing electrodes. The simultaneous activation of the writing electrodes gives rise to the disadvantage of circuit bridging between electrodes.

It is an object of this invention to provide a method and apparatus for activating a multiplicity of juxtaposed writing electrodes to produce or reproduce graphic material, which avoids the disadvantage of bridging between electrodes.

SUBJECT MATTER OF THE PRESENT INVENTION

Briefly, the electrodes are activated and controlled sequentially and the individual periods for which a single electrode is in circuit is kept shorter than the time in which a limiting effect in the writing is reached as the result of local burnout. Electrographic writing on metallized sheet material produces a small arc that causes metal particles to coalesce. By thus destroying the continuity of the metal film locally, the maximum electrographic effect is reached when the arc burns out. It is desirable to conduct the operation without any of the electrodes being activated long enough to reach burnout, even on a maximum signal. The electrodes are preferably arranged in a line which sweeps across the paper and they are preferably energized in a progressive sequence in with each is connected for energization after the preceding one in line. Any arbitrary sequence can be used, however, especially for encoded transmission cases. The electrodes may, if desired, be arranged for closer packing in a staggered array, for instance, rather than all in one line.

To produce the sequential operation of the writing electrodes, a time-division demultiplexer is used to distribute time subdivisions of the signal to the respective electrodes. The number of outputs of the demultiplexer must then be equal to the number of writing electrodes of the electrode group.

The invention is particularly useful for reproduction of line drawings and incidental lettering and printing, and other two-valued (black and white, for example) graphic information. The information to be displayed on the electrosensitive sheet material is first supplied to one input of a two input NAND gate, the other input of which is constituted by the clock pulses supplied by a timing circuit. The result is a series of pulses of length determined by the clock pulses (i.e., by their period, duty cycle and polarity) and their presence or absence in any clock pulse period is dependent on the state of the input information in that period. The demultiplexer is advanced by means of a binary counter which operates in response to the same clock pulses that are applied to the aforesaid NAND gate. The input to the demultiplexer is thus switched in turn to each of the outputs. Successive signal pulses proceed from each of these outputs in turn to the respective control electrodes of semiconductor devices, each of which electrically drives one of the writing electrodes. The maximum pulse length is less than the clock pulse period, so that each electrode is activated for just one pulse and one signal pulse reaches only a single electrode.

In a further developed form of the invention, it is found desirable to provide a monostable flip-flop ("monoflop") circuit having a manually adjustable period to determine the pulse length and to interpose this circuit between the output of the NAND gate and the signal input of the demultiplexer. In this case, the pulses furnished by the NAND gate to the monostable flip-flop may be either short or long, however the clock pulse gating may produce them, since the monoflop can operate either as a pulse stretcher or a pulse shortener. The modification of the writing time made possible by the adjustment of the period of the monoflop circuit provides control over the point size and hence the degree of blackness of the graphic display, so that writing at various values of gray is possible.

In another illustrative embodiment of the invention the writing electrodes are grouped in a plurality of adjacent groups or sub-arrays, each of which comprises the same number of writing electrodes. Such an apparatus is also drven so that all of the writing electrodes are driven in sequence and that the period for which a single electrode is activated each time is less than the period in which the writing process would come to an end by burnout. In this embodiment of the invention, each sub array of electrodes and their respective driving semiconductors is provided with one of a number of identical demultiplexers, all of which are advanced by a common binary counter. A number of additional flip-flops form a 3 bit binary counter provided for enabling each of the demultiplexers in turn for a complete demultiplexing cycle, so that the signal inputs of all the demultiplexers may be continuously fed in parallel with the same input signal. An extra set of NAND, is interposed between the pulse length determining (monoflop) circuit and each of the demultiplexers, completes the counting function of the flip-flops, in association with additional inputs on each of the demultiplexers interconnected in the counting circuit to provide the necessary sequencing of the demultiplexers. The several demultiplexer units, the 3 bit flip-flop counter, and the 4 bit binary counter used to advance all the demultiplexer units may be regarded as a two-stage demultiplexing means.

An additional pulse forming circuit is used to provide a suitable reset pulse after all of the demultiplexer units have each gone through one demultiplexing cycle.

The invention will be described further by way of example with reference to the accompanying drawings, wherein:

FIG. 1 is a diagram of a circuit according to the invention in which an array of 16 adjacent electrodes is operated through a demultiplexer with 16 outputs;

FIG. 2 is a diagram of a circuit in accordance with the invention in which five groups of 16 electrodes are operated through five demultiplexers, and

FIG. 3 is a graph showing pulses present in the circuits of FIGS. 1 and 2.

In FIG. 1 the electrosensitive paper used as the medium for graphical signal display is designated with the reference numeral **20.** For writing information on the electrosensitive paper **20,** there is provided a group **21** of 16 writing electrodes S_0, S_1, S_2 . . . S_{15} which are arranged next to each other and electrically insulated from each other. These writing electrodes are respectively driven by writing transistors T_0, T_1, T_2 . . . T_{15}. The collectors of the writing transistors are connected to the respective writing electrodes and their emitters are grounded, to the apparatus chassis, for example. The electrosensitive paper **20** is connected to the writing voltage of −35 volts over a resistor **26.**

A demultiplexer **31** of the time-division type serves the electrode group **21.** This demultiplexer is provided with 16 information outputs designated **0, 1, 2 . . . 15** and has four binary switching inputs A_1, B_1, C_1, D_1 serving as tming information inputs and two enable inputs $G_{1,1}$ and $G_{2,1}$. The demultiplexer **31** can accordingly be a commercial type of TTL-demultiplexer built in accordance with integrated circuit techniques, such as the type SN 74154 made by Texas Instruments.

The NAND gates may likewise be provided in integrated circuit form with several on one substrate (e.g., SN 7400 made by Texas Instruments). The binary counter **50** used to step the demultiplexer **31** may likewise by a type SN 7493 Texas Instruments circuit unit. The monoflop **41** may be an SN 74121 device of the same series.

The SN 74154 units used as demultiplexers are TTL logic devices in which the selected output is at "LOW" logic voltage level while all the others are at "HIGH" logic level provided that both of the enable (or "strobe") inputs G_1 and G_2 are likewise at "LOW" logic levl (otherwise the selected output is at "HIGH" logic level, the same as the unselected outputs, which corresponds to no electrographic writing in the present apparatus). The "LOW" logic level could, for example, be 0.8 volts or less, and the "HIGH" logic level 2 or more volts, in a low impedance circuit.

The writing electrodes S_0, S_1, S_2 . . . S_{15} through individual transistors T_0, T_1, T_2 . . . T_{15} which, since of black and one of white are involved, may in this case be of a "switching" type. The information outputs **0, 1, 2, . . . 15** of the demultiplexer **31** are connected over protective resistors R_0, R_1, R_2, . . . R_{15} respectively to the bases of the writing transistors T_0, T_1, T_2 . . . T_{15}.

A NAND gate N_0 with two inputs $E_{1,0}$ and $E_{2,0}$ is provided, to the first input of which the signal to be displayed graphically is first supplied. The output P_0 of the NAND gate N_0 is connected to the input **41** of a monostable flip-flop circuit **40,** the output pulse of which has a variable period the length of which is adjustable by a potentiometer which is not shown in the drawing. The output **42** of the monostable flip-flop ("monoflop") **40** is connected to the first "enable" input $G_{1,1}$ of the demultiplexer **31.** The second input $E_{2,0}$ of the NAND gate N_0 is connected to the pulse input **51** of a 4 bit binary counter **50,** of which the information outputs A_0, B_0, C_0, D_0 are connected to the information inputs A_1, B_1, C_1, D_1 of the demultiplexer **31** to advance the switching circuits of the latter. The second "enable" input $G_{2,1}$ of the demultiplexer **31** is grounded and thus is held in "LOW" condition. Finally a second monostable flip-flop circuit **60** is provided of which the noninverting output **61** is connected to the reset input **52** of the 4 bit binary counter **50.** The reset control input of monoflop **60** may be derived from the counter **50,** from the demultiplexer **31** or from an external timer.

The manner of operation of the circuit of FIG. **1** is as follows:

The information (VIDEO) to be graphically displayed on the electrosensitive paper is applied as a signal to the first input $E_{1,0}$ of NAND gate N_0 (FIG. **3,** second line). At the second input $E_{2,0}$ of NAND gate N_0, a clock pulse c_P externally supplied to the circuit appears which also advances the 4 bit binary counter **50.** The pulses appearing at the output P_0 of NAND gate N_0 are shortened in duration in monoflop circuit **40** to a value t_S corresponding to the switching time of each of the writing electrodes S_0, S_1, S_2, . . . S_{15}, this value being adjustable by a potentiometer not shown in the drawing. This period t_S of the pulses appearing at the output of monoflop **40** is so adjusted that it is shorter than the time in which the electrographic effect would come to an end by burnout.

If short pulses rather than long pulses are put out by the NAND gate N_0, which as previously discussed depends upon the polarity and duty cycle of the clock pulses and the polarity in which the output pulses are effective, then the monoflop **40** can operate as a pulse stretcher instead of as a pulse shortener, with the result in any event being the same. Furthermore, if the signals to be represented graphically are not two-valued, but are of various levels that are to be reproduced with gradation in the electrographic process, then the NAND gate N_0 is not an ordinary digital gate but it is in effect a switched amplifier and the monoflop **40** switches on an amplifier or other device (not shown) during the length of its output pulse so that the output of the combined arrangement will have an amplitude corresponding to the signal at the input of the system and a pulse length determined by the setting of the monoflop **40.** It is also possible to have the amplitude of the input signal very the duration of the pulse produced by monoflop **40,** by means not shown, instead of the provision of the manual pulse length adjustment.

The pulses taken from the output of monoflop **40** are supplied to the signal input $G_{1,1}$ of demultiplexer **31,** whereas the second signal input $G_{2,1}$ is held in the "LOW" condition. The clock pulse c_P, as already mentioned, advances the 4 bit binary counter **50,** which is to say that it causes the outputs A_0, B_0, C_0, D_0 of the counter **50** to go through all 16 possible sets of binary conditions in logical sequence. These output count pulses of the 4 bit binary counter **50** are provided to the information inputs A_1, B_1, C_1, D_1 of the demultiplexer **31,** causing the switching circuits of the latter to be advanced as previously mentioned. In this way the information outputs **0, 1, 2, . . . 15** of demultiplexer **31** are caused to produce one after the other in sequence as timed by the pulses present at the first input $G_{1,1}$ are switched to the "LOW" condition for the period p_S of a single pulse. A writing pulse consequently appears only at the particular information outputs which, at that moment, receive a VIDEO signal with the necessary information to produce a pulse. The writing pulses transmitted from the information outputs **0, 1, 2, . . . 15** of demultiplexer **31** are led to the base electrodes of writing transistors T_0, T_1, T_2 . . . T_{15}, respectively over resistors R_0, R_1, R_2, . . . R_{15}. After all of the writing electrodes have been connected in turn to the demultiplexer, the 4 bit binary counter **50** is reset to its original

condition by a reset pulse, the duration of which is determined by monoflop **60.**

FIG. **2** shows a second embodiment of the invention. For the graphic display of information on electrosensitive paper, there are here provided five adjacent electrode groups **21, 22, 23, 24, 25,** each of which contains 16 writing electrodes arranged next to each other and insulated from each other. The writing electrodes of the first group **21** are designated $S_{0,1}$, $S_{1,1}$, $S_{2,1}$, . . . $S_{15,1}$; those of the second group **22** are designated $S_{0,2}$, $S_{1,2}$, $S_{2,2}$, . . . $S_{15,2}$ and so on. The writing electrodes $S_{0,i}$, $S_{1,i}$, $S_{2,i}$, . . . $S_{15,i}$ of each group are controlled over writing transistors $T_{0,i}$, $T_{1,i}$, $T_{2,i}$, . . . $T_{15,i}$ where the subscript i may take the value 1, 2, 3, 4 and 5 according to whether it refers to the writing electrode or to the writing transistor in the first group **21,** the second group **22,** the third group **23,** etc. The collectors of the writing transistors are connected to the writing electrodes, while their emitters are grounded. The electrosensitive paper **20** is connected to the writing voltage of −35 volts over a resistor **26.** Each of the five electrode groups **21, 22, 23, 24, 25** is provided with one of the five identical demultiplexers **31, 32, 33, 34, 35.** Each demultiplexer is provided with two signal inputs $G_{1,i}$, $G_{2,i}$ and with four binary information inputs A_i, B_i, C_i, D_i, where the subscript i may take the values **1, 2, 3, 4, 5** according to whethr the demultiplexer is associated with the first electrode group **21,** the second electrode group **22,** and so on. Each of the demultiplexers also has 16 information outputs, in each case designated **0, 1, 2 . . . 15.** These information outputs are connected to the base of the respective writing transistors $T_{0,i}$, $T_{1,i}$, $T_{2,i}$ . . . $T_{15,i}$ over the resistors $R_{0,i}$, $R_{1,i}$, $R_{2,i}$ . . . $R_{15,i}$, respectively.

The NAND gate N_0 is provided with two inputs $E_{1,0}$ and $E_{2,0}$. The output P_0 of the NAND gate N_0 is connected to the input **41** of a monoflop **40** of which the output pulses have a variable pulse duration t_S, which may be varied by adjustment of a potentiometer not shown in the drawing. The second input $E_{2,0}$ of NAND gate N_0 is connected to a clock pulse source (not shown) and to the pulse input **51** of a 4 bit binary counter **50,** the information of which are designated A_0, B_0, C_0 and D_0. These information outputs are connected to the information inputs A_i, B_i, C_i, D_i of all the demultiplexers **31, 32, 33, 34, 35,** in which arrangement the output A_0 is connected with all the inputs A_i ($i = 1$ to 5), the output B_0 is connected with all the inputs D_i ($i = 1$ to 5), the output C_0 is connected with all the inputs C_i ($i = 1$ to 5) and the output D_0 is connected with all the inputs D_i ($i = 1$ to 5).

Five NAND gates N_1, N_2, N_3, N_4 and N_5, each with three inputs $E_{1,i}$, $E_{2,i}$, $E_{3,i}$, are provided in connection with each of the five demultiplexers **31, 32, 33, 34, 35.** The outputs of these NAND gates are designated P_i, where $i = 1$ to 5. The first enable input $G_{1,2}$ of the first demultiplexer **31** is connected to the output P_1 of NAND gate N_1, the first enable input $G_{1,2}$ of the second demultiplexer **32** is connected to the output P_2 of NAND gate N_2, and so on. Each of the first inputs $E_{1,i}$ of the five NAND gates N_1, N_2, N_3, N_4, N_5 is connected to the output **42** of monoflop **40.**

In this circuit three flip-flops F_1, F_2 and F_3 are provided. The input **70** of first flip-flop F_1 is connected to the output D_0 of 4 bit binary counter **50.** The input **80** of second flip-flop F_2 is connected to the noninverting output Q_1 of first flip-flop F_1. The input **90** of third flip-flop F_3 is connected to the noninverting output Q_2 of second flip-flop F_2. The inverting output $\overline{Q}_3$ of third flip-flop F_3 is connected to the second enable input $G_{2,5}$ of fifth demultiplexer **35.** The noninverting output Q_3 of third flip-flop F_3 is connected to the second enable inputs $G_{2,1}$, $G_{2,2}$, $G_{2,3}$ and $G_{2,4}$ of the remaining four demultiplexers **31, 32, 33, 34.** The second input $E_{2,1}$ of NAND gate N_1 is connected to the inverting output $\overline{Q}_1$ of first flip-flop F_1. The third input $E_{3,1}$ of NAND gate N_1 is connected to the inverting output $\overline{Q}_2$ of second flip-flop F_2. The second input $E_{2,2}$ of NAND gate N_2 is connected to the noninverting output Q_1 of first flip-flop F_1. The third input $E_{3,2}$ of NAND gate N_2 is connected to the inverting output $\overline{Q}_2$ of second flip-flop F_2. The second input $E_{2,3}$ of NAND gate N_3 is connected to the inverting output $\overline{Q}_1$ of first flip-flop F_1. The third input $E_{3,3}$ of NAND gate N_3 is connected to the noninverting output Q_2 of second flip-flop F_2. The second input $E_{2,4}$ of NAND gate N_4 is connected to the noninverting output Q_1 of first flip-flop F_1. The third input $E_{3,4}$ of NAND gate N_4 is connected to the noninverting output Q_2 of second flip-flop F_2. The second input $E_{2,5}$ of NAND gate N_5 is connected to the noninverting output Q_3 of third flip-flop F_3. The third input $E_{3,5}$ of NAND gate N_5 is held in "HIGH" condition by connection to the supply voltage U_{cc}.

A second monoflop **60** is also provided. The noninverting output **61** of monoflop **60** is connected to the reset input **52** of the 4 bit binary counter **50.** The inverting output **62** of monoflop **60** is connected to the reset inputs **71, 81, 91** of the three flip-flops F_1, F_2 and F_3.

The reset control connection of monoflop **60** may be derived from multiplexer **35,** from flip-flop F_3 or from an external timer or synchronizer (not shown).

The manner of operation of the circuit of FIG. **2** is as follows:

The information (VIDEO) to be graphically displayed on electrosensitive paper is applied to the first input $E_{1,0}$ of NAND gate N_0. Such a VIDEO signal is shown in the second line of FIG. **3** by way of example. At the second input $E_{2,0}$ of NAND gate N_0, there is applied a clock pulse c_P which is also applied to the input of 4 bit binary counter **50** to advance that counter. The pulses appearing at the output P_0 of NAND gate N_0 has their duration shortened in monoflop **40** to a value which corresponds to the switching interval t_S of each of the individual electrodes S_0, S_1, S_2 . . . S_{15}, this value being adjustable by means of a potentiometer not shown in the drawing. This duration t_S of the pulses formed at the output **42** of monoflop **40** is so adjusted that it is shorter than the time that would end the writing process by burnout. These pulses taken from the output **42** of monoflop **40** are applied to the first inputs $E_{1,i}$ of the NAND gates N_i, of which the outputs P_i are connected to the first signal inputs $G_{1,i}$ of the demultiplexers.

The clock pulse c_P, as already mentioned, advances at the same time the 4 bit binary counter **50,** so that at its information outputs A_0, B_0, C_0, D_0 all 16 possible output combinations are provided in logical sequence. These output pulses of the 4 bit binary counter **50** are supplied to the several parallel connected information inputs A_i, B_i, C_i and D_i of the demultiplexers **31, 32, 33, 34, 35.** If both of the signal inputs $G_{1,i}$ and $G_{2,i}$ of the demultiplexers were simultaneously in the "LOW" condition, then the information outputs **0, 1, 2 . . . 15**

of the demultiplexers **31, 32, 33, 34** and **35** would each in sequence and in the red above the writing impulses be connected to the "LOW" condition for the duration t_S of a single pulse. The **0** outputs of all demultiplexers would simultaneously be switched to "LOW," and then all the **1** outputs, then all the **2** outputs and so on until what the sixteenth, all the **15** outputs would be connected to "LOW" and then it would begin again with all the **0** outputs.

By means of the flip-flops F_1, F_2 and F_3, however, the second signal inputs $G_{2,i}$ of the demultiplexers are so switched that only one demultiplexer is free to accept signals at any time. The signals appearing at the output **42** of monoflop **40** are combined with the output signals of the flip-flops F_1, F_2 and F_3 and then provided to the first signal input $G_{1,i}$ of the demultiplexers. Consequently, only the output of one demultiplexer writes the demultiplexer being selected sequentially by the counter composed of flip-flops F_1, F_2, F_3 and associated circuits, the selection being made in accordance with the distribution plan for the VIDEO signal. The writing pulses arising at the information outputs **0, 1, 2 . . . 15** of the demultiplexers **31, 32, 33, 34, 35** are furnished over the protective resistances $R_{0,i}$, $R_{1,i}$, $R_{2,i}$, . . . $R_{15,i}$ to the base electrodes of the respective writing transistors $T_{0,i}$, $T_{1,i}$, $T_{2,i}$, . . . $T_{15,i}$, which each in turn switch the writing voltage through to the electrode for the duration t_S of the pulse. After all of the writing electrodes $S_{0,i}$, $S_{1,i}$, $S_{2,i}$, . . . $S_{15,i}$ of all groups **21, 22, 23, 24** and **25** have been run through in sequence, in the illustrated case, therefore, after 80 clock pulses, all of the counters **50**, F_1, F_2, F_3 are reset to the initial condition by a reset pulse which has its duration defined by the operation of monoflop **60.**

The invention has been described in connection with VIDEO signals of a binary or two-valued kind, because in the illustrated case of metallized paper writing material the darkness of writing is difficult to control linearally with reference to pulse voltage, so that degrees of blackness are adjusted by the monoflop pulse duration rather than otherwise. Consequently, the driving transistors T_0, T_1, T_2 . . . T_{15} may be switching type transistors, since their function is to switch the writing voltage to the electrode or not according to whether a VIDEO signal is present or not during the period that the particular transistor is connected through to the monoflop pulse generator **40** through the demultiplexer. If there is no VIDEO signal present at the time of the corresponding clock pulse, the monopulse flip-flop **40** will not be activated and the particular electrode connected through the demultiplexer at that particular time will not write at its turn in that particular sequence.

A particularly convenient way of providing the electrodes is to assemble a multiplicity of electrodes in an electrode comb organization together with the corresponding driving transistors, protective resistors and the multiplexers and such an electrode comb can consist of individual segments if more than one demultiplexer is used, with one segment for the equipment associated with each demultiplexer. The writing electrodes are preferably made of tungsten wire and they may very conveniently be provided by plating the end of the tungsten wire, which used to be connected to the transistor by electroplating with copper, gold, silver, tin or a combination of those metals and then soldering the plated end of the tungsten wire directly to the collector connection of the driving transistor with soft solder.

Although the invention has been disclosed with reference to specific embodiments, it will be understood that variations and modifications may be made within the inventive concept without departing from the spirit of the invention.

We claim:

1. The method of visually recording electrical information by means of a multiplicity of writing electrodes, arranged in a substantially linear array and electrically insulated from each other, on electrosensitive sheet material, which method comprises the steps of:

preparing information to be recorded in sequential form;

gating said information at intervals to produce a sequence of pulses having a predetermined duration less than the shortest time required to produce local burnout on said sheet material therefrom, and

connecting individual electrodes of said array in succession, for time intervals longer than the duration of said pulses to a circuit supplying said sequence of pulses,

thereby energizing those electrodes so connected when one of said pulses is present and then only for the duration of said respective pulses.

2. The method of visually recording information by means of a multiplicity of writing electrodes, arranged next to each other and electrically insulated from each other, on electrosensitive sheet material the electrographic effect on which is limited by a localized burnout characteristic, which method comprises the steps of:

modifying information to be recorded into the form of information pulses of a duration less than the period in which the activation of one of said electrodes would come to a stop by local burnout;

connecting said electrodes in time sequence to a source of information so modified at switching intervals greater than the duration of said information pulses,

thereby energizing those electrodes so connected when one of said pulses is present and then for the duration of said respective pulses.

3. The method of visually recording electrical information by means of a multiplicity of writing electrodes, arranged in a substantially linear array and electrically insulated from each other, on electrosensitive sheet material, which method comprises the steps of:

generating a sequence of clock pulses (c_p);

counting said pulses and driving with count indicating signals (A, B, C, D) thereby produced the distributive switching of a time-division demultiplexer (**31**);

applying said clock pulses and also electrical information to be recorded to gate means (N_0) to produce gated pulses of said electrical information;

applying said gated pulses, or pulses derived therefrom, to the signal input of said multiplexer;

applying the distributed outputs of said demultiplexer respectively to the control electrodes of controlled semiconductor devices (T_0, T_1, T_2 . . .), and

controlling the energization of said writing electrodes (S_0, S_1, S_2 . . .) respectively by means of said controlled semiconductor devices in such a manner as to energize said electrodes sequentially, and each only when one of said gated pulses is present and then only for the duration of such gated pulse.

4. A method as defined in claim 3 in which the modifying of the electrical information to be recorded comprises the steps of:

applying said clock pulses and electrical information to be recorded to said gate means (N_0) to produce gated pulses of said information;

deriving, from said gated pulses, pulses of a different time length less than said burnout period, and

applying said derived pulses to the signal input of said multiplexer.

5. Apparatus for displaying information on electrosensitive sheet material, the electrographic effect on which is limited by a localized burnout characteristic comprising:

an array of a multiplicity of adjacent writing electrodes electrically insulated from each other;

a clock pulse generator;

gate means (N_0) for producing gated pulses timed by said clock pulses from a signal representative of information to be displayed;

demultiplexing means (**31**) having a successive sequencing interval, determined by said clock pulse generation, at least as long as the time required to produce local burnout on said sheet material and including a binary counter (**15**) responsive to said clock pulses for distributing said pulses produced in response to operation of said gate means in sequence to the individual writing electrodes of said array, said gate means accordingly being the same for all pulses, and

circuit means incorporated in said gate means for assuring that the duration of pulses supplied to said demultiplexing means in response to operation of said gate means is less than the time required to produce local burnout on said sheet material.

6. Apparatus as defined in claim 5 in which said circuit means incorporated in said gate means is a monostable pulse forming means (**40**) of adjustable pulse length interposed between said gate means and said multiplexer.

7. Apparatus as defined in claim 5 in which a multiplicity of controlled semiconductor devices (T_0, T_1, T_2 . . . T_{15}) are interposed between the outputs of said demultiplexing means (**31**) and the respective writing electrodes (S_0, S_1, S_2 . . . S_{15}) of said array to control the energization of said writing electrodes.

8. Apparatus for displaying information on electrosensitive sheet material, the electrographic effect on which is limited by a localized burnout characteristic, comprising:

an array of a multiplicity of adjacent writing electrodes electrically insulated from each other, said electrodes of said array being disposed in a plurality of sub arrays (**21, 22, 23, 24, 25**), each comprising the same number of writing electrodes (S_0, *i*, S_1, *i*, S_2, *i* . . . S_{15}, *i*);

a clock pulse generator;

monostable gate means (N_0) for producing, from a signal representative of information to be displayed, gated pulses timed by said clock pulse generator and having a duration less than the time required to produce local burnout on said sheet material;

a plurality of functionally identical demultiplexers (**31, 32, 33, 34, 35**) timed by said clock pulse generation and respectively arranged to distribute said gated pulses in turn to each sub array (**21, 22, 23, 24, 25**) of said writing electrodes, each of said demultiplexers hiving two signal inputs and having individual gate means connected between a first signal input of said demultiplexer and the output of said monostable gate means, said individual gate means having a first input to which the output of said monostable circuit is connected and two additional inputs;

a resetting circuit; and

a plurality of flip-flop circuits are interconnected with each other, with the second and third inputs of said individual gate means and with the second inputs of said demultiplexers and also with said resetting circuit, so that each of said demultiplexers will be activated for a complete cycle of operation in sequence while the others of said demultiplexers are furnishing no output, whereby each one of said writing electrodes will be activated in turn.

9. Apparatus as defined in claim 8 in which one or more of said sub arrays of writing electrodes are mounted on an electrode comb consisting of individual segments which contain writing electrodes, driving semiconductor devices therefor, and demultiplexers.

10. Apparatus as defined in claim 9 in which the writing electrodes are made up of tungsten wires.

11. A method of making an apparatus for electrographically displaying formation in which the ends of the tungsten wires forming the writing electrodes of said apparatus which are to be connected to the respective driving semiconductor devices of said apparatus are electroplated with a metallic material selected from the group consisting of the metals copper, gold, silver, tin, and combinations of said metals as simultaneously electroplated, and are then affixed with the thus electroplated end soldered with soft solder to the collector connection of the corresponding driving semiconductor device.

* * * * *