(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
23 June 2016 (23.06.2016)

WIPO | PCT

(10) International Publication Number
WO 2016/099783 A1

(51) International Patent Classification:
G01R 31/28 (2006.01) *G01R 1/073* (2006.01)
G01R 31/26 (2006.01)

(21) International Application Number:
PCT/US2015/061502

(22) International Filing Date:
19 November 2015 (19.11.2015)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
14/577,687 19 December 2014 (19.12.2014) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) **Title**: CONTROLLING A PER-PIN MEASUREMENT UNIT

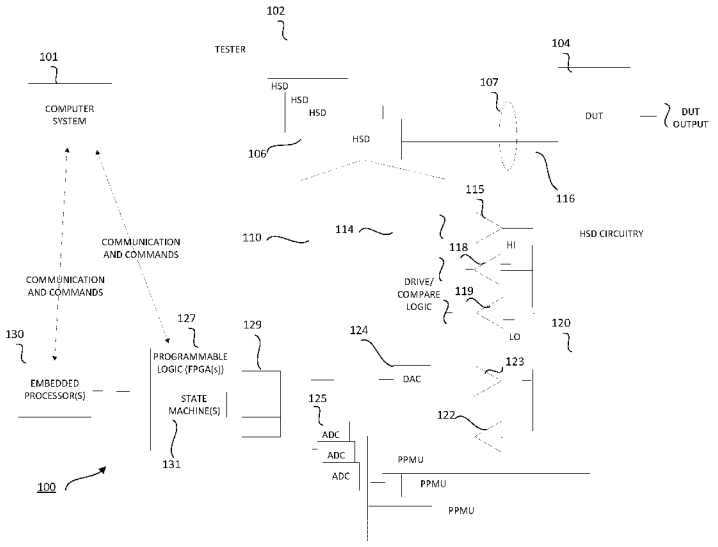


FIG. 1

(57) **Abstract**: Example automatic test equipment (ATE) includes: a per-pin measurement unit (PPMU); logic configured to execute a state machine to control the PPMU; memory that is part of, or separate from, the logic; and a control system to command the logic; where, in response to a command from the control system, the state machine is configured to obtain, at a known interval or ATE event, data that is based on an output of a measurement by the PPMU and to store the data in the memory, or to output data to the PPMU from the memory at a known interval or synchronous to an event.

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CONTROLLING A PER-PIN MEASUREMENT UNIT

TECHNICAL FIELD

This specification relates generally to controlling a per-pin measurement unit (PPMU) that is part of automatic test equipment (ATE).

BACKGROUND

Automatic Test Equipment (ATE) refers to an automated, usually computer-driven, system for testing devices, such as semiconductors, electronic circuits, and printed circuit board assemblies. Devices tested by ATE are referred to as devices under test (DUT). ATE includes a per-pin measurement unit (PPMU). In some ATE, the PPMU is configured to receive analog signals from a DUT, and to output analog signals to the DUT as part of a test process.

SUMMARY

Example automatic test equipment (ATE) comprises: a per-pin measurement unit (PPMU); logic configured to run a state machine to control the PPMU; memory that is part of, or separate from, the logic; and a control system to command the logic; where, in response to a command from the control system, the state machine is configured to obtain, at a known interval or in synchronous to an event, data that is based on an output of a measurement by the PPMU and to store the data in the memory, or to output data to the PPMU from the memory at a known interval or

synchronous to an event. The example ATE may include one or more of the following features, either alone or in combination.

The ATE may be configured to test a device under test (DUT), the DUT having multiple pins. The ATE may be configured to obtain, via the PPMU, data that is based on values at a single pin of the DUT and to store the data in the memory. The ATE may be configured to test a DUT having multiple pins. The ATE may be configured to obtain, via the PPMU, data that is based on values at multiple pins of the DUT and to store the data in the memory. The known intervals may be programmable.

The ATE may comprise: an analog-to-digital converter (ADC) between the logic and the PPMU, the ADC for servicing one or multiple PPMUs including the PPMU; where the logic is configured to obtain the data by retrieving the data from the ADC. The ATE may be configured to test a DUT having multiple pins; where: the ATE is configured to obtain, via the PPMU, data that is based on values at a single pin of the DUT and to store the data in the memory; the logic is configured to provide the data to the control system; and the control system is configured to reconstruct a waveform based on the data.

The ATE may be configured to test a DUT having multiple pins; where the ATE is configured to obtain, via the PPMU, data that is based on values at a single pin of the DUT and to store the data in the memory; wherein the data is usable to perform one or more operations comprising measuring signal noise or extracting signal peak amplitude.

The ATE may be configured to output a digital pattern to the DUT, the digital pattern containing control data; and the ATE may be configured to use the control data to control the logic based on the control data. The ATE may be configured to control when the logic obtains data that is based on an output of the PPMU, or outputs data to the PPMU from the memory. The ATE may be configured to control the logic to obtain data at a time that is based on the control data.

The ATE may comprise a processing device that is responsive to the control system to control operation of the logic. The logic may comprise a field programmable gate array (FPGA); where the ATE comprises multiple FPGAs, each of the multiple FPGAs being configured to run a state machine to control one or more PPMUs; and wherein the processing device is configured to control the multiple FPGAs.

The PPMU may comprise a digital-to-analog converter and the memory stores signal data; and the logic may be configured to send the signal data to the memory, and the PPMU is configured to generate an AC waveform for delivery to the DUT based on the signal data.

The AC waveform may be an analog waveform.

The PPMU may be configurable to measure or to source a current waveform, or to measure or source a voltage waveform.

Any two or more of the features described in this specification, including in this summary section, can be combined to form implementations not specifically described herein.

The test systems and techniques described herein, or portions thereof, can be implemented as/controlled by a computer program product that includes instructions that are stored on one or more non-transitory machine-readable storage media, and that are executable on one or more processing devices to control (e.g., coordinate) the operations described herein. The test systems and techniques described herein, or portions thereof, can be implemented as an apparatus, method, or electronic system that can include one or more processing devices and memory to store executable instructions to implement various operations.

The details of one or more implementations are set forth in the accompanying drawings and the description below. Other features and advantages will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of example circuitry in automatic test equipment (ATE), including example per-pin measurement unit (PPMU) circuitry.

Fig. 2 is a high-level block diagram of example ATE, which may include the circuitry and components of Fig. 1.

Like reference numerals in different figures indicate like elements.

DETAILED DESCRIPTION

Manufacturers may test devices at various stages of manufacturing. Manufacturers have an economic incentive to detect and discard faulty components

as early as possible in the manufacturing process. Accordingly, many manufacturers test integrated circuits at the wafer level, before a wafer is cut into dice. Defective circuits are marked and generally discarded prior to packaging, thus saving the cost of packaging defective dice. As a final check, many manufacturers test each finished product before it is shipped. Such a process tests parts in packages which have had additional expense added to them over bare die. So, having accurate test results reduces the need to discard valuable parts.

To test quantities of components, manufacturers commonly use ATE (or "testers"). In response to instructions in a test program set (TPS), some ATE automatically generates input signals to be applied to a device under test (DUT), and monitors output signals. The ATE compares the output signals with expected responses to determine whether the DUT is defective. ATE typically includes a computer system and a test instrument or a single device having corresponding functionalities. In some cases, the test instrument provides power to a DUT.

Fig. 1 shows example components of an example ATE 100. These components include a computer system 101 and a tester 102. In some examples, computer system 101 controls operations of tester 102, and receives data from tester 102 for further processing. Tester 102 interfaces to DUT 104, either directly or indirectly (e.g., through a device interface board (DIB) (not shown)). In this example, tester 102 communicates data to, and receives test data from, DUT 104. For example, as described with respect to Fig. 2 below, tester 102 sends test data to DUT 104, and analyzes the DUT's response to that test data in order to determine if

the DUT is operating correctly or within acceptable operational parameters. In some implementations, tester 102 includes circuitry called high-speed digital instruments (HSDs) 106, which are shown in Fig. 1. HSDs have one or more circuits known as channels. DUTs have one or more pins which they use to connect to other circuitry. HSD channels may be connected to DUT pins to provide communication between and HSD instruments and the DUT.

In an example, each HSD 106 includes circuitry to provide digital data, also referred to as digital "test patterns", to a DUT. These test patterns may be designed to elicit particular responses from the DUT. The DUT's reaction to these test patterns is captured by the ATE in order to determine if the DUT has passed, or failed, a test that is based on the test pattern. Communications occur between each HSD channel 107 and corresponding DUT pin. Although only several communication channels 107 are shown, there are typically more communication channels than are shown in the figure. In an example implementation, there may be one DUT pin per HSD channel. The number of signals between the ATE and the DUT may vary depending upon the circumstances; however, that number may reach into the hundreds or thousands in some cases.

In some examples, each HSD may include circuitry on each channel to detect signals on the channel, and to output signals to the channel. An example of this circuitry 110 is shown in Fig. 1. In some implementations, this circuitry, or portion(s) thereof, is included in the tester but not in an HSD. In this example, circuitry 110 includes a digital drive and compare unit 114. Digital drive and compare unit 114

includes a driver 115 for driving digital signals on a channel 116 to the DUT, comparators 118, 119 having respective low and high inputs for digital signals. In this example, circuitry 110 also includes one or more per-pin measurement units (PPMU). Any appropriate number of PPMUs may be included. PPMUs can be used to measure parametric, or analog, qualities of a DUT pin or to source parametric or analog signals to the DUT. PPMUs may be capable of sourcing and measuring both voltages and currents.

Example PPMU 120 may be configured to receive signals from the DUT or to source signals to the DUT. In this example, PPMU 120 includes an analog input 122, an analog output 123, and a digital-to-analog converter (DAC) 124 connected to the analog output. In some implementations, there may be multiple PPMUs, as shown. In some examples, the PPMUs may include different, substitute, and/or additional circuitry than that shown. In this example, an analog-to-digital converter (ADC) 125 receives analog signals measured by the PPMU from the DUT, and converts those signals to digital form. In some implementations, a single ADC serves multiple PPMUs (as shown); however, that is not a requirement. DACs and ADCs may be integrated into PPMUs or may be independent components. Programmable logic 127 - in this example, a field programmable gate array (FPGA) - is connected to both ADC 125 and to DAC 124. In some implementations, programmable logic 127 may be replaced by, or augmented by, other appropriate logic and/or circuitry, such as an application-specific integrated circuit (ASIC) or other processing devices. In addition, there may be multiple such devices. In some

examples, programmable logic 127 is part of an HSD (as shown), whereas in other examples programmable logic 127 is resident elsewhere on the tester or system.

In this example, programmable logic 127 implements a processing device and memory. In other implementations the memory may be external to the processing device, or the memory may be part internal to the logic and part external, or entirely external to the logic. In this example, the processing device is used to execute one or more state machines 131. In this example, a state machine implemented by the programmable logic interacts with one or more ADCs, such as ADC 125. A state machine may also be responsive to one or more commands output by computer system 101. For example, in response to a command (e.g., a single command) or other instruction from computer system 101, the state machine may retrieve (e.g., read or request and receive) data from one or more ADCs. The data may represent outputs of PPMU 120 and, therefore, may represent measurements generated by the PPMU.

By providing a state machine to control interaction with the PPMUs, the example ATE described herein is able, through the PPMUs, to retrieve data at fixed, known, or programmable intervals, and to source data at fixed, known, or programmable intervals. For example, the state machine running in the programmable logic may be dedicated to tasks of obtaining and sourcing data (in contrast to the computer system, which also performs other tasks). As a result, in some cases, the state machine is able to maintain more precise timing than the computer system for data retrieval and sourcing. Furthermore, in some

implementations, the state machine may be responsive to a single command of the computer system. Therefore, once the state machine receives that command, control over data retrieval or sourcing is passed to the state machine, which can perform those operations at fixed, known, or programmable intervals. The fixed, known, or programmable intervals may be hard-coded or programmable.

In some implementations, the state machine may be configured to obtain data from multiple DUT channels. For example, the state machine may be configured to obtain data from different channels by communicating with ADCs connected to PPMUs for those channels. In an example, the ADC may request, in sequence, data from each channel, and then repeat this request as instructed. The data may be stored, in sequence, in locations of memory 129 in the programmable logic. In some implementations, the state machine may be configured to obtain data from a single DUT pin by communicating with an ADC connected to a PPMU for the corresponding channel. For example, the state machine may be configured to obtain, at a known intervals, data that is based on an output of a measurement by PPMU 120 and to store the data in memory on the programmable logic (or, in some implementations, to output data to the PPMU from the memory at a known intervals). For example, the state machine may read data from ADC 125 at known intervals (e.g., every 8 milliseconds) to obtain a reading that corresponds to a waveform at the DUT. This data may be stored, in sequence, in memory. Accordingly, effectively, the PPMU may be used to sample a signal at a DUT pin at known intervals. The data stored in memory 129 may be used to reconstruct the waveform

at the DUT, to measure noise in the signal, to determine a peak amplitude of the signal, and/or to determine any other appropriate parameters relating to the DUT signal that can be ascertained based on the data. In some implementations, the data may be transferred to computer system 101, and computer system 101 may perform the processing used to reconstruct the waveform at the DUT, to measure noise in the signal, to determine a peak amplitude of the signal, etc. In other implementations, this processing may be performed in the programmable logic or in an embedded processor 130 in the tester.

In some implementations, memory 129 is used both to store digitized ADC data and source DAC data. In some implementations, pattern data to output to the PPMU DACs may reside externally to memory 129, while capture memory may be integrated into the PPMU.

In some implementations, the foregoing circuitry may be used to sample signals at multiple DUT pins. For example, to sample signals at two DUT pins, the state machine may obtain data, alternately or simultaneously, from two different PPMUs connected to those two channels corresponding to those DUT pins. The obtained data may be stored in memory (e.g., for each DUT pin, at every other memory location), and used to reconstruct the two signals or to perform any other appropriate processing associated therewith. This concept may be extended to any number of channels, pins and signals.

As noted above, in some implementations, the PPMU may be operated as a source for data to the DUT. For example, the state machine may read-out, at known

intervals, data from memory 129 and output that data to DAC 124. The DAC may generate an analog signal based on the data, and output the analog signal to a DUT pin 116. Thus, the programmable logic may be configured to send signal data from the memory, and the PPMU may be configured to generate an AC (e.g., a low-frequency analog) waveform for delivery to the DUT based on the signal data.

As noted above, data may be read from the ADC at a fixed, known, or programmable intervals, or supplied to the DAC at a fixed, known, or programmable intervals, by the state machine. In some implementations, the fixed, known, or programmable intervals may be programmed, by the computer system, into the state machine. In some implementations, that fixed, known, or intervals may be changeable or not changeable.

In some implementations, ATE 100 may include multiple programmable logic devices (e.g., multiple FPGAs), each of which may be configured to serve multiple PPMUs and to run a state machine of the type described above. An embedded processor 130 may be programmed to control and/or coordinate operations of the various programmable logic devices. The embedded processor 130 may be controlled/programmed by commands provided from computer system 101. In some implementations, there may be multiple embedded processors included in ATE. Since the embedded processors may be dedicated devices, timing control over the programmable logic may be maintained within appropriate tolerances. In some examples, the embedded processor(s) are part of one or more HSDs (as shown),

whereas in other examples the embedded processor(s) are resident elsewhere on the tester or system.

In some implementations, sampling a signal at a DUT pin is not synchronized to any particular timing. For example, the time at which the data may be sampled is not known beforehand, thereby obtaining a sampling of an unspecified interval of a signal. In some implementations, control data in the test pattern, or sent along with the test pattern, may be used to synchronize sampling of data from a DUT, or providing signals to the DUT. For example, the control data may be sent from the HSDs, or elsewhere, to the programmable logic. The programmable logic may use the control data to synchronize sampling of DUT data with data output to the DUT, thereby enabling signals at DUT (input or output) to be sampled at a known time. IN this regard, the programmable logic may use the control data to synchronize the state machine with any appropriate ATE events/operations.

As noted above, the example techniques described herein may be implemented, at least in part, on ATE. In an example operation, ATE (also referred to as "testers" or "test systems") operates in accordance with instructions in a test program set (TPS) to automatically generate input signals to be applied to a DUT, and to monitor output signals from the DUT. The ATE compares the output signals with expected responses to determine whether the DUT is defective. ATE typically includes a computer system and a test instrument or a single device having corresponding functionalities.

Referring to Fig. 2, an example ATE 200 for testing a DUT 205 includes a tester (or "test instrument") 202. Tester 202 may include the circuitry described above with respect to Fig. 1. DUT 205 may be interfaced to a DIB 201, which may interface to one or more of the example instrument modules of the type described herein to send signals to, and receive signals, from the DUT.

Tester 202 may include a number of channels, each of which may be PART OF an HSD, as described above. To control tester 202, system 200 includes a computer system 204 that interfaces with tester 202 over a hardwire connection 206. In an example operation, computer system 204 sends commands to tester 202 to initiate execution of routines and functions for testing DUT 205. Such executing test routines may initiate the generation and transmission of test signals to the DUT 205 and collect responses from the DUT (e.g., via an instrument module). Various types of DUTs may be tested by system 200. In some implementations, the DUTs may be RF, microwave, or other wireless devices. In some implementations, the DUT may be any appropriate semiconductor or other device, such as an integrated circuit (IC) chip (e.g., memory chip, microprocessor, analog-to-digital converter, digital-to-analog converter, etc.) or other devices.

To provide test signals and collect responses from the DUT, tester 202 is connected to an interface to the internal circuitry of DUT 205. For example, the DUT may be inserted into a socket in DIB 201, which contains interfaces to electrical connections between the DUT and an instrument module in the tester. A conductor 208 (e.g., one or more conductive pathways) is connected to the interface and is

used to deliver test signals (e.g., switching or DC test signals, etc.) to the internal circuitry of DUT 205. Conductor 208 also senses signals in response to the test signals provided by tester 202. For example, a voltage signal or a current signal may be sensed at pin 210 (e.g., by a PPMU, as described above) in response to a test signal and sent over conductor 208 to tester 202 for analysis. Such single port tests may also be performed on other pins included in DUT 205. For example, tester 202 may provide test signals to other pins and collect associated signals reflected back over conductors (that deliver the provided signals). By collecting the reflected signals, the input impedance of the pins may be characterized along with other single port testing quantities. In other test scenarios, a digital signal may be sent over conductor 208 to pin 210 for storing a digital value on DUT 205. Once stored, DUT 205 may be accessed to retrieve and send the stored digital value over conductor 208 to tester 202. The retrieved digital value may then be identified to determine if the proper value was stored on DUT 205.

Along with performing single port measurements, a two-port or multi-port test may also be performed by tester 202. For example, a test signal may be injected over conductor 208 into pin 210 and a response signal may be collected from one or more other pins of DUT 205. This response signal may be provided to tester 202 to determine quantities, such as gain response, phase response, and other throughput measurement quantities. Other tests may also be performed.

While this specification describes example implementations related to "testing" and a "test system," the devices and method described herein may be used

in any appropriate system, and are not limited to test systems or to the example test systems described herein.

Testing performed as described herein may be implemented using hardware or a combination of hardware and software. For example, a test system like the ones described herein may include various controllers and/or processing devices located at various points. A central computer may coordinate operation among the various controllers or processing devices. The central computer, controllers, and processing devices may execute various software routines to effect control and coordination of testing and calibration.

Testing can be controlled, at least in part, using one or more computer program products, e.g., one or more computer program tangibly embodied in one or more information carriers, such as one or more non-transitory machine-readable media, for execution by, or to control the operation of, one or more data processing apparatus, e.g., a programmable processor, a computer, multiple computers, and/or programmable logic components.

A computer program can be written in any form of programming language, including compiled or interpreted languages, and it can be deployed in any form, including as a stand-alone program or as a module, component, subroutine, or other unit suitable for use in a computing environment. A computer program can be deployed to be executed on one computer or on multiple computers at one location or distributed across multiple locations and interconnected by a network.

Actions associated with implementing all or part of the testing and calibration can be performed by one or more programmable processors executing one or more computer programs to perform the functions described herein. All or part of the testing and calibration can be implemented using special purpose logic circuitry, e.g., an FPGA (field programmable gate array) and/or an ASIC (application-specific integrated circuit).

Processors suitable for the execution of a computer program include, by way of example, both general and special purpose microprocessors, and any one or more processors of any kind of digital computer. Generally, a processor will receive instructions and data from a read-only storage area or a random access storage area or both. Elements of a computer (including a server) include one or more processors for executing instructions and one or more storage area devices for storing instructions and data. Generally, a computer will also include, or be operatively coupled to receive data from, or transfer data to, or both, one or more machine-readable storage media, such as mass PCBs for storing data, e.g., magnetic, magneto-optical disks, or optical disks. Machine-readable storage media suitable for embodying computer program instructions and data include all forms of non-volatile storage area, including by way of example, semiconductor storage area devices, e.g., EPROM, EEPROM, and flash storage area devices; magnetic disks, e.g., internal hard disks or removable disks; magneto-optical disks; and CD-ROM and DVD-ROM disks.

Any “electrical connection” as used herein may imply a direct physical connection or a connection that includes intervening components but that nevertheless allows electrical signals (including wireless signals) to flow between connected components. Any “connection” involving electrical circuitry mentioned herein, unless stated otherwise, is an electrical connection and not necessarily a direct physical connection regardless of whether the word “electrical” is used to modify “connection”.

Elements of different implementations described herein may be combined to form other embodiments not specifically set forth above. Elements may be left out of the structures described herein without adversely affecting their operation. Furthermore, various separate elements may be combined into one or more individual elements to perform the functions described herein.

What is claimed is:

1. Automatic test equipment (ATE) comprising:

a per-pin measurement unit (PPMU);

logic configured to execute a state machine to control the PPMU;

memory that is part of, or separate from, the logic; and

a control system to command the logic;

wherein, in response to a command from the control system, the state machine is configured to obtain, at a known interval or synchronous to an event, data that is based on an output of a measurement by the PPMU and to store the data in the memory, or to output data to the PPMU from the memory at a known interval or synchronous to an event.

2. The ATE of claim 1, wherein the ATE is configured to test a device under test (DUT), the DUT having multiple pins; and

wherein the ATE is configured to obtain, via the PPMU, data that is based on values at a single pin of the DUT and to store the data in the memory.

3. The ATE of claim 1, wherein the ATE is configured to test a device under test (DUT), the DUT having multiple pins; and

wherein the ATE is configured to obtain, via the PPMU, data that is based on values at multiple pins of the DUT and to store the data in the memory.

4. The ATE of claim 1, wherein the known intervals are programmable.

5. The ATE of claim 1, further comprising:

an analog-to-digital converter (ADC) between the logic and the PPMU, the ADC for servicing one or multiple PPMUs including the PPMU;

wherein the logic is configured to obtain the data by retrieving the data from the ADC.

6. The ATE of claim 1, wherein the ATE is configured to test a device under test (DUT), the DUT having multiple pins;

wherein the ATE is configured to obtain, via the PPMU, data that is based on values at a single pin of the DUT and to store the data in the memory;

wherein the logic is configured to provide the data to the control system; and

wherein the control system is configured to reconstruct a waveform based on the data.

7. The ATE of claim 1, wherein the ATE is configured to test a device under test (DUT), the DUT having multiple pins;

wherein the ATE is configured to obtain, via the PPMU, data that is based on values at a single pin of the DUT and to store the data in the memory;

wherein the data is usable to perform one or more operations comprising measuring signal noise or extracting signal peak amplitude.

8. The ATE of claim 1, wherein the ATE is configured to output a digital pattern to the DUT, the digital pattern containing control data; and

wherein the ATE comprises is configured to use the control data to control the logic based on the control data.

9. The ATE of claim 8, wherein the ATE is configured to control when the logic obtains data that is based on an output of the PPMU, or outputs data to the PPMU from the memory.

10. The ATE of claim 9, wherein the ATE is configured to control the logic to obtain data at a time that is based on the control data.

11. The ATE of claim 1, further comprising:

a processing device that is responsive to the control system to control operation of the logic.

12. The ATE of claim 11, wherein the logic comprises a field programmable gate array (FPGA);

wherein the ATE comprises multiple FPGAs, each of the multiple FPGAs being configured to execute a state machine to control one or more PPMUs; and

wherein the processing device is configured to control the multiple FPGAs.

13. The ATE of claim 1, wherein the PPMU comprises a digital-to-analog converter and the memory stores signal data; and

wherein the logic is configured to send the signal data to the memory, and the PPMU is configured to generate an AC waveform for delivery to the DUT based on the signal data.

14. The ATE of claim 13, wherein the AC waveform is an analog waveform.

15. The ATE of claim 1, wherein the PPMU is configurable to measure or to source a current waveform, or to measure or source a voltage waveform.

16. A method of operating automatic test equipment (ATE) comprising a per-pin measurement unit (PPMU), logic configured to execute a state machine to control the PPMU, memory that is part of, or separate from, the logic, and a control system to command the logic, the method comprising:

in response to a command from the control system, executing the state machine to obtain, at a known interval or synchronous to an event, data that is based on an output of a measurement by the PPMU and to store the data in the memory, or to output data to the PPMU from the memory at a known interval or synchronous to an event.

17. One or more non-transitory machine-readable storage media storing instructions that are executable during operation of automatic test equipment (ATE), the ATE comprising a per-pin measurement unit (PPMU), logic configured to execute a state machine to control the PPMU, memory that is part of, or separate from, the logic, and a control system to command the logic, the operations comprising:

in response to a command from the control system, executing the state machine to obtain, at a known interval or synchronous to an event, data that is based on an output of a measurement by the PPMU and to store the data in the memory, or to output data to the PPMU from the memory at a known interval or synchronous to an event.

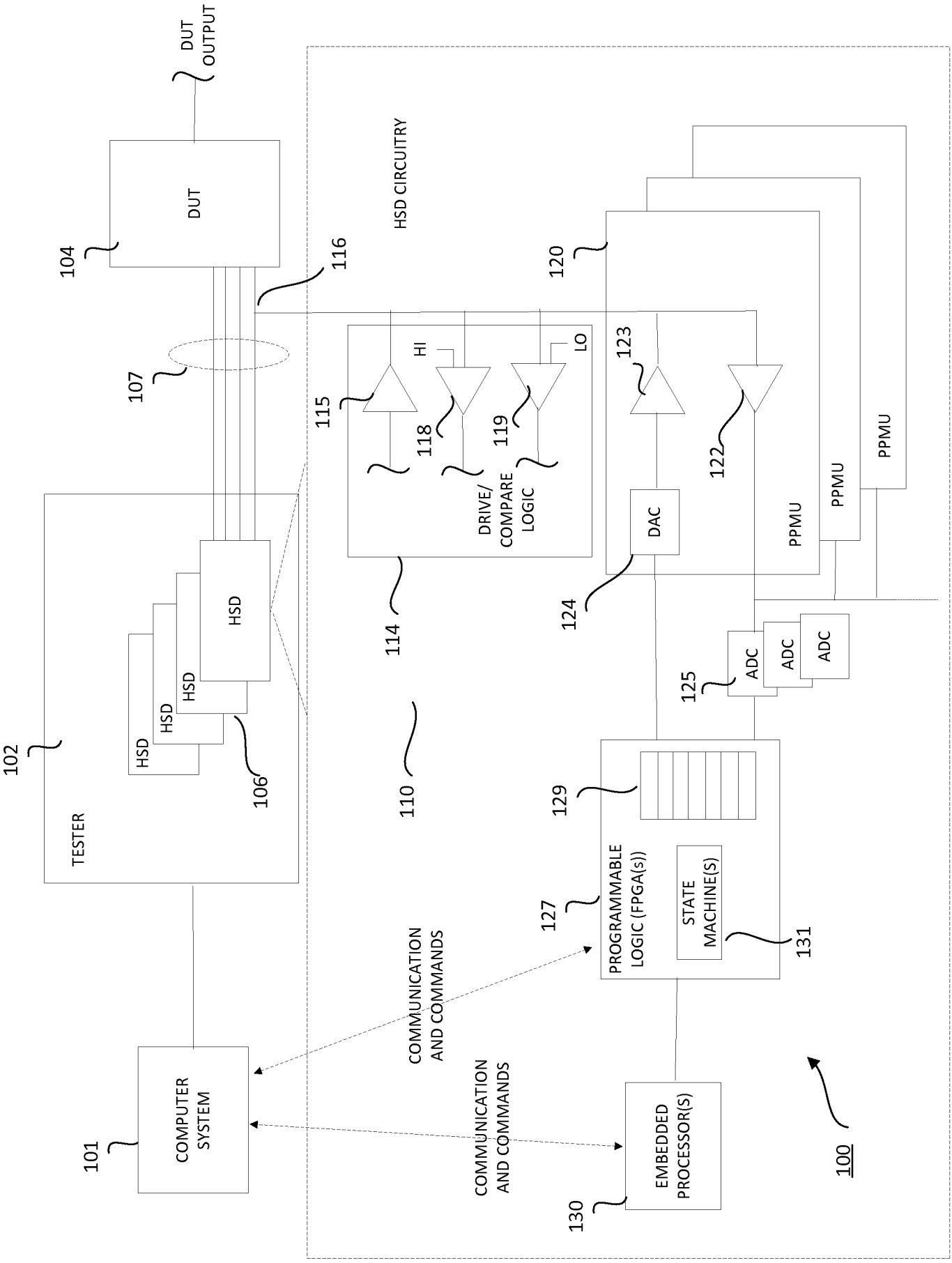

DUT OUTPUT
DUT
104
116
HSD CIRCUITRY
120
107
115
HI
LO
123
118
119
122
DRIVE/ COMPARE LOGIC
DAC
PPMU
PPMU
PPMU
HSD
HSD
HSD
HSD
102
106
114
124
110
ADC
ADC
ADC
125
129
TESTER
PROGRAMMABLE LOGIC (FPGA(s))
STATE MACHINE(S)
127
131
COMMUNICATION AND COMMANDS
COMMUNICATION AND COMMANDS
COMPUTER SYSTEM
EMBEDDED PROCESSOR(S)
101
130
100

FIG. 1

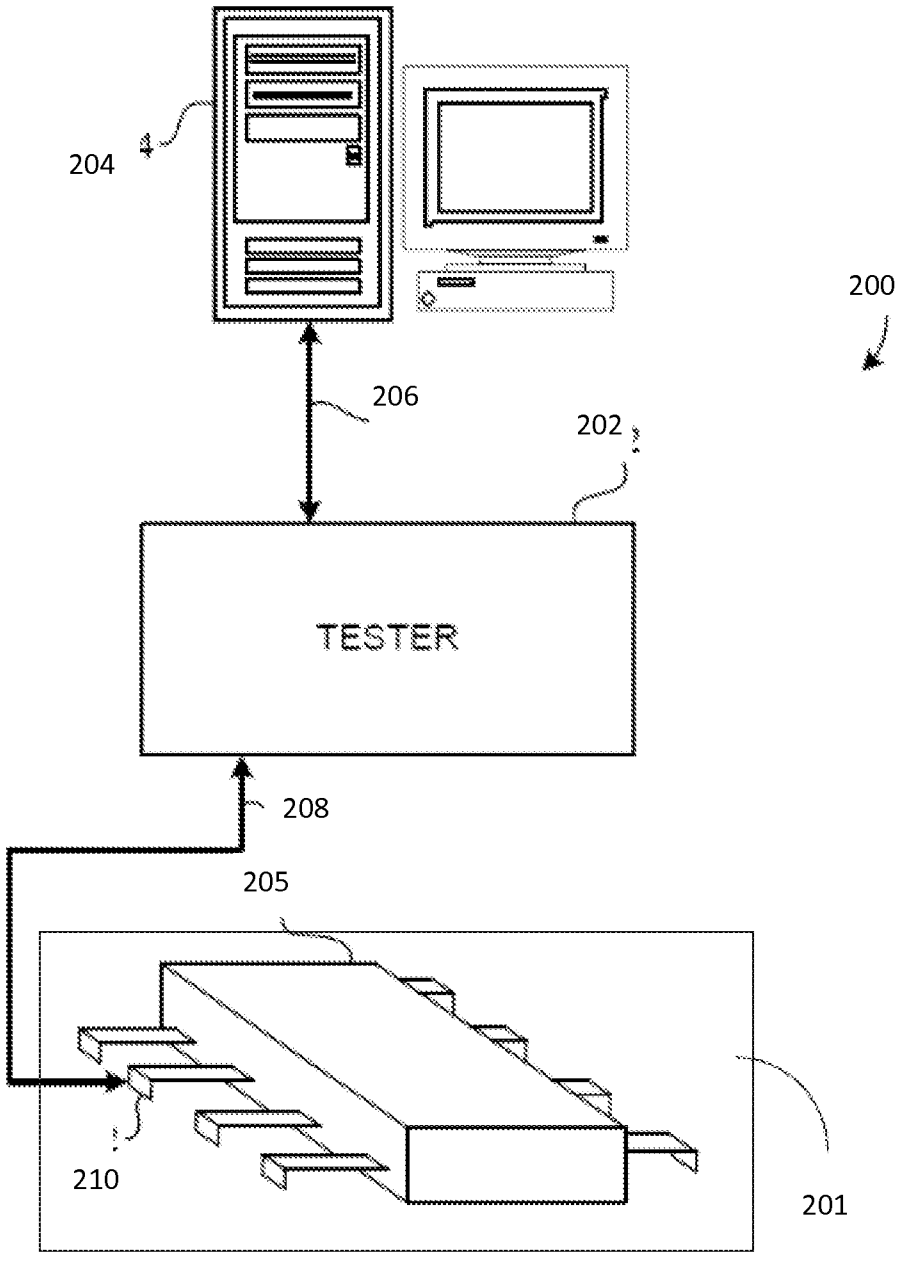


FIG. 2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/061502

A. CLASSIFICATION OF SUBJECT MATTER

G01R 31/28(2006.01)i, G01R 31/26(2006.01)i, G01R 1/073(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G01R 31/28; G01R 1/00; G01R 31/02; G06F 11/00; G01R 31/26; G01R 1/073

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: ATE, DUT, interval, per pin

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2002-0070725 A1 (HILLIGES) 13 June 2002 See paragraphs [0056]-[0162], claims 1-4 and figures 7-10.	1-17
Y	US 2007-0168817 A1 (VIENS) 19 July 2007 See abstract, paragraphs [0013]-[0029], claim 10 and figures 1-2.	1-17
A	US 2006-0202707 A1 (HARJUNG) 14 September 2006 See abstract and figures 1-4.	1-17
A	US 5127011 A (COMBS et al.) 30 June 1992 See figures 2-3.	1-17
A	US 2005-0246603 A1 (ROTTACKER et al.) 03 November 2005 See figures 1-4.	1-17

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 March 2016 (24.03.2016)	**28 March 2016 (28.03.2016)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2015/061502

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